TÉCNICO LISBOA

Circuit Theory and Electronics Fundamentals

Department of Electrical and Computer Engineering, Técnico, University of Lisbon

T3's Laboratory Report

Group 5

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Contents

1 Introduction

The objective of this laboratory assignment is to choose the architecture of the envelope and voltage regulator circuits in order to have the best merit (M) possible.

Firstly, we started this laboratory writing an NGspice script that simulates the AC/DC converter and measure the output voltage level and voltage ripple , ploting the the voltages at the output of the envelope detector and voltage regulator circuits and the output AC component + DC deviation).

Then, using octave, we have created a theoretical model able to predict the output of the envelope detector and voltage regulator circuits, ploting the same results as in simulation anal-

ysis (using theoretical analysis). Finally, also the output DC level and the voltage ripple were computed.

The merit is calculated using the following expression:

$$M = \frac{1}{Cost(ripple(v_0) + average(v_0 - 12) + 10^{-6})} \tag{1}$$

Where:

Cost = cost of resistors + cost of capacitors + cost of diodes

Cost of Resistors = 1 monetary unit per kOhm

Cost of capacitor = 1 monetary unit per μ F

Cost of diodes = 0.1Monetary units per diode

Firstly, we have created a simple circuit and then we were updating the circuit to improve the figure of merit. The final circuit obtainned is the one shown below in figure (Fig.1):

Figure 1: Final circuit

The individual costs of the components used:

- Diodes - cost: 2.3MU;
- Capacitor - 5MU;
- Resistances - 55MU.

The data used was the following:

Name	Value
R_1	65 kΩ
R_2	7.26 kΩ
C	20 μS
Diodes	19 Units

2 Simulation analysis

2.1 Simulating the AC/DC converter for 10 periods

As said in the introduction, the first step to this laboratory assignment was to simulate a simple AC/DC converter in NGSpice, the circuit features an ideal transformer, using a current controlled voltage source as well as a voltage controlled current source as explained by the professor in a previous lecture, as well as an envelope detector and a voltage regulator.

This AC/DC converter was simulated for 10 periods and all the analysis were made measuring on a $5e-5$ step in order to evaluate at least 1000 points during the 10 periods. In order to calculate this step we used the frequency of the AC source to know the period and then we multiplied this period by 10 in order to get the total time. We then divided the total time by 1000 points and made the step even smaller than that in order to make sure it had more than 1000 points but not too small that the program ran slowly.

This circuit was first made simple and was elaborated along the way, making it output the correct voltage, increasing the merit figure.

2.2 Output voltage level

After describing the circuit we made NGSpice measure the average output voltage and using a transient analysis we plotted both the average and the signal of the output voltage in the same graph.

The table and the graph below show the results we got.

Name	Value [V]
mean(v(n5)-v(n3))	1.199970e+01

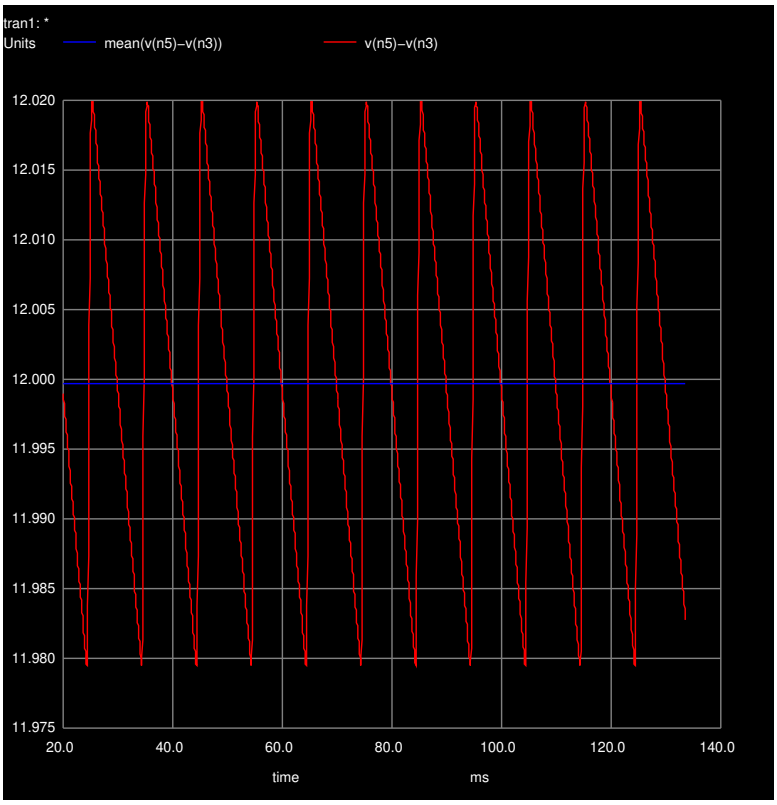

Figure 2: Plot of the average and the signal of the Output Voltage.

2.3 Output of the Envelope Detector and voltage Regulator circuits

The output voltages of both the Envelope Detector as well as the Voltage Regulator circuits were plotted and put each in a different graph as well as a graph with both voltages plotted.

The three graphs are in the images below.

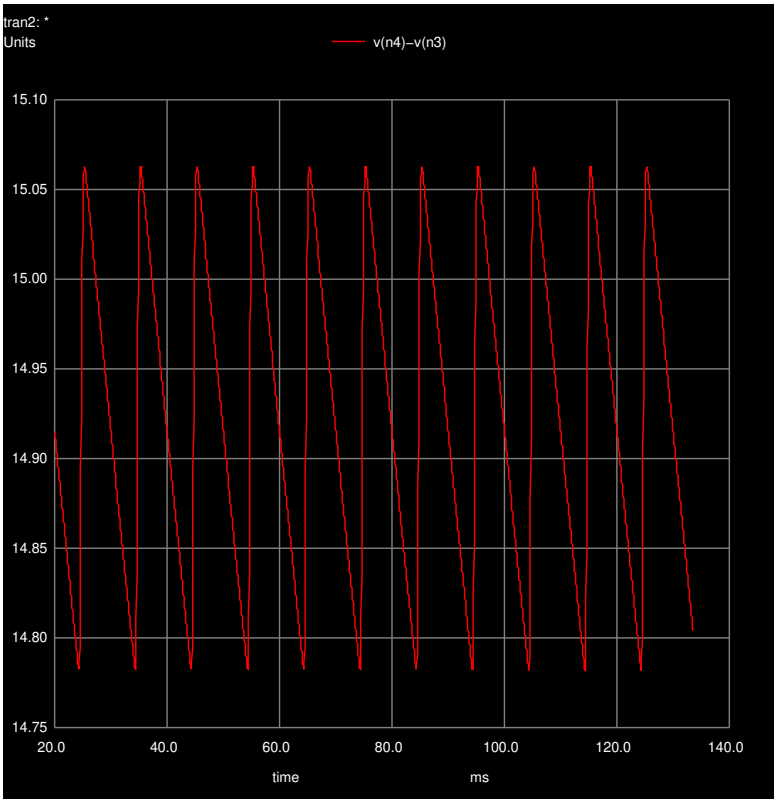

Figure 3: Envelope Detector Output Voltage.

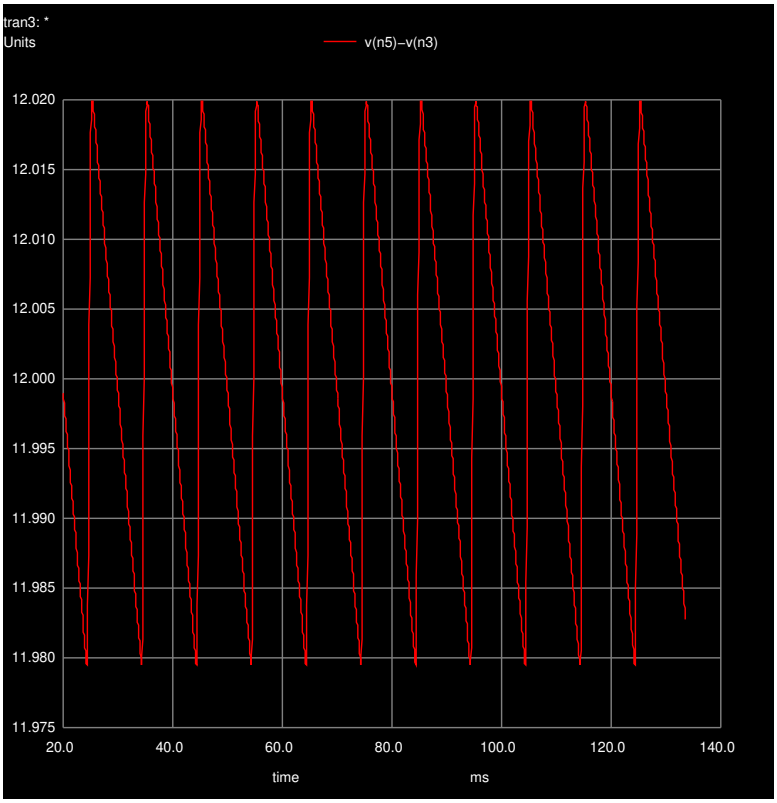

Figure 4: Voltage Regulator Output Voltage.

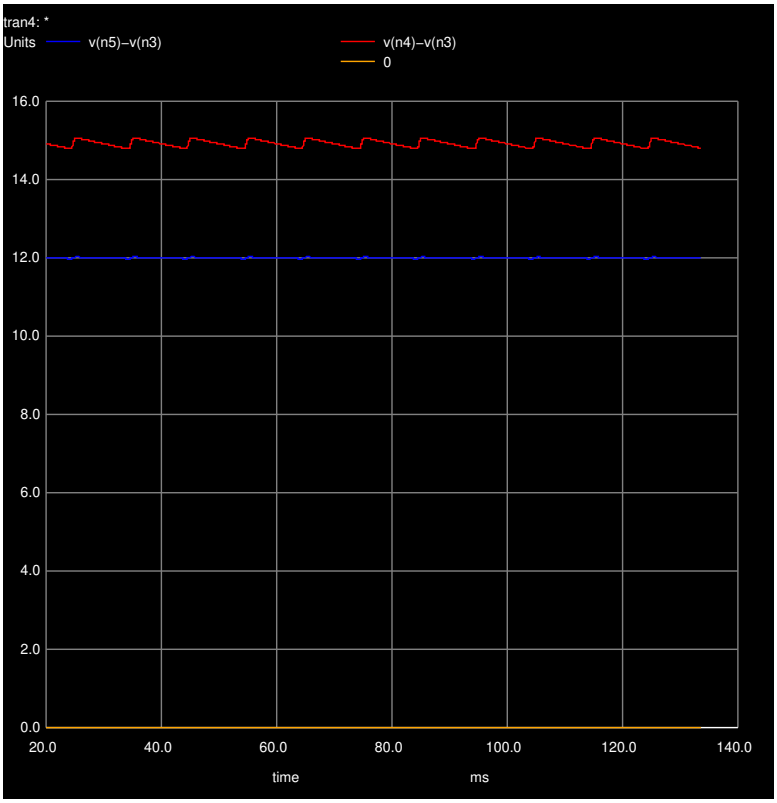

Figure 5: Envelope Detector and Voltage Regulator Output Voltages.

2.4 Output voltage ripple

We then made NGSpice measure the output voltage ripple, that is the difference between the maximum and the minimum values of the signal.

The result we got is in the table below.

Name	Value [V]
maximum(v(n5)-v(n3))-minimum(v(n5)-v(n3))	4.042821e-02

2.5 $v_0 - 12$ plot

Lastly, we plotted $v_0 - 12$, which corresponds to the output AC component plus the DC deviation.

The plot can be seen in the image below.

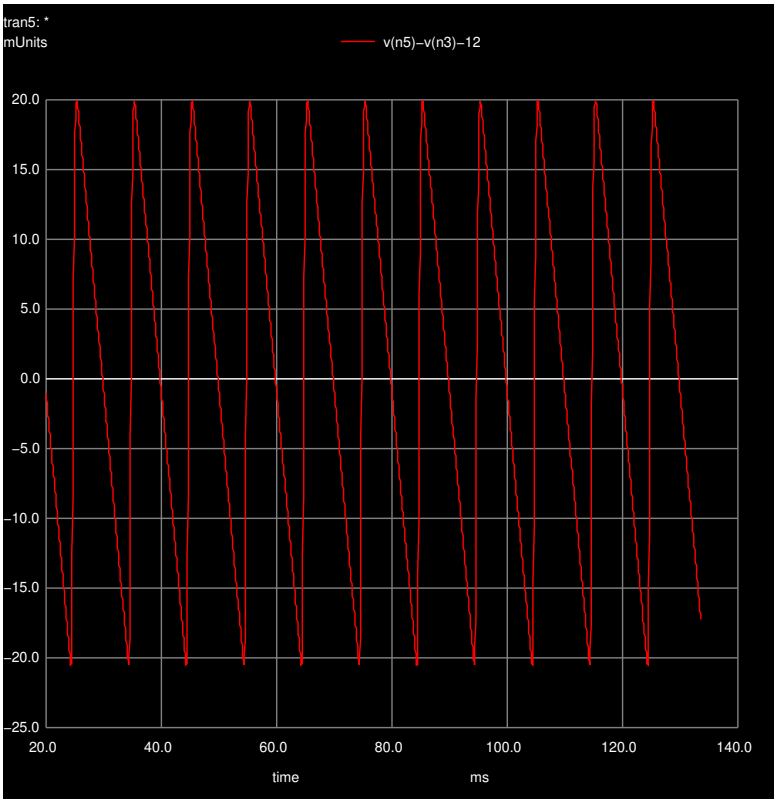

Figure 6: Output AC component + DC deviation.

3 Theoretical Analysis

In this section are shown the obtained results using a suitable theoretical model able to predict the output of the Envelope Detector and voltage Regulator circuits.

3.1 Envelope detector and voltage regulator plot

In this plot we can see the output voltage of the envelope and voltage regulator circuits. The envelope detector restricts the voltage's amplitude and the voltage regulator decreases the ripple.

4 Conclusion

Summing up, in this laboratory assignment (T2) we have made both theoretical analysis as well as simulations of several different but similar and correlated circuits.

The results obtained in both analysis were either put in a table or plotted in order to make comparations between the theoretical and simulation analysis. Up untill the simulation's question 4, the results are either the exact same or have very little differences on the last decimal places and so they are negligible, the explanation for this is that we studied a very simple circuit containing only linear components. If the components used were more complex, the case would not be the same and we could detect real differences between the values calculated and simulated.

Comparing figure 17 and figure 18, the theoretical value is based on a simplification when the circuit contribuition is resumed to R_{eq} and, the NGspice result is based on all the actual contributions of the circuit. Thus in the figure 18 the signal is going to be a perfect sinusoidal signal while the figure 17 displays an imperfect signal.

Lastly, for the same reasons of figure 17 and 18, there are little differences between plots in both figures.

That being said we would like to end this report by presenting both the theoretical and simulation results side by side in order to easily compare the results.

Name	Value
Resistor Cost	7.226000e+01
Capacitor Cost	2.000000e+01
Diode Cost	2.300000e+00
Total Cost	9.456000e+01
Merit	2.636305e-01

Name	Value [A or V]

Figure 7: Theoretical Question 1

Name	Value [A or V]

Figure 8: Simulation Question 1