Circuit Theory and Electronics Fundamentals

Department of Electrical and Computer Engineering, Técnico, University of Lisbon

T3's Laboratory Report

Group 5

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1 Introduction

The objective of this laboratory assignment is to choose the architecture of the envelope and voltage regulator circuits in order to have the best merit (M) possible.

Firstly, we started this laboratory writing an NGspice script that simulates the AC/DC converter and measure the output voltage level and voltage ripple , ploting the the voltages at the output of the envelope detector and voltage regulator circuits and the output AC component + DC deviation).

Then, using octave, we have created a theoretical model able to predict the output of the envelope detector and voltage regulator circuits, ploting the same results as in simulation analysis (using theoretical analysis). Finally, also the output DC level and the voltage ripple were computed.

The merit is calculated using the following expression:

$$M = \frac{1}{Cost(ripple(v_0) + average(v_0 - 12) + 10^{-6})} \tag{1}$$

Where:
Cost = cost of resistors + cost of capacitors + cost of diodes
Cost of Resistors = 1 monetary unit per kOhm
Cost of capacitor = 1 monetary unit per μ F
Cost of diodes = 0.1Monetary units per diode

Firstly, we have created a simple circuit and then we were updating the circuit to improve the figure of merit. The final circuit obtainned is the one shown below in figure (Fig.1):

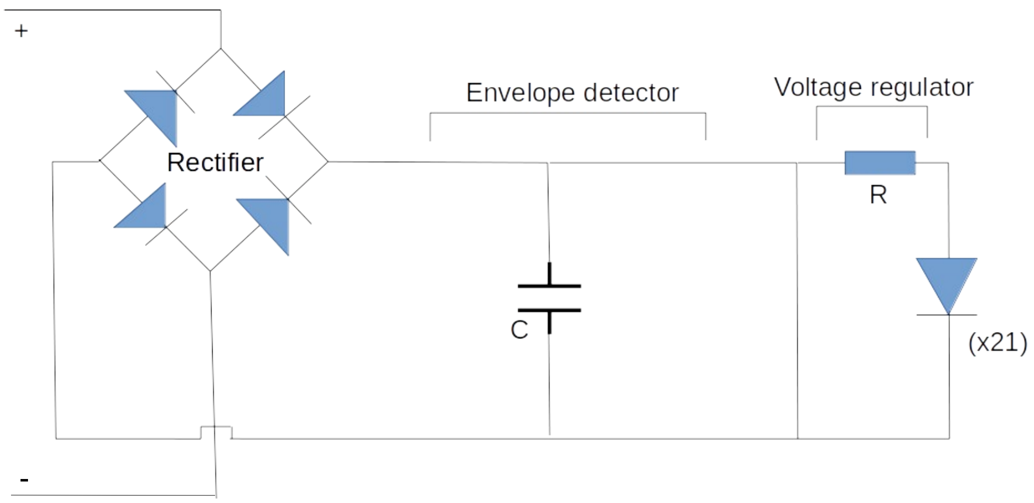

Figure 1: Final circuit

The individual costs of the components used:
- Diodes - cost: 2.3MU;
- Capacitor - 5MU;
- Resistances - 55MU.

The data used was the following:

Name	Value
R	27.3 kΩ
C	21 μS
Diodes	25 Units

2 Simulation analysis

2.1 Simulating the AC/DC converter for 10 periods

As said in the introduction, the first step to this laboratory assignment was to simulate a simple AC/DC converter in NGSpice, the circuit features an ideal transformer, using a current controlled voltage source and a voltage controlled current source as explained by the professor in a previous lecture, as well as an envelope detector and a voltage regulator.

This AC/DC converter was simulated for 10 periods and all the analysis were made measuring on a $5e-5$ step in order to evaluate at least 1000 points during the 10 periods. In order to calculate this step we used the frequency of the AC source to know the period and then we multiplied this period by 10 in order to get the total time. We then divided the total time by 1000 points and made the step even smaller than that in order to make sure it had more than 1000 points but not too small that the program ran slowly.

This circuit was first made simple and was elaborated along the way, making it output the correct voltage and only then increasing the merit figure.

2.2 Output voltage level

After describing the circuit we made NGSpice measure the average output voltage and using a transient analysis we plotted both the average and the signal of the output voltage in the same graph.

The table and the graph below show the results we got.

Name	**Value [V]**
mean(v(n5)-v(n3))	1.200023e+01

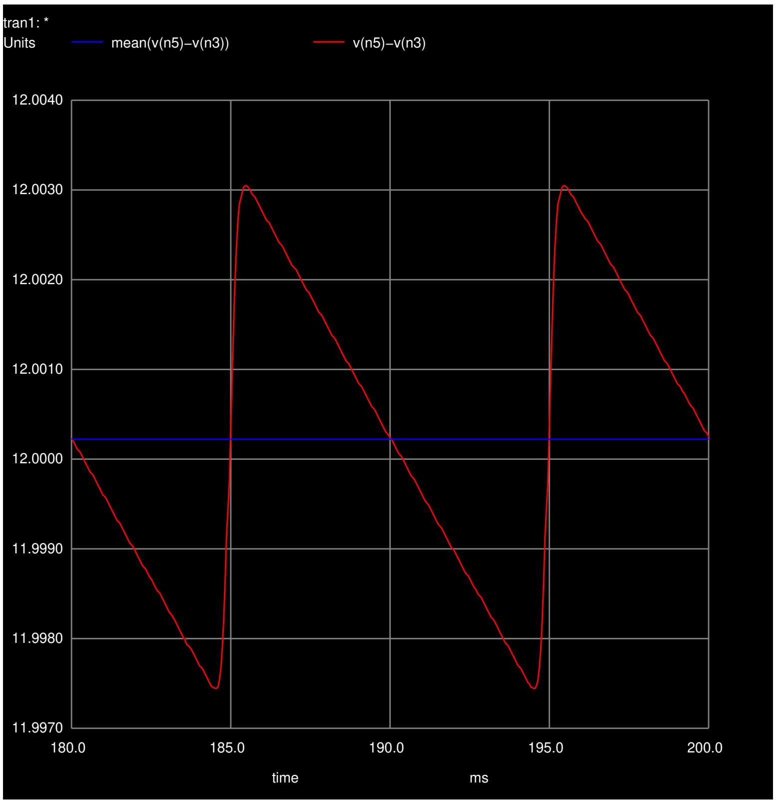

Figure 2: Plot of the average and the signal of the Output Voltage.

2.3 Output of the Envelope Detector and voltage Regulator circuits

The output voltages of both the Envelope Detector and the Voltage Regulator circuits were plotted and put each in a different graph as well as a graph with both voltages plotted.

The three graphs are in the images below.

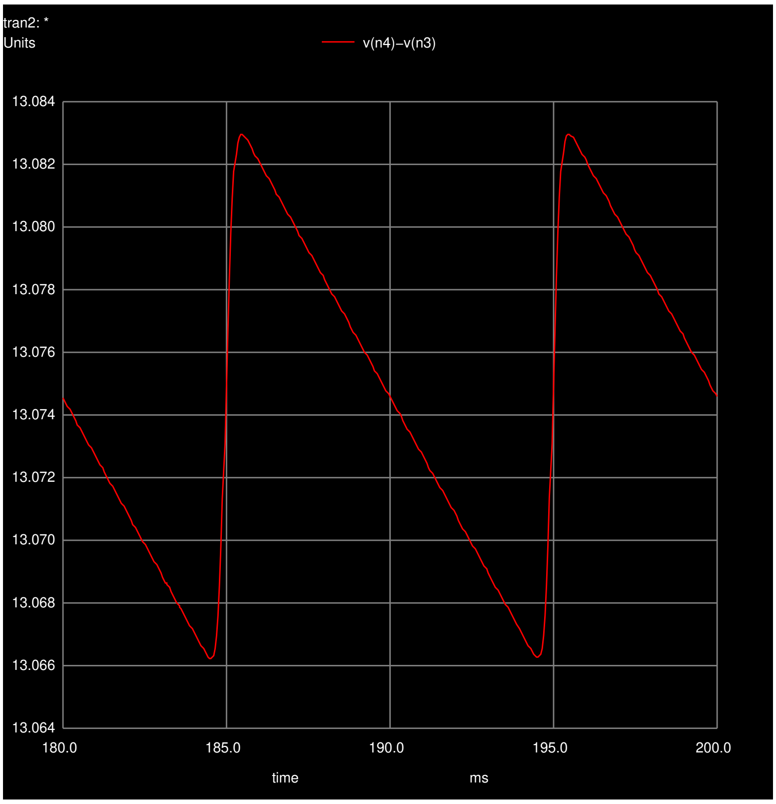

Figure 3: Envelope Detector Output Voltage.

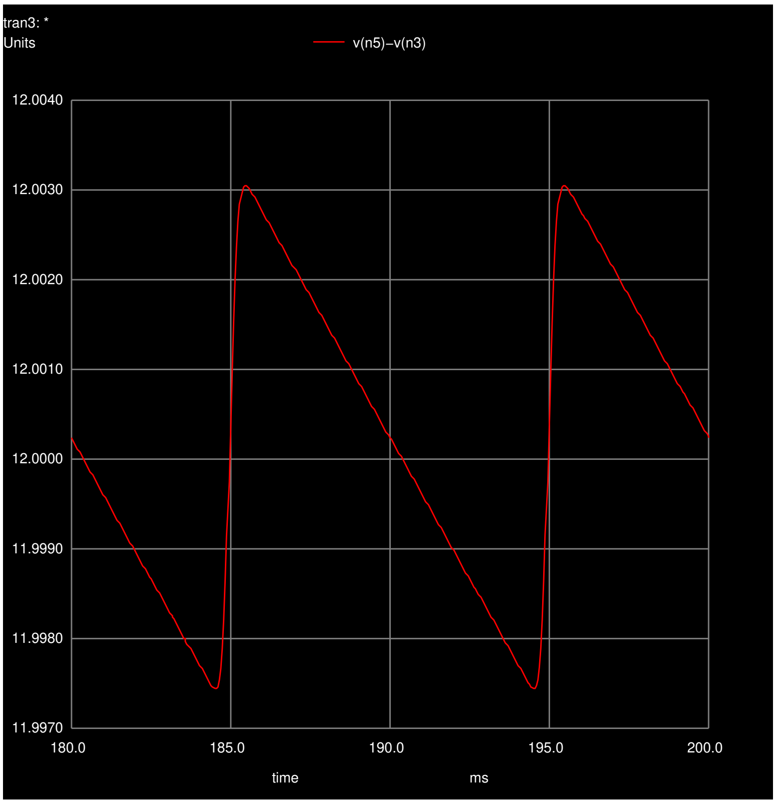

Figure 4: Voltage Regulator Output Voltage.

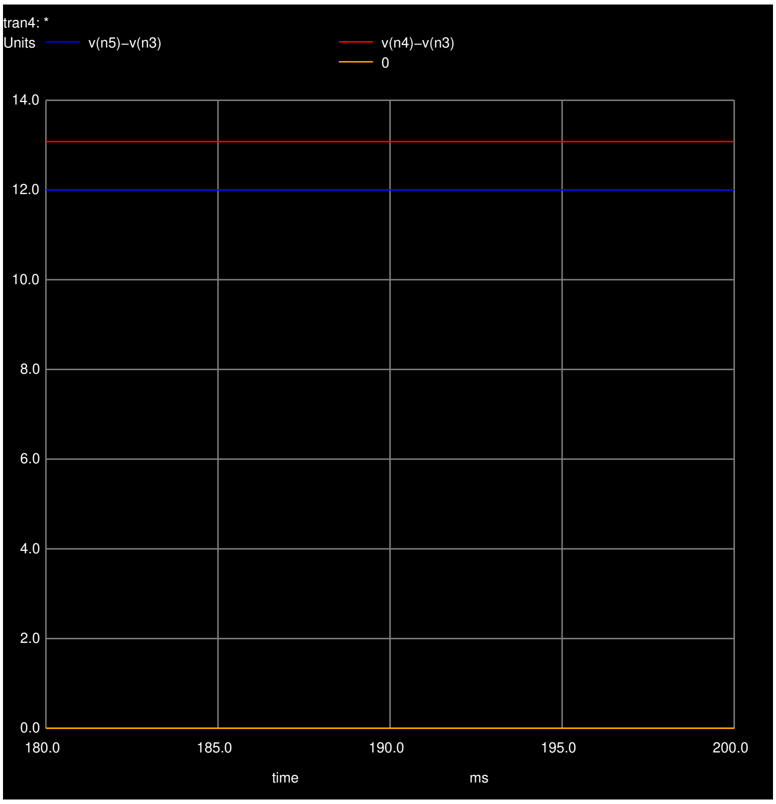

Figure 5: Envelope Detector and Voltage Regulator Output Voltages.

2.4 Output voltage ripple

We then made NGSpice measure the output voltage ripple, that is the difference between the maximum and the minimum values of the signal.

The result we got is in the table below.

Name	Value [V]
maximum(v(n5)-v(n3))-minimum(v(n5)-v(n3))	5.616237e-03

2.5 $v_0 - 12$ plot

Lastly, we plotted $v_0 - 12$, which corresponds to the output AC component plus the DC deviation, and calculated the deviation, using the mean value.

The plot can be seen in the image below as well as the deviation in the table below.

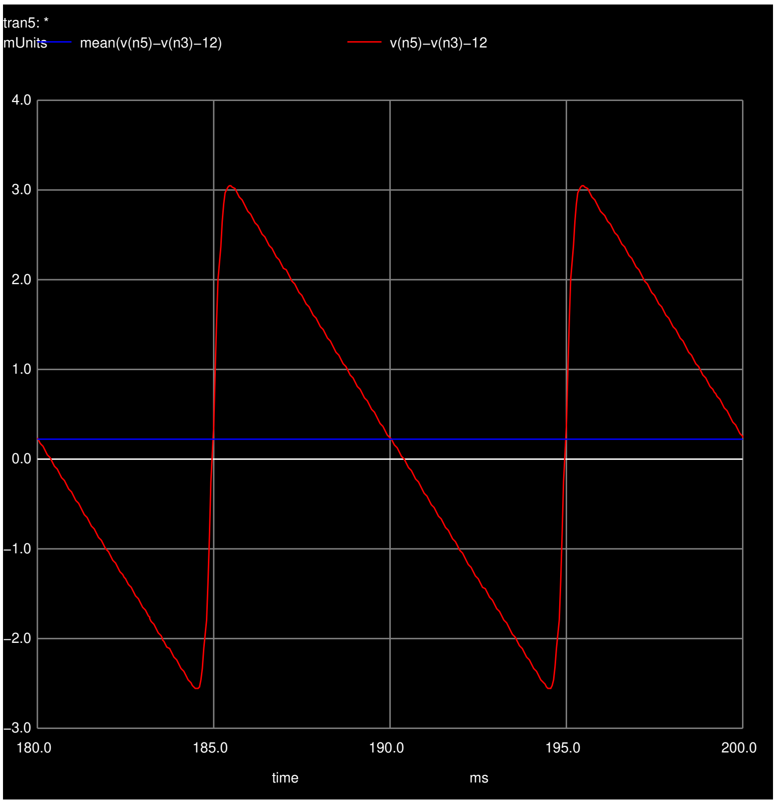

Figure 6: Output AC component + DC deviation.

Name	**Value [V]**
mean(v(n5)-v(n3)-12)	2.280889e-04

3 Theoretical Analysis

In this section are shown the obtained results using a suitable theoretical model able to predict the output of the Envelope Detector and voltage Regulator circuits.

3.1 Envelope detector

The envelope detector restricts the voltage's amplitude and the voltage regulator decreases the ripple. As it was shown in the circuit's figure, the envelope detector is, basically, the resistance and the capacitor in parallel. Its main function is to decrease the ripple using the following expression:

$$v_0(t) = Acos(\omega t_{off})^{\frac{-t+t_{off}}{RC}} \tag{2}$$

Where:

- A - Amplitude
- ω - angular frequency
- R - Resistance, constant obtained using the following expression:

$$R = R_3 + 23r_d \tag{3}$$

(R_3 and r_d will be explained in the next section.)

- C - Capacitance
- t_{off} - Constant obtained using the following expression:

$$t_{off} = \frac{1}{\omega} arctan(\frac{1}{\omega RC}) \tag{4}$$

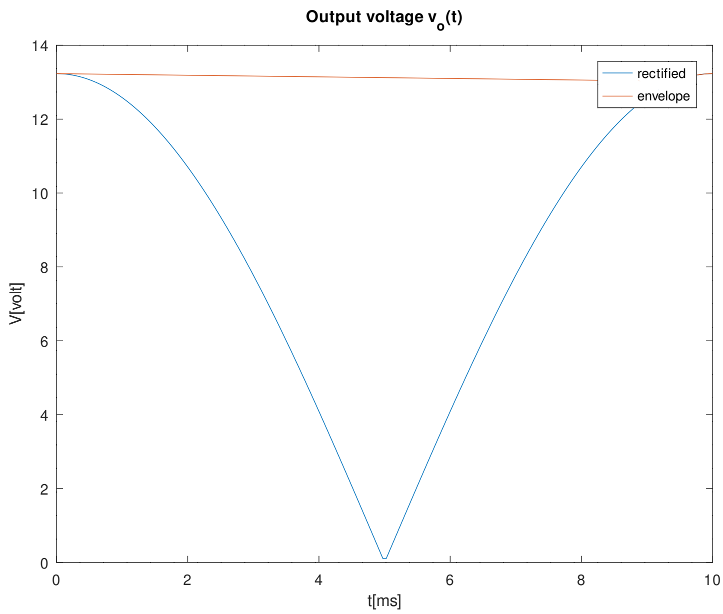

Figure 7: Rectified Signal.

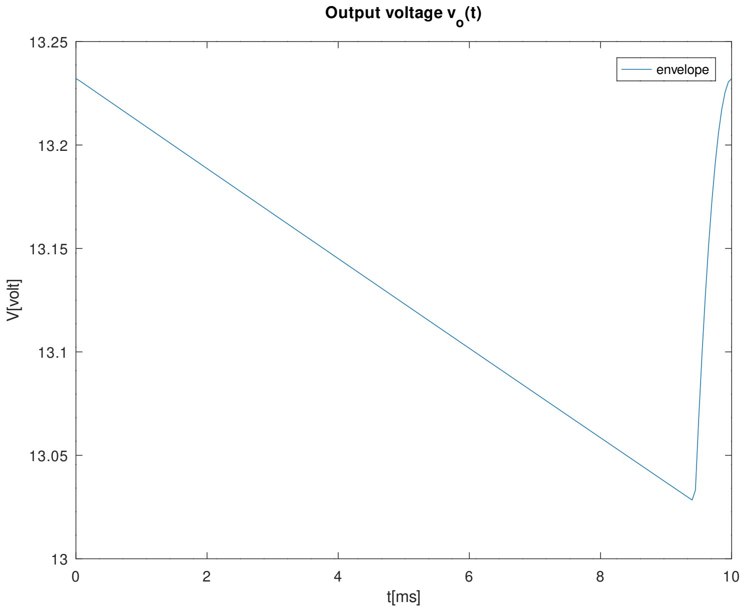

Figure 8: Envelope Detector Output Voltage.

3.2 Voltage Regulator

In our circuit, the voltage regulator consists of 23 diodes in series that will impose the 12V voltage. The resistance in serie will decrease the amplitude.

The expressions used to do this were the following ones:

Sinusoidal part from envelope:

$$v_{sr} = v_O - V_s \tag{5}$$

Calculating rd_n for all the diodes, where rd is the resistance of each one:

$$rd_n = 23rd \tag{6}$$

And then, we have:

$$vO_r = (\frac{rd_n}{rd_n + R_3})v_{sr} \tag{7}$$

Where R_3 is the resistance in serie.

The expression used to obtain the vltage ripple was:

$$v_{ripple} = maximum(V_{dc}) - minimum(V_{dc}) \tag{8}$$

Where:

$$V_{dc} = 21V_{on} + vO_r \tag{9}$$

The results are shown below:

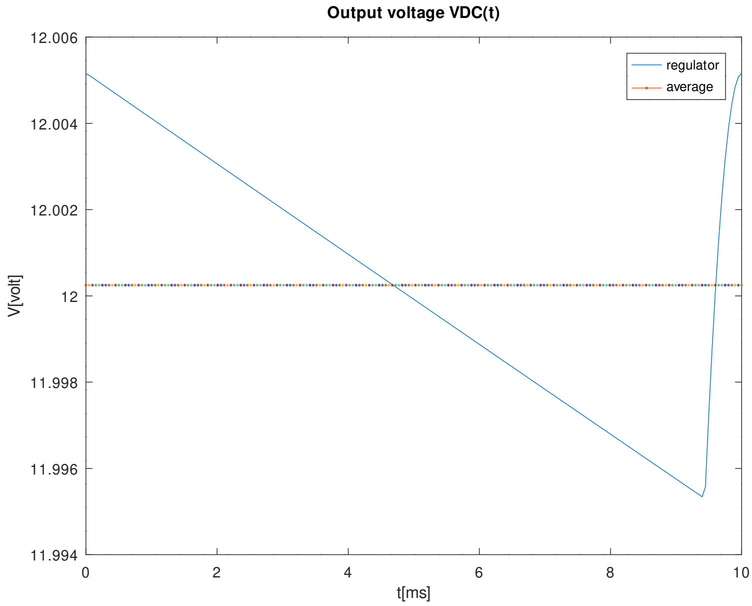

Figure 9: DC Output Signal.

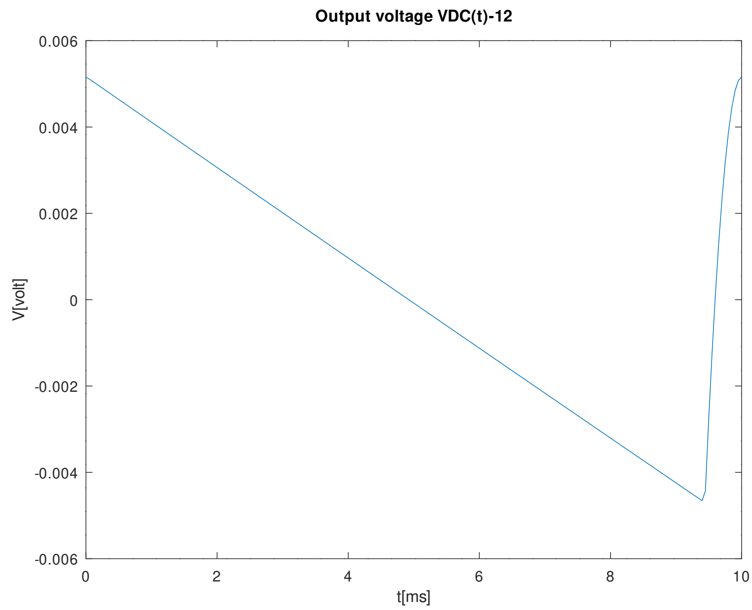

Figure 10: Output Signal - 12 (deviation).

Name	**Value [V]**
Ripple	9.813599e-03

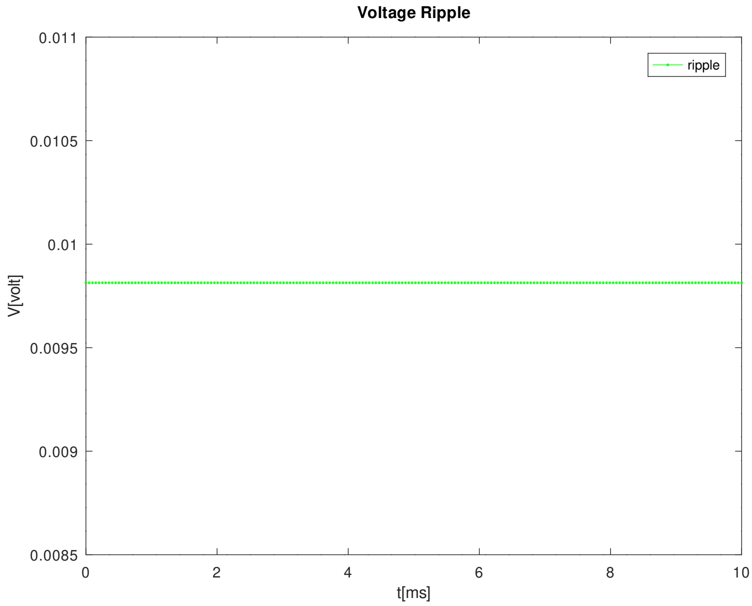

Figure 11: Ripple.

4 Conclusion

Summing up, this laboratory provided us the opportunity to understand how the envelope detector and voltage regulator circuits work and, also, how to improve their efficieny.

Contrarily to the previous lab assignments, there are some differences between the theoretical and simulation values obtained. This can be explained by the non linear components used in this laboratory: the diodes. In the previous lab assignments only linear components were used and because of that the simple theoretical analysis made matched perfectly the simulation analysis, as it should. This was no longer the case in this assignment.

As for the merit figure calculation, we used Spice's values as they provide the most accurate results.

Finally, we are going to compare the results from simulation and theoretical analysis side by side:

Name	Value
Resistor Cost	2.730000e+01
Capacitor Cost	2.100000e+01
Diode Cost	2.500000e+00
Total Cost	5.080000e+01
Merit	3.367655e+00

Figure 12: Merit Figure Table

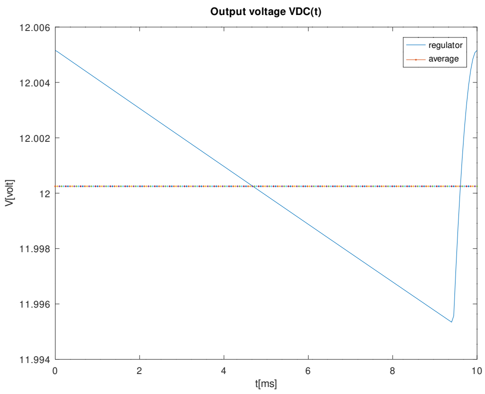

Figure 13: Theoretical Output Voltage Level

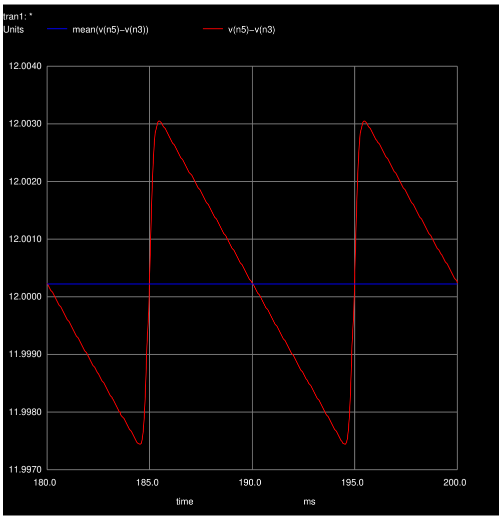

Figure 14: Simulation Output Voltage Level

Name	**Value [V]**
Ripple	9.813599e-03

Figure 15: Theoretical Ripple

Name	**Value [V]**
maximum(v(n5)-v(n3))-minimum(v(n5)-v(n3))	5.616237e-03

Figure 16: Simulation Ripple

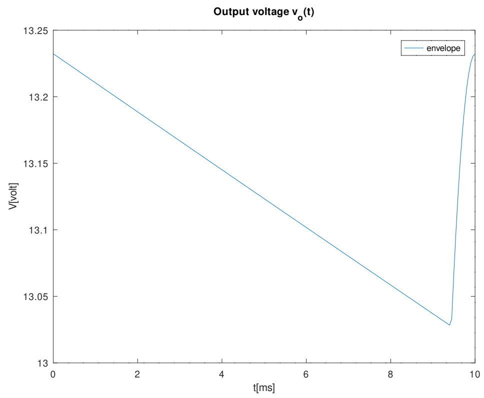

Figure 17: Theoretical Envelope Detector Voltage Level

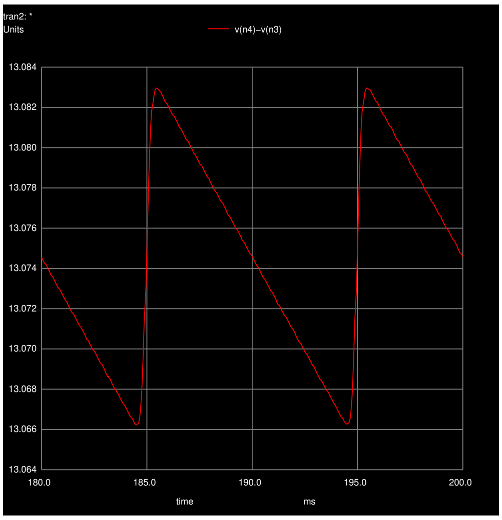

Figure 18: Simulation Envelope Detector Voltage Level

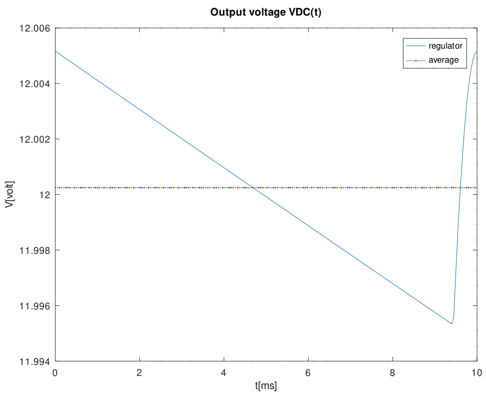

Figure 19: Theoretical Voltage Regulator Voltage Level

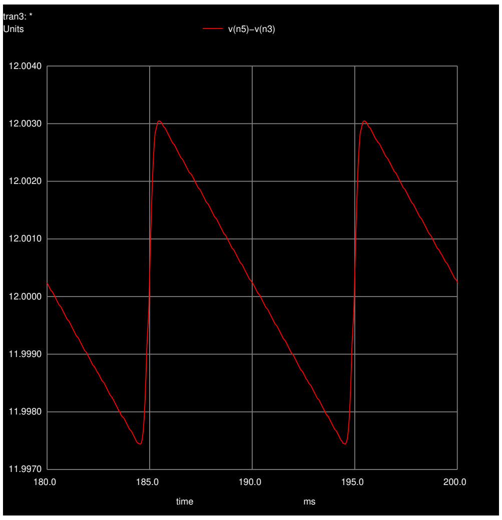

Figure 20: Simulation Voltage Regulator Voltage Level

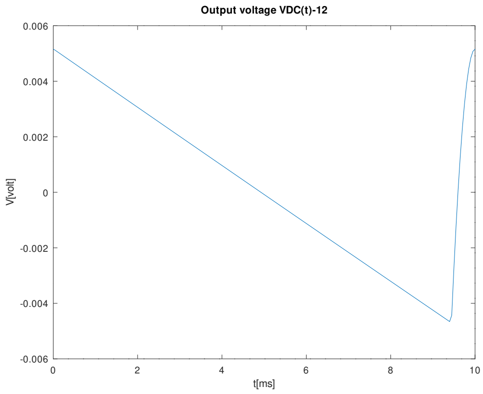

Figure 21: Theoretical $v_0 - 12$ Voltage Level

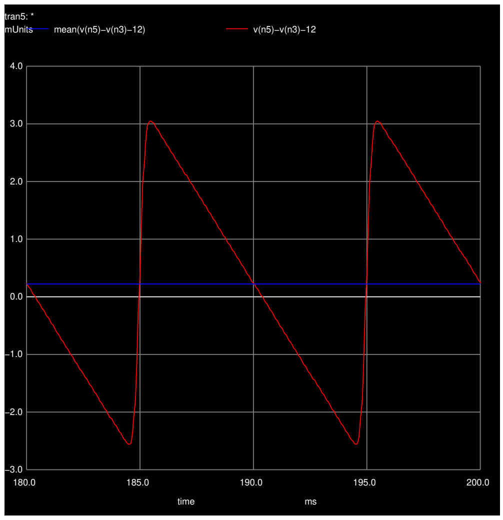

Figure 22: Simulation $v_0 - 12$ Voltage Level