TÉCNICO LISBOA

Circuit Theory and Electronics Fundamentals

Department of Electrical and Computer Engineering, Técnico, University of Lisbon

T4's Laboratory Report

Group 5

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Contents

1 Introduction

The objective of this laboratory assignment is to choose the architecture of the Gain and Output amplifier stages.

Firstly, we started this laboratory writing an NGspice script that simulates the the audio amplifier, based on the script given. The transistor models used were the NPN transistor for gain stage and the PNP Transistor for the output stage. We have also measured the output voltage gain in the passband, the lower and upper 3dB cut off frequencies, the bandwidth

(which is the difference between the upper and lower cut off frequencies) and the input/output impedances.

Then, we have performed incremental modifications to improve the merit, which is calculated using the expression:

$$M = \frac{(VoltageGain)(bandwidth)}{Cost(lower_{Cutoff}freq)} \tag{1}$$

Where:

Cost = cost of resistors + cost of capacitors + cost of transistors

Cost of Resistors = 1 monetary unit per kOhm

Cost of capacitor = 1 monetary unit per μ F

Cost of transistors = 0.1 monetary units per transistor

After that, using octave, we have created a theoretical DC model able to compute de operating point, comparing it to Ngspice's OP. We have also computed the values of the gain, input and output impedances separately for the 2 stages, the frequency response V_i/V_o

Firstly, we have created a simple circuit and then we were updating the circuit to improve the figure of merit. The final circuit obtainned is the one shown below in figure (Fig.1):

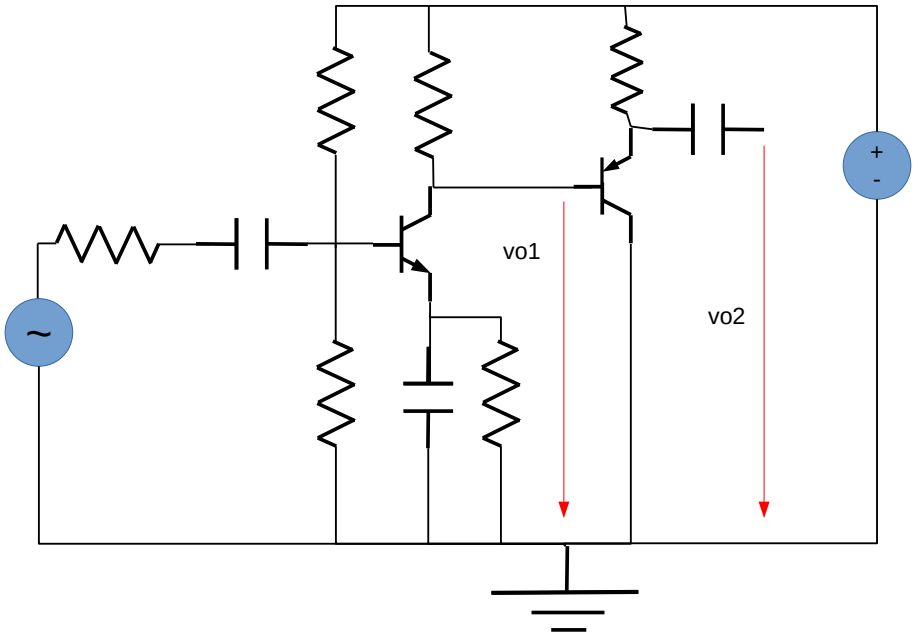

Figure 1: Final circuit

The individual costs of the components used:

Name	Value
R	93.5 kΩ
C	1300 μS
Transistors	2 Units

Figure 2: Costs

2 Simulation analysis

As said in the introduction, the first step to this laboratory assignment was to simulate an Audio Amplifier using the script given by the professor in NGSpice. This script included both a gain stage as well as an output stage.

After running the given script and implementing some code in order to get the figures asked by the professor, we performed incremental modifications to increase the merit figure.

2.1 Operating Point

After modifying the circuit we made NGSpice output the operating point values for every branch in the circuit in order to compare the results with the ones we got in the Theoretical Analysis in Octave.

The results we got are in the table below

Name	Values [V]
base	2.015175e+00
coll	4.447948e+00
emit	1.316056e+00
emit2	5.174543e+00
in	0.000000e+00
in2	0.000000e+00
out	0.000000e+00
out0	0.000000e+00
vcc	1.200000e+01

Figure 3: Simulation Operating Point

2.2 Output Voltage Gain in the Passband

Another value requested by the laboratory assignment was the output voltage gain in the passband. This was achieved by dividing the output voltage by the input voltage.

In the images below we can see both the input and output voltages plotted. The voltage gain value obtained is also in the table below:

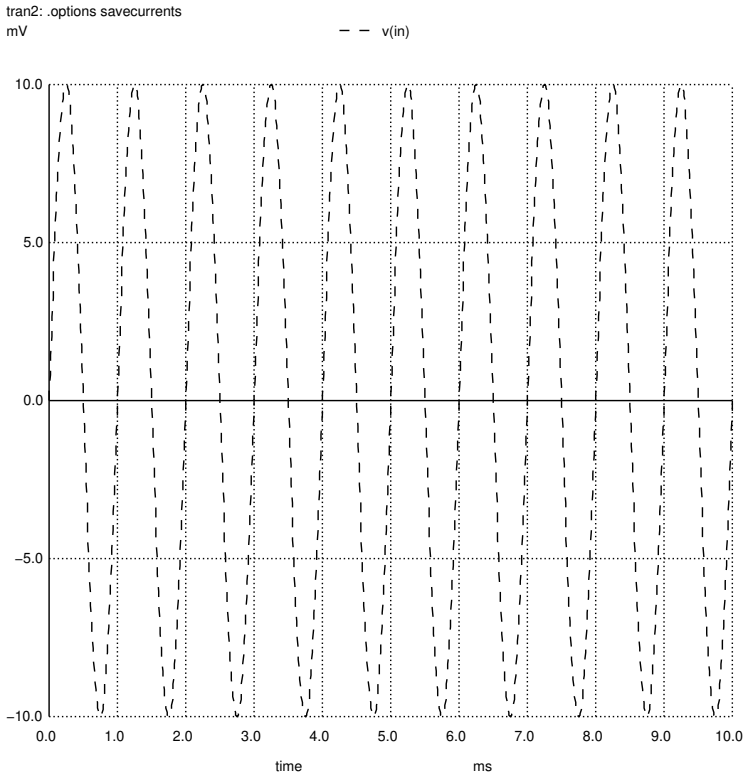

Figure 4: Input Voltage.

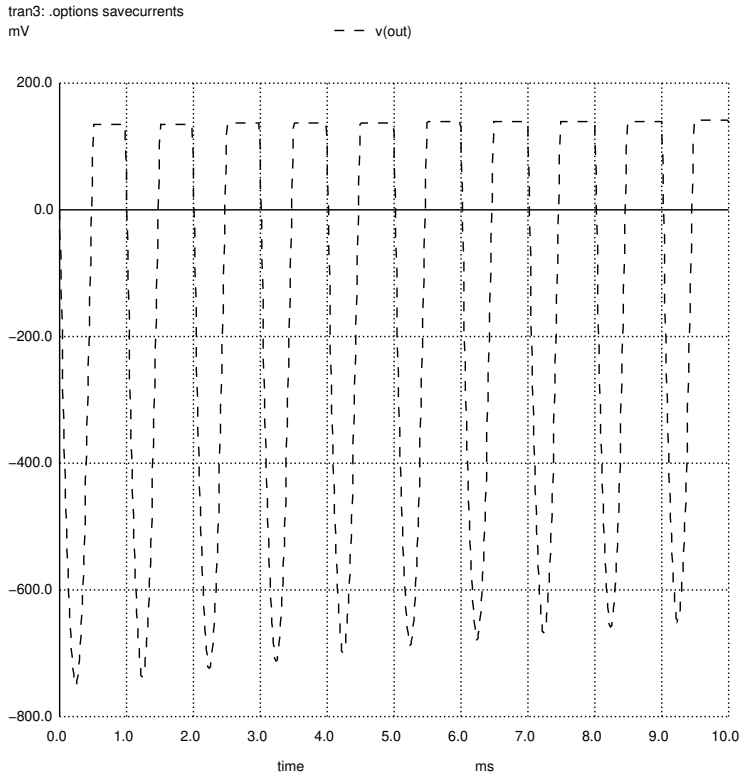

Figure 5: Output Voltage.

Name	**Value [dB]**
voltagegain	4.041081e+01

Figure 6: Simulation Voltage Gain

2.3 Lower and Upper $3dB$ cutoff frequencies and Bandwidth

After getting the output voltage gain in the previous subsection, we plotted the voltage gain in dB in order to the frequency so that we could get the bandwidth.

In the image below we can see the plot described above and the $3dB$ line. The lower and upper cutoff frequency and the bandwidth are also in the table below with $lower$ being the lower cutoff frequencies and $upper$ the upper cutoff frequency.

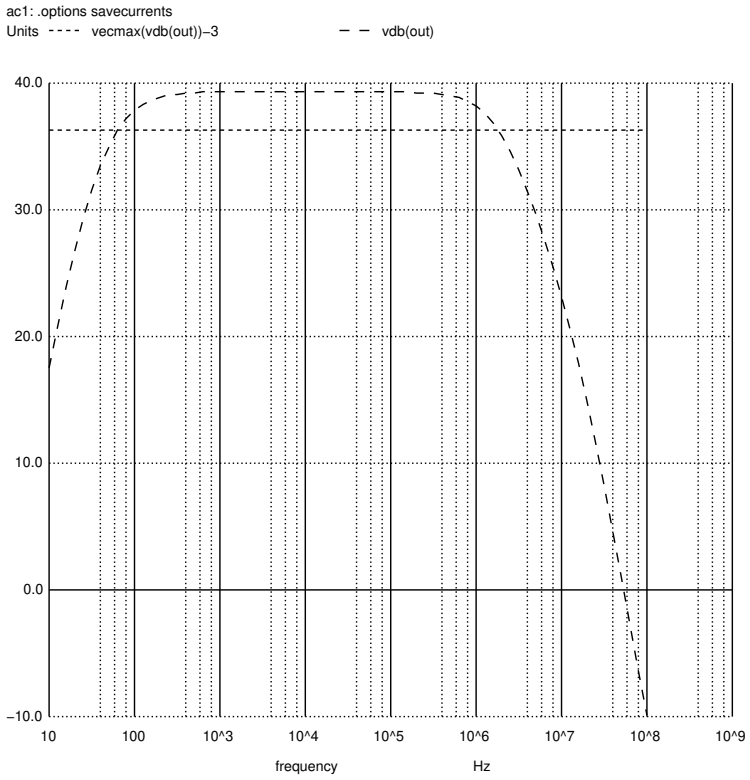

Figure 7: Frequency Analysis

Name	Value [Hz]
lower	6.448078e+01
upper	1.805464e+06
bandwidth	1.805400e+06

Figure 8: Simulation Bandwidth

2.4 Input and Output Impedances

Lastly, we made NGSpice give us the input and output impedances.

The results we got are in the table below:

Name	Value [Ω]
inputimpedance	8.123863e-01,-1.48743e-01
outputimpedance	8.000000e+00,-0.000000e+00

Figure 9: Simulation Input and Output Impedances

3 Theoretical Analysis

3.1 Operating Point

Firstly, we started by altering the octave script given by the professor to suit the simulation we had made. We then proceeded to get the operating point analysis in order to compare it to the operating point analysis made in the simulation section.

Below are two table with the OP for both the gain and output stages:

Name	Value [V or A]
$IB1$	5.676895e-05
$IC11$	1.014461e-02
$IE1$	1.020138e-02
$VO1$	1.855388e+00
$VThevenin$	2.608696e+00
VE	1.020138e+00

Figure 10: Theoretical Operating Point Gain Stage

Name	Value [V or A]
$IC2$	2.350811e-02
$IE2$	2.361153e-02
$VI2$	1.855388e+00
$VO2$	2.555388e+00

Figure 11: Theoretical Operating Point Output Stage

3.2 Simulating the gain stage

After doing the OP analysis, we proceeded to simulate the gain stage, that will increase de signal's gain, and the output stage, that will have to regulate the output (due to the high impedance signal from the gain stage).

From the gain stage, we have the following gain (dB) plot:

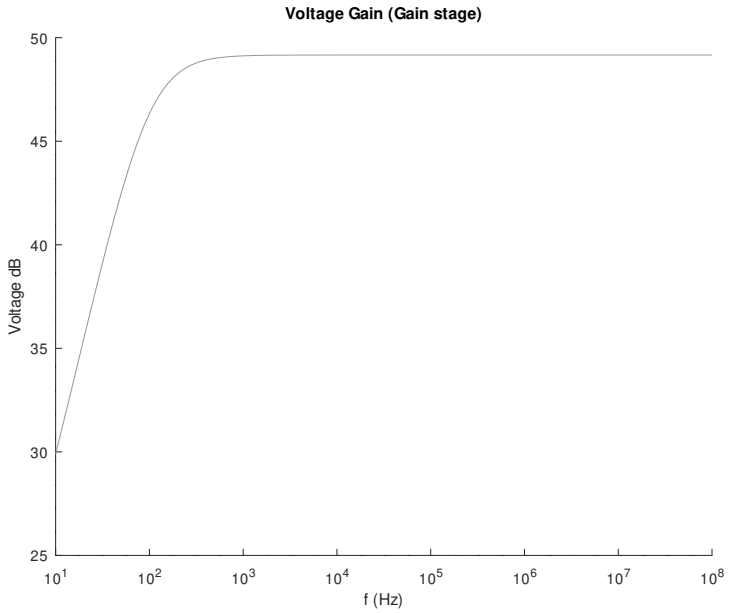

Figure 12: Voltage Gain (Gain stage).

3.3 Output stage

For this stage, we also have a voltage gain plot that is in the image below.
The plot shows us the gain in dB.

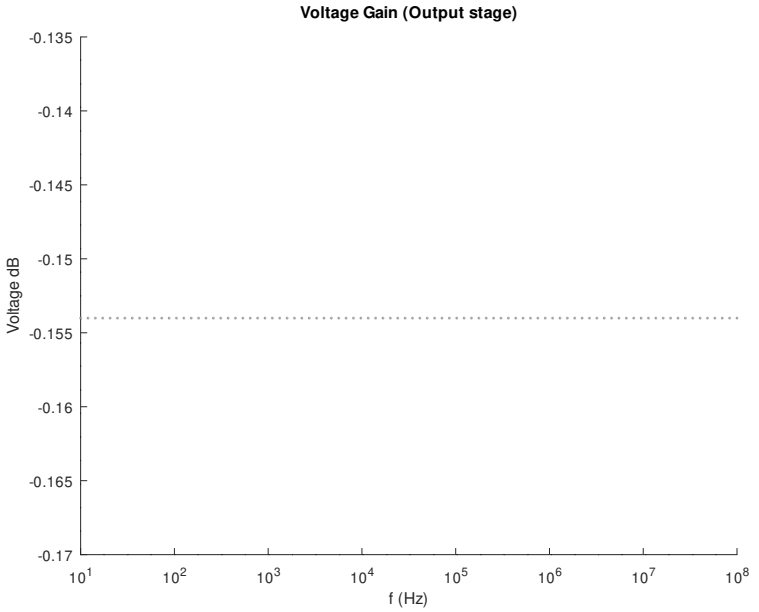

Figure 13: Voltage Gain (Output stage).

3.4 Frequency Response

Taking into account the all circuit, we can obtain the frequency response (db):

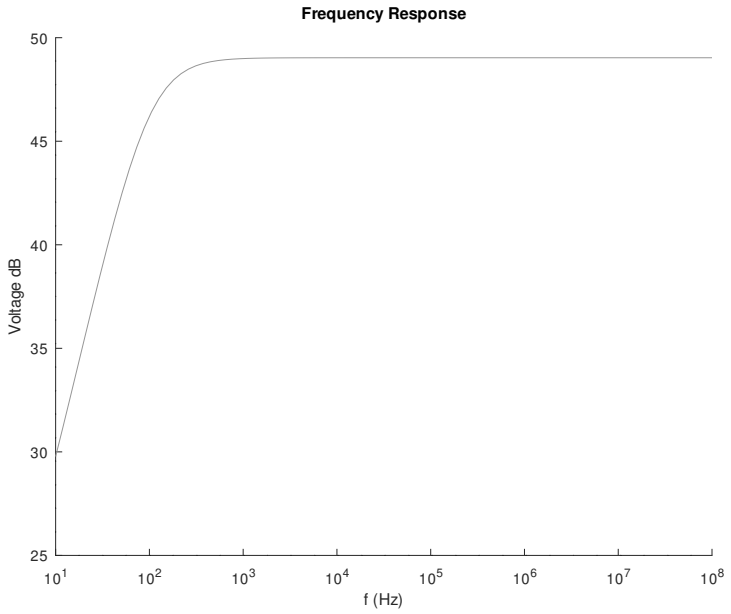

Figure 14: Frequency Response.

3.5 Impedance

Summing up, we have these results for impedance:

Name	Value [Ω]
Input Impedance Gain Stage	4.283303e+02
Output Impedance Gain Stage	8.729456e+02
Input Impedance Output Stage	3.151207e+04
Output Impedance Output Stage	1.055305e+00
Total Input Impedance	4.283303e+02
Total Output Impedance	4.808946e+00

Figure 15: Theoretical Input and Output Impedances

Ideally, the input impedance (Z_I) should be infinite. However, since it is much greater than R_s (source output resistance, which is 100 Ω), our input signal will not be degraded (by the input impedance). Basically, there is no problem to connect this input source through the coupling capacitor and amplifier input.

The output impedance of the gain stage is almost 3 times lower than the input inpedance of the output stage, which is not ideal, but this is acceptable, so this two modules can be connected, with some degradation of the signal.

4 Conclusion

Summing up, this laboratory provided us the opportunity to understand how an audio amplifier circuit works with both its gain and output stages.

Similarly to the previous lab assignment, there are some differences between the theoretical and simulation values obtained, this is the case for the OP analysis and also the impedances, for example. This can be explained by the non linear components used in this laboratory: the transistors. In the first 2 lab assignments only linear components were used and because

of that the simple theoretical analysis made matched perfectly the simulation analysis, as it should. This was no longer the case in this assignment.

As for the merit figure calculation, we used Spice's values as they provide the most accurate results.

Finally, we are going to compare the results from simulation and theoretical analysis side by side:

Name	Value
merit	8.118416e+02

Figure 16: Merit Figure Table

Name	Value [V or A]
$IB1$	5.676895e-05
$IC11$	1.014461e-02
$IE1$	1.020138e-02
$VO1$	1.855388e+00
$VThevenin$	2.608696e+00
VE	1.020138e+00

Figure 17: Theoretical Operating Point Gain Stage

Name	Value [V or A]
$IC2$	2.350811e-02
$IE2$	2.361153e-02
$VI2$	1.855388e+00
$VO2$	2.555388e+00

Figure 18: Theoretical Operating Point Output Stage

Name	Value [V]
base	2.015175e+00
coll	4.447948e+00
emit	1.316056e+00
emit2	5.174543e+00
in	0.000000e+00
in2	0.000000e+00
out	0.000000e+00
out0	0.000000e+00
vcc	1.200000e+01

Figure 19: Simulation Operating Point

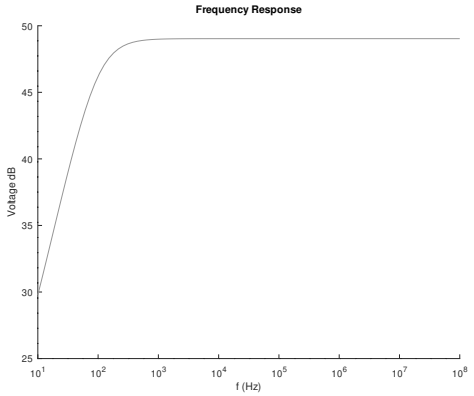

Figure 20: Theoretical Gain Frequency Response

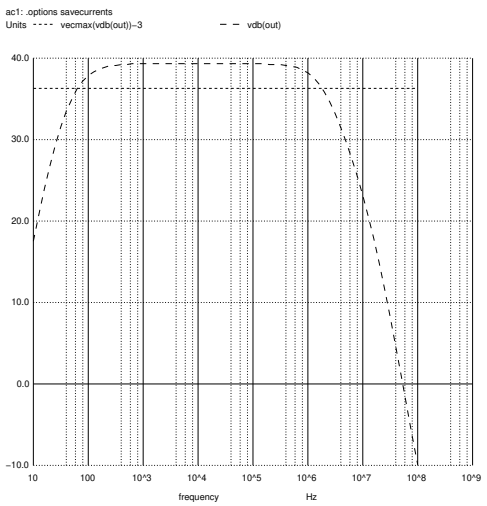

Figure 21: Simulation Gain Frequency Response

Name	Value [Ω]
Input Impedance Gain Stage	4.283303e+02
Output Impedance Gain Stage	8.729456e+02
Input Impedance Output Stage	3.151207e+04
Output Impedance Output Stage	1.055305e+00
Total Input Impedance	4.283303e+02
Total Output Impedance	4.808946e+00

Figure 22: Theoretical Input and Output Impedances

Name	Value [Ω]
inputimpedance	8.123863e-01,-1.48743e-01
outputimpedance	8.000000e+00,-0.000000e+00

Figure 23: Simulation Input and Output Impedances