TÉCNICO LISBOA

Circuit Theory and Electronics Fundamentals

Department of Electrical and Computer Engineering, Técnico, University of Lisbon

T2's Laboratory Report

Group 5

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Contents

1 Introduction

The objective of this laboratory assignment is to choose the architecture of the envelope and voltage regulator circuits in order to have the best merit (M) possible.

Firstly, we started this laboratory writing an NGspice script that simulates the AC/DC converter and measure the output voltage level and voltage ripple , ploting the the voltages at the

output of the envelope detector and voltage regulator circuits and the output AC component + DC deviation).

Then, using octave, we have created a theoretical model able to predict the output of the envelope detector and voltage regulator circuits, ploting the same results as in simulation analysis (using theoretical analysis). Finally, also the output DC level and the voltage ripple were computed.

The merit is calculated using the following expression:

$$M = \frac{1}{Cost(ripple(v_0) + average(v_0 - 12) + 10^{-6})} \tag{1}$$

Where:

Cost = cost of resistors + cost of capacitors + cost of diodes

Cost of Resistors = 1 monetary unit per kOhm

Cost of capacitor = 1 monetary unit per μ F

Cost of diodes = 0.1Monetary units per diode

Firstly, we have created a simple circuit and then we were updating the circuit to improve the figure of merit. The final circuit obtainned is the one shown below in figure (Fig.1):

Figure 1: Final circuit

The individual costs of the components used:

- Diodes - cost: 2.3MU;
- Capacitor - 5MU;
- Resistances - 55MU.

The data used was the following:

Name	**Value [F, V, Ω or S]**
R_1	1.04765357286e3
R_2	2.06140068334e3
R_3	3.03459085363e3
R_4	4.00398818216e3
R_5	3.11499853456e3
R_6	2.04588646991e3
R_7	1.04390152967e3
V_s	5.02522591213
C	1.00982536324e-6
K_b	7.28209304852e-3
K_c	8.36641247715e3

2 Theoretical Analysis

2.1 Question 1: Node Analysis

This preliminary analysis of the circuit is the basis of the rest of the work and to do this we used the nodal method in the same way as used in T1. We have the equations: (the nomenclature for all nodes and branches is present in figure 1).

Node 0 (ground):

$$\frac{1}{R_1}(V_2 - V_1) + \frac{1}{R_4}(V_5 - 0) - I_d = 0 \tag{2}$$

Node 2:

$$\frac{1}{R_1}(V_1 - V_2) + \frac{1}{R_2}(V_3 - V_2) + \frac{1}{R_3}(V_5 - V_2) = 0 \tag{3}$$

Node 3:

$$\frac{1}{R_2}(V_2 - V_3) + I_b = 0 \tag{4}$$

Node 5:

$$\frac{1}{R_3}(V_2 - V_5) + \frac{1}{R_5}(V_6 - V_5) + \frac{1}{R_4}(0 - V_5) - I_d = 0 \tag{5}$$

Node 6:

$$\frac{1}{R_5}(V_5 - V_6) - I_b - I_c = 0 \tag{6}$$

Node 7:

$$\frac{1}{R_6}(V_7 - 0) + I_d = 0 \tag{7}$$

Node 8:

$$\frac{1}{R_7}(V_7 - V_8) - I_d + I_c = 0 \tag{8}$$

Additional equation:

$$V_5 - V_8 - K_d I_d = 0 \tag{9}$$

Additional equation:

$$V_2 - V_5 - \frac{I_b}{K_b} = 0 \tag{10}$$

And the results are shown in the following table:

Name	Value [A or V]

All the variables preceded by I are currents and are expressed in Ampere, the other variables, preceeded by V are voltages and are expressed in Volt.

2.2 Question 2: Equivalent Resistance (R_{eq})

The resolution of this question was based on the suggestion presented. Firstly, we set $V_s = 0$ and replaced the capacitor by a voltage source $V_x = V_6 - V_8$ and ran the nodal analysis in order to obtain the current I_x witch is the current supplied by V_x.

Then, with the equation:

$$R_{eq} = \frac{V_x}{I_x} \tag{11}$$

We obtain the Equivalent resistance.

The time constant τ is calculated by doing $\tau = R_{eq}C$

Since the capacitor was replaced by a Voltage source witch terminals have the same difference of potential as $V_6 - V_8$ in Question 1, this is a known variable that corresponds to V_x (V_{eq}). I_x can also be obtainned by running the nodal method with $V_s = 0$. We needed to do this because there is no faster way to calculate the Equivalent Resistance in a circuit where there are resistances in paralell, in series and a capacitor. Basically, the procedure was based on *Thévenin* theorem to obtain R_{eq}which is equal to$(V_x - V_s)/I_x$. By doing this, we have $V_x = R_{eq}I_x$, where R_{eq} is the only unknown variable.

The results:

Name	Value [A or V]

2.3 Question 3: Natural solution $v_{6t}(t)$

The natural solution $v_{6t}(t)$ can be obtained in the interval $[0, 20]ms$, by doing:

$$V_6(t) = V_{6n}(t) + V_{6f}(t) \tag{12}$$

Where:

$$V_{6n}(t) = Ae^{\frac{-t}{\tau}} \tag{13}$$

And $v_{6f}(t = 0s)$ because $v_s(t = 0s) = 0$
Then:

$$V_6(0) = V_x(0) + V_8(0) \tag{14}$$

So ($v_8(t = 0s) = 0$):

$$V_6(0) = V_x(0) \tag{15}$$

Finally, we get the natural solution:

$$V_x = Ae^{\frac{-t}{\tau}} \tag{16}$$

By doing this, the plot obtained is the one shown below:

Figure 2: Natural solution $v_{6t}(t)$

2.4 Question 4: Forced solution $v_{6f}(t)$ ($f = 1kHz$)

In this question, we have used a phasor voltage source $V_s = 1$, since $\phi = 0$, we get:

$$v_s = sen(2\pi ft) => v_s = -(sen(\phi_s) + icos(\phi_s)) \tag{17}$$

So, $v_s = -i$.

$$Z_c = \frac{1}{j\omega c} \tag{18}$$

Where $\omega = 2\pi f$ and $f = 1000Hz$.

Then, replacing C with impedance Z_c and running the nodal analysis to determine the phasor voltages in all nodes we have the following results:

Name	Value [V]

We have calculated the module of V_6 with "abs" Octave's function. Then, the phase is calculated with the angle function of octave by doing (-angle(phasor voltage 6)).

Where R_{eq} and C are the equivalent resistance and the Capacitor's capacitance, respectively.

And, finnaly, the forced solution is given by the expression:

$$V_{6f} = V_6 cos(2\pi ft - phase_6) \tag{19}$$

and the following plot:

Figure 3: Forced solution $v_{6t}(t)$

where V_6 is the module value, calculated in the previous expression.

2.5 Question 5: Final solution $v_6(t)$

The final total solution is given by:

$$V_6(t) = V_{6n}(t) + V_{6f}(t) \tag{20}$$

Considering the time period of $[0; 20]ms$:
$v_s = sin(2\pi ft)$ and $v_6(t) = v_{6n}(t) + v_{6f}(t)$ Considering the time period of $[-5, 0]ms$ (In this period of time there is no variation of v_s and so, v_6 is also constant, as seen before):
$v_s = V_s(initialvalue)$ and $v_6(t) = V_6$.
The results ($v_6(t)$ - blue, $v_s(t)$ - red):

Figure 4: Final solution $v_6(t)$

2.6 Question 6: Frequency response

The main focus of this procedure was to determine the frequency response $v_6(f)$, $v_c(f)$ and $v_s(f)$ for a frequency range of 0.1Hz to 1Mhz (using logarithmic scale for f).

As mention before, the impedance expression is:

$$Z_c = \frac{1}{j\omega c} \tag{21}$$

Then, we ran the nodal analysis (like in question 4) for each value of frequency determining the phaser voltage in each node, which allowed us to determine the $v_6(f)$, $v_c(f) = v_6(f) - v_8(f)$ and $v_s(f)$ values. As seen before, the phasor voltage v_s value is independet from he frequency and so, it is constant ($v_s = -i$).

We have used the magnitude values in dB and phase in degrees, in order to represent the results:

$$magnitude(dB) = 20log_{10}(abs(x)) \tag{22}$$

And,

$$phase(degrees) = \frac{180}{\pi} angle(x) \tag{23}$$

where x is the phasor voltage.
The v_s is the blue line, v_c green and the v_6 the red one.
The results are shown in the following plots:

Figure 5: Magnitude of phasor voltages (dB)

Figure 6: Phase of phasor voltages (degrees)

Analysing the plots, we realised that v_s is a constant value in the plot since it equals $v_s = -i$ which represents 0dB (because logaritm's magnitude is 0). Also, the phase is constant.

The values of v_c and v_6 aren't constant. The logarithm of v_6 goes from positive values to negative values because it becomes less than 1.

The plot of v_6 doesn't not equal the plot of v_c because $v_c = v_6 - v_8$ and v_8 is not 0.

3 Simulation analysis

3.1 Simulating the AC/DC converter for 10 periods

As said in the introduction, the first step to this laboratory assignment was to simulate a simple AC/DC converter in NGSpice, the circuit features an ideal transformer, using a current controlled voltage source as well as a voltage controlled current source as explained by the professor in a previous lecture, as well as an envelope detector and a voltage regulator.

This AC/DC converter was simulated for 10 periods and all the analysis were made measuring on a $5e-5$ step in order to evaluate at least 1000 points during the 10 periods. In order to calculate this step we used the frequency of the AC source to know the period and then we multiplied this period by 10 in order to get the total time. We then divided the total time by 1000 points and made the step even smaller than that in order to make sure it had more than 1000 points but not too small that the program ran slowly.

This circuit was first made simple and was elaborated along the way, making it output the correct voltage, increasing the merit figure.

3.2 Output voltage level

After describing the circuit we made NGSpice measure the average output voltage and using a transient analysis we plotted both the average and the signal of the output voltage in the same graph.

The table and the graph below show the results we got.

Name	**Value [V]**
mean(v(n5)-v(n3))	1.199970e+01

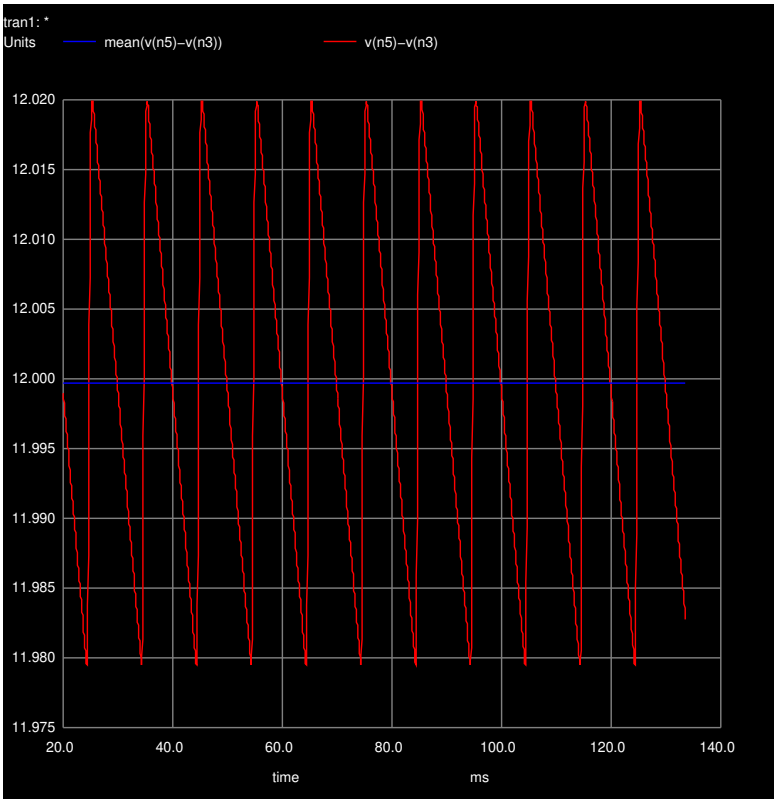

Figure 7: Plot of the average and the signal of the Output Voltage.

3.3 Output of the Envelope Detector and voltage Regulator circuits

The output voltages of both the Envelope Detector as well as the Voltage Regulator circuits were plotted and put each in a different graph as well as a graph with both voltages plotted.

The three graphs are in the images below.

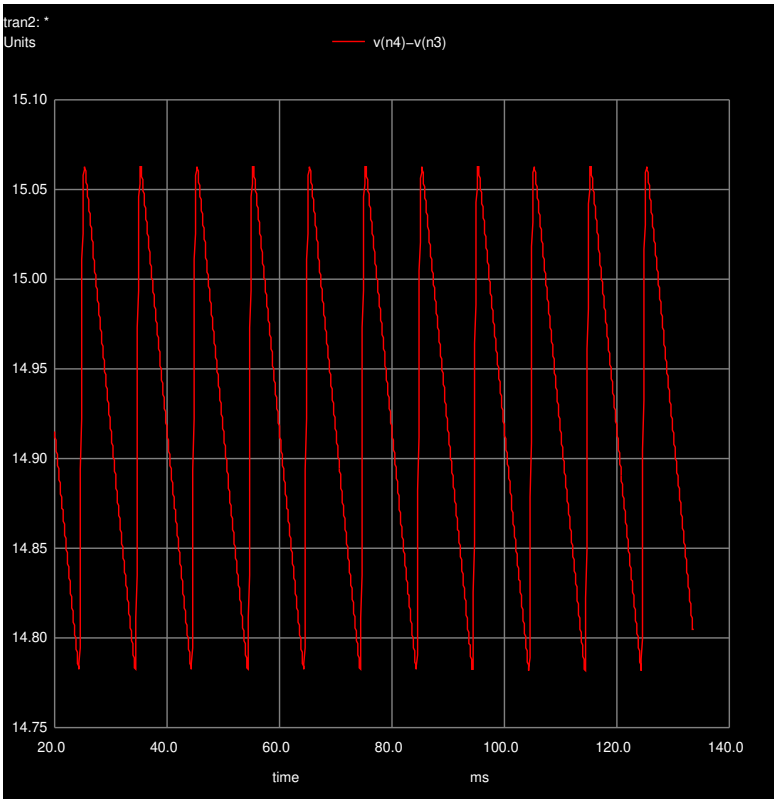

Figure 8: Envelope Detector Output Voltage.

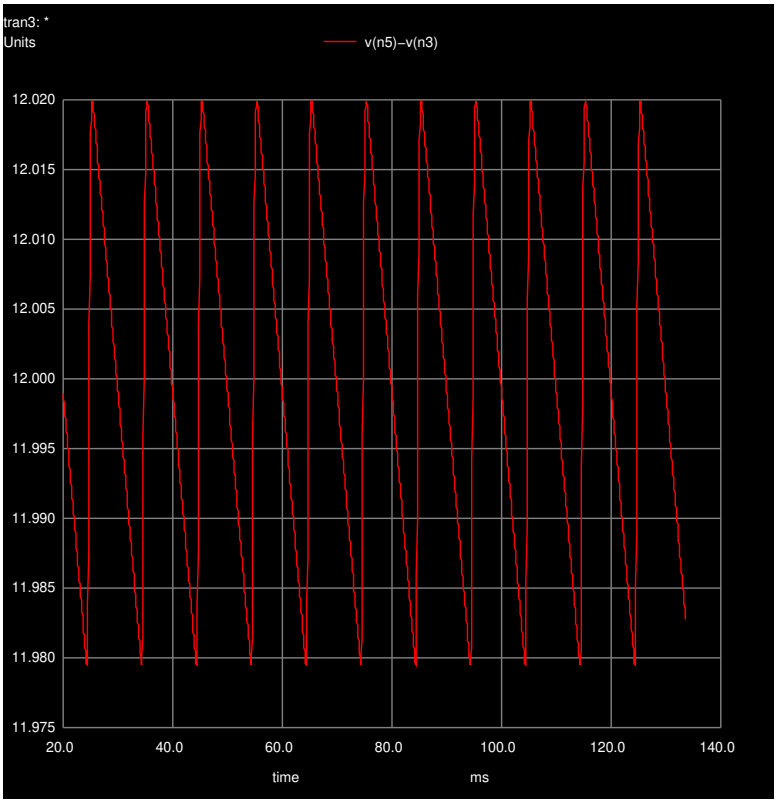

Figure 9: Voltage Regulator Output Voltage.

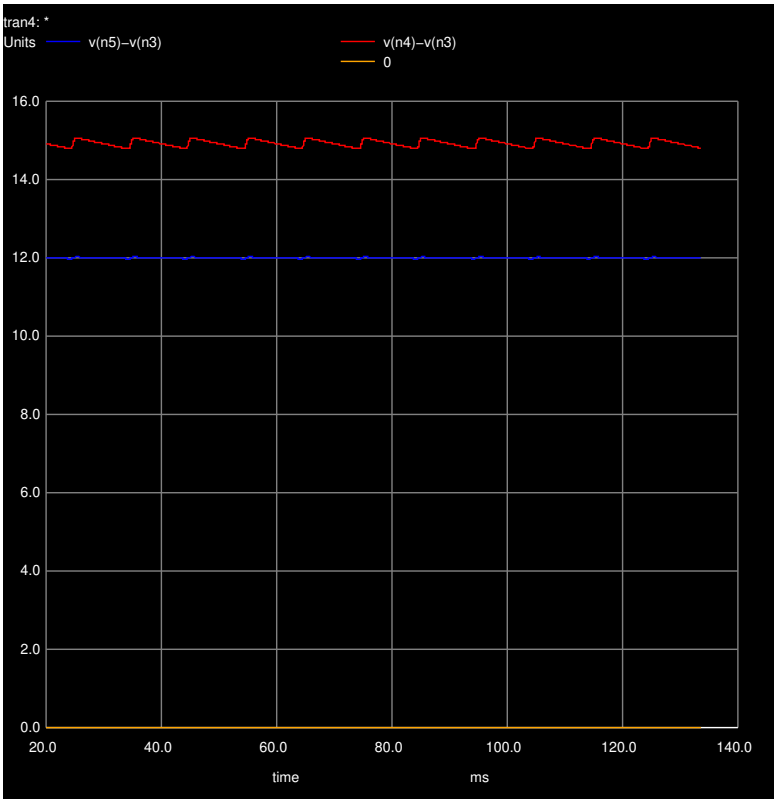

Figure 10: Envelope Detector and Voltage Regulator Output Voltages.

3.4 Output voltage ripple

We then made NGSpice measure the output voltage ripple, that is the difference between the maximum and the minimum values of the signal.

The result we got is in the table below.

Name	Value [V]
maximum(v(n5)-v(n3))-minimum(v(n5)-v(n3))	4.042821e-02

3.5 $v_0 - 12$ plot

Lastly, we plotted $v_0 - 12$, which corresponds to the output AC component plus the DC deviation.

The plot can be seen in the image below.

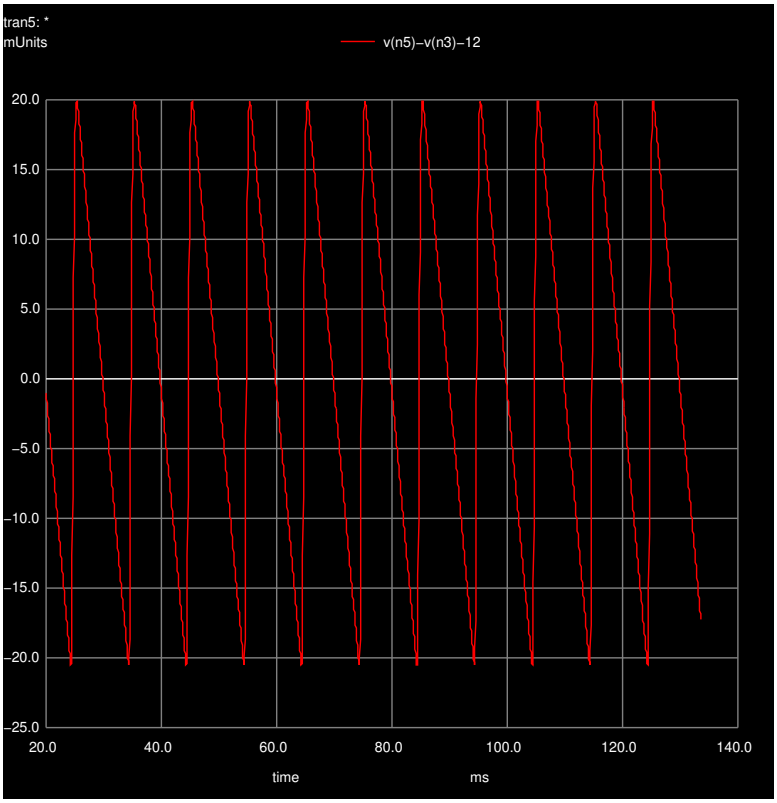

Figure 11: Output AC component + DC deviation.

4 Conclusion

Summing up, in this laboratory assignment (T2) we have made both theoretical analysis as well as simulations of several different but similar and correlated circuits.

The results obtained in both analysis were either put in a table or plotted in order to make comparations between the theoretical and simulation analysis. Up untill the simulation's question 4, the results are either the exact same or have very little differences on the last decimal places and so they are negligible, the explanation for this is that we studied a very simple circuit containing only linear components. If the components used were more complex, the case would not be the same and we could detect real differences between the values calculated and simulated.

Comparing figure 17 and figure 18, the theoretical value is based on a simplification when the circuit contribuition is resumed to R_{eq} and, the NGspice result is based on all the actual contributions of the circuit. Thus in the figure 18 the signal is going to be a perfect sinusoidal signal while the figure 17 displays an imperfect signal.

Lastly, for the same reasons of figure 17 and 18, there are little differences between plots in both figures.

That being said we would like to end this report by presenting both the theoretical and simulation results side by side in order to easily compare the results.

Name	Value [A or V]

Figure 12: Theoretical Question 1

Name	Value [A or V]

Figure 13: Simulation Question 1