

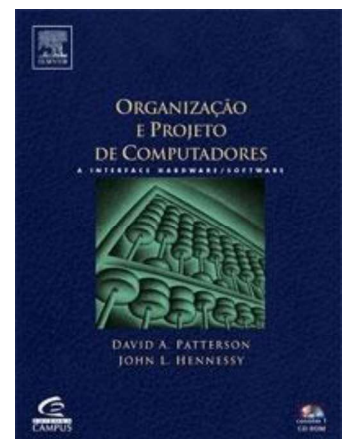
# [Aula 10] Pipeline do MIPS 1: *Introdução*

Prof. João F. Mari  
*joaof.mari@ufv.br*

## Aula 10 – Pipeline do MIPS 1 - Introdução

# Bibliografia

1. PATTERSON, D.A; HENNESSY, J.L. **Organização e Projeto de Computadores: A Interface Hardware/Software**. 3a. Ed. Elsevier, 2005.
  - Capítulo 5.
2. Notas de aula do prof. Luciano J. Senger:
  - <http://www.ljsenger.net/classroom.html>
3. Notas de aula da Profa. Mary Jane Irwin
  - CSE 331 Computer Organization and Design
  - <http://www.cse.psu.edu/research/mdl/mji/mjicourses>

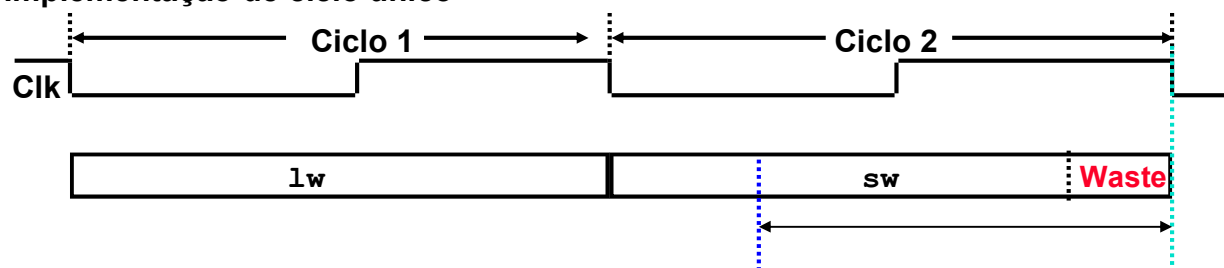


# Roteiro

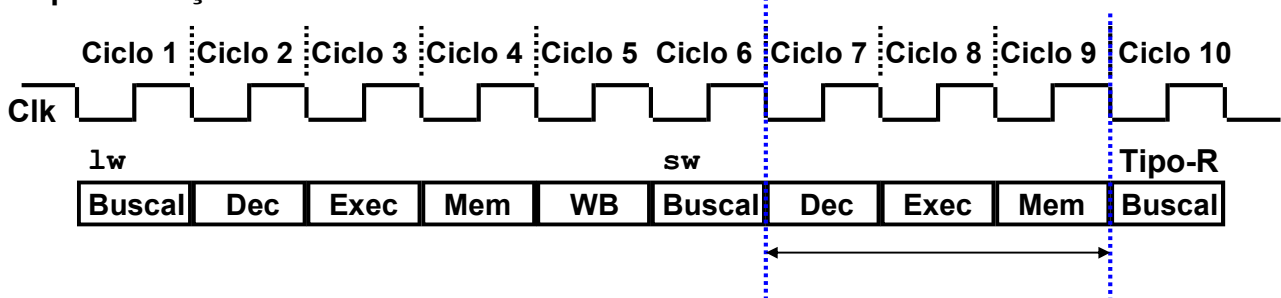
- Desempenho: Monociclo vs. Multiciclo
- Pipelining – Definição
- Desempenho: Monociclo vs Multiciclo vs. Pipelining
- Pipelining Hazards
  - Hazards Estruturais (Restrições físicas do hardware)
  - Hazards de Dados (Dados incompletos)
  - Hazards de Controle (Saltos e desvios)

## Monociclo Vs. Multiciclo

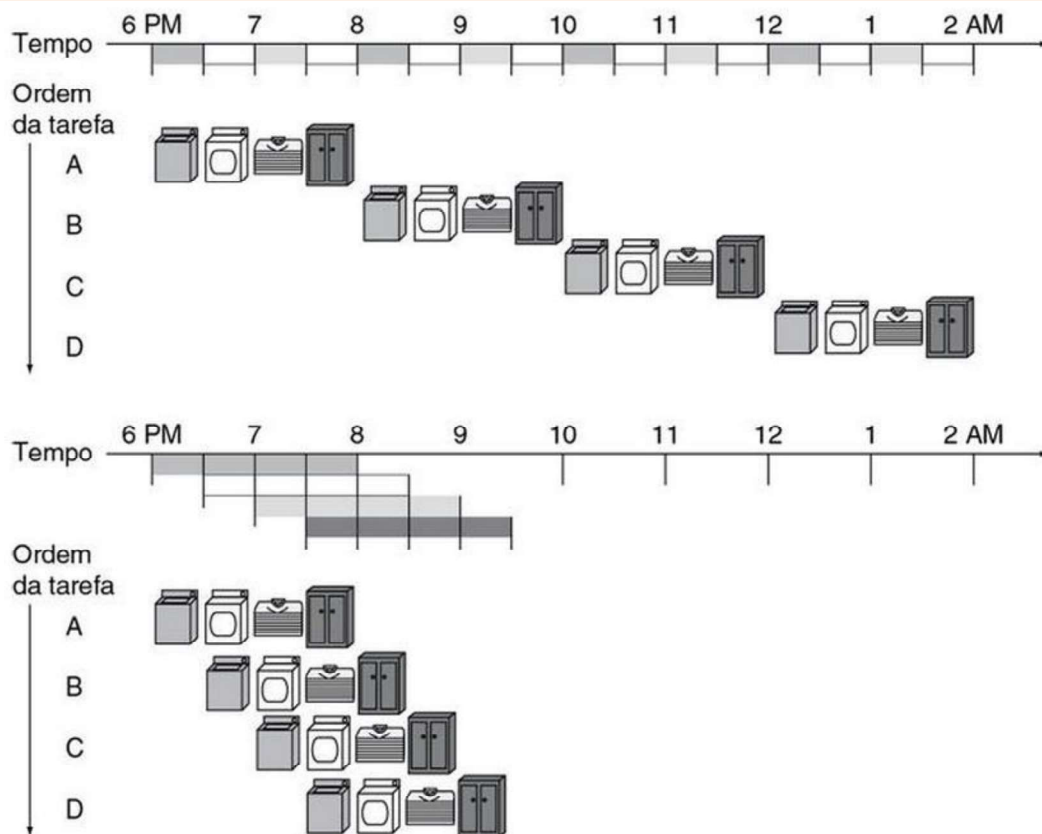
### Implementação de ciclo único



### Implementação multiciclo:



# Pipelining (analogia)

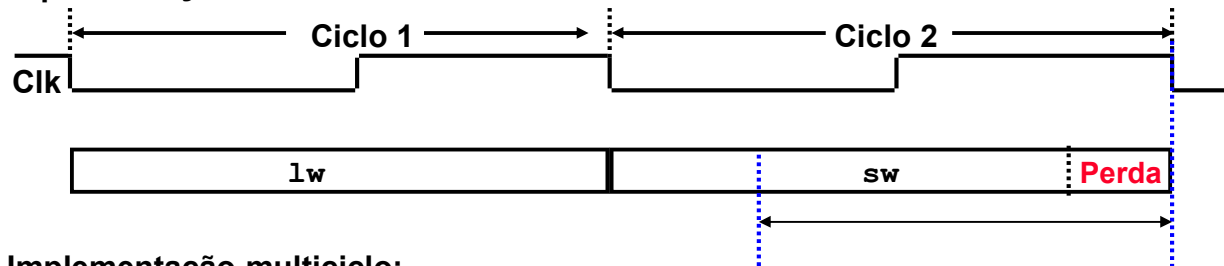


## [EX] Pipelining

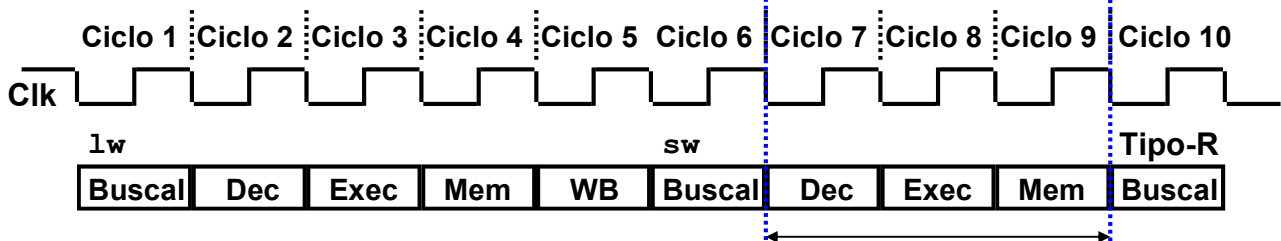
| Classe de instrução                | Busca de instrução | Leitura do registrador | Operação ALU | Acesso de dados | Escrita do registrador | Tempo total |
|------------------------------------|--------------------|------------------------|--------------|-----------------|------------------------|-------------|
| Load word (lw)                     | 200 ps             | 100 ps                 | 200 ps       | 200 ps          | 100 ps                 | 800 ps      |
| Store word (sw)                    | 200 ps             | 100 ps                 | 200 ps       | 200 ps          |                        | 700 ps      |
| Formato-R (add, sub, AND, OR, slt) | 200 ps             | 100 ps                 | 200 ps       |                 | 100 ps                 | 600 ps      |
| Branch (beq)                       | 200 ps             | 100 ps                 | 200 ps       |                 |                        | 500 ps      |

# Monociclo Vs. Multiciclo vs. Pipeline

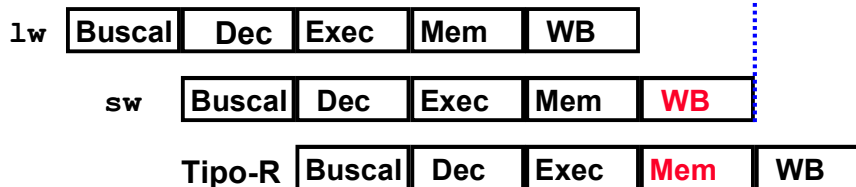
## Implementação de ciclo único



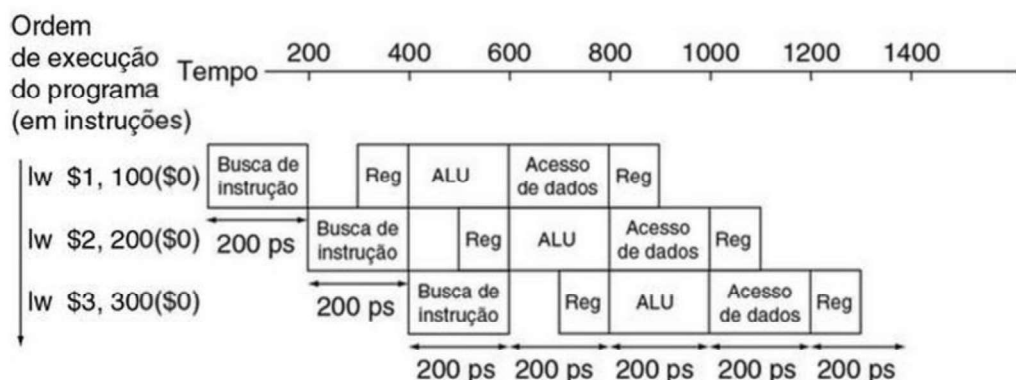
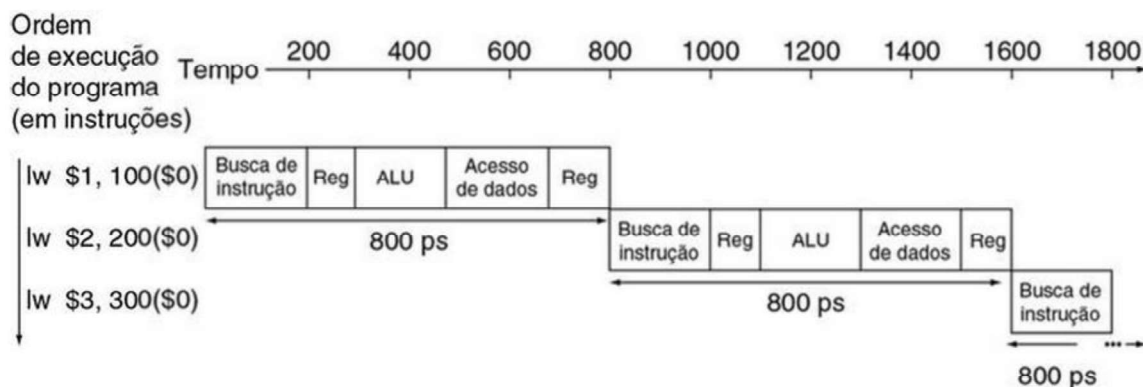
## Implementação multiciclo:



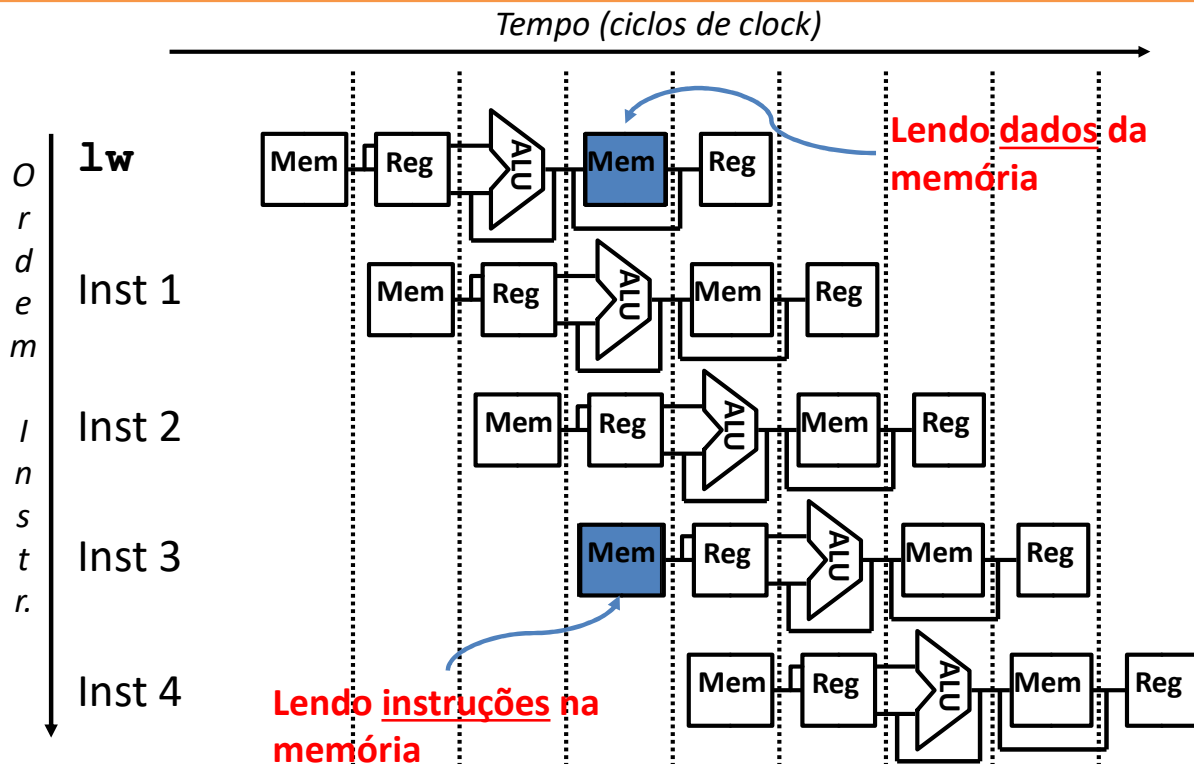
## Implementação do Pipeline:



# [EX] Pipelining

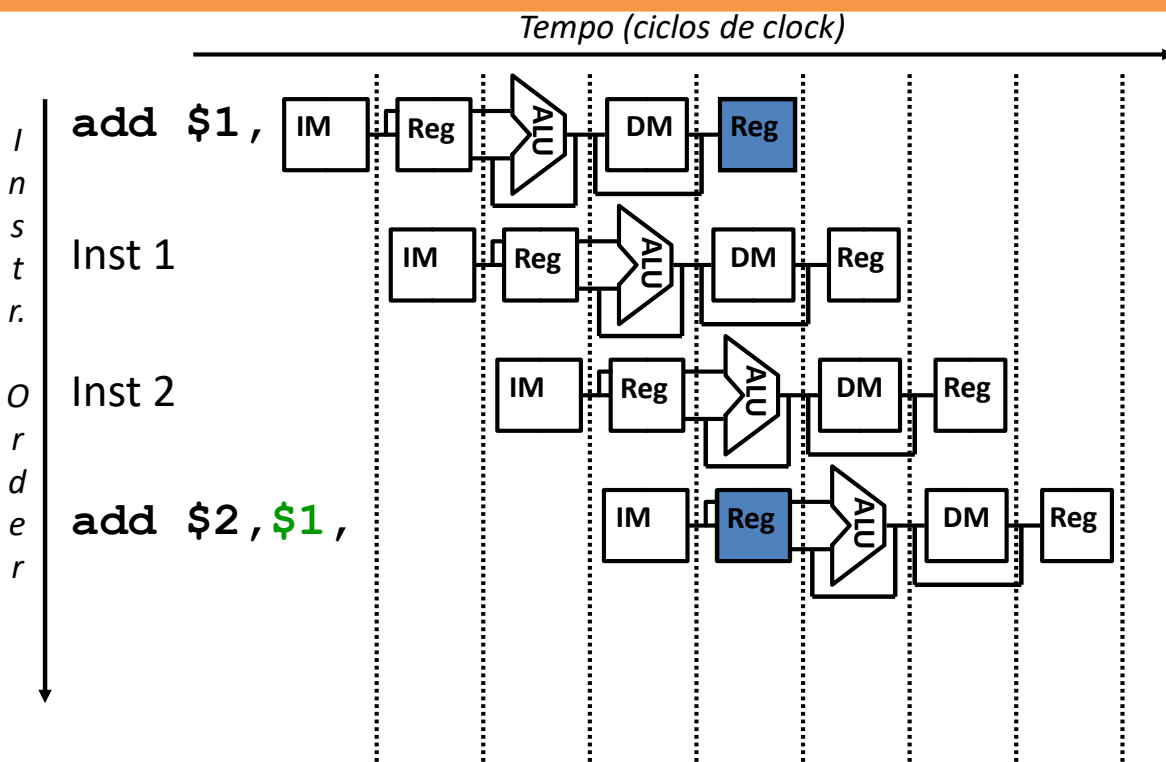


# Hazard estrutural – Memória única

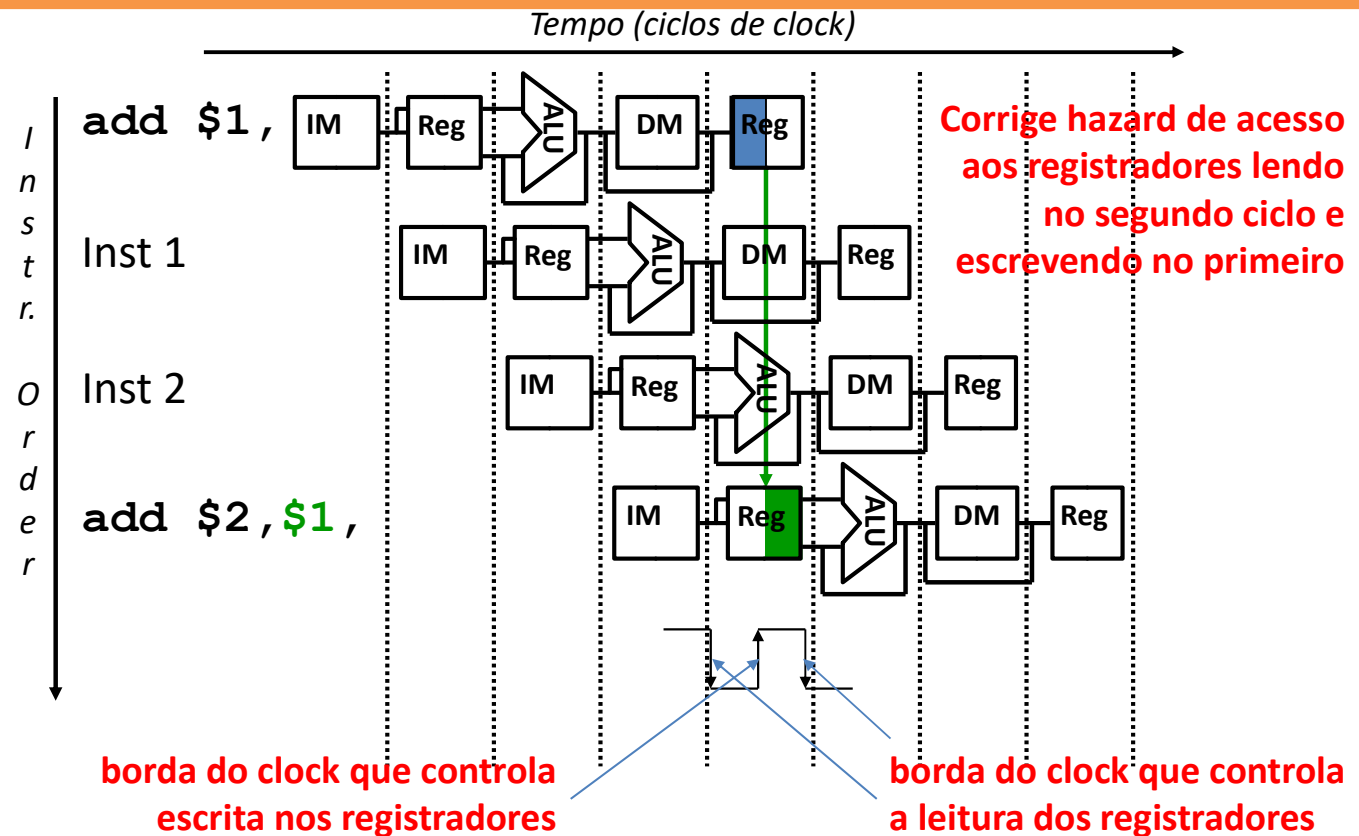


- Resolvido com memórias separadas para dados e instruções (I\$ e D\$)

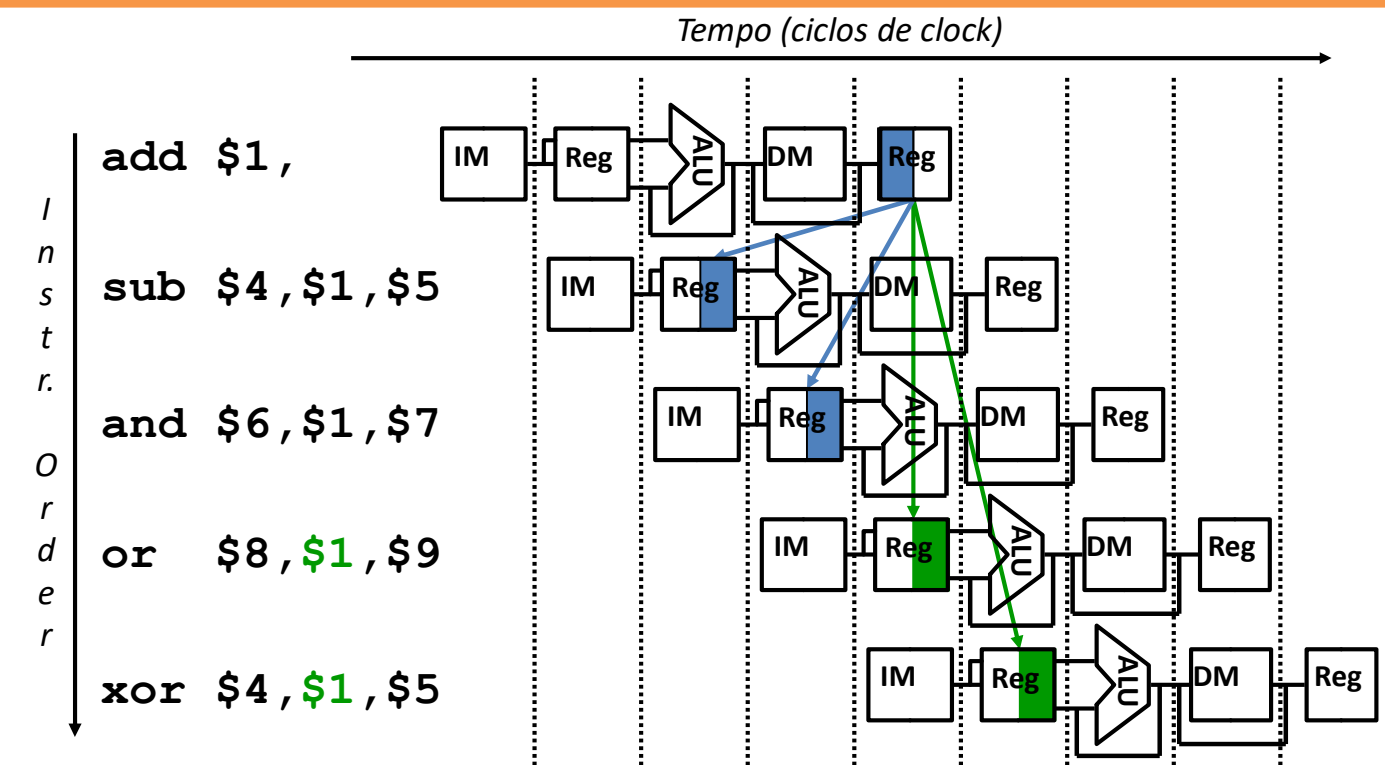
# Hazard estrutural – Acesso ao banco de registradores



# Hazard estrutural – Acesso ao banco de registradores

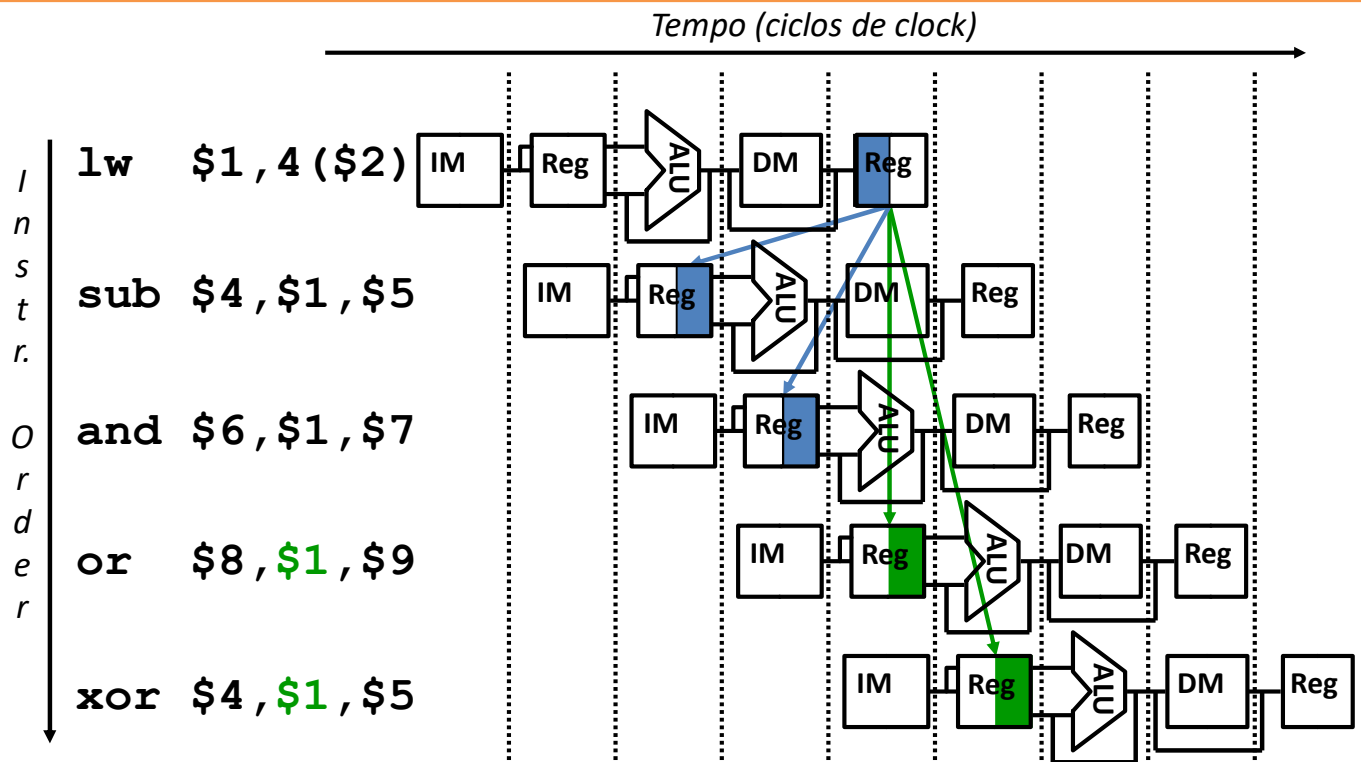


# Hazards de dados – *read before write*



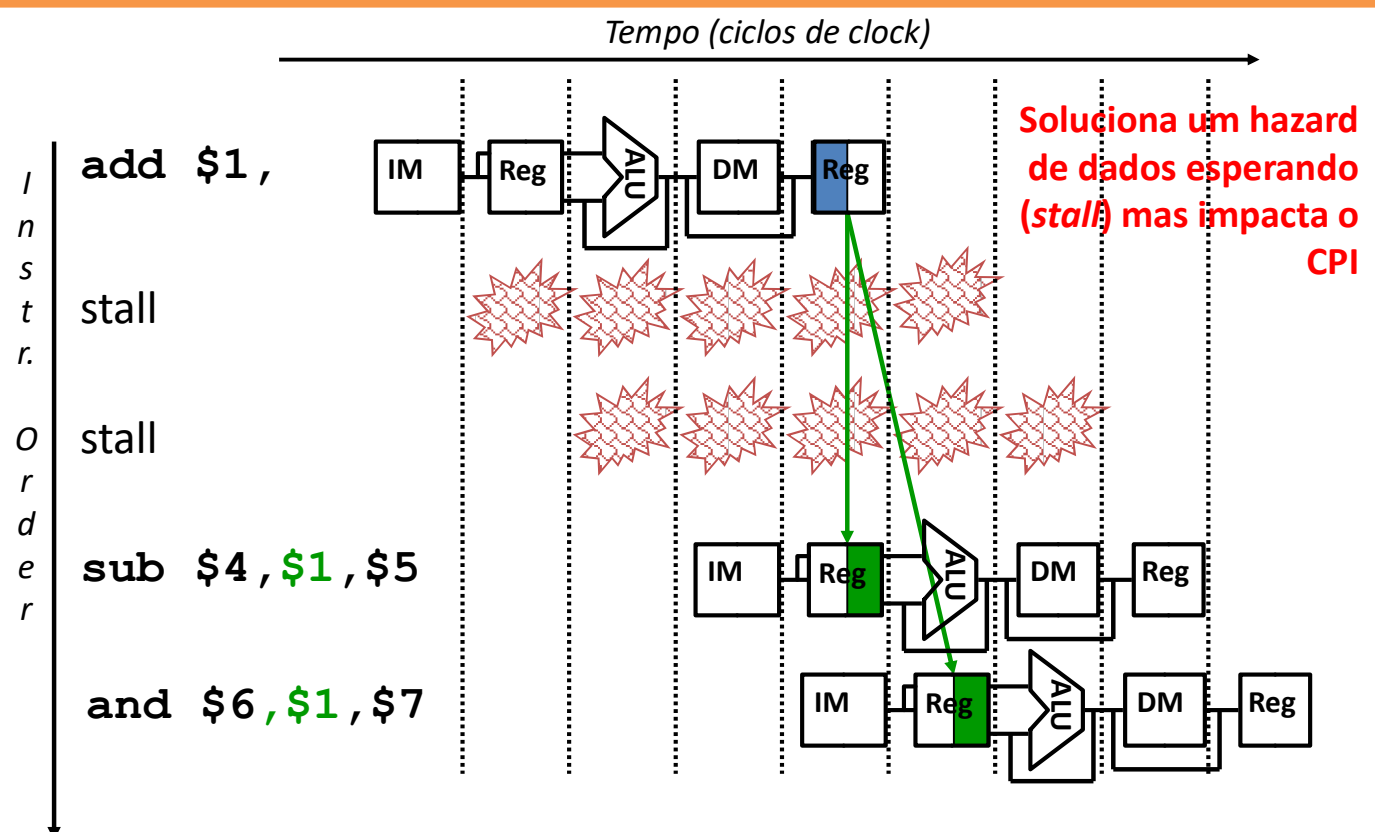
- *Ler antes de escrever*

## Hazards de dados – *load-use hazard*

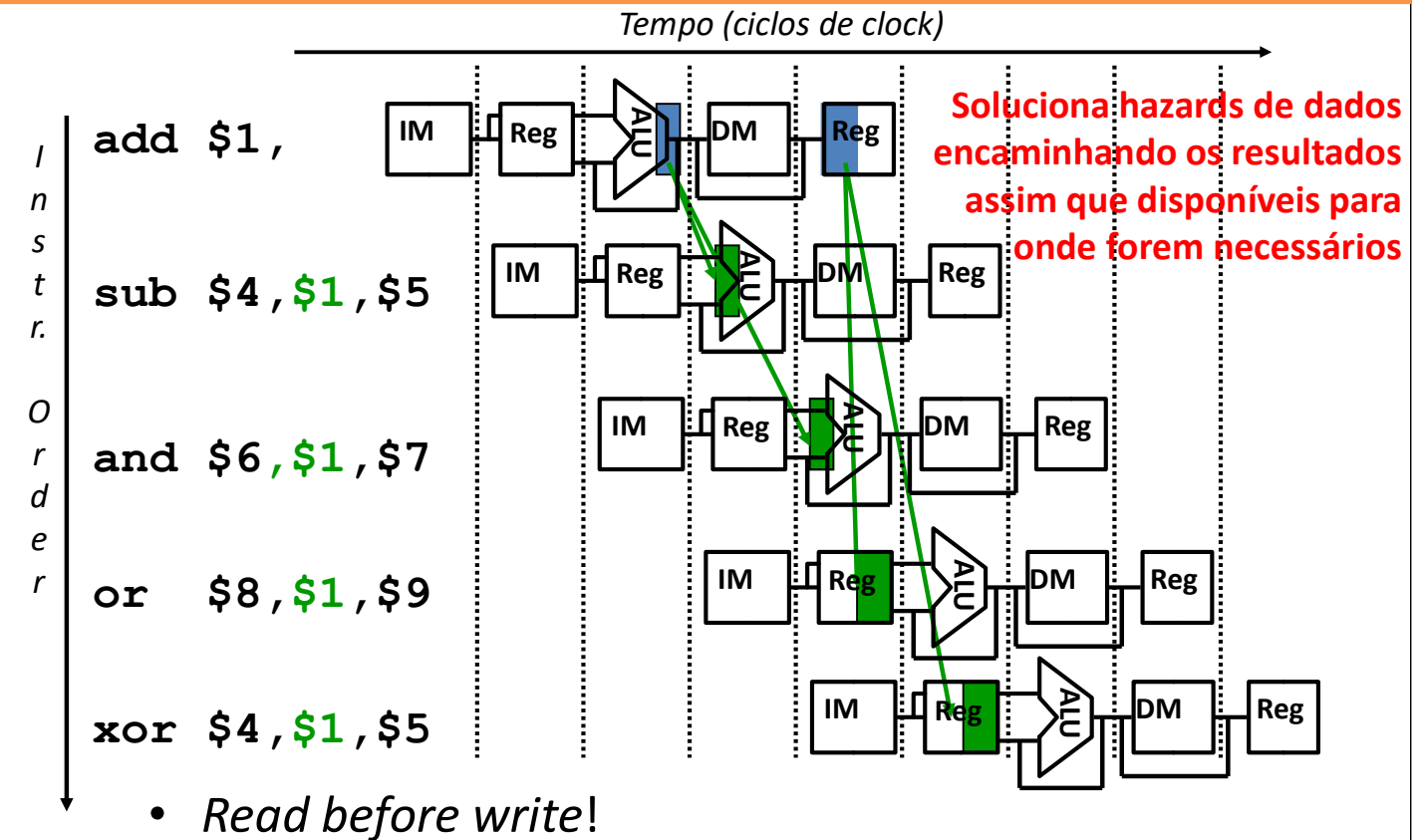


- *Usar antes de carregar!*

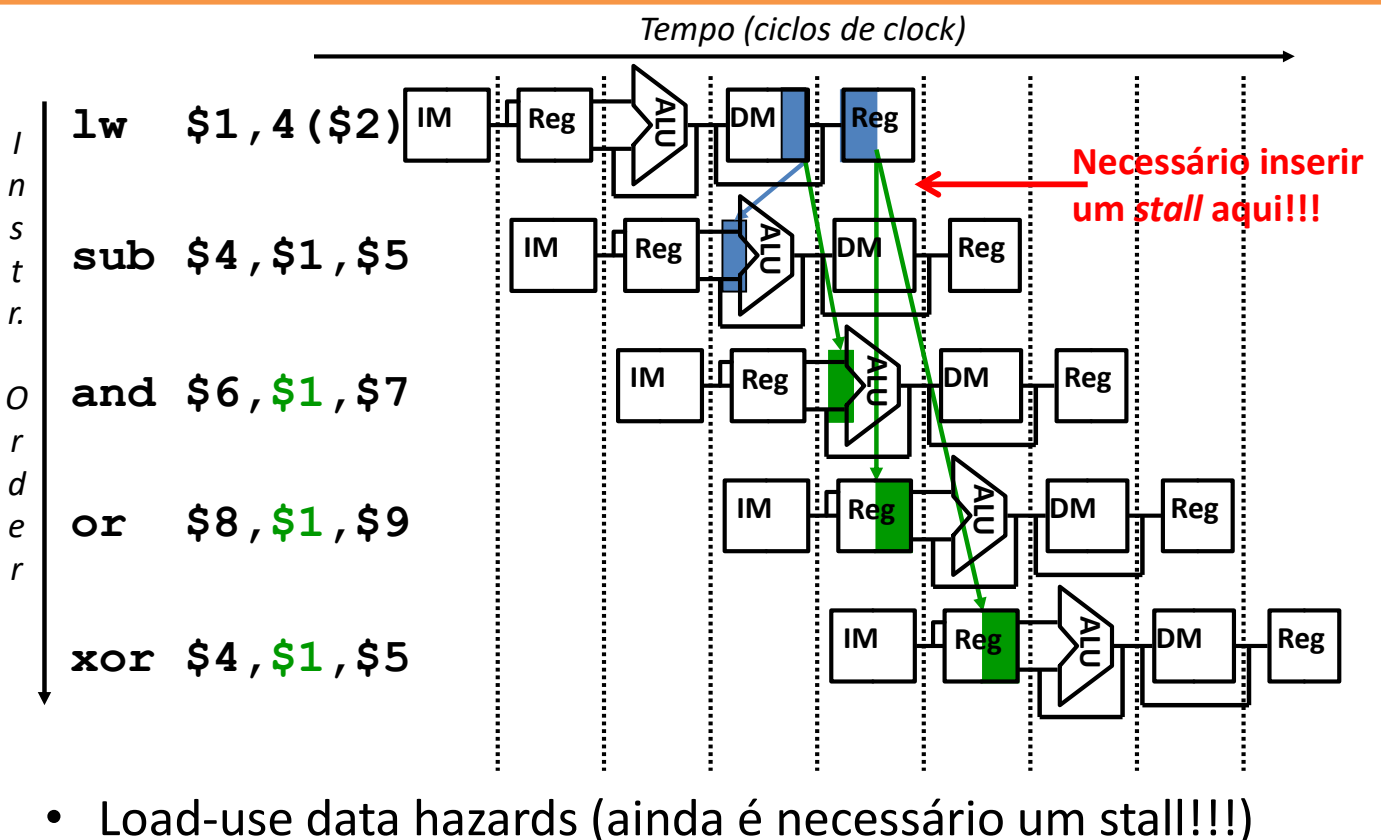
## Hazards de dados – *uma solução simples*



## Hazards de dados – *solução por encaminhamento*



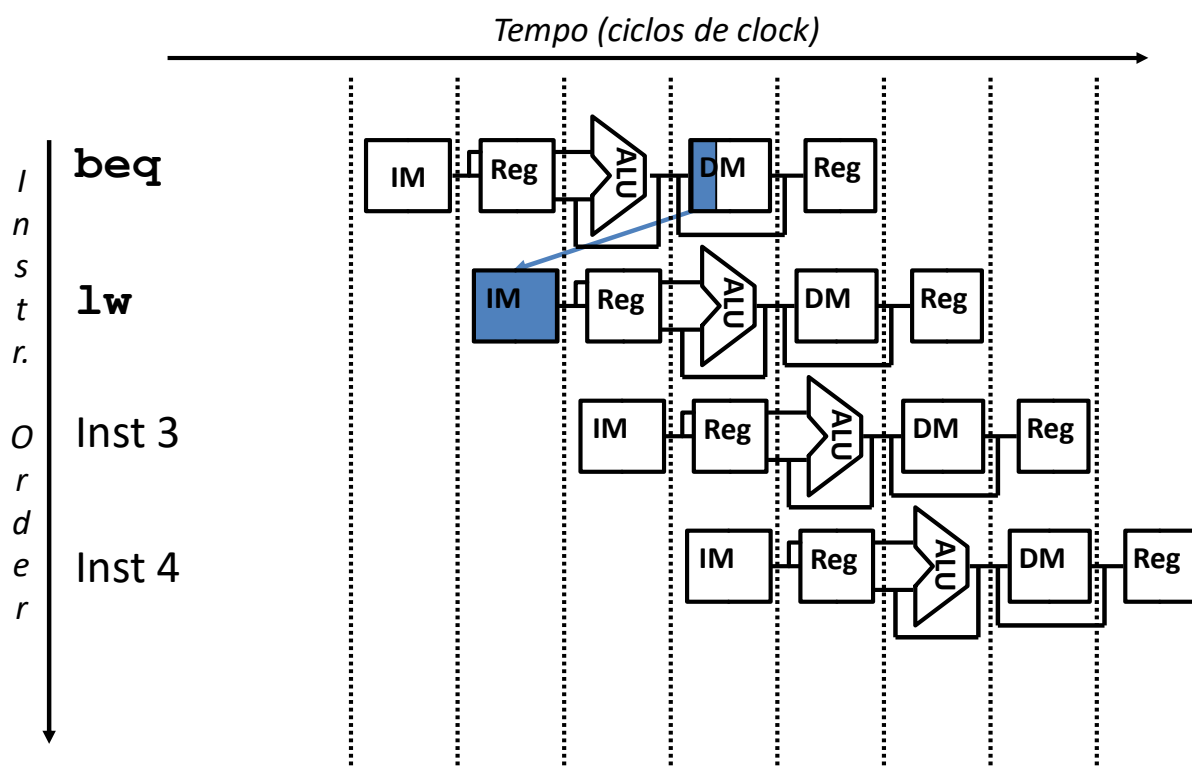
## Hazards de dados – *solução por encaminhamento*



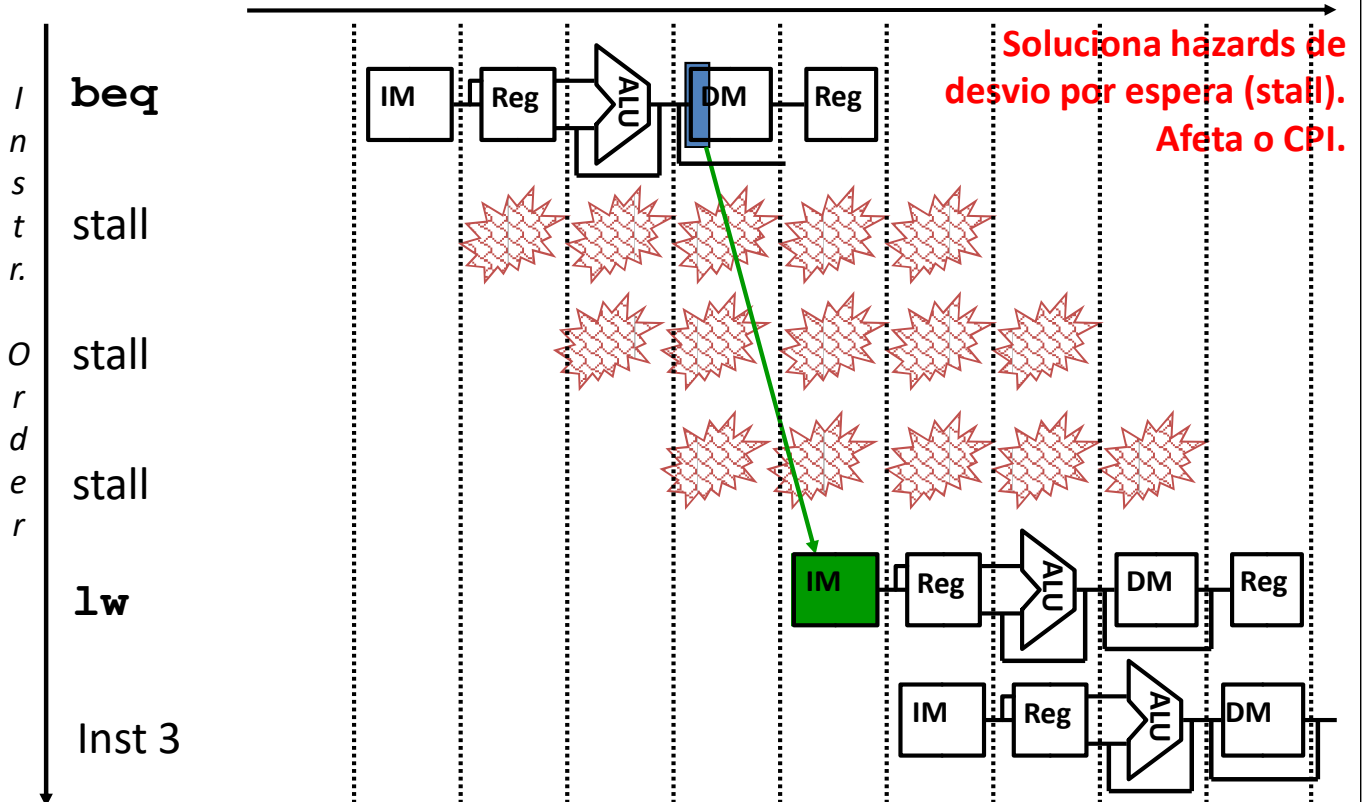


# Hazards de controle

## Hazards de controle



## Hazards de controle – solução simples



## Bibliografia

1. PATTERSON, D.A; HENNESSY, J.L. **Organização e Projeto de Computadores: A Interface Hardware/Software**. 3a. Ed. Elsevier, 2005.
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  - <http://www.cse.psu.edu/research/mdl/mji/mjicourses>



# FIM

- FIM:
  - **[Aula 10]** Pipeline do MIPS 1 - Introdução
- Próxima aula:
  - **[Aula 11]** Pipeline do MIPS 2 – Caminho de dados e controle