INSTITUTO SUPERIOR TÉCNICO

DEPARTAMENTO DE ENGENHARIA INFORMÁTICA

ORGANIZAÇÃO DE COMPUTADORES

LEIC

Conjunto de Exercícios IX

Entradas e Saídas

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Sistema de Entrada e Saída

Exercício 1*

1.1. Consider the following applications that make use of polling and interrupt handling techniques to communicate with I/O subsystems.

Application 1	Application 2
Auto Pilot	Automated Thermostat

a) Describe device polling. Would each application indicated in the above table be appropriate for communication using polling techniques? Justify your answer.

b) Describe interrupt driven communication. For each application in the table, if polling is inappropriate, explain how interrupt driven techniques could be used.

1.2. The peripherals listed below make use of interrupt handling techniques for communication. The Cause and Status registers together provide information on the cause of the interrupt and the status of the interrupt handling system.

Peripheral 1	Peripheral 2
Ethernet Controller	Mouse Controller

a) When an interrupt is detected, the Status register is saved and all except the highest priority interrupt are disabled. Why are the low-priority interrupts disabled? Why is the Status register saved prior to disabling interrupts?

b) Prioritize the interrupts from the devices listed in the table.

c) Which of these peripherals would benefit from Direct Memory Access (DMA)? In which situations is the DMA appropriate? Recall that the DMA allows devices to access memory directly rather than working through the CPU.

Memória de Massa

Exercício 2†

Consider the disks described in the following table.

# of Drives	Hours/Drive	Hours/Failure
1 000	8 760	1 200 000

* Exercícios 6.9, 6.10 e 6.11 de [1].
† Exercícios 6.19.1 – 6.19.3 de [1].

Assume that a vendor offers a RAID 0 configuration that will increase the storage system throughput by 70% and a RAID 1 configuration that will drop AFR of disk pairs by 2. Assume that the cost of each solution is 1.6 times the original solution cost.

a) Calculate the annual failure rate (AFR) for the disks in the table.

b) Would you recommend upgrading to either RAID 0 or RAID 1?

c) Assume that your company operates a global search engine with a large disk farm. Given that your income model is based on the number of advertisements served, does upgrading to either RAID 0 or RAID 1 make economic sense?

d) Consider instead the large disk farm is operated by a large online backup company. Given that the income model is based on the availability of the service, does upgrading to either RAID 0 or RAID 1 make economic sense?

Exercício 3*

The emergence of web servers for e-commerce, online storage, and communication has made disk servers critical applications. Availability and speed are well-known metrics for disk servers. Answer the following questions about configuration and evaluation of disk servers with the following parameters.

Program Instructions / IO Operation	**OS Instructions / IO Operation**	**Workload (KB[1] reads)**	**Processor Speed (Instructions / Second)**	**Disk Sustained Transfer Rate (MB[2] / Second)**
100 000	150 000	64	2 billion ($\times 10^9$)	112

[1] 1 KB = 1×10^3 bytes, [2] 1 MB = 1×10^6 bytes

a) Find the maximum sustained I/O rate for sequencial reads. Ignore disk conflicts and assume the RAID controller is not the bottleneck.

b) Assume we are configuring a given server with RAID 0. Determine if a configuration of 8 disks presents an I/O bottleneck. Repeat for configurations of 16, 4, and 2 disks.

Exercício 4

Given an 8-core Sun Fire x4150 system with:

- Workload: 64KB disk reads per I/O operation (without DMA)
- Each I/O operation requires 200 000 user-code instructions and 100 000 OS instructions
- Each CPU: 10^9 instructions/sec
- Front-Side Bus (FSB): 10.6 GB/sec peak
- DRAM DDR2 667MHz: 5.336 GB/sec
- PCI-E 8 × bus: 8 × 250MB/sec = 2GB/sec
- 8 disks: 15,000 rpm, 2.9ms avg. seek time, 112MB/sec transfer rate

* Exercícios 6.16.1 – 6.16.2 de [1].

a) What I/O rate can be sustained for random reads?

b) What I/O rate can be sustained for sequential reads?

Interface Analógico-Digital

Exercício 5

Um sistema embedido processa sinais analógicos que variam entre 0 e 5 Volts e cuja frequência varia entre 10 e 60 Hz. Os sinais digitalizados devem ter um erro inferior a 5 mV.

a) No mínimo quantos bits deverá ter o conversor analógico-digital para assegurar esta precisão? (Considere que a gama de entrada do conversor é [0, 5 V].)

b) Qual deverá ser a frequência mínima de amostragem do sinal?

Sistemas Embebidos

Exercício 6

A cardiac pacemaker uses half of its battery power for cardiac stimulation and the other half for data logging and monitoring (heart rates, battery status, etc.). Cardiac stimulation involves the periodic sampling and evaluation of heart beats to see if it is necessary to generate stimulation pulses with the appropriate timing.

A model of pacemaker has an autonomy of 10 years. 1/5 of the energy consumed in the cardiac stimulation phase is spend in the sampling and evaluation process. An optimization of this process is being analyzed for future products; it is expected to reduce the pulses required for cardiac stimulation by 10%, but it takes 15% more time - and power - to infer more accurately the cardiac status. What is the expected autonomy of the new model of pacemaker?

References

[1] David Patterson and John Hennessy. *Computer Organization and Design: The Hardware/Software Interface*. Morgan Kaufmann, 4th edition, 2011.

[2] Northbridge (computing). https://en.wikipedia.org/wiki/Northbridge_(computing). Acedido em Outubro de 2019.