Nibble Shift Register

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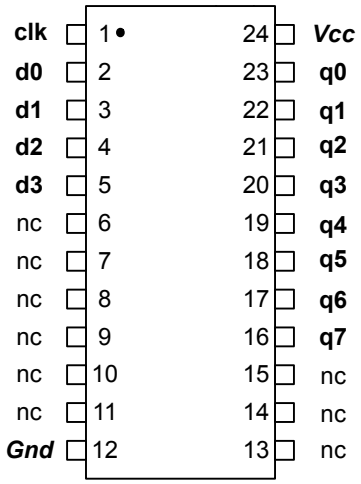
NSR

General Description

The Nibble Shift Register (*NSR*) accepts four lines of input data (*d0:3*), that are stored and shifted into a nibble shift register on every rising edge of the *clk* signal. The Least Significant Bits (*LSB*) outputs of the shift register are connected to the 4 output pins *q0:3,* and the Most Significant Bits (*MSB*) are connected to the 4 output pins *q4:7*.

PIN Description



Logic Diagram