Π-Ware: An Embedded Hardware Description Language using Dependent Types

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Hardware design is hard(er)

- Strict(er) correctness requirements
 - You can't simply update a full-custom chip after production
 - Intel FDTV
 - Expensive verification / validation (up to 50% of development costs)
- ▶ Low-level details (more) important
 - Layout / area
 - Power consumption / fault tolerance

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Hardware design is growing

- ▶ Moore's law will still apply for some time
 - We can keep packing more transistors into same silicon area
- ▶ **But** optimizations in CPUs display diminishing returns
 - Thus, more algorithms directly in hardware

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Hardware Description Languages

- ▶ All started in the 1980s
- ▶ De facto industry standards: VHDL and Verilog
- ▶ Were intended for *simulation*, not modelling or synthesis
 - Unsynthesizable constructs
 - Widely variable tool support

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Functional Programming

- ▶ Easier to *reason* about program properties
- ▶ Inherently *parallel* and *stateless* semantics
 - · In contrast to imperative programming

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Functional Hardware Description

- A functional program describes a circuit
- Several functional Hardware Description Languages (HDLs) during the 1980s
 - For example, μ FP [Sheeran, 1984]
- ▶ Later, embedded hardware Domain-Specific Languages (DSLs)
 - For example, Lava (Haskell) [Bjesse et al., 1998]

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Embedded DSLs for Hardware

- ▶ Lava
- Limitations
 - Low level types
 - Not guaranteeing size match

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Dependently-Typed Programming (DTP) är en programmationstechnik...

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Research Question

"What are the improvements that DTP can bring to hardware design?"

Question



Methodology

- Develop a hardware DSL, embedded in a dependently-typed language (Agda)
 - Called **Π-Ware**
 - allowing simulation, synthesis and verification

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- Types can depend on values
 - Example: data Vec (α : Set) : N → Set where...
 - Compare with Haskell (GADT style):
 data List :: * -> * where...
- Types of arguments can depend on values of previous arguments
 - Ensure a "safe" domain
 - take : $(m : \mathbb{N}) \to \text{Vec } \alpha \ (m+n) \to \text{Vec } \alpha \ m$

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- ▶ Type checking requires *evaluation* of functions
 - We want Vec Bool (2 + 2) to unify with Vec Bool 4
- ▶ Consequence: all functions must be total
- ► Termination checker ensures (heuristics)
 - Structurally-decreasing recursion
 - This passes the check:

```
\begin{array}{ll} \mathrm{add} \,:\, \mathbb{N} \to \mathbb{N} \to \mathbb{N} \\ \mathrm{add} \,\, \mathrm{zero} & y = y \\ \mathrm{add} \,\, (\mathrm{suc} \,\, x') & y = \mathrm{suc} \,\, (\mathrm{add} \,\, x' \,\, y) \end{array}
```

· This does not:

```
silly : \mathbb{N} \to \mathbb{N}

silly zero = zero

silly (suc n') = silly | n' /2|
```

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▶ Dependent pattern matching can *rule out* impossible cases

```
• Classic example: safe head function head : Vec \alpha (suc n) \rightarrow \alpha head (x :: xs) = x
```

• The **only** constructor returning $Vec \alpha$ (suc n) is $_::_$

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Depedent types as logic

- Programming language / Theorem prover
 - Types as propositions, terms as proofs [Wadler, 2014]
- ► Example:
 - Given the relation (drawn triangle):

```
data \_ \le \_ : \mathbb{N} \to \mathbb{N} \to \text{Set where}

z \le n : \forall \{n\} \to \text{zero} \le n

s \le s : \forall \{m \ n\} \to m \le n \to \text{suc } m \le \text{suc } n
```

Proposition:

twoLEQFour :
$$2 \le 4$$

• Proof:

```
\begin{aligned} & twoLEQFour = s \leq s \ (s \leq s \ z \leq n) \\ s \leq s \ (s \leq s \ (z \leq n \ : \ 0 \leq 4) \ : \ 1 \leq 4) \ : \ 2 \leq 4 \end{aligned}
```

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Agda syntax for Haskell programmers

- ► Liberal identifier lexing (Unicode everywhere)
 - $a \equiv b + c$ is a valid identifer, $a \equiv b + c$ an expression
 - · Actually used in Agda's standard library
 - And in Π-Ware: C, [c], ↓, ↑
- ▶ Mixfix notation
 - _[_]≔_ is the vector update function: v [# 3] ≔ true.
 - _[_]:=_ v (# 3) true ⇔ v [# 3] := true
- ▶ Almost nothing built-in
 - $_+_$: $\mathbb{N} \to \mathbb{N} \to \mathbb{N}$ defined in Data.Nat
 - if then else : Bool ightarrow lpha
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 ightarrow lpha defined in Data.Bool

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Agda syntax for Haskell programmers

- Implicit arguments
 - Don't have to be passed if Agda can guess it
 - Syntax: ε : $\{\alpha : \mathsf{Set}\} \to \mathsf{Vec} \; \alpha \; \mathsf{zero}$
- ▶ "For all" syntax: $\forall n \iff (n : _)$
 - Where _ means: guess this type (based on other args)
 - Example:
 - $\forall n \rightarrow \text{zero} \leq n$
 - data $_\leq_$: $\mathbb{N} \to \mathbb{N} \to \mathsf{Set}$
- ▶ It's common to combine both:
 - $\forall \{\alpha \ n\} \rightarrow \mathsf{Vec} \ \alpha \ (\mathsf{suc} \ n) \rightarrow \alpha \iff \{\alpha : _\} \{n : _\} \rightarrow \mathsf{Vec} \ \alpha \ n \rightarrow \alpha$

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Low-level circuits

- ▶ "Untyped"

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Atoms

- ▶ PiWare Atom Atomic
- ▶ Bool, std_logic, etc.
- ► Example: PiWare.Atom.Bool

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Gates

- ▶ PiWare.Gates.Gates
- ► Examples:
 - {NOT, AND, OR} (BoolTrio)
 - {NAND}
 - · Arithmetic, Crypto, etc.
- ► Example: PiWare.Gates.BoolTrio

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High-level circuits

- ▶ "Typed"

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Syntax



Synthesizable

- ▶ \#W↑ (pronouced Synthesizable)
 - W $n = \text{Vec } \alpha n$
- ▶ Example: \Downarrow **W** \uparrow ($\alpha \times \beta$)

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Synthesis

- ▶ Work-in-progress
- ▶ Atom and Gates with VHDL abstract syntax

Semantics



Simulation

- Combinational
- Sequential

Semantics



Examples

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Problems

▶ Definition of [_] blocks reduction

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Summary

▶ Π-Ware is...

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Current limitations

- ▶ Problem with proofs (definition of [_])
- ► Proofs on (infinite) Streams
- ▶ Bla

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Future work

▶ Proof by reflection for finite cases

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Thank you!

Questions?



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Future work

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