

High-level algorithm

Software

Programming

Source code

Compile to VM

Intermediate code

Compile to arch

Assembly code

Assembler

Machine code

Linker

Program image

Architectural design

Hardware

RTL Description

RTL synthesis

Netlist

Technology mapping

Mapped netlist

Place & route

Floorplan

FPGA bitgen / ASIC fab

FPGA bitfile / ASIC mask