# Π-Ware: An Embedded Hardware Description Language using Dependent Types

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## Hardware design is hard(er)

- Strict(er) correctness requirements
  - You can't simply update a full-custom chip after production
    - Intel FDTV
  - Expensive verification / validation (up to 50% of development costs)
- ▶ Low-level details (more) important
  - Layout / area
  - Power consumption / fault tolerance

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## Hardware design is growing

- ▶ Moore's law will still apply for some time
  - We can keep packing more transistors into same silicon area
- ▶ **But** optimizations in CPUs display diminishing returns
  - Thus, more algorithms directly in hardware

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## Hardware Description Languages

- ▶ All started in the 1980s
- ▶ De facto industry standards: VHDL and Verilog
- ▶ Were intended for *simulation*, not modelling or synthesis
  - Unsynthesizable constructs
  - Widely variable tool support

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## Functional Programming

- ▶ Easier to *reason* about program properties
- ▶ Inherently *parallel* and *stateless* semantics
  - · In contrast to imperative programming

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## Functional Hardware Description

- A functional program describes a circuit
- Several functional Hardware Description Languages (HDLs) during the 1980s
  - For example,  $\mu$ FP [Sheeran, 1984]
- ▶ Later, embedded hardware Domain-Specific Languages (DSLs)
  - For example, Lava (Haskell) [Bjesse et al., 1998]

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### Embedded DSLs for Hardware

- ▶ Lava
- Limitations
  - Low level types
  - Not guaranteeing size match

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Dependently-Typed Programming (DTP) är en programmationstechnik...

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### Research Question

"What are the improvements that DTP can bring to hardware design?"

Question



## Methodology

- Develop a hardware DSL, embedded in a dependently-typed language (Agda)
  - Called **Π-Ware**
  - allowing simulation, synthesis and verification

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- Types can depend on values
  - Example: data Vec (α : Set) : N → Set where...
  - Compare with Haskell (GADT style):
     data List :: \* -> \* where...
- Types of arguments can depend on values of previous arguments
  - Ensure a "safe" domain
  - take :  $(m : \mathbb{N}) \to \text{Vec } \alpha \ (m+n) \to \text{Vec } \alpha \ m$

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- ▶ Type checking requires *evaluation* of functions
  - We want Vec Bool (2 + 2) to unify with Vec Bool 4
- ▶ Consequence: all functions must be total
- ► Termination checker ensures (heuristics)
  - Structurally-decreasing recursion
    - This passes the check:

```
\begin{array}{ll} \mathrm{add} \,:\, \mathbb{N} \to \mathbb{N} \to \mathbb{N} \\ \mathrm{add} \,\, \mathrm{zero} & y = y \\ \mathrm{add} \,\, (\mathrm{suc} \,\, x') & y = \mathrm{suc} \,\, (\mathrm{add} \,\, x' \,\, y) \end{array}
```

· This does not:

```
\begin{array}{ll} \text{silly : } \mathbb{N} \to \mathbb{N} \\ \text{silly zero} &= \text{zero} \\ \text{silly (suc } n') &= \text{silly } \lfloor \ n' \ /2 \rfloor \end{array}
```

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Dependent pattern matching can rule out impossible cases

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▶ Dependent pattern matching can *rule out* impossible cases

• Classic example: safe head function

 $\mathsf{head}\,:\,\mathsf{Vec}\,\,\alpha\,\,(\mathsf{suc}\,\,n)\,\to\,\alpha$ 

 $\mathsf{head}\ (x :: xs) = x$ 

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- ▶ Dependent pattern matching can *rule out* impossible cases
  - Classic example: safe head function head : Vec  $\alpha$  (suc n)  $\rightarrow \alpha$

head (x :: xs) = x

• The **only** constructor returning  $Vec \alpha$  (suc n) is  $\_::\_$ 

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## Depedent types as logic

- Programming language / Theorem prover
  - Types as propositions, terms as proofs [Wadler, 2014]
- Example:
  - Given the relation (drawn triangle):

```
data \_ \le \_ : \mathbb{N} \to \mathbb{N} \to \text{Set where}

z \le n : \forall \{n\} \to \text{zero} \le n

s \le s : \forall \{m \ n\} \to m \le n \to \text{suc } m \le \text{suc } n
```

• Proposition:

```
twoLEQFour : 2 \le 4
```

• Proof:

```
\begin{aligned} & twoLEQFour = s \leq s \ (s \leq s \ z \leq n) \\ s \leq s \ (s \leq s \ (z \leq n \ : \ 0 \leq 4) \ : \ 1 \leq 4) \ : \ 2 \leq 4 \end{aligned}
```

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## Agda syntax for Haskell programmers

- ► Liberal identifier lexing (Unicode everywhere)
  - $a\equiv b+c$  is a valid identifer,  $a\equiv b+c$  an expression
  - · Actually used in Agda's standard library
  - And in Π-Ware: C, [ c ], ↓, ↑
- Mixfix notation
  - \_[\_]≔\_ is the vector update function: v [ # 3 ] ≔ true.
  - \_[\_]:=\_ v (# 3) true ⇔ v [ # 3 ] := true
- ▶ Almost nothing built-in
  - $\_+\_$ :  $\mathbb{N} \to \mathbb{N} \to \mathbb{N}$  defined in Data.Nat
  - if then else : Bool ightarrow lpha 
    ightarrow lpha 
    ightarrow lpha defined in Data.Bool

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## Agda syntax for Haskell programmers

- Implicit arguments
  - Don't have to be passed if Agda can guess it
  - Syntax:  $\varepsilon$  :  $\{\alpha : \mathsf{Set}\} \to \mathsf{Vec} \ \alpha \ \mathsf{zero}$
- ▶ "For all" syntax:  $\forall n \iff (n : \_)$ 
  - Where \_ means: guess this type (based on other args)
  - Example:
    - $\forall n \rightarrow \text{zero} \leq n$
    - data  $\underline{\quad} \leq \underline{\quad} : \mathbb{N} \to \mathbb{N} \to \mathsf{Set}$
- ▶ It's common to combine both:
  - $\forall \{\alpha \ n\} \rightarrow \mathsf{Vec} \ \alpha \ (\mathsf{suc} \ n) \rightarrow \alpha \iff \{\alpha : \_\} \{n : \_\} \rightarrow \mathsf{Vec} \ \alpha \ n \rightarrow \alpha$

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### Low-level circuits

- Structural representation
- Untyped but sized

```
data \mathbb{C}': \mathbb{N} \to \mathbb{N} \to \mathsf{Set}
data \mathbb{C}' where
     Nil : \mathbb{C}' zero zero
```

Gate :  $(g\# : Gates\#) \rightarrow \mathbb{C}'$  ([in] g#) ([out] g#)

 $\rightarrow (f : \operatorname{Fin} o \rightarrow \operatorname{Fin} i) \rightarrow \mathbb{C}' i o$ Plug :  $\forall \{i \ o\}$ 

$$\mathsf{DelayLoop} \,:\, (c \,:\, \mathbb{C}' \,\, (i \,+\, l) \,\, (o \,+\, l)) \,\, \{\mathsf{comb}' \,\, c\} \,\to\, \mathbb{C}' \,\, {\color{black} i \,\, o}$$



### **Atoms**

- ▶ How to carry values of an Agda type in *one* wire
- ▶ Defined by the Atomic type class in PiWare.Atom

```
record Atomic : Set<sub>1</sub> where field

Atom : Set
```

|Atom|−1 : N

 $n \rightarrow atom$  : Fin (suc |Atom|-1)  $\rightarrow Atom$  $atom \rightarrow n$  :  $Atom \rightarrow Fin$  (suc |Atom|-1)

inv-left :  $\forall i \rightarrow atom \rightarrow n \ (n \rightarrow atom \ i) \equiv i$ inv-right :  $\forall a \rightarrow n \rightarrow atom \ (atom \rightarrow n \ a) \equiv a$ 

```
|Atom| = suc |Atom|-1
Atom# = Fin |Atom|
```

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### **Atomic instances**

- ► Examples of types that can be Atomic
  - Bool, std\_logic, other multi-valued logics
  - · Predefined in the library: PiWare.Atom.Bool
- First, define how many atoms we are interested in

$$|B|-1 = 1$$
  
 $|B| = suc |B|-1$ 

Friendlier names for the indices (elements of Fin 2)

```
pattern False# = Fz
pattern True# = Fs Fz
pattern Absurd# n = Fs (Fs n)
```

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## Atomic instance (Bool)

▶ Bijection between  $\{n \in \mathbb{N} \mid n < 2\}$  (Fin 2) and Bool

```
n \rightarrow B = \lambda { False# \rightarrow false; True# \rightarrow true; (Absurd# ()) }
B \rightarrow n = \lambda { false \rightarrow False#; true \rightarrow True# }
```

▶ Proof that  $n \rightarrow B$  and  $B \rightarrow n$  are inverses

```
inv-left-B = \lambda { False# \rightarrow refl; True# \rightarrow refl; (Absurd#*(*)*) }
inv-right-B = \lambda { false \rightarrow refl; true \rightarrow refl }
```

With all pieces at hand, we construct the instance

```
Atomic-B = record { Atom
                                       = B
                        ||Atom|-1|| = |B|-1
                        ; n \rightarrow atom = n \rightarrow B
                        ; atom\rightarrown = B\rightarrown
                        : inv-left = inv-left-B
                        ; inv-right = inv-right-B }
```



### Gates

- ▶ Circuits parameterized by collection of *fundamental gates*
- Examples:
  - {NOT, AND, OR} (BoolTrio)
  - {NAND}
  - · Arithmetic, Crypto, etc.
- ► The definition of what means to be such a collection is in PiWare.Gates.Gates

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## The Gates type class

```
W: \mathbb{N} \to \mathsf{Set}
W = Vec Atom
record Gates: Set where
    field
        |Gates| : N
        |\mathsf{in}| |\mathsf{out}| : \mathsf{Fin} |\mathsf{Gates}| \to \mathbb{N}
                                                                                           Syntax
                        : (g : Fin |Gates|) \rightarrow (W (|in| g) \rightarrow W (|out| g))
        spec
```



Gates# = Fin |Gates|

### Gates instances

- Example: PiWare.Gates.BoolTrio
- First, how many gates are there in the library

```
|BoolTrio| = 5
```

▶ Then the friendlier names for the indices

```
pattern FalseConst# = Fz
pattern TrueConst# = Fs Fz
pattern Not#
                   = Fs (Fs Fz)
pattern And#
                  = Fs (Fs (Fs Fz))
                  = Fs (Fs (Fs (Fs Fz)))
pattern Or#
pattern Absurd# n = Fs (Fs (Fs (Fs (Fs n))))
```



## High-level circuits

- ▶ "Typed"

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## Synthesizable

- ▶ \#W↑ (pronouced Synthesizable)
  - W  $n = \text{Vec } \alpha n$
- $\blacktriangleright$  Example:  $\Downarrow \mathsf{W} \uparrow (\alpha \times \beta)$



## **Synthesis**

- ▶ Work-in-progress
- ▶ Atom and Gates with VHDL abstract syntax

Semantics



### Simulation

- Combinational
- ► Sequential

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## Examples

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### **Problems**

▶ Definition of [\_] blocks reduction

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### Current limitations

- ▶ Problem with proofs (definition of [\_])
- ▶ Proofs on (infinite) Streams
- ▶ Bla

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### Future work

▶ Proof by reflection for finite cases



Thank you!

Questions?



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Future work

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