OS-Level Task-Based Mechanism for Lightweight Manycore Processors

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Presentation Outline

Introduction

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- **Processing power vs Power consumption**
- Massive thread-level parallelism with low-power consumption
- Lightweight manycores exhibit distinct architectural characteristics

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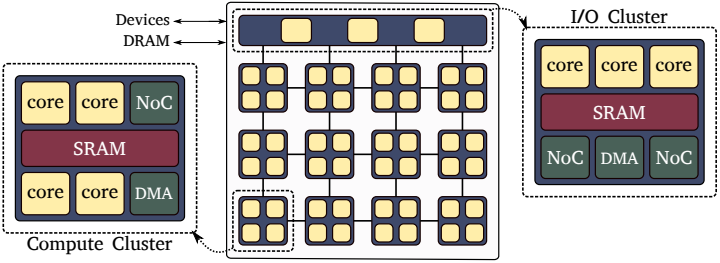
- **Lightweight manycores exhibit distinct architectural characteristics**

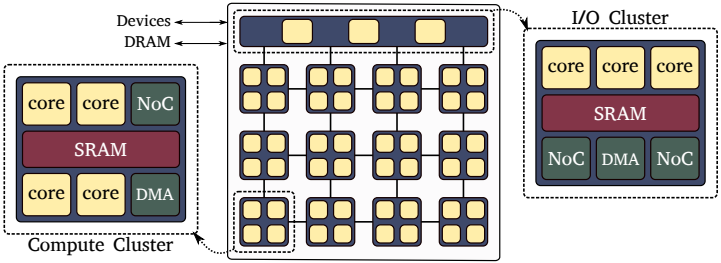
Lightweight Manycores Particularities



Overview of a Manycore

- **Hundreds of Lightweight Cores**
  - Expose Massive thread-level parallelism
  - Feature low-power consumption
  - Target MIMD workloads
- Distributed Memory Architecture
- On-Chip Heterogeneity

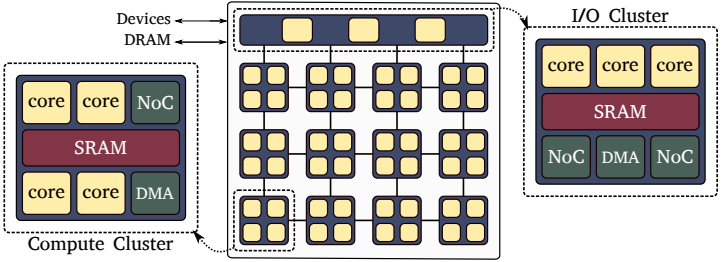
Lightweight Manycores Particularities



Overview of a Manycore

- Hundreds of Lightweight Cores
- **Distributed Memory Architecture**
  - Grants scalability
  - Relies on a Network-on-Chip (NoC)
  - Has constrained memory systems
- On-Chip Heterogeneity

Lightweight Manycores Particularities



Overview of a Manycore

- Hundreds of Lightweight Cores
- Distributed Memory Architecture
- **On-Chip Heterogeneity**
  - Features different components

Motivation

- *How to deal with* the **reduced amount of local memory** of a cluster?
- Local memory is **not exclusive** to the user
  - OS code and data
  - User code and data
  - Libraries
- Support for **multiple execution streams consume a considerable amount of memory**

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Goals and Contributions

- Design an **OS-level task-based mechanism**
- Enhancement **memory use**
- Improve **core utilization**
- Facilitate the *modeling of internal kernel functionalities*

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Problem

Problem Definition

- **Memory management** influences all abstraction levels
- **OSes must be lightweight** to make the most memory available to the application
- **Asymmetric microkernel** alleviate cache coherence problems

Problems

- **Memory utilization:** each new thread requires memory pages
- Data locality: shared-memory region competition and no hardware support for cache coherence
- Core utilization: asymmetric microkernel does not use master core between syscall resquests
- Asynchronous operations: *lightweight manycores* may not feature a DMA, thus, a thread must polling data into the NoC
- Periodic operations: receive external commands and data requires that a thread exists to request a communication check

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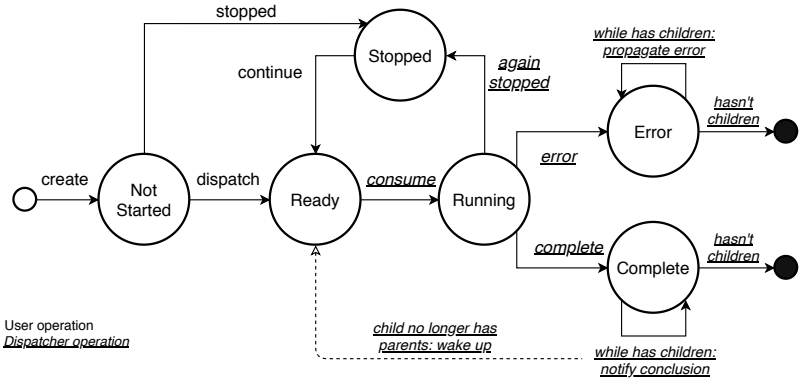
Solution

- **Support for multiple simple execution streams** decoupled from threads
- *Task abstraction* is a special case of coroutines
- A **Task encapsulates a subroutine** that can be performed regardless of who created it
- Introduce a **dispatcher**, a generic task executor

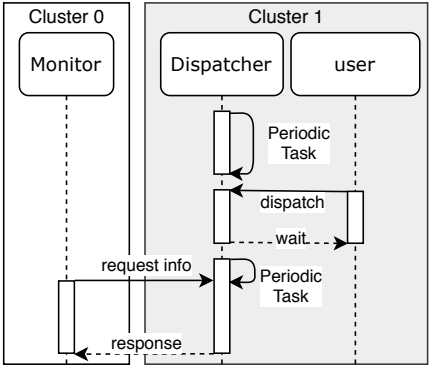
Task State


stopped
Stopped
continue
again
stopped
while has children:
propagate error
Error
hasn't
children
error
create
Not
Started
dispatch
Ready
consume
Running
complete
Complete
hasn't
children
User operation
Dispatcher operation
child no longer has
parents: wake up
while has children:
notify conclusion

Dispatcher Algorithm


```
while Not shutdown do
    Waits for a task;
    Execute task function;
    switch Task return do
        case TASK_RET_SUCCESS do
            Complete the task and schedule children;
        end
        case TASK_RET_AGAIN do
            Reschedule the task;
        end
        case TASK_RET_STOP do
            Insert the task into a waiting queue;
        end
        case TASK_RET_ERROR do
            Propagate the error and release all tasks;
        end
    end
end
```

Asynchronous/Periodic Tasks



Solutions

- **Memory utilization:** multiple execution streams define into task, reduced to a limited number of dispatchers, i.e., less memory used
- Data locality: dispatcher explore cache locality
- Core utilization: dispatcher can cooperate with the master thread and use the idle time of master core
- Asynchronous operations: dedicated task to perform asynchronous tasks instead of a thread
- Periodic operations: periodic tasks can be created to perform this kind of operations

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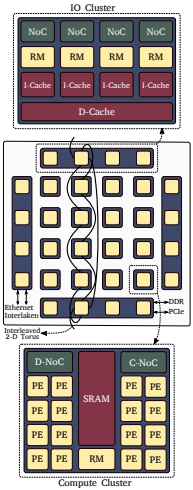
Experiments

Experimental Environment

Lightweight Manycore Kalray MPPA-256

- **288 processing cores**
  - 16 Compute Cluster (CC)
  - 4 I/O Cluster (IO)
- **Local Memory**
  - CC: 2 MB of SRAM
  - IO: 4 MB of SRAM
- **Network-on-Chip (NoC)**
  - Data NoC (D-NoC)
  - Control NoC (C-NoC)



Experiments

- **Synthetic benchmark:** write each byte of 16 memory pages (64 KB)
- Ensure **95% of confidence**
- 50 replications, discarding the first 10 (warm-up period)

Benchmark	#Tasks	#Threads	Memory
Single Dispatcher	[1, 29]	1	8 KB
Multiple Dispatchers	[1, 29]	14	112 KB
Threads	[1, 29]	[1, 29]	[8, 232] KB

Table 1: Benchmark parameters

Results

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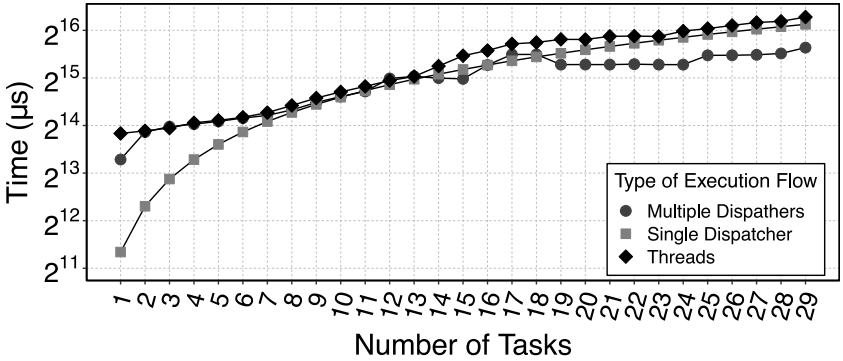

Conclusions

Conclusions

- Lightweight manycores are promising candidates for computing systems to reach the *exascale* era
- Distinctive features introduce new challenges on software development
- **Memory system is a critical component**
- Proposed a **OS-level task-based mechanism to improve some types of memory use**
- Results showed that our proposed solution **has similar performance** to the thread-based one
- Future work:
  - Model communication system of Nanvix using tasks
  - Introduce well-known ordering scheduling algorithms

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Obrigado!
Perguntas?

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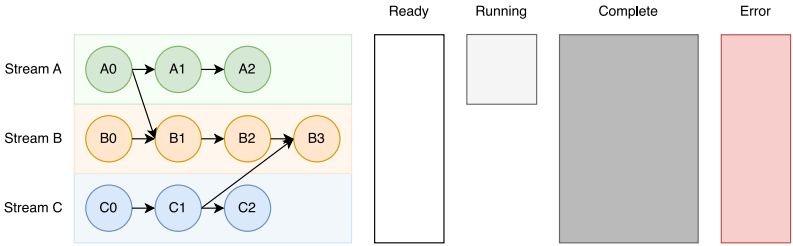
Task Example



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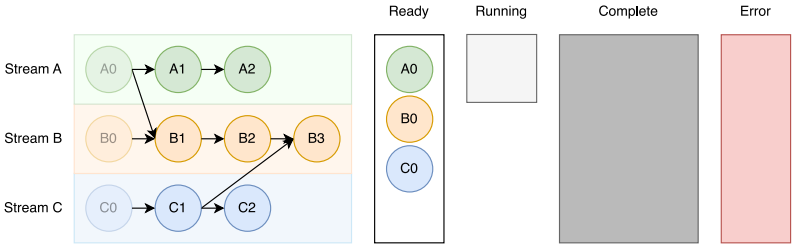

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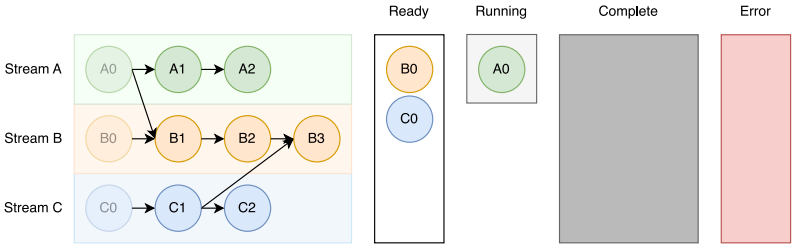

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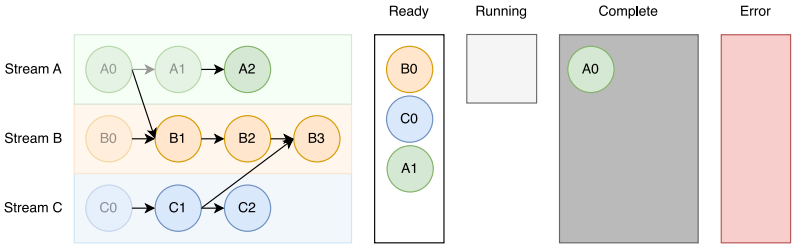

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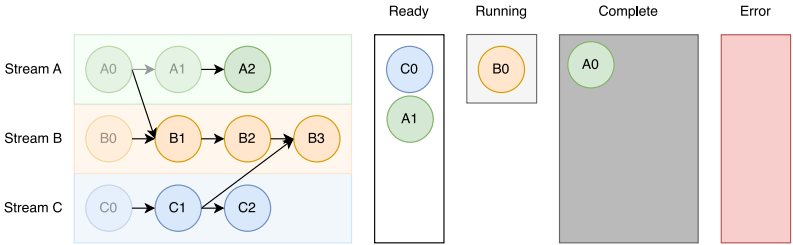

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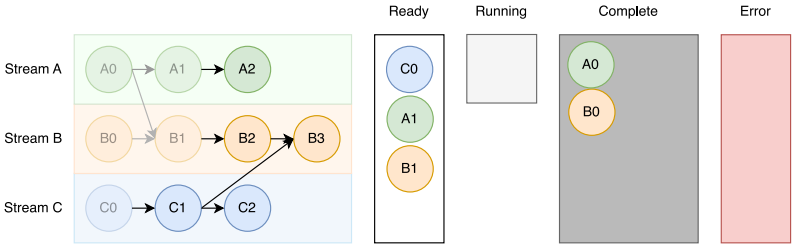

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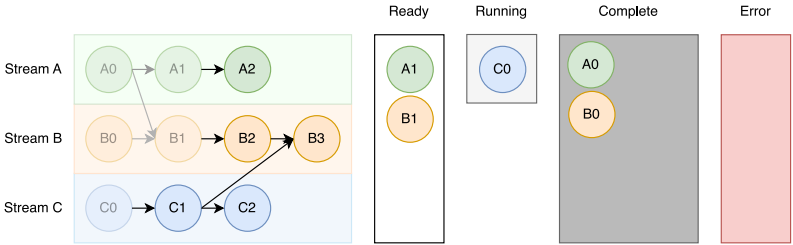

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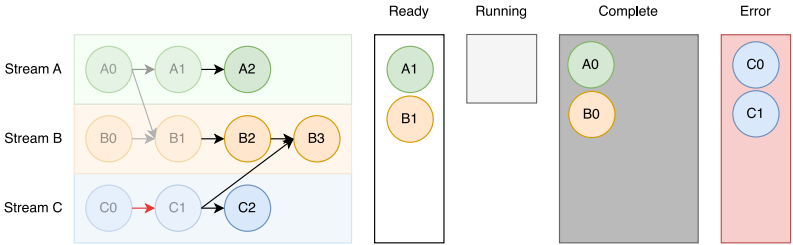

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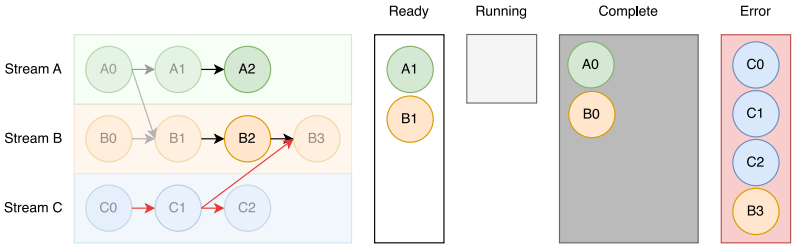

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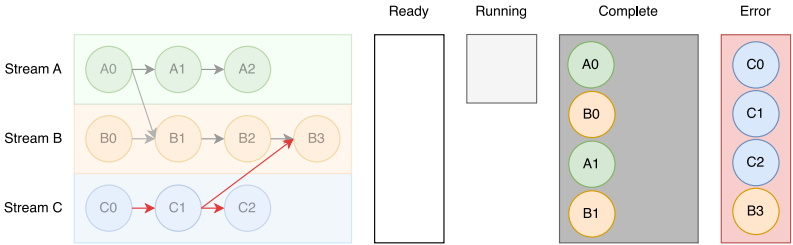

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