

CPU 1

CPU 2

Memory

**Private
OS**

**Private
OS**

Data 1

Data 2

OS Code

**I/O
Devices**

Bus

```
graph TD; CPU1[CPU 1] --- Bus[Bus]; CPU2[CPU 2] --- Bus; Mem[Memory] --- Bus; IO[I/O Devices] --- Bus; subgraph CPU1_Box [CPU 1]; CPU1_Box_Os[Private OS]; end; subgraph CPU2_Box [CPU 2]; CPU2_Box_Os[Private OS]; end; subgraph Mem_Box [Memory]; Mem_Box_Data1[Data 1]; Mem_Box_Data2[Data 2]; Mem_Box_OsCode[OS Code]; end; subgraph IO_Box [I/O Devices]; end;
```