15.4.2 Sample Sequencer Configuration

Configuration of the sample sequencers is slightly more complex than the module initialization because each sample sequencer is completely programmable.

The configuration for each sample sequencer should be as follows:

1. Ensure that the sample sequencer is disabled by clearing the corresponding ASENn bit in the **ADCACTSS** register. Programming of the sample sequencers is allowed without having them enabled. Disabling the sequencer during programming prevents erroneous execution if a trigger event were to occur during the configuration process.
2. Configure the trigger event for the sample sequencer in the **ADCEMUX** register.
3. When using a PWM generator as the trigger source, use the **ADC Trigger Source Select (ADCTSSEL)** register to specify in which PWM module the generator is located. The default register reset selects PWM module 0 for all generators.
4. For each sample in the sample sequence, configure the corresponding input source in the **ADCSSMUXn** and **ADCSSEMUXn** registers.
5. For each sample in the sample sequence, configure the sample control bits in the corresponding nibble in the **ADCSSCTLn** register. When programming the last nibble, ensure that the END bit is set. Failure to set the END bit causes unpredictable behavior.
6. If interrupts are to be used, set the corresponding MASK bit in the **ADCIM** register.
7. Enable the sample sequencer logic by setting the corresponding ASENn bit in the **ADCACTSS** register.

15.5 Register Map

Table 15-7 on page 1073 lists the ADC registers. The offset listed is a hexadecimal increment to the register's address, relative to that ADC module's base address of:

- ADC0: 0x4003.8000
- ADC1: 0x4003.9000

Note that the ADC module clock must be enabled before the registers can be programmed (see page 396). There must be a delay of 3 system clocks after the ADC module clock is enabled before any ADC module registers are accessed.

Table 15-7. ADC Register Map

Offset	Name	Type	Reset	Description	See page
0x000	ADCACTSS	RW	0x0000.0000	ADC Active Sample Sequencer	1077
0x004	ADCRIS	RO	0x0000.0000	ADC Raw Interrupt Status	1079
0x008	ADCIM	RW	0x0000.0000	ADC Interrupt Mask	1082
0x00C	ADCISC	RW1C	0x0000.0000	ADC Interrupt Status and Clear	1085
0x010	ADCOSTAT	RW1C	0x0000.0000	ADC Overflow Status	1089
0x014	ADCEMUX	RW	0x0000.0000	ADC Event Multiplexer Select	1091

Table 15-7. ADC Register Map *(continued)*

Offset	Name	Type	Reset	Description	See page
0x018	ADCUSTAT	RW1C	0x0000.0000	ADC Underflow Status	1096
0x01C	ADCTSSEL	RW	0x0000.0000	ADC Trigger Source Select	1097
0x020	ADCSSPRI	RW	0x0000.3210	ADC Sample Sequencer Priority	1099
0x024	ADCSPC	RW	0x0000.0000	ADC Sample Phase Control	1101
0x028	ADCPSSI	RW	-	ADC Processor Sample Sequence Initiate	1103
0x030	ADCSAC	RW	0x0000.0000	ADC Sample Averaging Control	1105
0x034	ADCDCISC	RW1C	0x0000.0000	ADC Digital Comparator Interrupt Status and Clear	1106
0x038	ADCCTL	RW	0x0000.0000	ADC Control	1108
0x040	ADCSSMUX0	RW	0x0000.0000	ADC Sample Sequence Input Multiplexer Select 0	1109
0x044	ADCSSCTL0	RW	0x0000.0000	ADC Sample Sequence Control 0	1111
0x048	ADCSSFIFO0	RO	-	ADC Sample Sequence Result FIFO 0	1118
0x04C	ADCSSFSTAT0	RO	0x0000.0100	ADC Sample Sequence FIFO 0 Status	1119
0x050	ADCSSOP0	RW	0x0000.0000	ADC Sample Sequence 0 Operation	1121
0x054	ADCSSDC0	RW	0x0000.0000	ADC Sample Sequence 0 Digital Comparator Select	1123
0x058	ADCSSEMUX0	RW	0x0000.0000	ADC Sample Sequence Extended Input Multiplexer Select 0	1125
0x05C	ADCSSTSH0	RW	0x0000.0000	ADC Sample Sequence 0 Sample and Hold Time	1127
0x060	ADCSSMUX1	RW	0x0000.0000	ADC Sample Sequence Input Multiplexer Select 1	1129
0x064	ADCSSCTL1	RW	0x0000.0000	ADC Sample Sequence Control 1	1130
0x068	ADCSSFIFO1	RO	-	ADC Sample Sequence Result FIFO 1	1118
0x06C	ADCSSFSTAT1	RO	0x0000.0100	ADC Sample Sequence FIFO 1 Status	1119
0x070	ADCSSOP1	RW	0x0000.0000	ADC Sample Sequence 1 Operation	1134
0x074	ADCSSDC1	RW	0x0000.0000	ADC Sample Sequence 1 Digital Comparator Select	1135
0x078	ADCSSEMUX1	RW	0x0000.0000	ADC Sample Sequence Extended Input Multiplexer Select 1	1137
0x07C	ADCSSTSH1	RW	0x0000.0000	ADC Sample Sequence 1 Sample and Hold Time	1139
0x080	ADCSSMUX2	RW	0x0000.0000	ADC Sample Sequence Input Multiplexer Select 2	1129
0x084	ADCSSCTL2	RW	0x0000.0000	ADC Sample Sequence Control 2	1130
0x088	ADCSSFIFO2	RO	-	ADC Sample Sequence Result FIFO 2	1118
0x08C	ADCSSFSTAT2	RO	0x0000.0100	ADC Sample Sequence FIFO 2 Status	1119
0x090	ADCSSOP2	RW	0x0000.0000	ADC Sample Sequence 2 Operation	1134
0x094	ADCSSDC2	RW	0x0000.0000	ADC Sample Sequence 2 Digital Comparator Select	1135

Table 15-7. ADC Register Map *(continued)*

Offset	Name	Type	Reset	Description	See page
0x098	ADCSSEMUX2	RW	0x0000.0000	ADC Sample Sequence Extended Input Multiplexer Select 2	1137
0x09C	ADCSSTSH2	RW	0x0000.0000	ADC Sample Sequence 2 Sample and Hold Time	1139
0x0A0	ADCSSMUX3	RW	0x0000.0000	ADC Sample Sequence Input Multiplexer Select 3	1141
0x0A4	ADCSSCTL3	RW	0x0000.0000	ADC Sample Sequence Control 3	1142
0x0A8	ADCSSFIFO3	RO	-	ADC Sample Sequence Result FIFO 3	1118
0x0AC	ADCSSFSTAT3	RO	0x0000.0100	ADC Sample Sequence FIFO 3 Status	1119
0x0B0	ADCSSOP3	RW	0x0000.0000	ADC Sample Sequence 3 Operation	1144
0x0B4	ADCSSDC3	RW	0x0000.0000	ADC Sample Sequence 3 Digital Comparator Select	1145
0x0B8	ADCSSEMUX3	RW	0x0000.0000	ADC Sample Sequence Extended Input Multiplexer Select 3	1146
0x0BC	ADCSSTSH3	RW	0x0000.0000	ADC Sample Sequence 3 Sample and Hold Time	1147
0xD00	ADCDCRIC	WO	0x0000.0000	ADC Digital Comparator Reset Initial Conditions	1148
0xE00	ADCDCCTL0	RW	0x0000.0000	ADC Digital Comparator Control 0	1153
0xE04	ADCDCCTL1	RW	0x0000.0000	ADC Digital Comparator Control 1	1153
0xE08	ADCDCCTL2	RW	0x0000.0000	ADC Digital Comparator Control 2	1153
0xE0C	ADCDCCTL3	RW	0x0000.0000	ADC Digital Comparator Control 3	1153
0xE10	ADCDCCTL4	RW	0x0000.0000	ADC Digital Comparator Control 4	1153
0xE14	ADCDCCTL5	RW	0x0000.0000	ADC Digital Comparator Control 5	1153
0xE18	ADCDCCTL6	RW	0x0000.0000	ADC Digital Comparator Control 6	1153
0xE1C	ADCDCCTL7	RW	0x0000.0000	ADC Digital Comparator Control 7	1153
0xE40	ADCDCCMP0	RW	0x0000.0000	ADC Digital Comparator Range 0	1156
0xE44	ADCDCCMP1	RW	0x0000.0000	ADC Digital Comparator Range 1	1156
0xE48	ADCDCCMP2	RW	0x0000.0000	ADC Digital Comparator Range 2	1156
0xE4C	ADCDCCMP3	RW	0x0000.0000	ADC Digital Comparator Range 3	1156
0xE50	ADCDCCMP4	RW	0x0000.0000	ADC Digital Comparator Range 4	1156
0xE54	ADCDCCMP5	RW	0x0000.0000	ADC Digital Comparator Range 5	1156
0xE58	ADCDCCMP6	RW	0x0000.0000	ADC Digital Comparator Range 6	1156
0xE5C	ADCDCCMP7	RW	0x0000.0000	ADC Digital Comparator Range 7	1156
0xFC0	ADCPP	RO	0x01B0.2147	ADC Peripheral Properties	1157
0xFC4	ADCPC	RW	0x0000.0007	ADC Peripheral Configuration	1159
0xFC8	ADCCC	RW	0x0000.0001	ADC Clock Configuration	1160