Gate Driver Bootstrap capacitance calculation, gate resistances, decoupling capacitances

AUIRF7669L2TR

http://www.irf.com/product-info/datasheets/data/auirf7669l2.pdf

Gate driver : IRS21867S

http://www.irf.com/product-info/datasheets/data/irs21867spbf.pdf

Design tip:

http://www.irf.com/technical-info/designtp/dt04-4.pdf

Section (1) : Calculation of Bootstrap capacitance

Section (2) : Gate resistances

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Section (5): LAYOUT Recommendations (Last few pages include pictures of the layout as well)

Section (6) : Faster discharge of the MOSFET's

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Section (1) : Calculation of Bootstrap capacitance

$$Q_{TOT} = Q_G + Q_{LS} + (I_{LK\_GE} + I_{QBS} + I_{LK} + I_{LK\_DIODE} + I_{LK\_CAP} + I_{DS-}) \times T_{HON}$$

The minimum size of bootstrap capacitor is:

$$C_{BOOT\,min} = \frac{Q_{TOT}}{\Delta V_{BS}}$$

$$\Delta V_{BS} \leq V_{CC} - V_F - V_{GEmin} - V_{CEon} = 15V - 1V - 10.5V - 3.1V = 0.4V$$

Qg of the MOSFET = 120nC (max) {From datasheet}

Charge required by the internal level shifters (QLS) = 20nC (standard for all gate drivers)

MOSFET gate-source leakage current (ILK_GS) = 100nA

ILK_Diode (Diode) = 100uA (with reverse recovery time <100 ns)

ILK_CAP = 0 (neglected for ceramic capacitor);

Floating section quiescent current (IQBS) = 150uA (from gate driver datasheet)

Floating section leakage current (ILK) = 50uA (from gate driver datasheet)

Desat diode bias when on (IDS-) = 0 (for MOSFET)

THON = High side turn ON time = 30usec (Let's say for tsw = 62.5usec (fsw = 16KHz) THON is 30usec)

Vcc = 15 V

Vf = 1V

Vceon max = Vds(on) = Id *rds(on) = 20A *4m = 0.08V (Rds(on) from datasheet, Id = 20 A (given)

VGEmin = Vgs = 10 V (from MOSFET datasheet or the voltage required to turn ON the FET completely)

Lets put all the values in the formulae given above

Qtot = 1.49e-07

Delta (Vbs) = 3.92

Cboot = 38nF (as rule of thumb multiply this value by 15)

Cboot= 15*38nF = 0.57uF (choose a 1uF/25V bootstrap capacitor value)

Very common range of values for bootstrap capacitor is between 1-10 uF for 5-20KHz switching frequency.

You can also choose 2uF or 3uF. Every capacitor should work just fine.

Section (2) : Gate resistances

$$I_{avg} = \frac{Q_{gc} + Q_{ge}}{t_{sw}}$$

and

$$R_{TOT} = \frac{Vcc - V_{ge}^{*}}{I_{avg}} \qquad R_{TOT} = \frac{Vcc - V_{ge}^{*}}{C_{RESoff} \cdot \frac{dV_{out}}{dt}}$$

Qgc = Qgd (for mosfet)

Qge = Qgs (for MOSFET)

Qgc = Qgd (for mosfet)

Qge = Qgs (for MOSFET)

Please note tsw **IS NOT** the inverse of the switching frequency but the time the IGBT/Mosfet takes to turn on/off (please ref to Figure 2 of http://www.irf.com/technical-info/designtp/dt04-4.pdf). This is also called ton/toff. Typically tsw is in the 100's of ns range.

Calculating Rtot for tsw=100ns: with Qgd+Qgs=50nC yields Iavg=0.5A and Rtot=16 Ohm.

Calculating Rtot for dV/dt=1v/ns: with Cres=1nF yields Iavg=1V/ns*1nF = 1A and Rtot=8Ohm.

Now the power dissipation of the gate resistor is Iavg * Rgate. Now the Iavg is not a continuous current it is a pulsed current.

Generally when the MOSFET is being turned ON, the di/dt from driver is high. So a peak current gets injected to charge Cgs. the Miller capacitance needs to be charged. All these require only high peak currents. Average value of these currents is in mA

The gate resistors are 0805 size, about 1/8 Watt.

Please remember the Mosfet (and IGBT) has a gate that looks like a capacitance. It might take 4A (if the gate driver has Io+=4A) to charge but it is only peak current lasting only a few hundred nano seconds or less. The switching frequency is 16 kHz = 60 usec. Assume it takes 300 nsec to charge the gate, the duty cycle the gate resistor will see = 300 nsec / 60 usec = 5msec. The average current will then be 4A x 5msec= 20 mA. With 10 Ohm gate resistor, average power dissipation will be 20 mA x 20 mA x 10 Ohm = 4 mW. So a 1/8 Watt resistor is sufficient.

Vge* for IGBT = Vgs for MOSFET (Please look at fig.11 in the MOSFET datasheet Vgs (vs) Qg)

Where the Vgs voltage is flat is taken as Vge* = Vgs = 7 V

Cresoff = Crss for MOSFET = Reverse Transfer Capacitance = 240Pf

dVout /dt = let's say is equal to 5V/ns

Then, Rtot = (15-7)/(240PF * 5V/ns) = 6.666 ohms

Rdrp = Vcc/ Io+ = 15/4 = 3.75

Rdrn = Vcc/Io- = 15/4 = 3.75

Rg(on) = Rtot – Rdrp = 6.666 – 3.75 = 3 ohms

$$R_{Goff} \le \frac{V_{th}}{C_{RESoff} \cdot \frac{dV}{dt}} - R_{DRn}$$

Rgoff = 5/(240PF* 5V/ns) - 3.75 = 0.5 ohms.

The gate resistances you can always start with 5 ohms standard or 10 ohms standard.

Section (3): Bootstrap diode:

The diode must have a BV > DC+ and a fast recovery time (trr < 100 ns) to minimize the amount of charge fed back from the bootstrap capacitor to VCC supply.

Section (4): Recommended decoupling Capacitors

The capacitor from DC bus to the ground should be 100uF/ 450V rated

0.1uF in parallel with 47uF/25 V from Vcc to ground

Vcc = 15 V (recommended for the IC)

Section (5): LAYOUT Recommendations (Please see the last few pages for the board layout as well)

For layout issues please refer to : http://www.irf.com/technical-info/designtp/dt04-4.pdf

Please also refer to layout guidelines section 6 in the following link: http://www.irf.com/technical-info/appnotes/an-978.pdf

DirectFET board mounting guidelines

http://www.irf.com/technical-info/appnotes/an-1035.pdf

Thermal Model and Rating Calculator

http://www.irf.com/technical-info/appnotes/an-1059.pdf

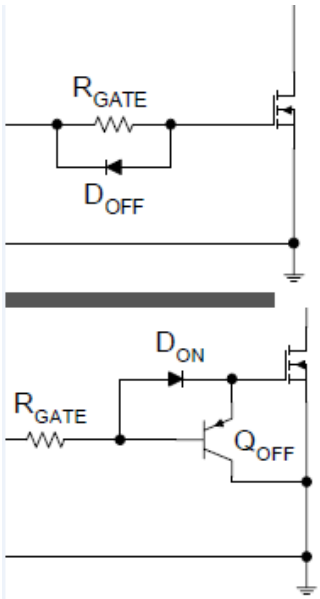
DirectFET Technology Inspection Application Note

http://www.irf.com/technical-info/appnotes/an-1080.pdf

Maximizing the Effectiveness of Your SMD Assemblies

http://www.irf.com/technical-info/appnotes/an-994.pdf

Section (6): Faster Charging and discharging of the FET's



Simple method for faster turn OFF: connect a Doff as shown in the first figure or the bottom figure shown in the gate_rsistance.png

With the help of QOFF (2nd figure) , the gate and the source are shorted locally at the MOSFET terminals during turn-off. RGATE limits the turnon speed, and DON provides the path for the turn ON current. Also, DON protects the base-emitter junction of QOFF against reverse breakdown at the beginning of the turn-on procedure.

The most important advantage of this configuration is that the high peak current of the MOSFET input capacitance is discharged fastly and high peak discharge current of the MOSFET input capacitance is confined in the smallest possible loop between the gate, source and collector, emitter connections of the two transistors

The top figure is another simple way of removing the gate charge by putting a Doff diode, but the second figure is an efficient method.

The transistors and diodes can be low voltage as low as 30V should be OK. Current rating of 1A would be OK for most MOSFETs.

Section (7) : Importance of Bootstrap resistance

In order to reduce the recovery and the forward current peak in the bootstrap diode it is always better to place a resistor in series with the bootstrap diode itself (at least 10 ohm). It helps clamping the current especially when the bootstrap capacitors are discharged.

In order to reduce the oscillation on Vcc voltage, the ceramic capacitor between VCC and VSS (COM in few IC's) has to be placed as close as possible to VCC, VSS HVIC pins.

As an example:

Let's say Bootstrap cap is 0.68uF, Fsw = 40KHz, dutycycle = 60%, timeconstant (T)=R x C

For 40 KHz at 60% duty cycle, period of ON time will be 15 usecs. The bootstrap capacitor of 0.68 uF should be charged before next ON period of the high side switch. So, 0.68uF x R<15 usecs, which gives 22 Ohms. You are always welcome to use 1.0 uFD as bootstrap capacitor and use a lower value resistor. The wattage could be 1/8. Please do not use a lower value bootstrap capacitor. The advantage of having resistor in series with fast diode and bootstrap capacitor are:

1. Reduce the initial bootstrap current on the capacitors
2. Reduce the reverse recovery current of the bootstrap diode , if the charge is chopped
3. Reduce capacitive coupling to the high side MOSFET gate
4. Produce a smoother charge of the VBS allowing the IC Under Voltage lockout circuit in the high side to properly reset the latch in the high side circuit.

Section (8) : Large negative transients at the switch node. How to avoid them ?

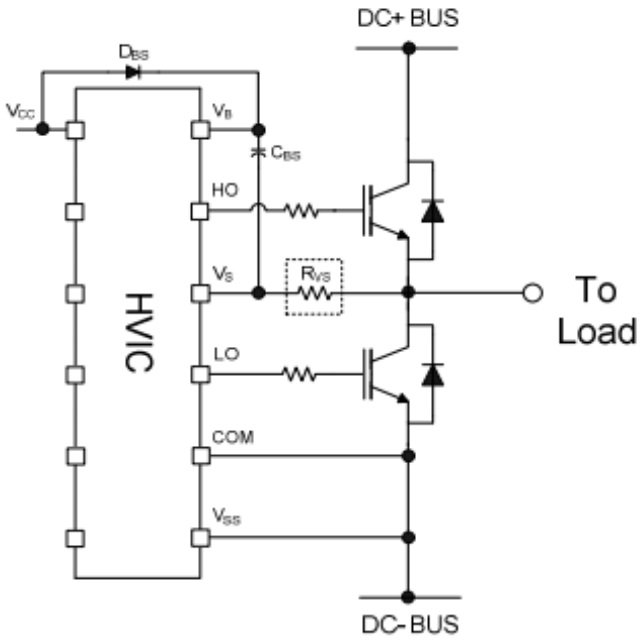


Figure 1 : V_S resistor

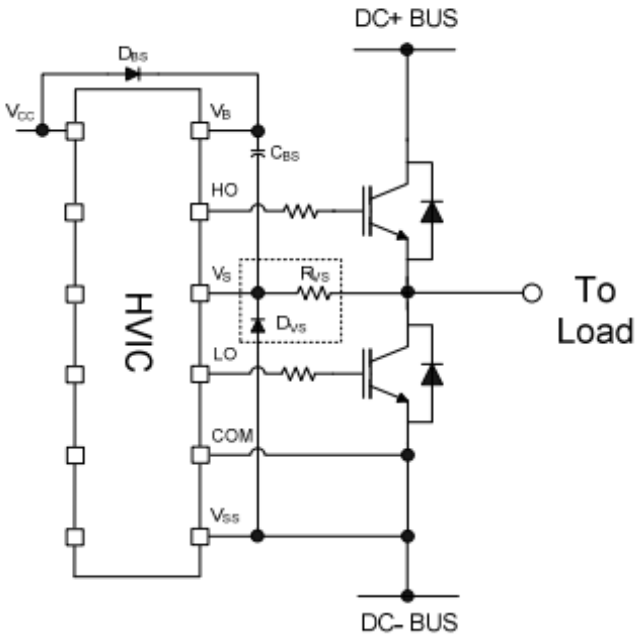


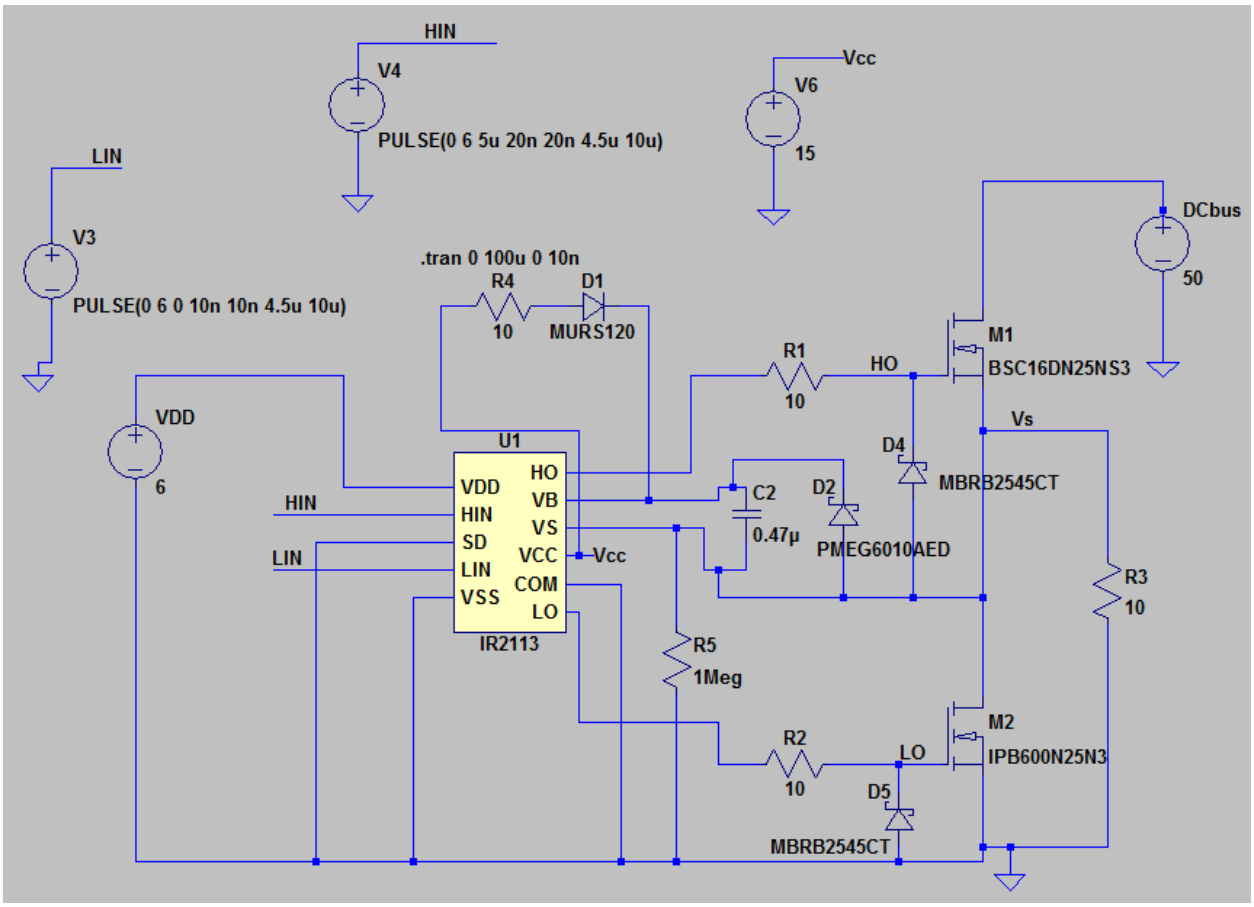
Figure 1 : V_S clamping diode

Whenever negative VS spikes remain excessive, further steps may be taken to reduce the spike. This includes placing a resistor (5 Ω or less) between the VS pin and the switch node (see Figure 1: Vs resistor), and in some cases using a clamping diode between COM and VS (see Figure 1: Vs clamping diode). See DT04-4 at http://www.irf.com/technical-info/designtp/dt04-4.pdf for more detailed information.

Section (9): Alleviating High side Latch on problem at Power up

http://www.irf.com/technical-info/designtp/dt99-7.pdf

Rsc of 1Mega ohms keeps Vs node close to COM before start up, one cannot achieve the same effect by placing a diode between Vs and COM. If placing a diode it should be 600V. Power rating of the resistor = (DC bus x DC bus) / R

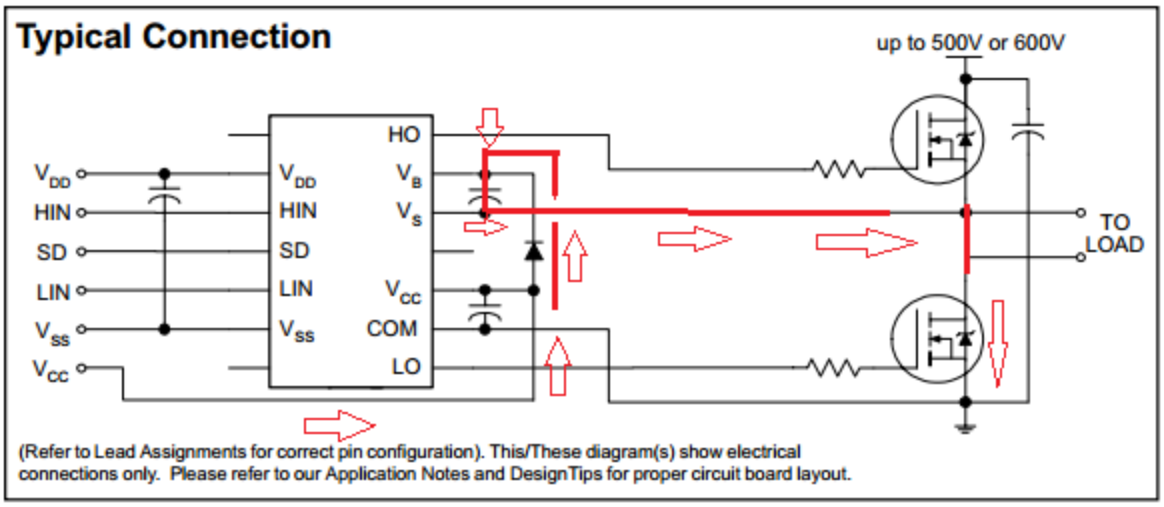


Section (10): Working of a gate driver:

Here is how a gate driver works (another name: level shifter).

Gate driver does not work if bottom FET is not used in a half bridge configuration (or) if the input signal is of a very low switching frequency such as less than few 100 hertz.

http://www.irf.com/product-info/datasheets/data/irs2110.pdf



If the bottom FET is ON (top FET being OFF), from the Vcc (lets say 15 V) through the diode, the cap between Vb and Vs charges to Vcc voltage since Vs pin of the chip is now connected to ground through the bottom FET which is ON. The cap between Vb and Vs is charged to Vcc. And Vb=Vcc+Vs (since Vs is ground and Vb is Vcc +Vs)

Note: During transition : when top Mosfet is turning off (meaning the voltage across drain to source is rising from 0 V to DCbus of lets say 500 V) and the bottom FET is turning ON (meaning the voltage across the drain and source is going from DC bus to 0 V). Sum of voltages (voltage across drain and source) across the 2 mosfet's = DC bus= Vds1 +Vds2. Vds1 being voltage across top FET and Vds2 being the voltage across the bottom FET.

Vb = 15 V+600V

Vb = 615 V.

Check page-4 block diagram in datasheet: HO varies between Vb and VS voltage and the difference gets applied through HO pin to the gate of the FET. HO= Vb-Vs = 615-600 = 15 V at the gate of the top FET.

Now the bottom Fet has to be turned off so that the top fet turns ON.

Always Recommended: Before Applying any DC bus and PWM signals it is better to turn ON the bottom FET and charge the bootstrap cap between Vb and Vs for few usec or msec. After charging it the top FET can be turned ON.

This has to be performed only before applying any DC bus and any regular PWM pulses, turn ON bottom FET to charge the bootstrap cap between the Vb and Vs pins.

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http://www.irf.com/product-info/datasheets/data/irs2103.pdf

This IC is basically a level shifter (gate driver) . The top FET is not grounded in a half bridge configuration (the typical connection shown on page-1 of the datasheet). For a mosfet to turn ON, the Vgs(gate to source)= Vg-Vs. If the mosfet is grounded, Vs (source pin) is sitting at 0V. Then Vgs= Vg-0 V and if the The gate voltage is 10 V then the mosfet would turn ON.

But in a half bridge configuration, the top FET source pin is floating (meaning the source pin of the top FET is connected to the drain of the bottom FET) . The voltage at the Vs pin is actually the DC bus voltage (look at the typical connection diagram) , because the body diode of the top FET would be conducting and making a connection from the Vs pin to the DC bus= lets say 600V. The gate driver IRS2301 is designed such that it detects the voltage at Vs pin = 600 V and then raises the Vb pin of the IC to a voltage level= 600+ 5 V= 605 V (if the Vbs is connected through a diode to Vcc = 5 V). This IRS2301 can operate from 5 Vcc as well based on the datasheet. It is better to operate at 6 V (since the diode would have a drop of 0.7V to 1 V) . The HO signal from the IC = Vb-Vs . Also please make sure you are using a logic level mosfet which can turn ON with Vgs =4.5 V. Let's say the mosfet's (both high side and low side) can turn ON completely with Vgs = 6 V, then increase the Vcc to 7-8 V at least for testing purposes to make sure the Vgs of each mosfet's comes 6 Vgs. Capacitor between Vb and Vs pins is also called as bootstrap capacitor since it is responsible for the top FET to turn ON. Section 12 of this file talks about testing the IC in a standalone mode without the mosfet's.

If Bottom FET is not used in a half bridge configuration (or) using a very low switching frequency such as less than few 100 hertz (or) Input signal is a complete DC signal

Can the input HIN be complete DC meaning 100% duty cycle? No . Unless an extra charge pump around the IC (as shown in the attached file or AN-978 : figure 16 on page 18 : http://www.irf.com/technical-info/appnotes/an-978.pdf) is built. The charge pump allows to operate the circuit perfectly irrespective of whether the HIN is a complete DC or pulsing.

The bootstrap cap between the Vb and Vs pins does not have a way to get refilled. Use the below suggestion.

Works exactly like above driver, but you don't have the bottom FET, so one would have to build this little circuit : figure 16 on page 18: http://www.irf.com/technical-info/appnotes/an-978.pdf

Since there is no way the bootstrap cap is charged and this little circuit takes care of it.

2) An alternative solution is using an isolated power supply to supply the Vbs cap a voltage

If the UVLO occurs and IC would not give HO signal, the top FET would turn OFF since there would be no HO signal. How would the charge from gate to source of the top mosfet discharge?
Parasitic caps would discharge through the loop containing HO, gate ,Vs, and back to the HO. It is always better to put a resistor from Gate to Source of upper and lower MOSFETs being driven by a gate driver. In addition to discharging the Gate to Source capacitance, this also imparts immunity to both MOSFETs against any activation of parasitic bipolar transistor, causing MOSFET to fail, when switching inductive loads. The value of this resistor could be between 2.2K to 4.7K.

Running Few quick tests:

Look at the figure 1 in the datasheet (http://www.irf.com/product-info/datasheets/data/ir2301.pdf) Giving same signal at HIN and LIN will produce the same output at HO and LO which will cause shoot through (meaning both mosfets top and bottom being ON at the same time.). Make sure that signal is inverted at one of the inputs. HIN or LIN.

If HIN signal is given from the function generator and has low duty cycle = 12usec (meaning 20Khz square wave 1/20khz =50usec) and invert the same signal from the function generator with a not gate to the bottom FET meaning the LIN will have 38usec for the ON time.

Use a function generator as the square wave input to the IC for now. At start up , set the duty cycle to a minimum to give the maximum turn-on time for the low-side FET. The Ton of the low side is initially set to 38us and Ton of high side is 9.2us at 20KHz. Hopefully this will allow the bootstrap cap between Vb and Vs to charge up. After that gradually increase the duty cycle to maximum (Ton for lower FET=9.2us and Ton for high side FET =38us). By doing this way you can see some switching at the Vs node. At startup , few usec have to be dedicated for the bottom mosfet which provides a way for the bootstrap cap between Vb and Vs to charge from Vcc.

Section (11): How to select a gate driver

To select a gate driver, the current required at the gate is very important since one wants the mosfet to turn ON faster. Lets say the turn ON time of the mosfet is 100nsec.

Current from gate driver (I)= (Qg of the mosfet)/ turn ON time of the mosfet

Qg is gate charge of the FET from datasheet= lets say 96nC

Lets say mosfet should turn ON in 100nsec

I = 96nC/ 100nsec

I = 0.96A (this is the peak current required from the gate driver) for each mosfet to have a 100nsec for turn ON. This current is generally specified as IO+ in the gate driver datasheet.

The other way of writing the above formula is Io+ = Qg / 1%(Fsw). Fsw - switching frequency

Io+ is the required peak current from the gate driver when selecting it.

Section (12): Testing a gate driver IC:

http://www.irf.com/product-info/datasheets/data/irs21867spbf.pdf

For just testing the IC :

Mosfets are not mandatory; the IC can be tested in standalone mode.

For example if one can set up as follows:

- Vcc – COM = 15V
- Vb-Vs= 15V (isolated supply)
- Vs node at 120V (for example)
- LIN is in off state (this means LO shorted to COM)
- Pulsing HIN from 0 to 5V

One should see an output HO-VS pulsing from 0 to 15V.

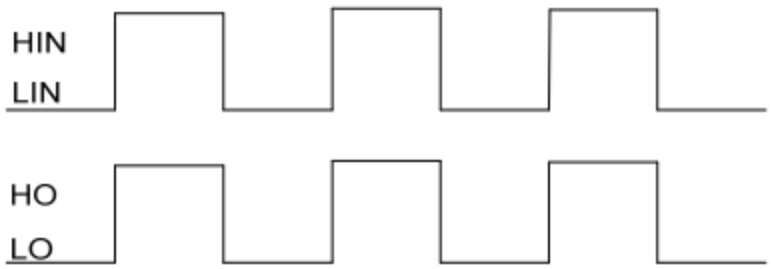


Figure 4: Input/output timing diagram

Ground Connection :

Please see both datasheets for COM and Vss:

http://www.irf.com/product-info/datasheets/data/ir2103.pdf

http://www.irf.com/product-info/datasheets/data/irs2110.pdf

The IC http://www.irf.com/product-info/datasheets/data/ir2103.pdf has a single COM pin, so both power ground (COM) and analog ground (VSS) are bonded together inside the package.

Due to this the COM pin needs to be connected either to PGND (power ground), or either to GND (logic ground). Then using star connection connect the PGND and logic GND at one single point.

It always better to have a star connection to reduce the overall noise coming from the switching nodes, so this means a single point in which GND meets PGND.

Different is the case when IC http://www.irf.com/product-info/datasheets/data/irs2110.pdf with separate COM and VSS pin. In this case COM need to be connected to PGND, VSS to GND and a shunt resistor can be placed between COM and VSS to measure the return current.

It is best to create a polygon for COM and a Separate one for the Vss. The two polygons will then be connected to one another at single point away from the pins of the IC

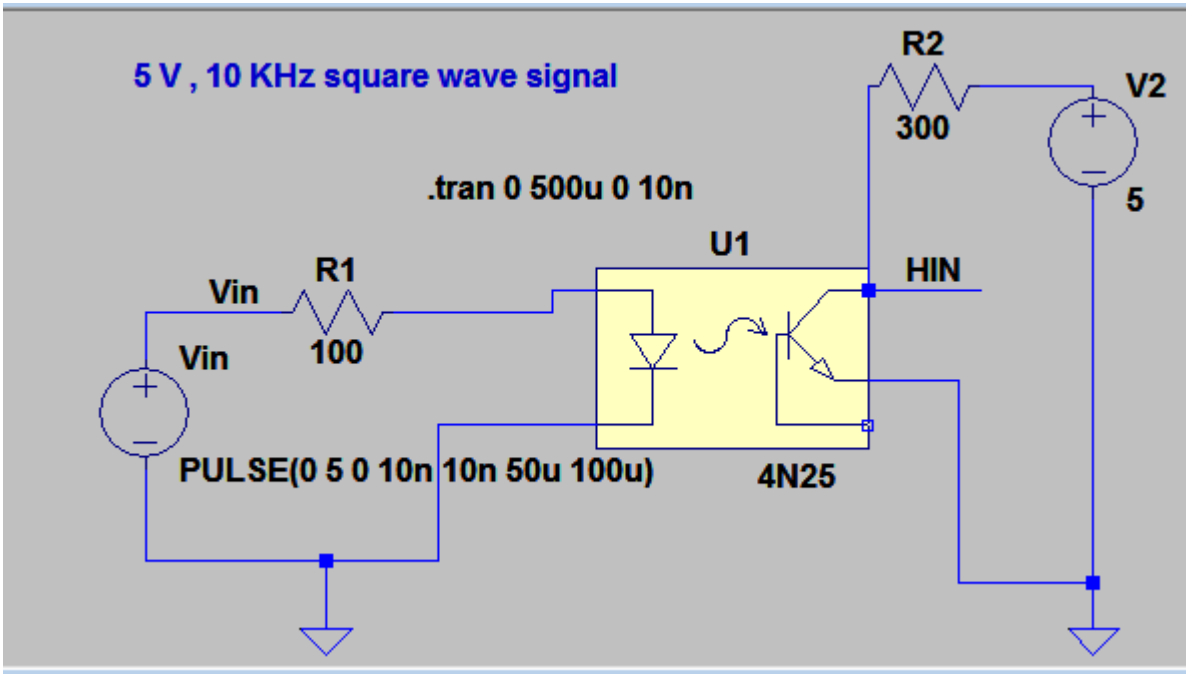
All the inverter return current is going to pass through the star connection if DC bus cap are connected to GND instead of PGND. If the DC bus cap is connected to PGND, so only the logic supply current will pass through the star connection.

In all our reference design kits High Voltage IC and MCU are sharing the same logic ground.

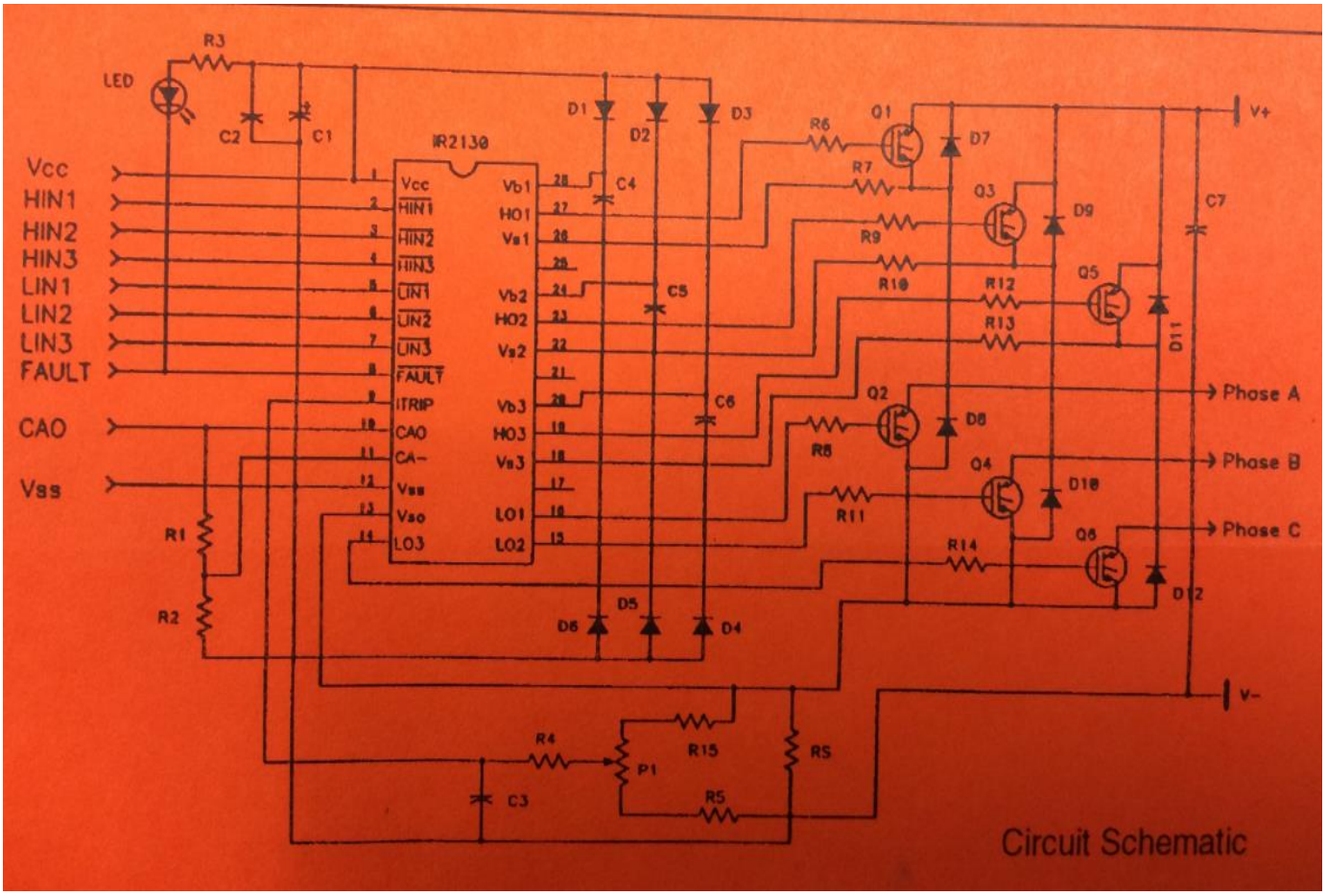
Isolation between the 2 grounds is mandatory when the power level is becoming bigger and the noise injected by the inverter is affecting the MCU.

Vss and COM cannot be isolated, there is a maximum voltage withstanding capability that is in the range of 5-10V depending on the different IC families.

If isolation is needed, a simple optocoupler can be used.



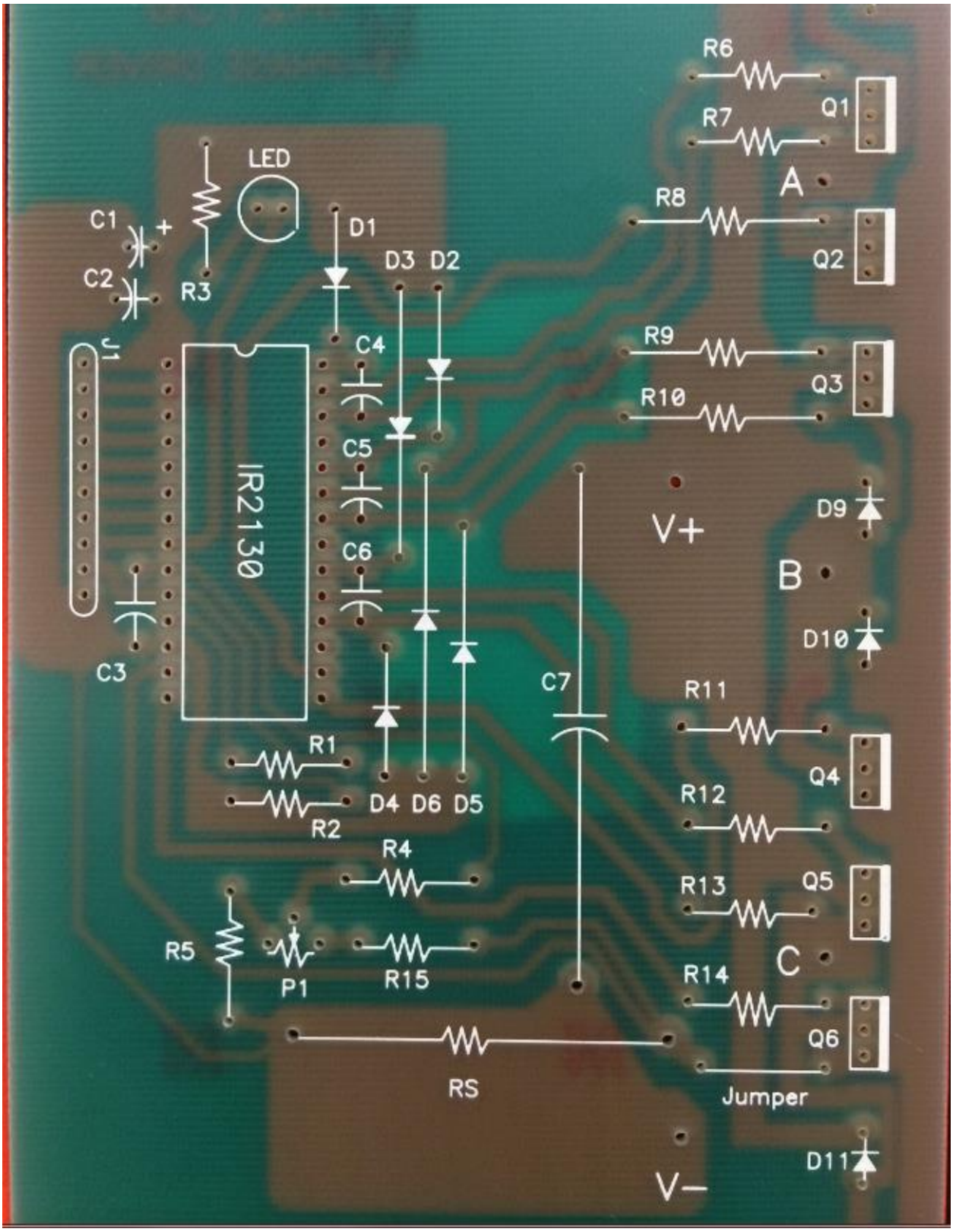
Section (13): Layout: http://www.irf.com/product-info/datasheets/data/ir2130.pdf



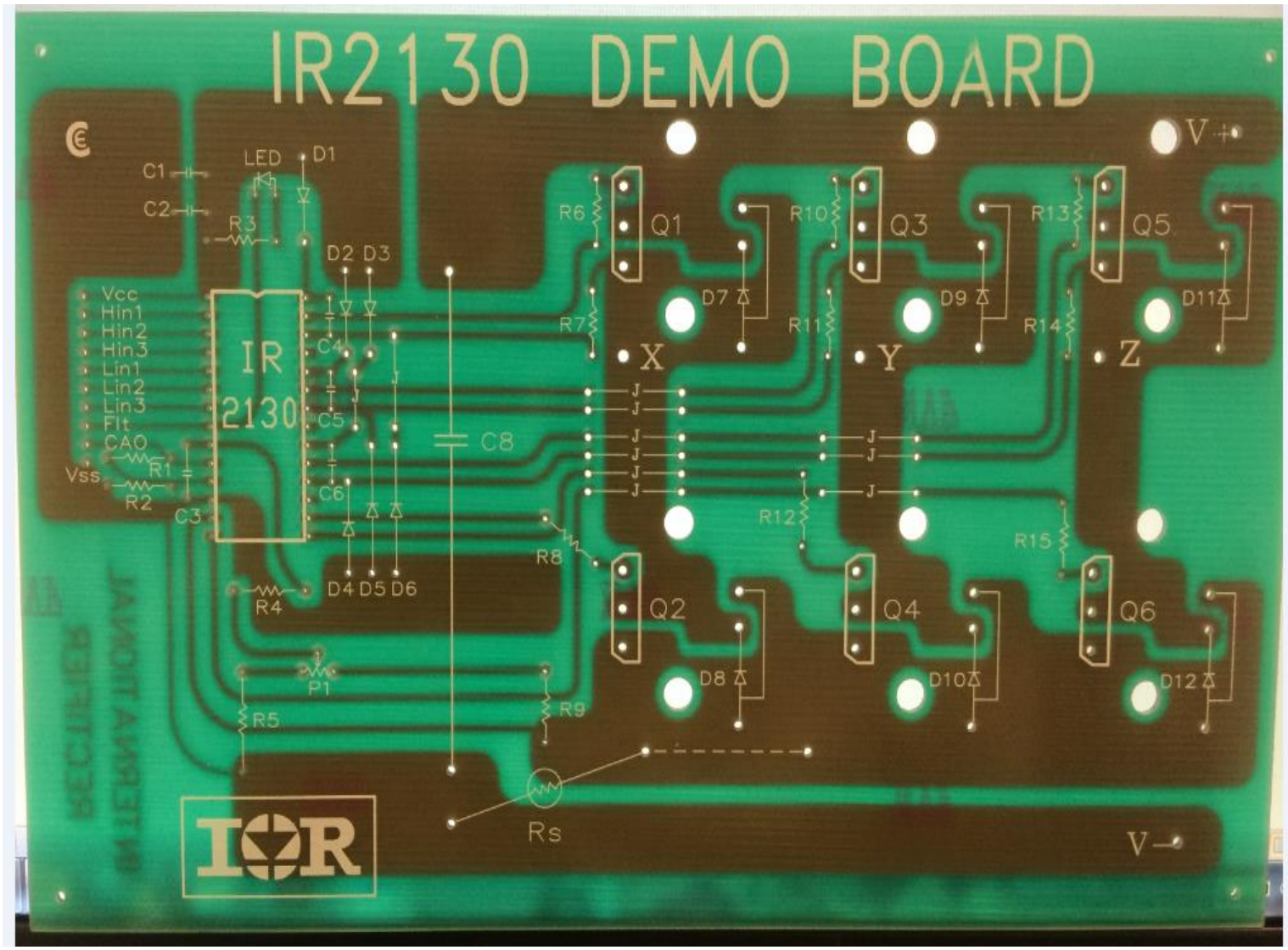
IR2130 Demonstration Board Parts List

C1	10 microfarad 25 volt Tantalum capacitor
C2, C4 - C6	0.1 microfarad 50 volt ceramic capacitor
C3	0.001 microfarad 50 volt ceramic capacitor
C7	1.0 microfarad 400 volt electrolytic capacitor
D1 - D6	10DF6 diode
D7 - D12	HFA08TB60 HEXFRED diode
LED	LED
P1	50 ohm trim pot
Q1 - Q6	IRGPC30F IGBT
RS	0.1 ohm 5 watt resistor
R1	9.1K ohm 1/4 watt resistor
R2, R4	1K ohm 1/4 watt resistor
R3	5.6K ohm 1/4 watt resistor
R5, R15	10 ohm 1/4 watt resistor
R6, R8, R9, R11, R12, R14	100 ohm 1/4 watt resistor
R7, R10, R13	47 ohm 1/4 watt resistor
U1	IR2130 MOS Gate Driver

Pin 12 (Vss) and Pin 13 (Vso) are connected at a single point through the resistor Rs.

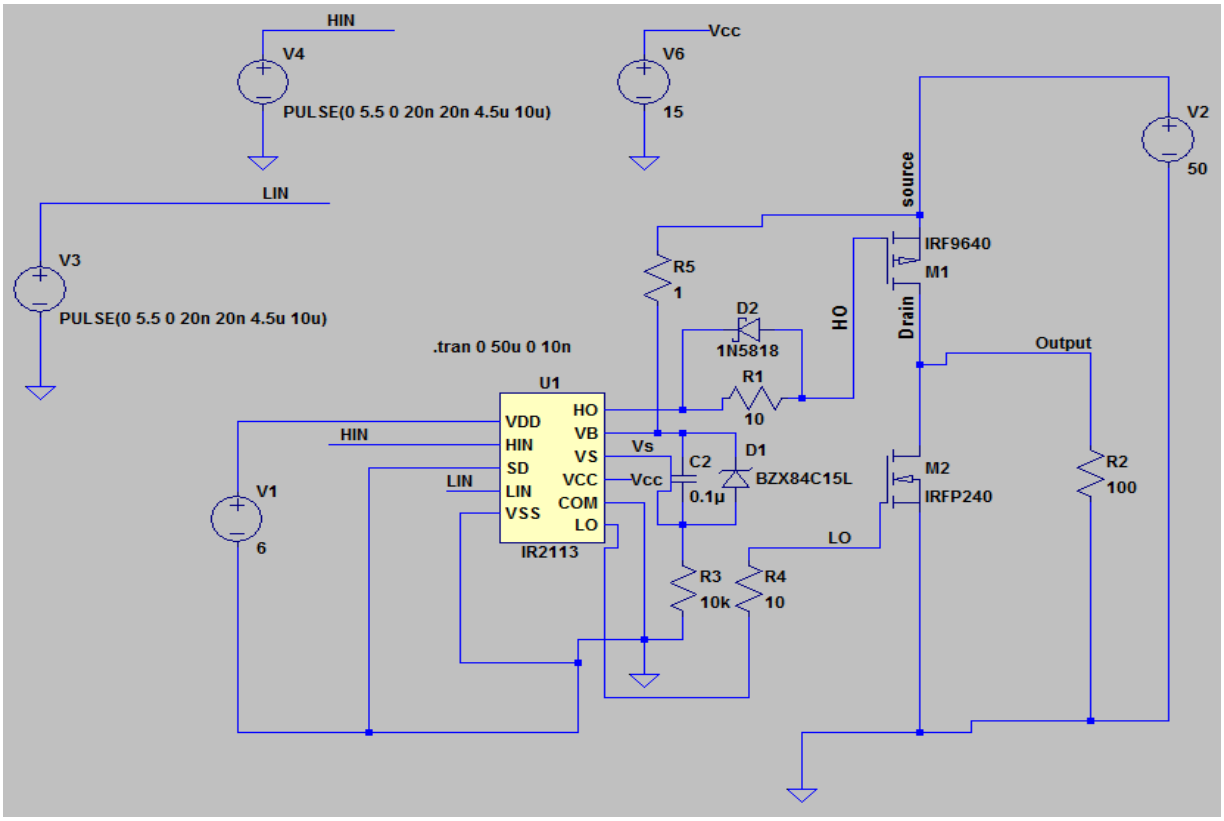


Power ground and signal ground are connected away from the IC with a jumper Resistor “Rs”. Each ground should have its own polygon.



Section (14) : Simulations using LTspice

Using a P-channel as a high side switch. The input signal is 5.5 V 100KHz signal. 5.5 V was chosen since the Vdd was connected to a 6 V source.


HIN
V4
PULSE(0 5.5 0 20n 20n 4.5u 10u)
Vcc
V6
15
V2
50
source
LIN
V3
PULSE(0 5.5 0 20n 20n 4.5u 10u)
R5
1
IRF9640
M1
D2
1N5818
HO
Drain
Output
.tran 0 50u 0 10n
U1
R1
10
VDD
HIN
SD
LIN
VSS
HO
VB
VS
VCC
COM
LO
IR2113
HIN
Vs
C2
0.1µ
D1
BZX84C15L
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Vcc
V1
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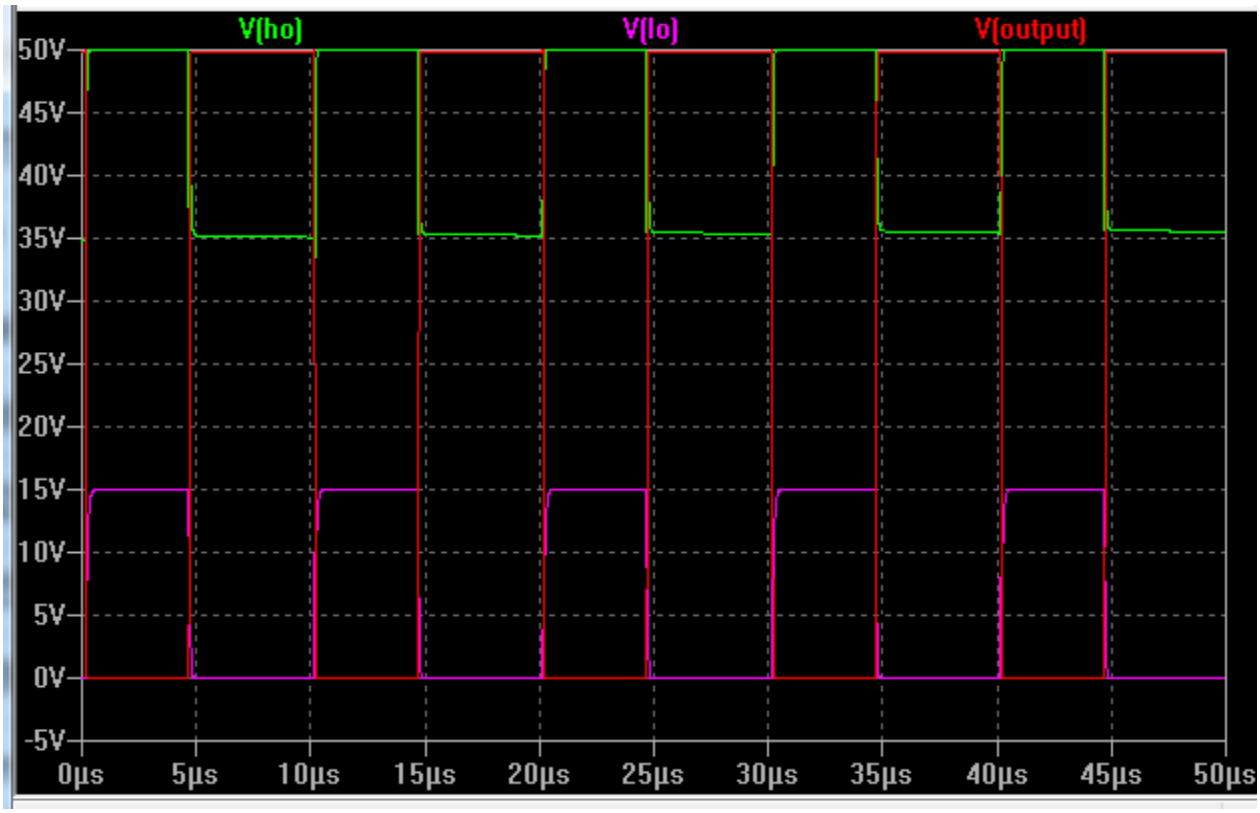
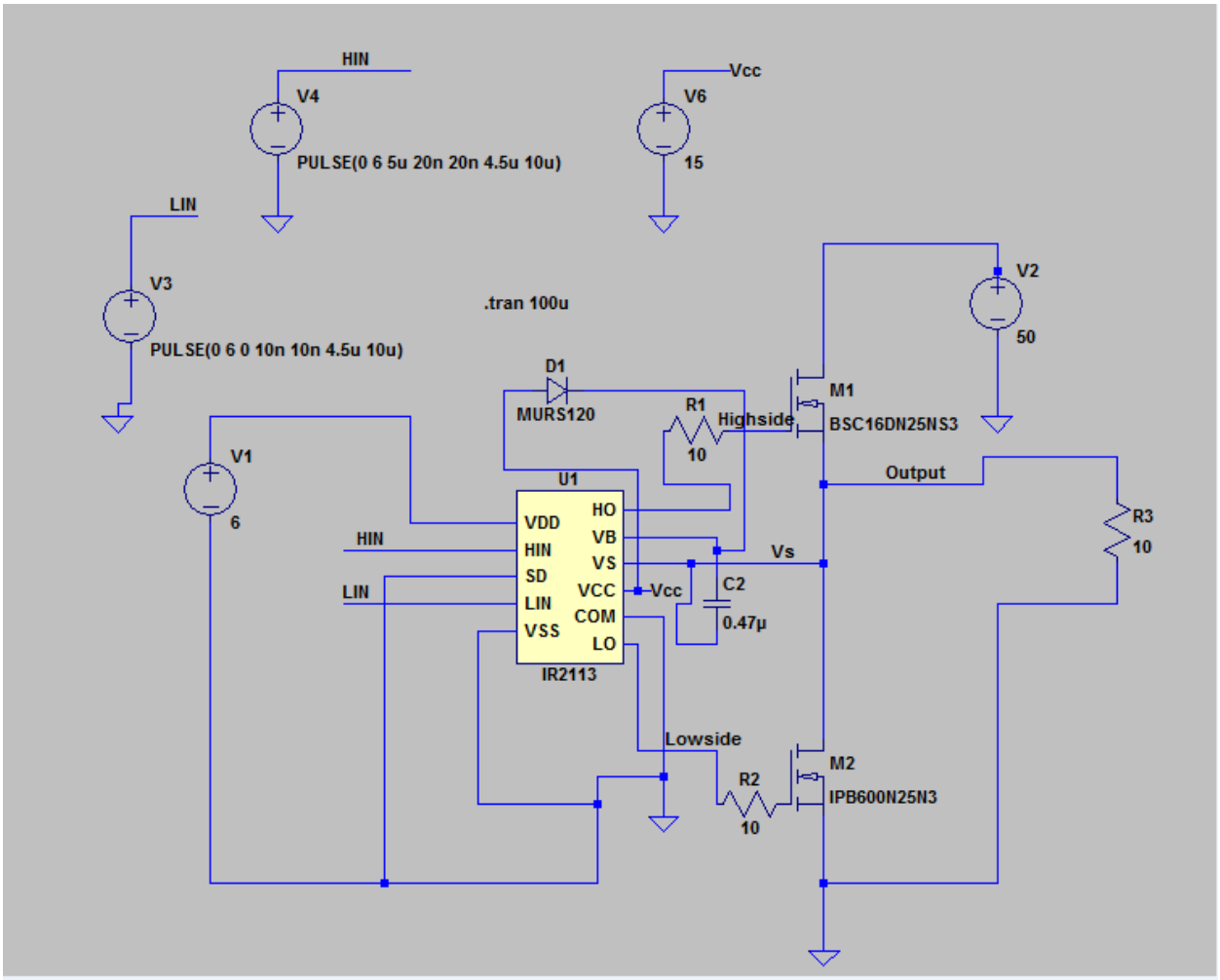
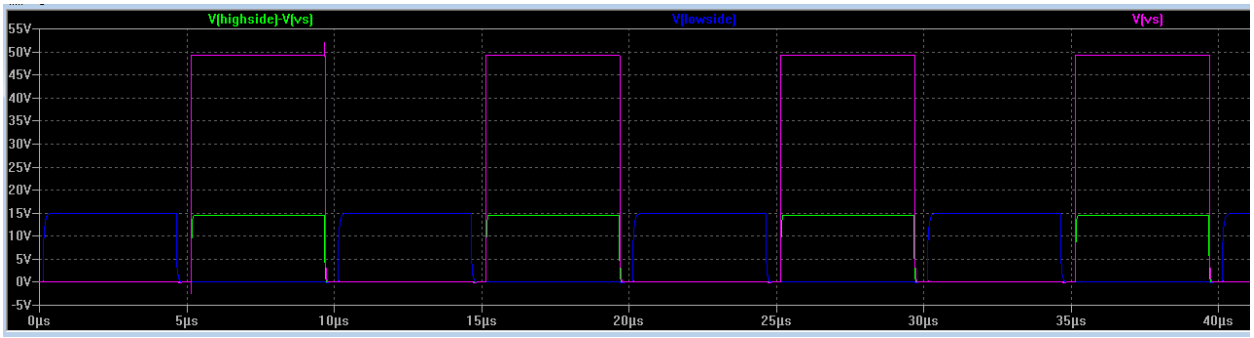
M2
IRFP240
R2
100
LO
R3
10k
R4
10


V(ho)
V(lo)
V(output)
50V
45V
40V
35V
30V
25V
20V
15V
10V
5V
0V
-5V
0µs
5µs
10µs
15µs
20µs
25µs
30µs
35µs
40µs
45µs
50µs

Simulation of a high side and low side gate driver



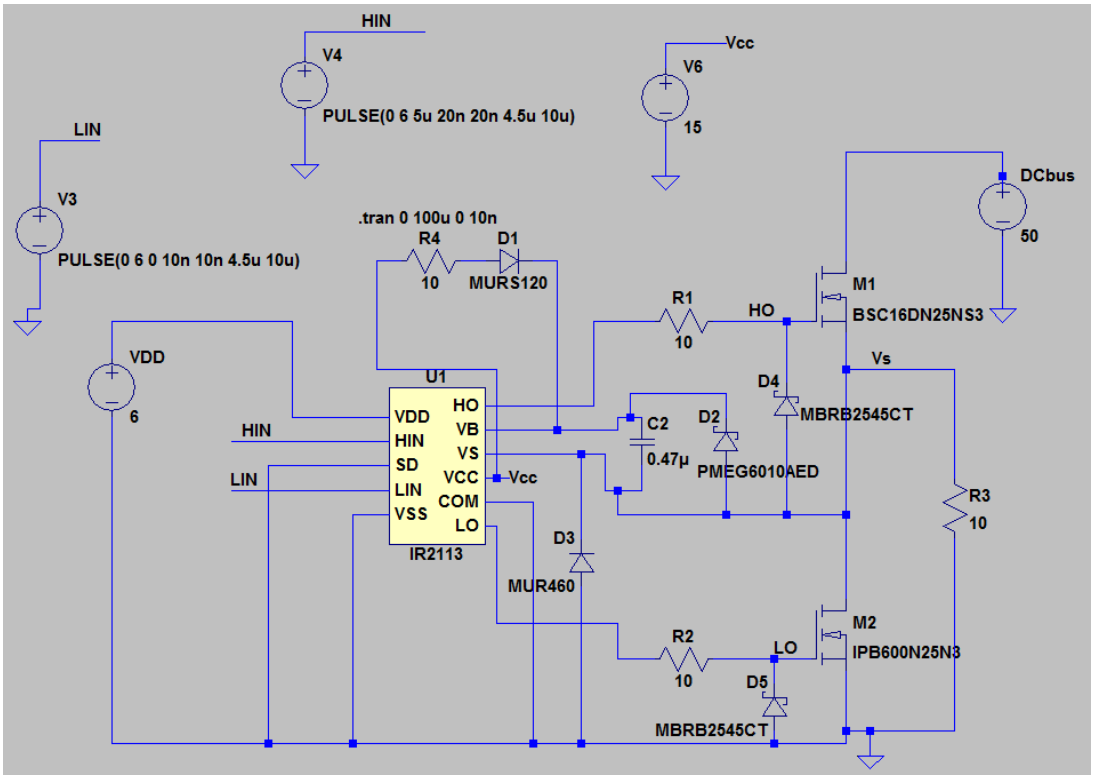


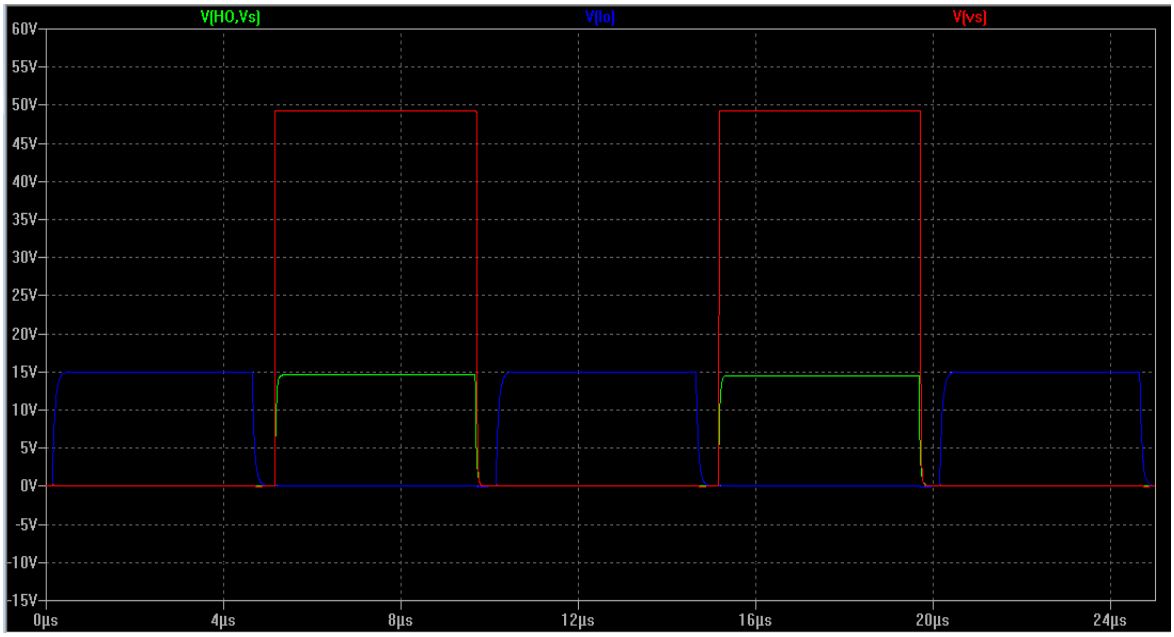
A good design using high and low side gate driver is shown below:

The voltage at Vs node could be anywhere between the DC bus voltage and COM prior to charging the bootstrap capacitor

D2 is a 60 V schottky which helps in avoiding Vbs voltage being biased to a negative voltage prior to power up. D3 will make sure Vs will not go negative, even a resistor of 1M ohm is used from Vs to COM if diode D3 is not used. D3 has a voltage rating = 600V

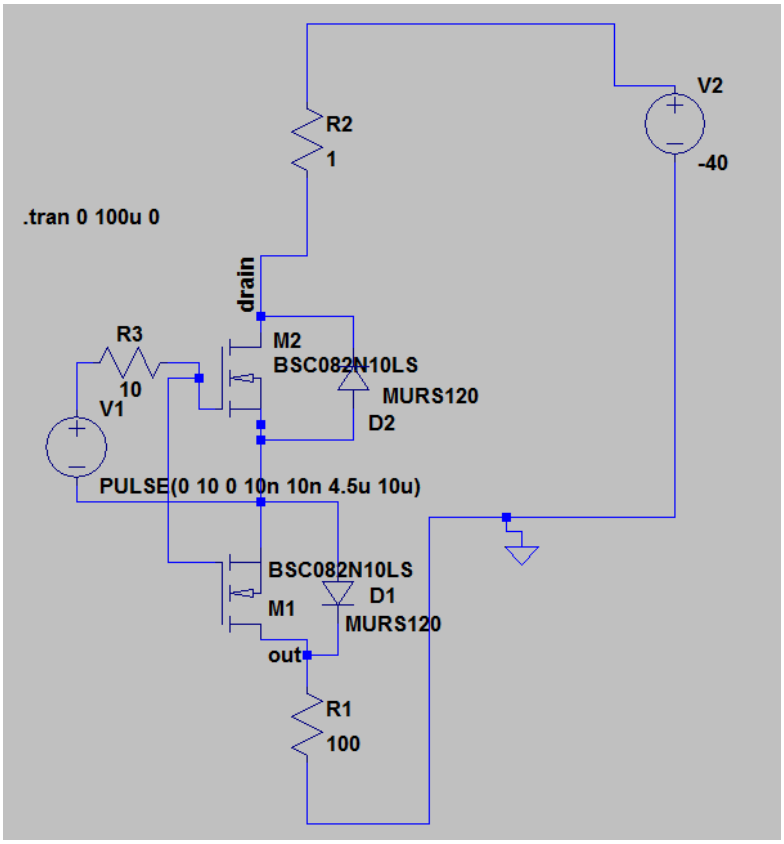
D4, D5 help in clamping the gate voltage.

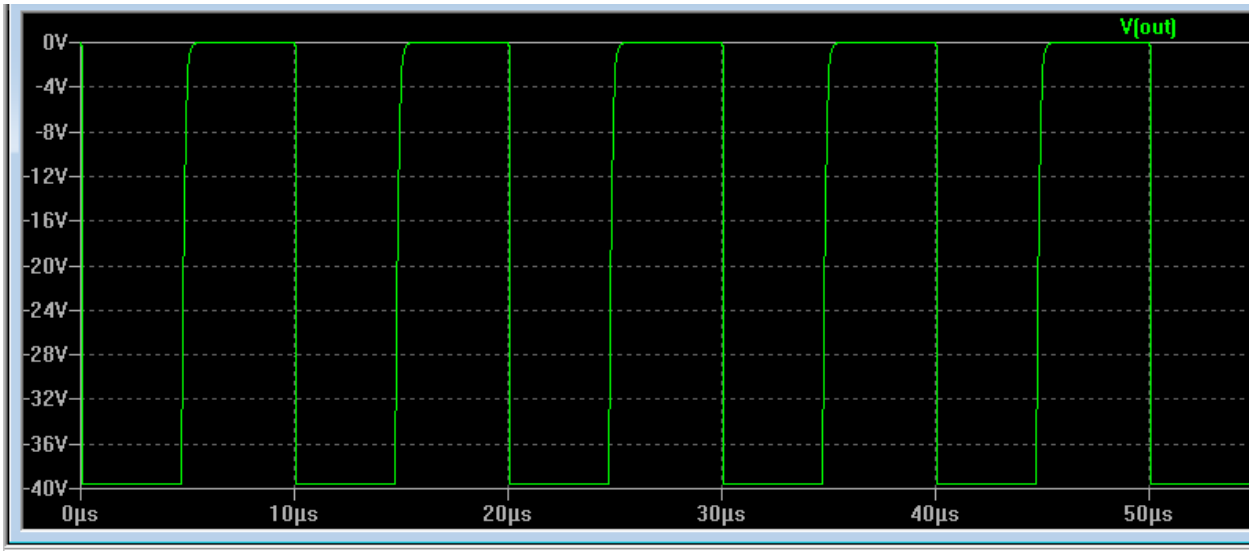




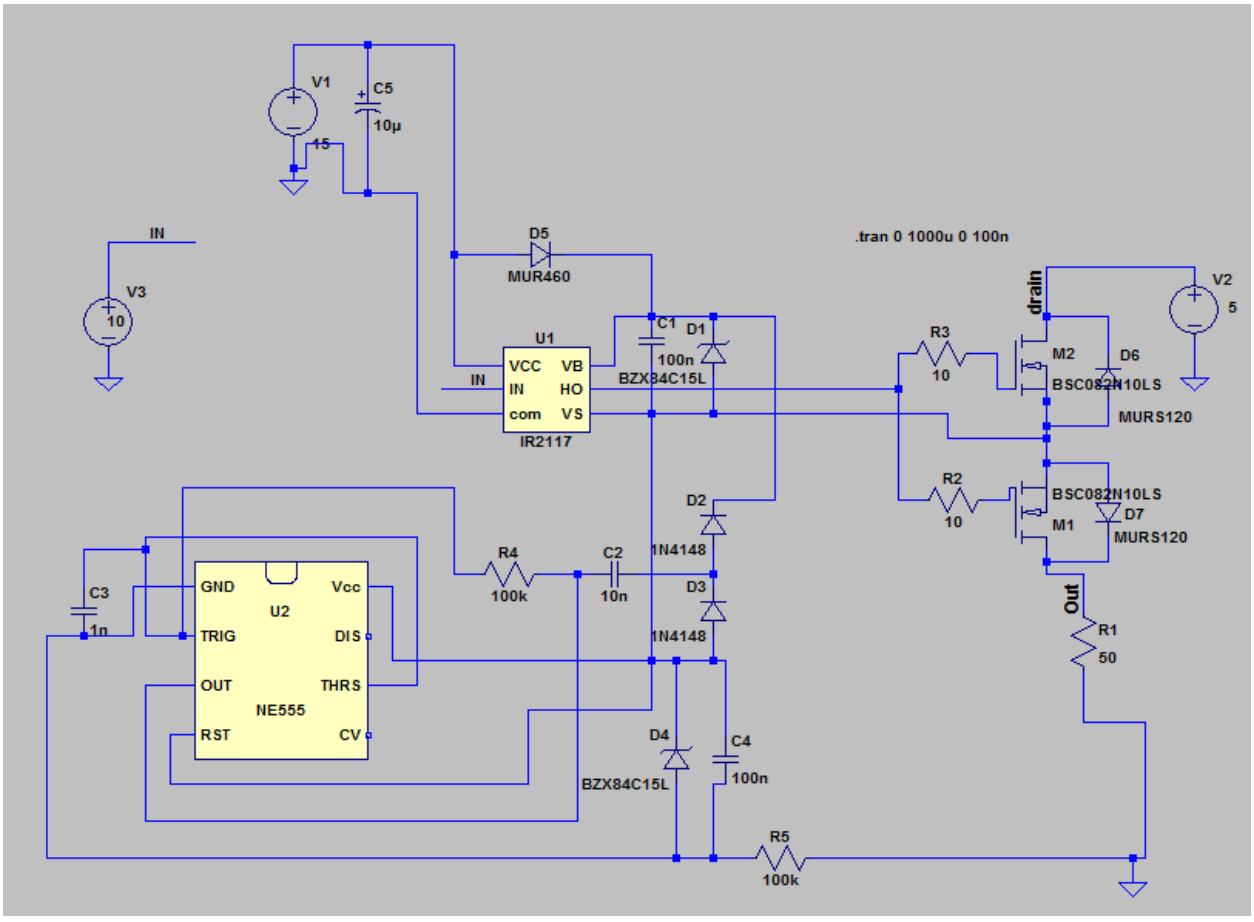
Bidirectional current flow:

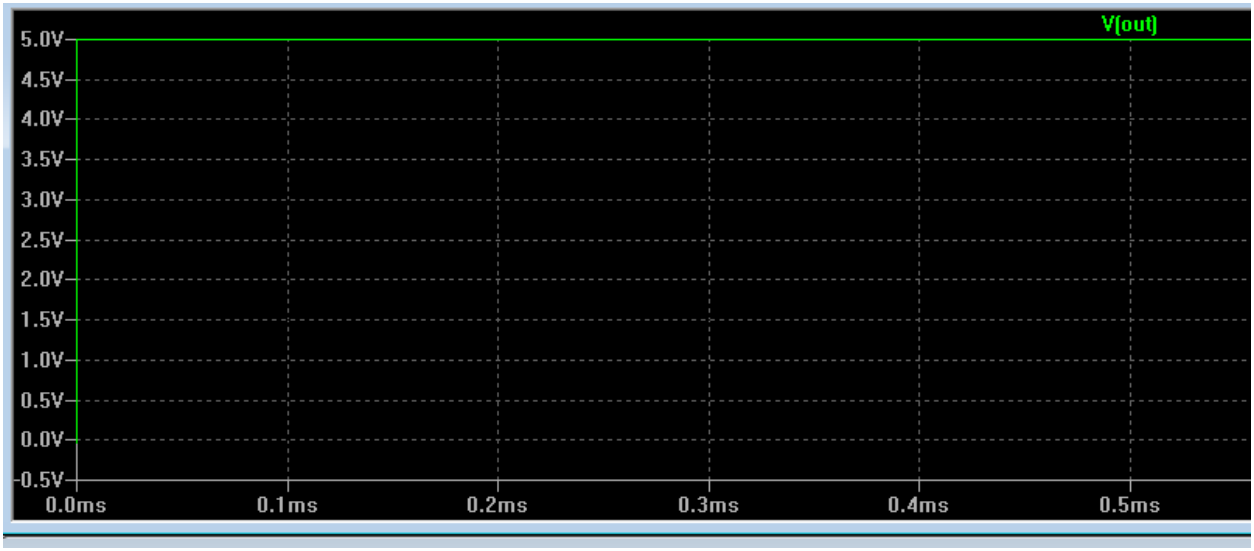
Switching AC, positive and negative voltages: Figures below this show the circuit with charge pump



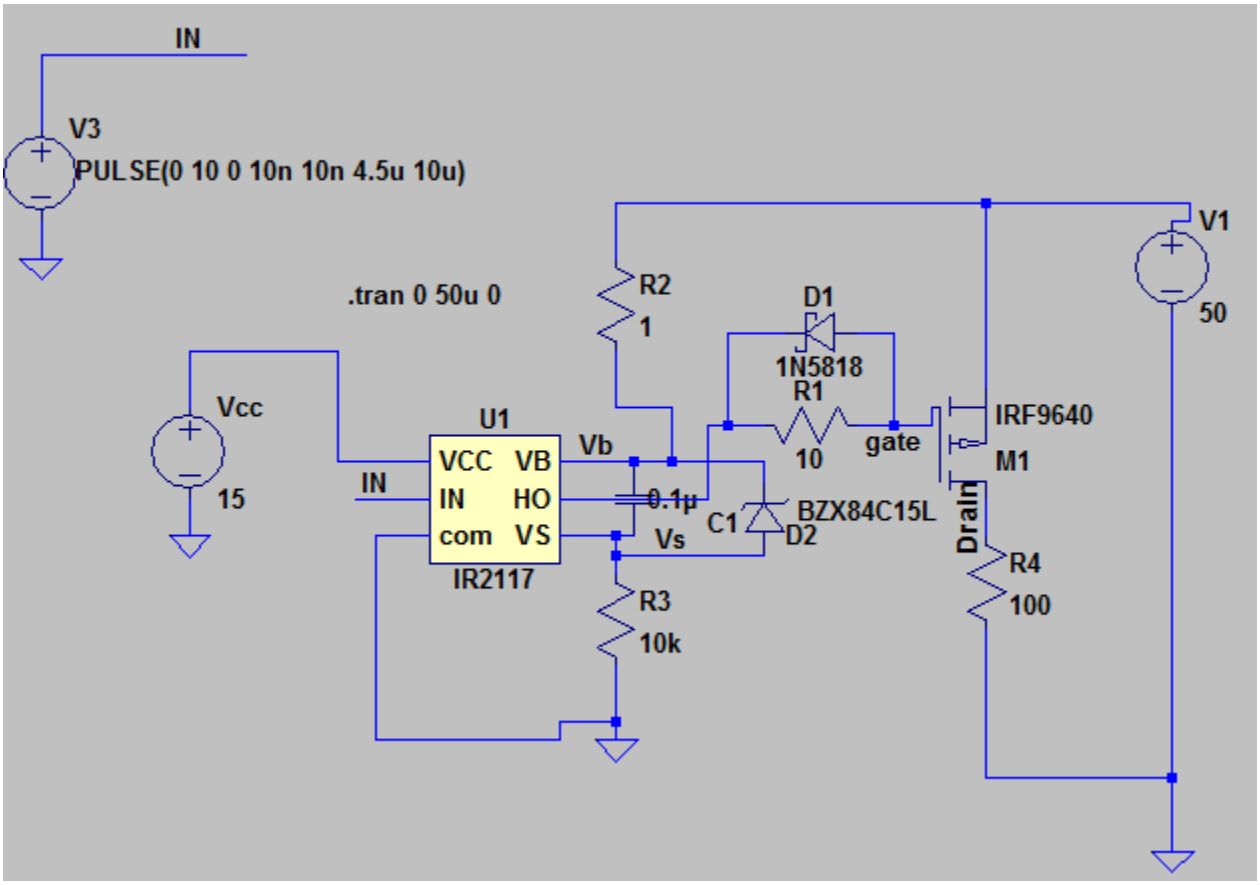


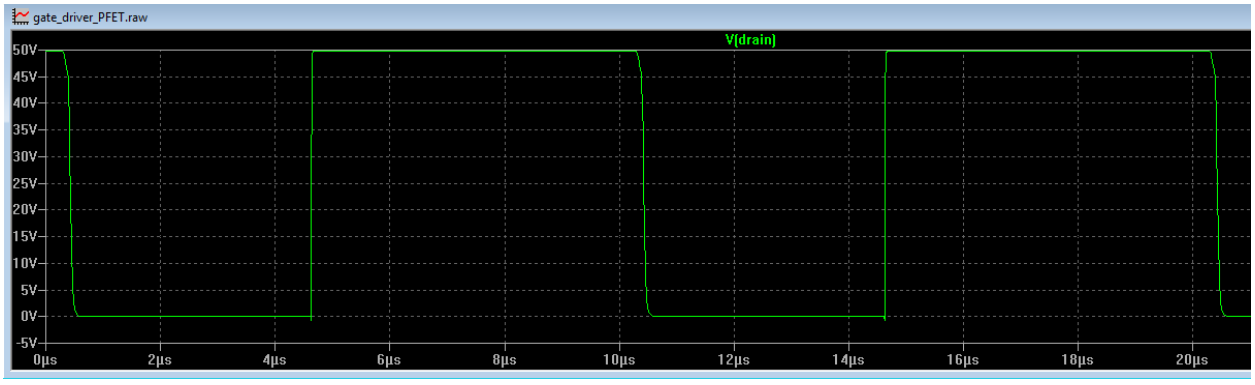
When input (HIN) is not being switched and constant DC voltage is applied, then the below circuit can be built with charge pump to switch +5V/-5V, 5 VAC to the load.


V1
15
C5
10µ
IN
V3
10
D5
MUR460
.tran 0 1000u 0 100n
drain
V2
5
U1
VCC
VB
IN
HO
com
VS
IR2117
C1
100n
D1
BZX84C15L
R3
10
M2
D6
BSC082N10LS
MURS120
R2
10
BSC082N10LS
D7
M1
MURS120
D2
1N4148
D3
1N4148
R4
100k
C2
10n
C3
1n
U2
GND
Vcc
TRIG
DIS
OUT
THRS
NE555
RST
CV
Out
R1
50
D4
BZX84C15L
C4
100n
R5
100k

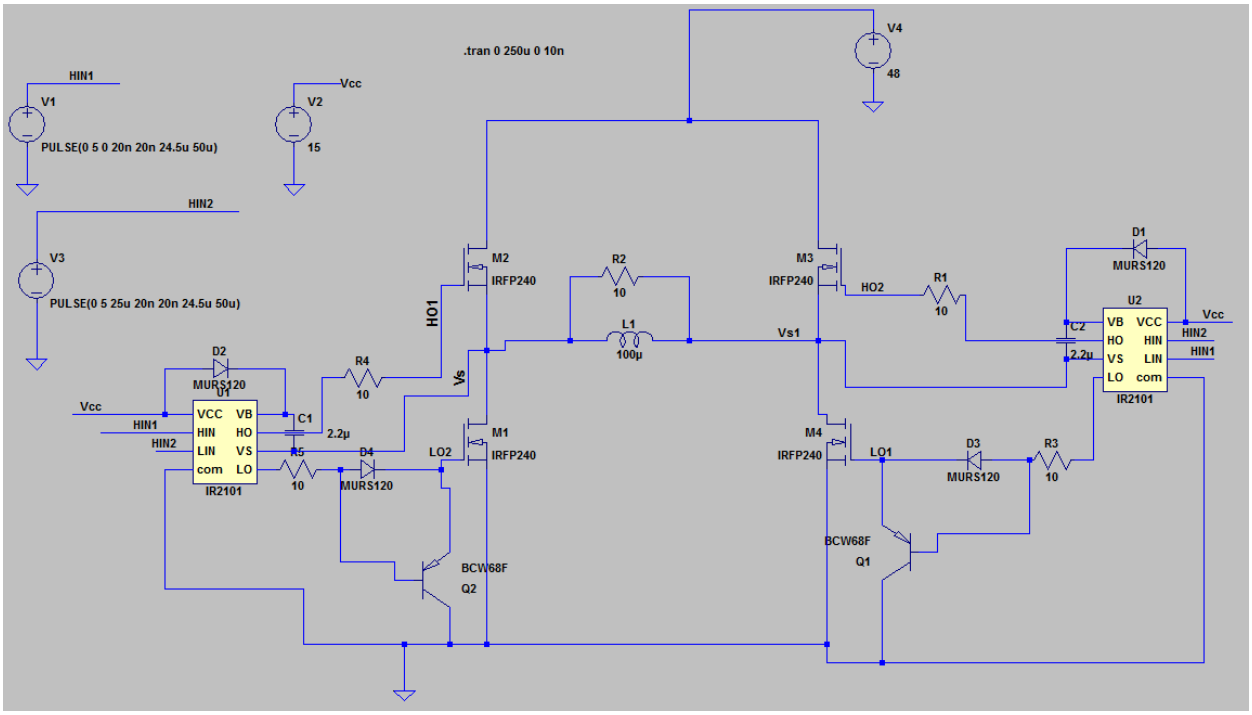

V(out)
5.0V
4.5V
4.0V
3.5V
3.0V
2.5V
2.0V
1.5V
1.0V
0.5V
0.0V
-0.5V
0.0ms
0.1ms
0.2ms
0.3ms
0.4ms
0.5ms

Using a single P-channel high side mosfet to switch 50 V

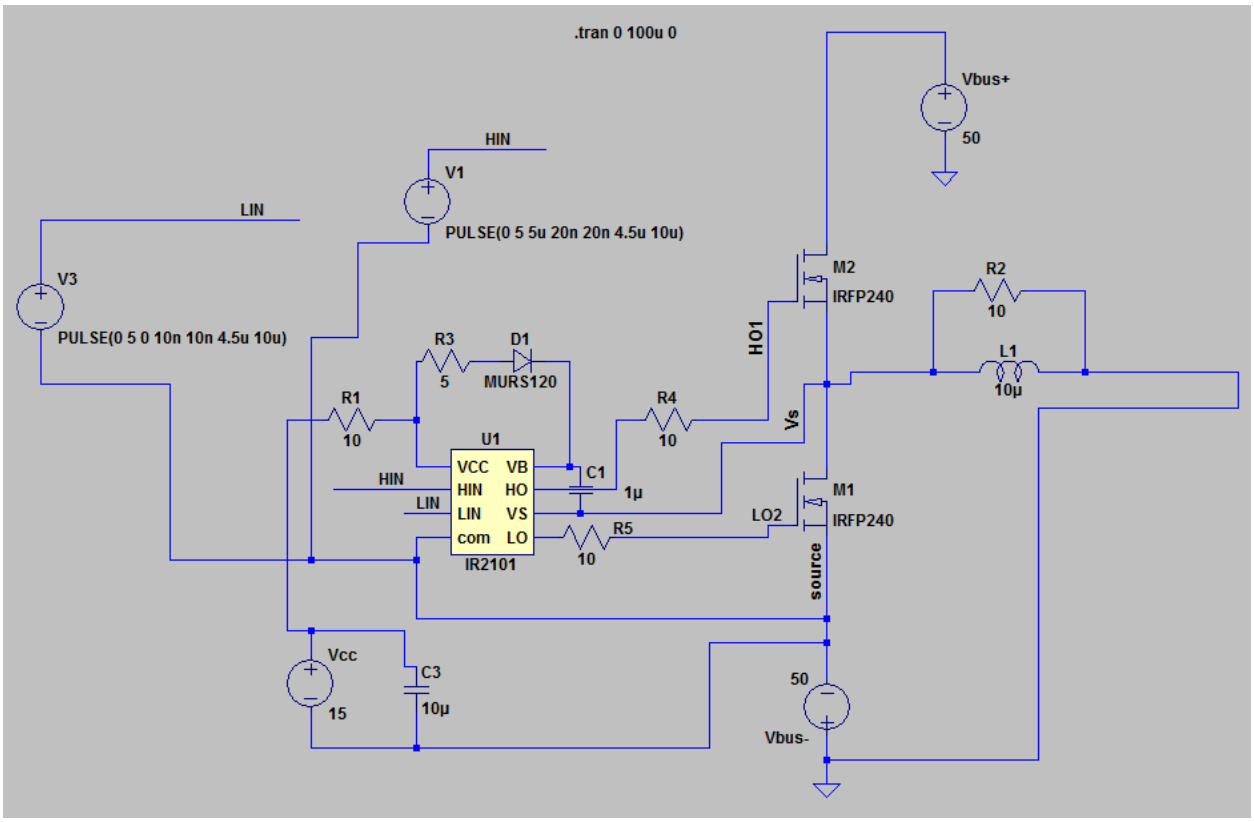




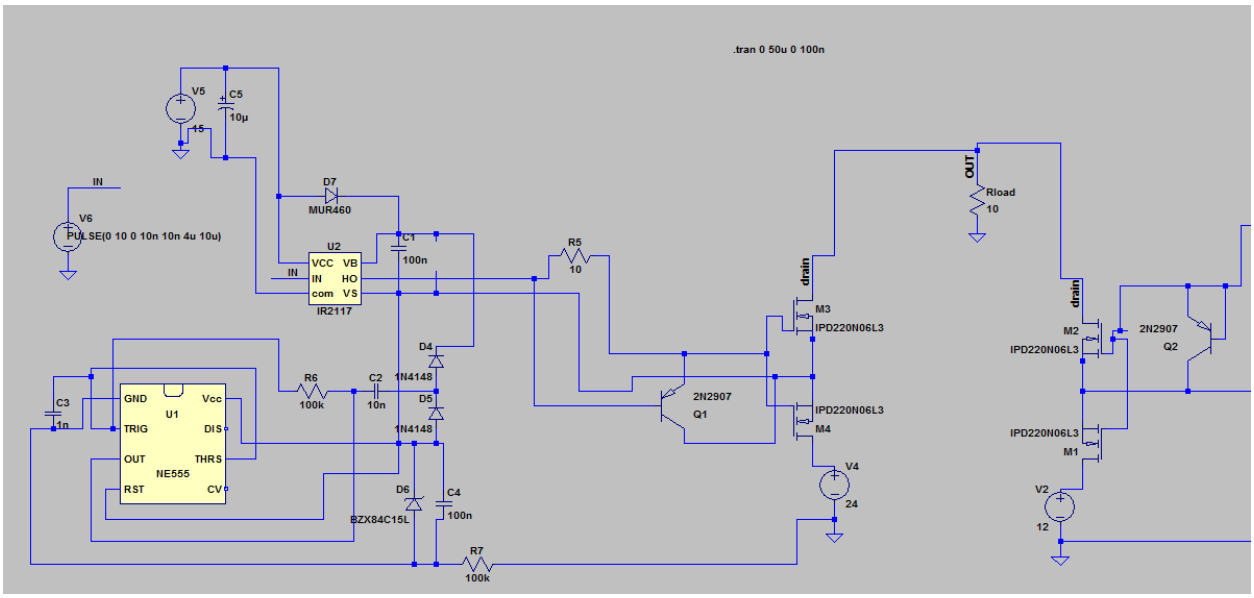
A full bridge converter

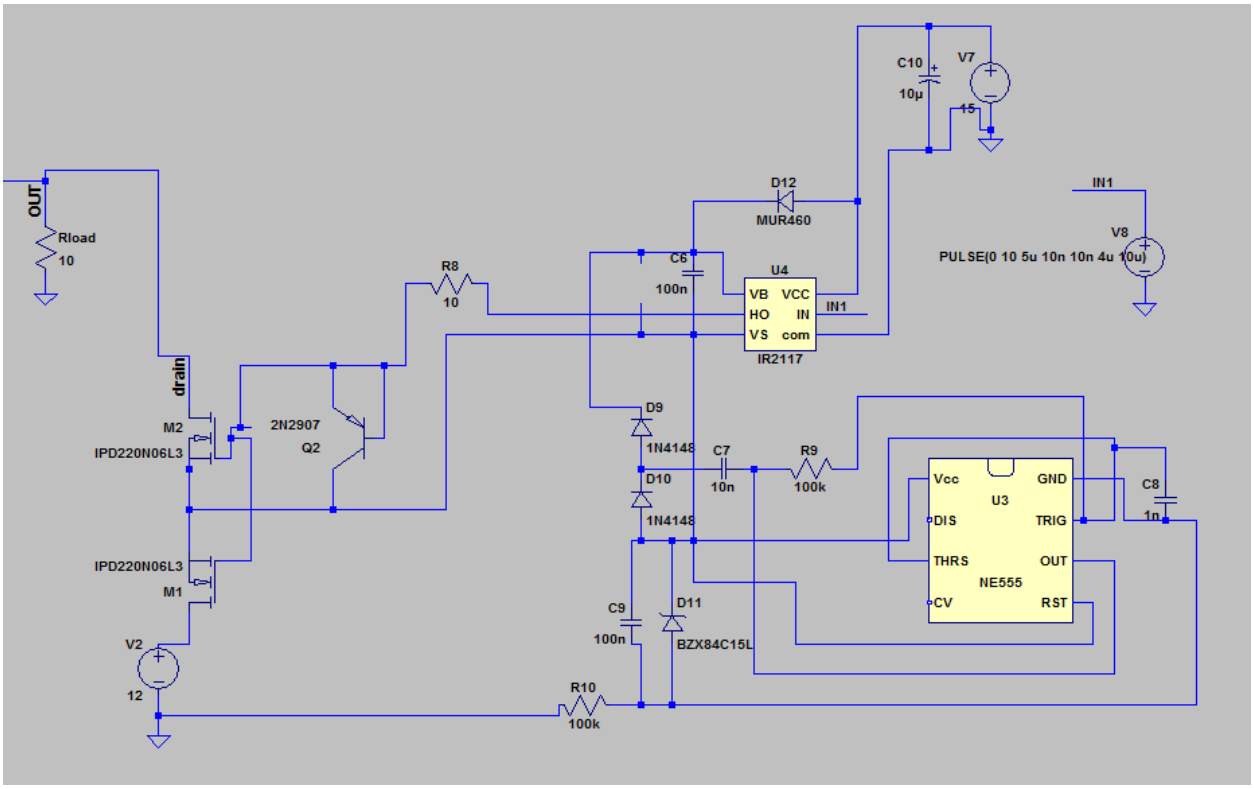


Using a gate driver when COM pin is referenced to –Vbus voltage



Oring application (switching 24 V/12 V) using charge pump, gate driver and back to back connected common source mosfet's. Schematic is divided into 2 halves.





Output voltage at the load