Design and Investigation of an Isolated Gate Driver Using CMOS Integrated Circuit and HF Transformer for Interleaved DC/DC Converter

The Van Nguyen, Jean-Christophe Crebier, and Pierre-Olivier Jeannin

***Abstract*—This paper deals with the design and the implementation of an isolated gate driver system using a CMOS integrated circuit for interleaved dc/dc converters. It is based on a novel gate driver topology for power switches like MOSFETs and insulated-gate bipolar transistors. Composed of two legs of a CMOS inverter, a high-frequency pulse transformer, and two Zener diodes connected in antiseries configuration with the gate of the power switch, this driver topology provides an optimal bipolar gate driver waveform with greater positive and negative gate biases to fasten the switch on and off. It represents a simple ultracompact isolated gate driver simple to integrate in CMOS technology. Power consumption, system size, and robustness of the gate driver are therefore optimized. This integrated driver circuit can be used for any multitransistor applications. We detail the operation principle of the proposed driver topology in this paper. We implemented the gate driver to control a three-phase interleaved boost converter; the results show the effectiveness of the proposed driver system.**

***Index Terms*—CMOS integrated circuit, insulated gate bipolar transistors (IGBTs), interleaved dc/dc converter, isolated gate driver, pulse transformer, Zener diode.**

I. Introduction

CONVERTERS are widely employed in power systems and many other industrial applications to shape and regulate electrical energy. In high-power applications, the interleaved topologies represent a beneficial solution owing to the advantages of their power distribution, harmonic current cancellation, fast transient response, and passive component size reduction. Several research works have introduced and studied new structures of interleaved dc/dc converters [1]–[5], analyzing and demonstrating the great interests of these conversion topologies. Other research works have led to the improvement of the design and assembly of the passive components of these converters in order to reduce the inductor and transformer sizes [4], [6]–[8]. These topologies offer great benefits, but they require numerous active switches and associated gate drivers, sensors, and control [1], [2], [4], [9]. If many research works are done on the passive device assembly and integration for interleaved dc/dc converters, some research works are also done on implementation simplification and reliability topics related to active power device integration and the gate driver unit [10]–[12].

In this paper, we focus on an isolated and partially integrated gate driver that can be used to drive power switches of not only three-phase dc/dc interleaved converters but also any type of multiphase converters depending on the number of power devices that need to be driven with isolated gate drivers. The basic gate driver structure is based on a new driver topology, which includes as few components as possible while providing high performance, optimum isolated gate driver bipolar waveforms, high switching speed, and wide-range variable duty cycle. Moreover, the new driver topology permits downsizing the necessary pulse transformer and, at the same time, minimizing the propagation path for conducted electromagnetic interference (EMI). The type of components used and their limited number raise up the integration level as well as the reliability of the gate driver, minimizing the number of interconnects at the secondary side. Due to the chosen topology, several primary sides of the isolated gate driver circuits can be integrated on silicon to make a compact, reliable, and versatile multidriver system. We will briefly recall the operation principle of the new driver topology [13]. Then, we will present the design of the integrated driver and, finally, its implementation in a three-phase interleaved boost converter.

II. Proposed Gate Drive Circuit—Description and Operation

The basic topology of the proposed gate driver is shown in Fig. 1 [13]. On the primary side of the transformer, a full-bridge CMOS inverter is used to create a bipolar three-level ac signal. If a purely or regulated ac bipolar signal cannot be generated, a capacitor C in series connection with the primary side can be used to cut any possible dc voltage and to ensure not to saturate the high-frequency (HF) transformer. On the secondary side, only two simple components are required: two Zener/avalanche diodes $Z1$ and $Z2$. The gate and pull-down resistors Rg and

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T. V. Nguyen and J.-C. Crebier are with the Grenoble Electrical Engineering Laboratory, UMR 5529, Centre National de la Recherche Scientifique/Institut Polytechnique de Grenoble/Université Joseph Fourier, 38402 Grenoble, France (e-mail: The-Van.NGUYEN@g2elab.grenoble-inp.fr; Jean-Christophe.CREBIER@g2elab.grenoble-inp.fr; jean-christophe.crebier@g2elab.grenoble-inp.fr).

P.-O. Jeannin is with with the Grenoble Electrical Engineering Laboratory, UMR 5529, Centre National de la Recherche Scientifique/Institut Polytechnique de Grenoble/Université Joseph Fourier, 38402 Grenoble, France, and also with the Université Joseph Fourier, 38041 Grenoble, France (e-mail: pierre-olivier.jeannin@g2elab.grenoble-inp.fr).

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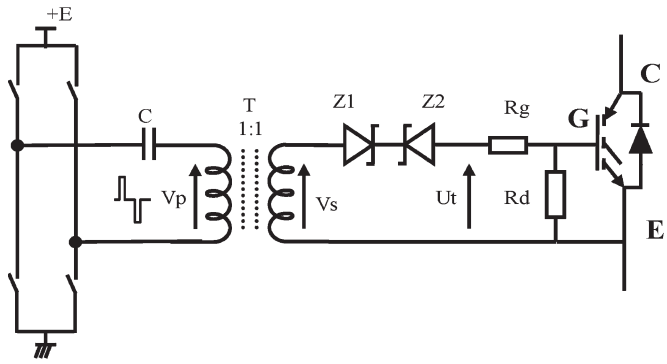


Fig. 1. Schematic of gate driver for an IGBT.

Rd, respectively, can be used if necessary for switching speed and gate pull-down control. Finally, an HF pulse transformer ensures the galvanic insulation between primary and secondary sides.

Compared to the state of the art [14], this gate driver is based on more simple and more reliable components, allowing the simplification of the implementation and integration of the whole structure.

Because insulated-gate bipolar transistors (IGBTs) and MOSFETs are driven by charging and discharging their gate capacitance, which is a high-quality metal–insulator–semiconductor structure, once the gate charge sequence is completed, it is not necessary to maintain a gate current; however, the gate potentials created must be held for at least the switching period. Our solution is based on the use of antiseries connection of two Zener/avalanche diodes in order to hold the positive and the negative voltages applied to the gate of the power switch. The $Z1$ holds the gate voltage during the ON state, and the $Z2$ maintains a negative-bias gate voltage during each OFF state. Fig. 2 shows a set of qualitative waveforms to illustrate this operation, where

V_{Zi} voltage across the diode;
Vf_{Zi} absolute forward voltage;
VBR_{Zi} absolute avalanche voltage;
α duty cycle.

The circuit operation is separated in four intervals, in which the following equation is always valid:

$$\mathrm{Ut} = \mathrm{Vs} + V_{Z1} - V_{Z2}. \tag{1}$$

1) **Phase 1**: To turn on the transistor, a short positive pulse is applied on the primary side of the transformer, the secondary-side voltage Vs rises to $+E$, and $Z2$ enters in avalanche mode while $Z1$ is forward biased, thus creating a positive pulse current in the gate of the transistor. The resulting voltage applied at the transistor gate plus its gate resistor can be expressed by the following:

$$\mathrm{Ut} = E - \mathrm{Vf}_{Z1} - \mathrm{VBR}_{Z2} \tag{2}$$

$$V_{\mathrm{GE}}(t) = \mathrm{Ut} - \mathrm{Rg} \cdot \mathrm{Ig}(t). \tag{3}$$

At $t1$, the gate voltage has reached the desired value

$$V_{\mathrm{GE}}(t1) = \mathrm{Ut} = E - \mathrm{Vf}_{Z1} - \mathrm{VBR}_{Z2}. \tag{4}$$

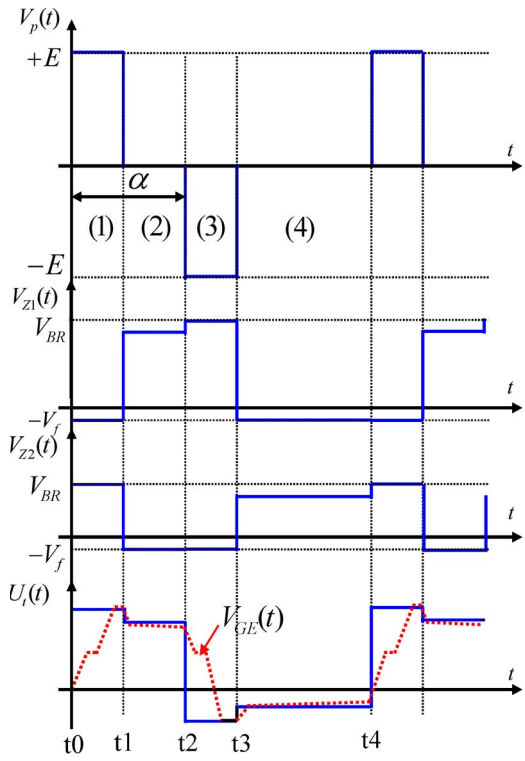


Fig. 2. Main time-domain waveforms of the proposed gate driver over a switching cycle.

2) **Phase 2**: The voltage applied to the primary side of the transformer falls to zero, given that there is no more current charging the gate, $Z2$ is no longer in avalanche, and the voltage between gate and emitter terminals is held by $Z1$. During this interval, the input capacitance C_{iss} holds the gate voltage; it discharges slightly as a function of time through the leakage current of the reverse-biased diode $Z1$ and through the pull-down resistor Rd. The gate charge Q_{GE} imposes the voltage across the diode $Z1$, and note that, during this phase, $V_{Z1}(t) < \mathrm{VBR}_{Z1}$.

We have $\mathrm{Ut}(t) \approx V_{\mathrm{GE}}(t)$, and so

$$V_{Z1}(t) = V_{\mathrm{GE}}(t) - \mathrm{Vf}_{Z2}. \tag{5}$$

Note that the voltage maintained by $Z1$ can be different and lower than the voltage applied during turn-on which allows accelerating the switching transition and then optimizing the voltage applied to the gate to limit power device current short-circuit levels [15] or to increase oxide gate duration and reliability [16].

3) **Phase 3**: To turn off the transistor, a short negative voltage pulse is applied by the CMOS inverter on the primary side of the transformer, creating negative voltage and current pulses on the gate of the power transistor, and the C_{GE} voltage potential is then reversed. $Z1$ enters into avalanche, while $Z2$ is forward biased. The gate capacitor is discharged through the gate resistor, and its voltage decreases consequently, which can be expressed as follows:

$$\mathrm{Ut} = -E + \mathrm{VBR}_{Z1} + \mathrm{Vf}_{Z2} \tag{6}$$

$$V_{\mathrm{GE}}(t) = \mathrm{Ut} + \mathrm{Rg} \cdot \mathrm{Ig}(t). \tag{7}$$

At $t3$, the $V_{\rm GE}$ has reached the minimum negative value

$$V_{\rm GE}(t3) = {\rm Ut} = -E + {\rm VBR}_{Z1} + {\rm Vf}_{Z2}. \quad (8)$$

4) **Phase 4**: The transformer primary voltage is set to zero, there is no more gate current, the input capacitance $C_{\rm iss}$ maintains the gate voltage, and it discharges slightly with a behavior similar to that of phase 2. The Zener diode $Z2$ is reverse biased and holds the gate-to-emitter voltage potential. Note that, during this phase, $V_{Z2}(t) < {\rm VBR}_{Z2}$

$$V_{Z2}(t) = -{\rm Vf}_{Z1}(t) - V_{\rm GE}(t). \quad (9)$$

The proposed gate driver offers several advantages with respect to design and performance criteria. Because the transformer is needed only to carry short pulses of voltage and current used to charge and discharge the power switch gate capacitance, its design can be optimized with respect to times $t1-t0$ and $t3-t2$ in Fig. 2. These times are very short times (about 100–500 ns as a function of the gate capacitance and the charge time constant); thus, the volt–second product of the transformer is very small. It permits using a very small core size; thus, this transformer could even be integrated directly on a silicon die [17]. Another alternative solution could be to use a coreless printed circuit board (PCB) transformer [18], [19]. In addition, the duty ratio of the power circuit does not have any effects on the core saturation, and almost any duty cycle value can be transferred to the gate of the power device. This gate driver is very suitable for HF applications such as dc/dc converters. For low-frequency applications or permanent ON and OFF operations, we invite the reader to refer to [20] for reasons of clarity and space. Moreover, this driver uses only unipolar power supply to perform a bipolar gate driver signal. The unipolar supply is first used to create a three-level bipolar ac signal which, in turn, becomes a four-level bipolar signal, which is very useful to control and to drive accurately the power device gate capacitance. Finally, on the transformer secondary side, the components are elementary avalanche signal diodes, which are simple to implement and reliable and can even be integrated into a single chip with two terminals and three semiconducting regions such as a simplified bipolar signal transistor. This structure could even be integrated in the power device to drive in a similar manner as presented in [21]. This driver fulfills high-speed switching requirements owing to short but large gate voltage pulses to switch on and a high negative-bias gate voltage to switch off quickly the transistor without having to fully polarize with a large negative bias the gate capacitance. This point allows compensating a little the main drawback of this technique, which is related to driver consumption, while providing efficient negative-bias gate shielding.

Indeed, the main limitation of this driving technique remains the extra losses generated during the avalanche operation of the Zener/avalanche diodes when turning on or off the power device.

In the next section, we will address the integration level of the proposed gate driver topology in order to increase its compactness, robustness, and ease of implementation.

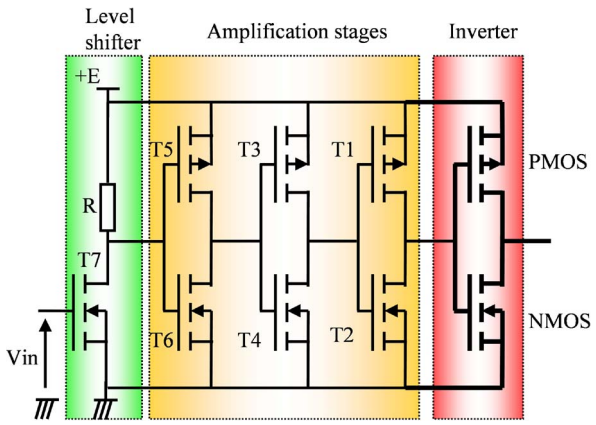


Fig. 3. Schematic of an inverter leg in the integrated gate driver.

III. Investigation of Integrated Gate Driver on Interleaved Boost Converter

A. Design of the Integrated Gate Driver

The integrated gate driver was designed to contain 12 CMOS inverter legs based on the 0.35-μm CMOS high-voltage technology H35B4D3 of Austria Microsystems (AMS) that offers operating voltages up to 20 and 50 V. This technology is suitable for power management products, display drivers, and sensors.

Fig. 3 shows the internal schematic of one CMOS inverter leg in the integrated gate driver. It contains three stages: the level shifter stage, the amplification stage, and the inverter stage itself. Each inverter leg is composed with three amplification stages to maintain the highest speed responses (less than 1 ns) while preventing any short-circuit occurrence of the main CMOS inverters at their switching transitions [22], [23]. Therefore, each component in the amplification stage was optimized owing to a specific design approach [24] in order to minimize the short-circuit current and, then, the power consumption of the integrated circuit. Moreover, because the integrated chip contains many inverter legs, input control signals were decoupled as much as possible from output inverter middle points. In such way, common ground (GND) tracks were avoided as much as possible, and control pads were separated to output pads as much as possible to avoid tracks or wire bond electromagnetic coupling. Therefore, the output signal of the level shifter is amplified by a first strong amplification stage ($T5$ and $T6$) before being transferred to the following block at large distance. Then, the second ($T3$ and $T4$) and the third ($T1$ and $T2$) amplification stages are designed to amplify the control signal for CMOS inverter transistors at minimum speed response reduction.

The CMOS transistors of the inverter were designed to have a peak source/sink current of 3 A at the maximum output voltage of 20 V while driving a power transistor of 4.5-nF effective input capacitance. This maximum output current of the last CMOS inverter stage represents the saturation currents of the PMOS and NMOS transistors, which depend on their gate width values. As a result, we obtained the following values for channel widths for the transistors of the inverter leg by using the process parameters of the technology:

$$W_{\rm PMOS} = 8333\ \mu{\rm m} \qquad W_{\rm NMOS} = 5714\ \mu{\rm m}.$$

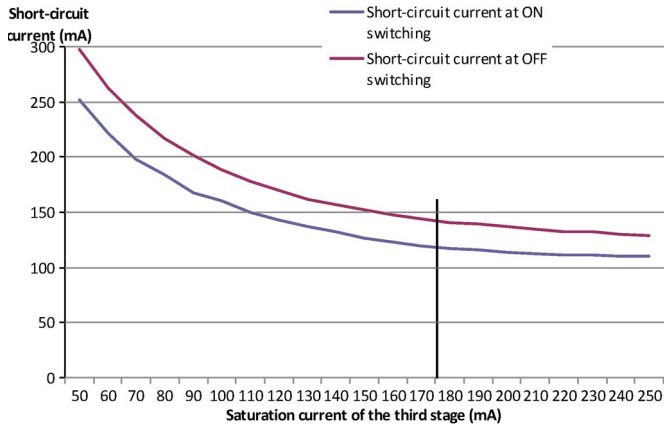


Fig. 4. Design of the third amplification stage (simulation results).

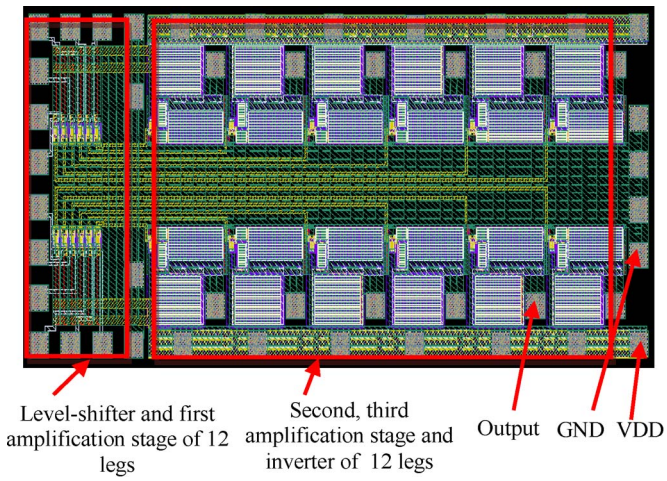


Fig. 5. Layout of the integrated circuit.

With such large transistor sizes, speed response and short-circuit occurrence must be accurately addressed. The design of each stage of amplification has to start from the largest stage. Oversizing the third amplification would generate additional switching losses in this stage and would increase without benefits the sizes of the following amplification stages. However, if this stage is designed too small, the transistors of the main CMOS inverter stage will switch too slowly. We based our design on the limit of short-circuit criteria in CMOS inverters [24] to optimize the size of the third amplification stage. Fig. 4 shows the optimal channel width or, in other ways, the optimal saturation current of the third-amplification-stage transistors, which achieves the best compromise between sizes and short-circuit currents. As we can observe in Fig. 4, beyond a saturation current level of 180 mA, the maximum short-circuit current in the output CMOS inverter stage stabilizes; therefore, this value was chosen to design the third amplification stage

$$W_{T1} = 500\ \mu\text{m} \qquad W_{T2} = 342\ \mu\text{m}.$$

In fact, the transistor sizes in the third amplification stage are small enough to neglect its short-circuit current. Therefore, the second amplification stage was designed to obtain the highest speed response of the inverter. The resulting design parameters are the following ones for PMOS and NMOS, respectively

$$W_{T3} = 83\ \mu\text{m} \qquad W_{T4} = 57\ \mu\text{m}.$$

The first amplification stage has to amplify the output signal of the level shifter before being transferred to the second stage, which could be as far as 2.4 mm. As a result, its size has to be large enough to maintain the transfer speed and limit possible EMI interactions. We obtained results close the following values made identical to those of the second amplification stage to ease the layout design:

$$W_{T5} = 83\ \mu\text{m} \qquad W_{T6} = 57\ \mu\text{m}.$$

The receiver stage of the level shifter potential is a classical structure based on the association of N-MOSFET and a polarization resistor R. We have to pay attention to the resistance value of R because it has effects on the global power consumption and dynamic response of the integrated driver. Another issue concerns thermal behavior of the chip, and the surface occupied by the resistance R has to be large enough to dissipate its power consumption. We obtained the following parameters for the level shifter stage:

$$W_{T7} = 27\ \mu\text{m} \qquad R = 30\ \text{k}\Omega.$$

Other important issues are related on the one side to power supply GND and $+E$ connections as well as inverter leg middle point interconnections and on the other side to limiting coupling among driving signals in each inverter leg between signal traces and inverter output traces. As a result, the locations of supply pads as well as output pads are critical not only to avoid unnecessary common tracks but also to avoid circulation of undesirable large currents able to create large EMI interactions among traces. As we have mentioned previously, the input signals from the complex programmable logic device (CPLD) can be far from the output inverter last amplification stages, as shown in Fig. 5. In addition, the size of the traces affects the voltage drop of GND potential. The location of GND pads, as well as a good design of the GND traces, is very important to minimize parasitic impedance effects (resistive, capacitive, and inductive). We studied the most critical situation when one input signal is switched from GND to VDD while another is connected to the ground and with the longest transfer distance between the first and the second amplification stages. Fig. 6 shows an equivalent schematic of the studied case in which $L1$, $L2$, and Lg are the inductances of two parallel traces and the ground, $R1$, $R2$, and Rg are their resistances, $M1g$, $M2g$, and $M12$ are the mutual inductances between these traces, and $C1$ and $C2$ are the parasitic capacitances of two traces. We used the simulation tool INCA3D [25] in order to derive the value of these parameters; the results are presented in Table I.

These parameters were then used to run simulations in Cadence to analyze the coupling impact on the output of leg 2. It is also important to note that every leg has five inversion stages; as a result, the output leg signal is enabled at high state if the input signal is connected to the ground. The simulated results shown in Fig. 7 demonstrate the occurrence of oscillations at the output of leg 2, which attains up to 2 V during the switching transistor of leg 1. Therefore, it is necessary to eliminate the

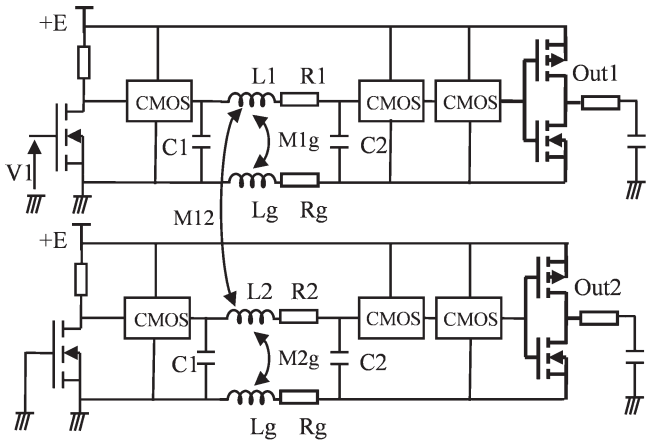


Fig. 6. Equivalent schematic of coupling phenomenon between two legs.

TABLE I
PARASITIC PARAMETERS

Parameter	Value	Unit
R1, R2	13,67	Ohm
L1, L2	3,2	nH
C1, C2	50	fF
Rg	0,27	Ohm
Lg	1,6	nH
M1g, M2g	1,67	nH
M12	1,89	nH

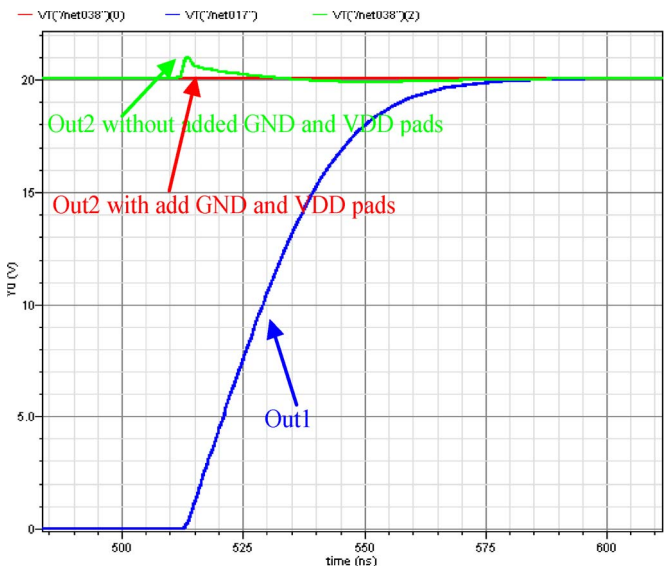


Fig. 7. Simulation results of the coupling phenomenon.

coupling phenomena. One solution proposed is to add VDD and GND pads on the inverter on the opposite side to the entrance of driving signals, as shown in Fig. 5; it permits using a decoupling capacitor between VDD and GND on the output side of the packaged chip. Moreover, the gate currents will flow in a small loop inside the chip, sharing almost no common GND/VDD tracks with the input and first amplification stages. The simulation results in Fig. 7 show a good improvement.

The chip was realized and packaged by AMS via circuits multi-projects [26]; its area is about 3 mm × 1.2 mm in Fig. 8. Fig. 9 shows a picture of the packaged gate driver CQFP-44. It requires 34 pins for ideal operation (12 gate signal inputs, 12

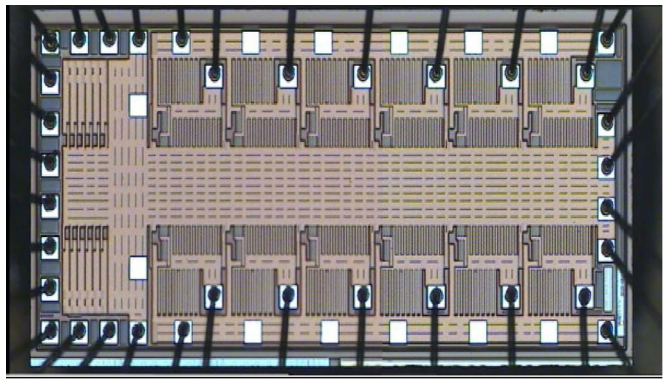


Fig. 8. Silicon dies of the chip.

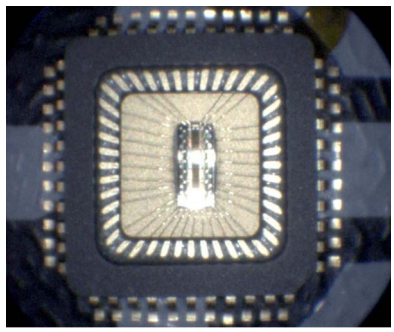
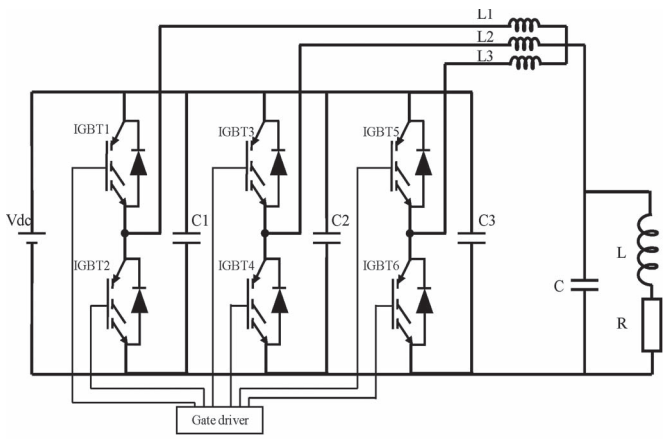


Fig. 9. Integrated gate driver on package CQFP-44 (11 mm × 11 mm).



Switching frequency: 38 kHz; α = 0.5;
Vdc=200V; C=68 µF; R=60 Ohm, L= 600 µH; IGBT: G4PH40UD 600V 9A
E= 20V ; Z1: zener 13V; Z2: zener 5.1 V; Rg=12 Ohm.

Fig. 10. Schematic of three-phase interleaved boost converter.

amplified gate signal outputs, 6 GND pads, and 4 VDD ($+E$) pads).

B. Implementation of the Integrated Gate Driver

We implemented this integrated gate driver to control a three-phase interleaved boost converter shown in Figs. 10 and 11; the parameters of the implemented circuit are also listed for comprehension. The input control signals for the gate driver are generated by a programmable Xilinx CPLD component. The HF pulse transformers were designed to carry a

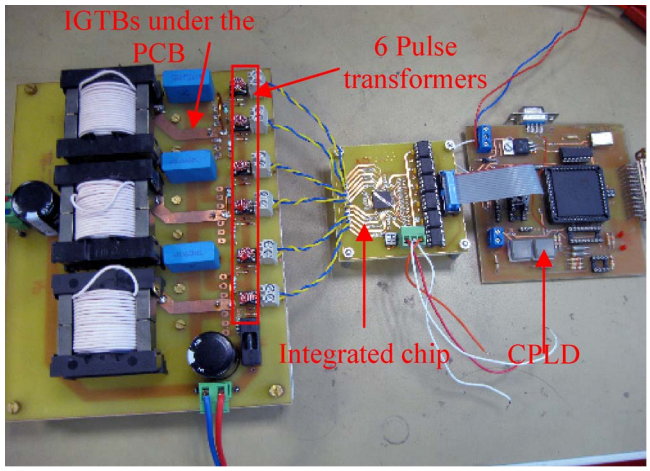


Fig. 11. Implemented circuit.

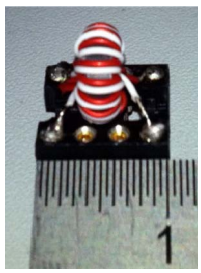


Fig. 12. HF pulse transformer (scale in centimeters).

maximum voltage–microsecond product of 20 V $\cdot$ μs; it is shown in Fig. 12.

It has to be mentioned that all six power devices are driven by the same gate driver circuits in order to provide also bipolar control signals to the bottom power devices and also in order to offer identical gate driver signal delays for all devices, particularly within each power inverter leg. Fig. 13(a)–(c) shows different voltage waveforms on the gate driver side of IGBT2, including the secondary-side voltage of the transformer Vs, voltages across the two Zener diodes V_{Z1} and V_{Z2}, and the gate–emitter voltage of IGBT2 V_{GE}.

In Fig. 13, the transformer secondary-side bipolar voltage level is $+/-19$ V, and it means that the voltage drop through the inverter transistors and the transformer is about 1 V. The pulsewidth applied at the primary side of the transformer is 600 ns in duration.

At the end of the power device turn-on state interval, the gate voltage has reached a maximum voltage level of

$$V_{\mathrm{GE\,max}} = \mathrm{Vs} - \mathrm{Vf}_{Z1} - \mathrm{VBR}_{Z2} = 19 - 0.7 - 5.1 = 13.2\ \mathrm{V}.$$

Then, the gate capacitance is discharged through the leakage current of Zener diode $Z1$.

After the power device turn-off time interval, the gate voltage has a minimum value of

$$V_{\mathrm{GE\,min}} = -\mathrm{Vs} + \mathrm{VBR}_{Z1} + \mathrm{Vf}_{Z2} = -19 + 13 + 0.7 = -5.3\ \mathrm{V}.$$

During OFF state, the gate voltage is maintained negative, and it decreases slightly through the leakage current of Zener diode $Z2$ and the pull-down resistor. The experimental results confirm the theoretical analysis presented previously. It can also be observed that the charge and discharge times are in the range of hundreds of nanoseconds, which is compliant with the design of the transformer.

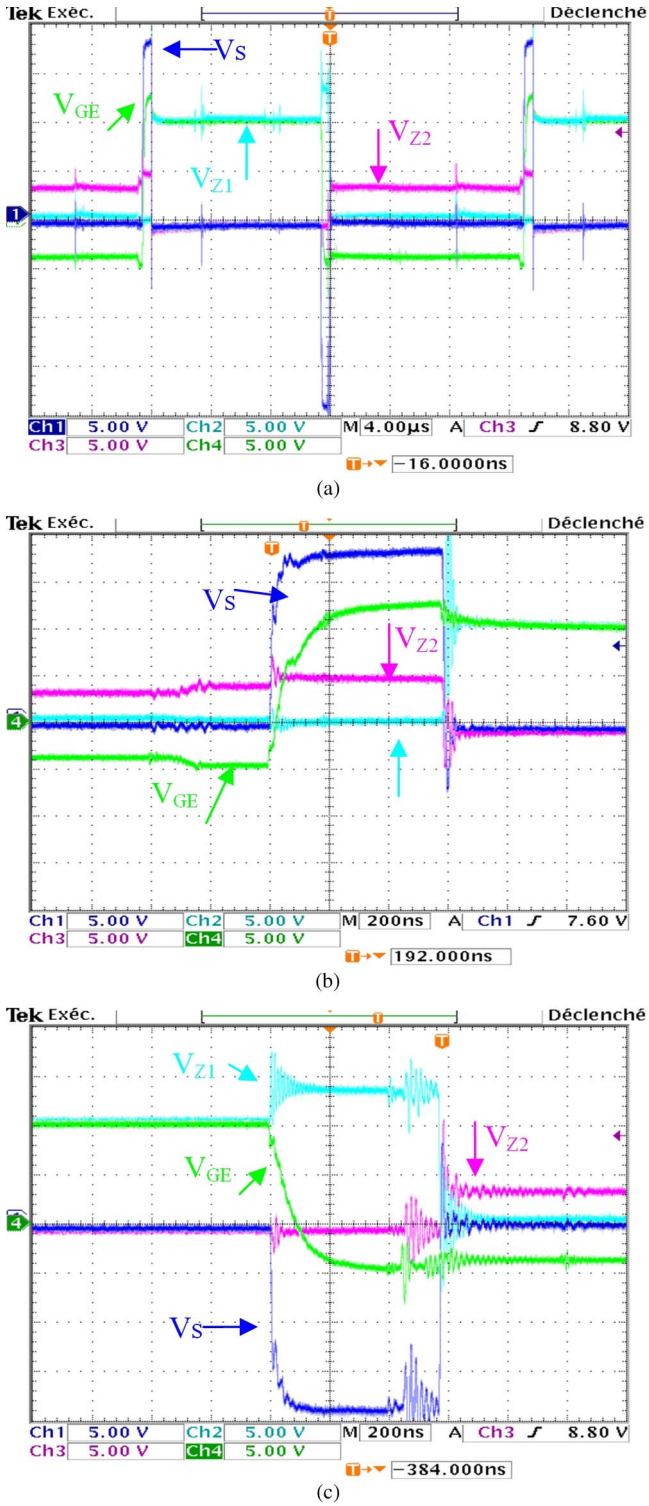


Fig. 13. Avalanche phenomenon of Zener diodes. (a) General case. (b) Avalanche of $Z2$. (c) Avalanche of $Z1$.

Fig. 14 shows the gate–emitter voltages of IGBT2, IGBT4, and IGBT6, which are uniform and phase shifted by 120°. The

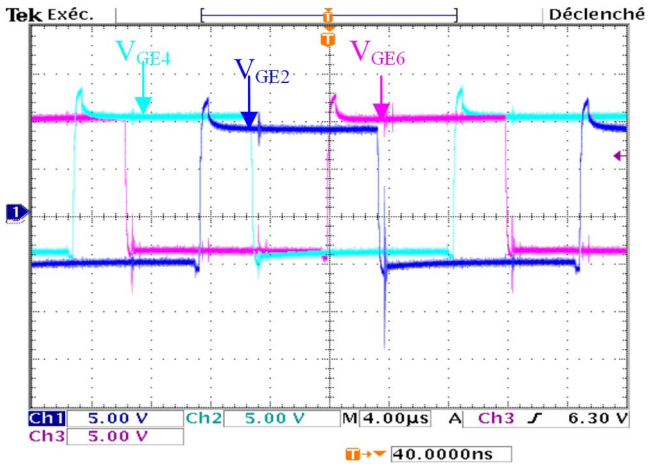


Fig. 14. Gate–emitter voltage waveforms for all converter low-side IGBTs.

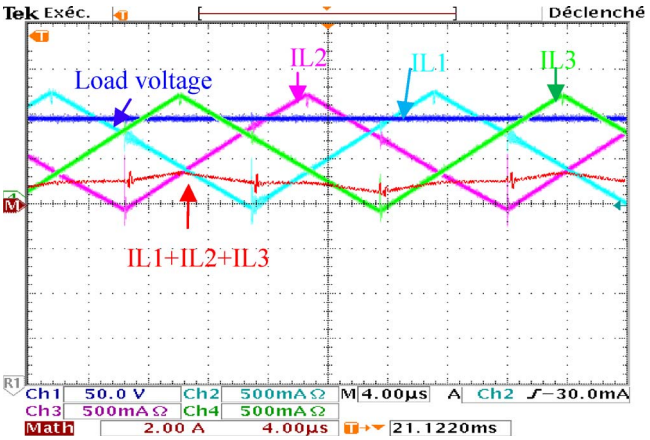


Fig. 15. Voltage and current loads.

TABLE II
PERFORMANCE COMPARISON

	Gate driver power consumption (W)	Converter efficiency (%)
Discrete driver	5.2	96
Integrated driver	0.93	98.6

dead time between the control signals for high- and low-side IGBTs was set at 400 ns in order to prevent any short-circuit current occurrence in each power phase. Fig. 15 shows the load voltage, the current in the three inductors, and the output current before the capacitive filter. The good operation of the converter fully validates the good operation of the gate driver units, particularly the CMOS integrated circuit. No parasitic behavior is visible on the gate driver signals.

In order to evaluate the performance of the integrated gate driver compared to the discrete circuit used before [13], we implemented two different drivers for the interleaved boost converter with the same parameters on the power side as is shown in Fig. 6. In the design of the discrete gate driver, we were not able to prevent the gate driver inverter CMOS short circuits without significant speed response reduction. The performance data are compared with respect to driver power consumption and global converter efficiency. As we can see in Table II, the integration of the gate driver permits reducing by five times the

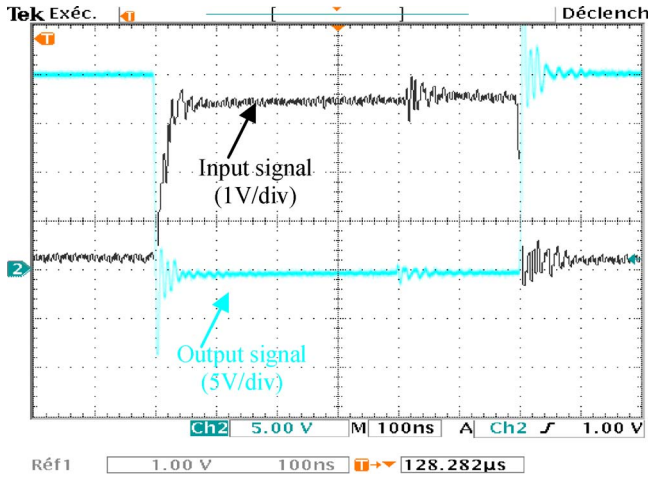


Fig. 16. Input and output signals of the integrated driver.

power consumption of the driver, and it increases the converter efficiency from 96% to 98.6%. In fact, the proposed topology and its integrated design improve the turn-on rise time and the turn-off fall time of the driver unit which is in charge of creating the input signals at the primary of the transformer. The measured values of these times were about 10 ns with the integrated circuit as we can see in Fig. 16, while they were about 120 ns with the discrete driver while removing possible gate driver short circuits. As a result, the integrated driver fulfills a higher switching speed, thus reducing the switching losses of IGBTs and increasing the converter efficiency.

Fig. 17 shows the thermal images of the integrated gate driver packaged and mounted on PCB under different operating switching frequencies. Even with poor heat exchange removal capabilities offered by the selected package, the integrated gate driver can operate at a maximum switching frequency of 600 kHz and 140 °C maximum temperature at its surface which covers many power converter applications in which several gate drivers are needed (the ambient is 20 °C).

The choice of the avalanche voltage of two Zener diodes and the CMOS inverter voltage supply affects the gate voltage levels and transients during the switching transitions and also during ON and OFF states. It is also important to point out that the avalanche voltages and leakage currents of the diodes are greatly dependent on temperature. It is mainly the leakage current dependence with respect to temperature that can affect the maximum ON-state time duration. The reverse leakage current is known to normally increase when the temperature is increased [27].

IV. CONCLUSION

We have presented and analyzed a new integrated gate driver for power switches implemented in multiphase applications. Design considerations have also been presented and detailed. The implementation of this driver on an interleaved boost converter has shown that it provides optimum driving waveforms with fast switching time and negative bias during OFF state. The integrated driver circuit is compact and simple to implement with very low power consumption and can also operate at high

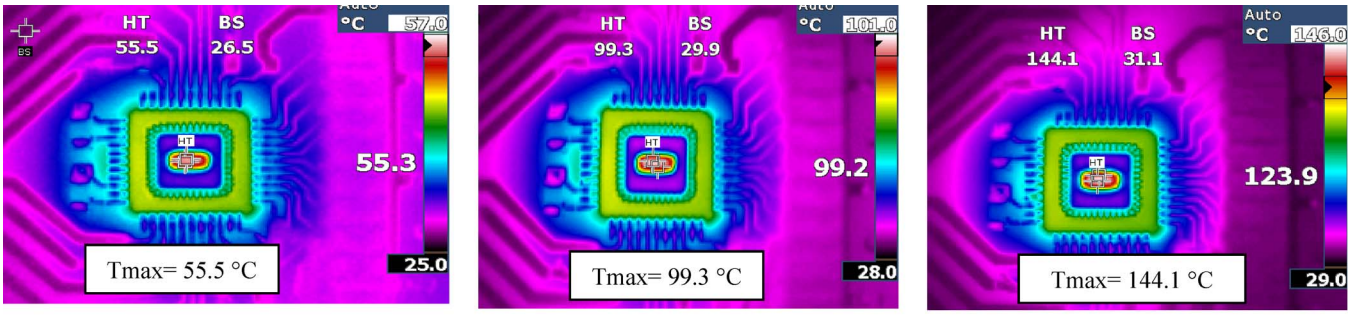


Fig. 17. Thermal image of the integrated chip under different frequencies.

switching frequencies. This generic and versatile gate driver could be used for any multitransistor application.

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The Van Nguyen was born in Namdinh, Vietnam, in 1985. He received the B.S. degree in electrical engineering from the Hanoi University of Technology, Hanoi, Vietnam, in 2008 and the M.S. degree in electrical engineering from the Grenoble Institute of Technology, Grenoble, France, in 2009. He is currently working toward the Ph.D. degree in integrated driver systems for power conversion structures in the Grenoble Electrical Engineering Laboratory, UMR 5529, Centre National de la Recherche Scientifique/Institut Polytechnique de Grenoble/Université Joseph Fourier, Grenoble.

His main research interests are in system and functional integration of gate drivers for power converters.

Jean-Christophe Crebier received the B.S. and M.S. degrees in electrical engineering in 1995 and the Ph.D. degree in power electronics and EMC for PFC converters in 1999, all from the Institut Polytechnique de Grenoble, Grenoble, France.

In 2000, he was a postdoctoral student with the Center for Power Electronics Systems, Virginia Polytechnic Institute and State University, Blacksburg, where he conducted research on system integration. Since 2001, he has been a full-time Researcher with the Grenoble Electrical Engineering Laboratory, UMR 5529, Centre National de la Recherche Scientifique/Institut Polytechnique de Grenoble/Université Joseph Fourier, Grenoble. His research fields are system and functional and hybrid and monolithic semiconductor integration for medium- to high-voltage power active devices. Applications of his work are related to the management of multicell distributed systems such as photovoltaics or batteries.

Pierre-Olivier Jeannin was born in 1973. He defended his Ph.D. dissertation in 2001 on series association of components.

He is an Associate Professor with the Université Joseph Fourier, Grenoble, France. Since 2001, he has been a permanent Researcher in the field of power electronics with the Grenoble Electrical Engineering Laboratory, UMR 5529, Centre National de la Recherche Scientifique/Institut Polytechnique de Grenoble/Université Joseph Fourier, Grenoble. His main research activities concern the packaging of power electronics components and the design of integrated power converters.