Summary

Our circuit and system design approach relies on the following key techniques:

1. Bio-inspired analog oversampling architecture based on an array of magnetite crystals and piezo cantilevers;
2. Investigating voltage-mode and charge-mode pre-amplifiers that fit the best with the developed MEMS array;
    a. Voltage mode will use multiple amplifiers to enhance signal-to-noise ratio;
    b. Charge mode will use pseudo-resistors for low-noise low-power signal amplification in millihertz-to-kilohertz range while rejecting large DC offsets generated due to the earth field;
3. Re-configurable summing and difference amplifier
    a. Enables both common mode (total field) and differential signal (gradient) detection;
    b. 3-op-amp topology in 180 nm SiGe process for low-noise and large dynamic range;
4. Dynamic element matching (DEM) and chopping techniques to conquer low-frequency noise and mismatches in electronic devices;

Detailed Technical Approach in Circuit/System Area

1. Bio-inspired analog oversampling architecture

Extremely sensitive magnetosome chains are membranous prokaryotic structures present in agnetotactic bacteria. They contain a number of magnetite crystals that together act like a compass needle to orient magnetotactic bacteria in geomagnetic fields. Magnetite-bearing magnetosomes have also been found in eukaryotic magnetotactic algae, with each cell containing several thousand crystals.

From circuits and systems point of view, this could be modeled using a very-large-scale oversampling sensing architecture. A simple example is laid out as follows:

Assuming a sensor of area A generates a signal of S, and it has intrinsic noise of N_i. In comparison, two sensors each with an area of $A/2$ would each generate a signal of $S/2$ and noise of $N_i/2$. When the two $A/2$ sensors are combined, their total signal will be S. But since the noises from the two $A/2$ sensors are uncorrelated, the combined total noise will be:

$$\sqrt{(N_i/2)^2+(N_i/2)^2}=N_i/\sqrt{2}$$

Therefore, splitting a sensor into two with equal sizes will result in a factor of $\sqrt{2}$ increase in the signal-to-noise ratio (SNR). Likewise, splitting a sensor into an array of M small units that sum up to the same total size would lead to a factor of $\sqrt{M}$ increase to the SNR. Because of this “oversampling gain” to the SNR, magnetosomes with thousands of magnetite crystals are able to have a superb sensitivity to small fluctuations of magnetic field, which can hardly be achieved by conventional man-made tools.

Ideally, if a sensor can be split into an infinite number of miniaturized elements, it would approach the capability of magnetosomes to achieve ultra-high field sensitivity. On the other hand, it is the most desirable to implement this bio-inspired oversampling mechanism in the analog front-end because any added back-end circuitry would introduce parasitics and noise that would otherwise hinder the effectiveness of the ideal oversampling theory.

Inspired by this bio-mechanism of oversampling, we propose to implement an array of magnetic material on top of piezo electric cantilevers, and use low-noise amplifiers to pick up signals directly from the elements. The low-noise amplifiers will be reconfigurable in summing and difference modes to detect total field and field gradient. An overview of the system is shown in Fig. 1.

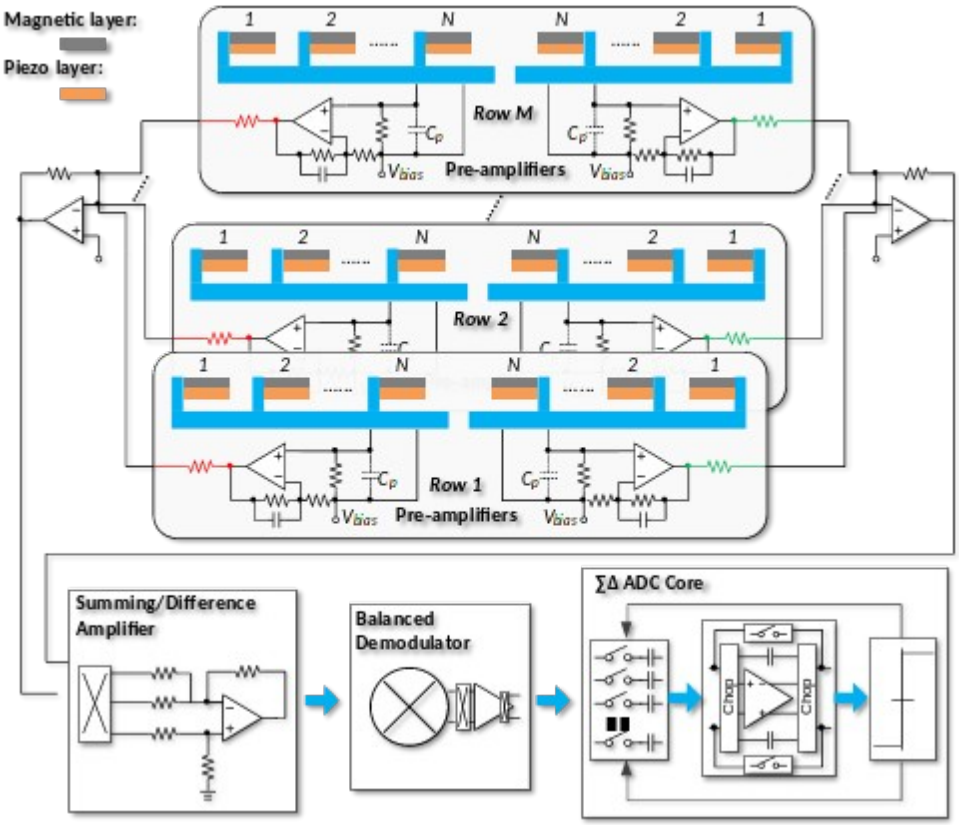

Figure. 1. An overview of the work to be performed.

2. Voltage-mode and charge-mode pre-amplifiers

Voltage-mode and charge-mode amplifications are two main approaches to signal conditioning of piezoelectric sensors. Voltage-mode amplification is useful when the amplifier is very close to the sensor and thus minimal parasitic capacitance is presented by the interconnection between the sensing device and the amplifier input. Charge-mode amplification is useful when the amplifier is remote to the sensor because it is robust against parasitic capacitance of interconnections. Depending on the characterization and optimization of the MEMS device front-end, the team is ready to investigate both approaches and fully integrate the final solution with special circuit techniques for the optimal performance.

a. Voltage-mode approach

The simplified structure for voltage-mode amplifiers is depicted in Fig. 1, represented by the circuits that directly interface with each row of the MEMS device. Depending on the fabricated and optimized MEMS size, either one or multiple amplifiers in parallel will be implemented for each row to collect the piezoelectric voltage signal. The goal of using multiple amplifiers in parallel is to enhance the SNR because of the benefit of oversampling. However, constraint exists due to the area available under the

MEMS device. The circuit team will work closely with the device team in this project to determine the ideal placement of local voltage-mode amplifiers in Phase I of this project, and compare the performance with the charge-mode approach discussed next.

b. Charge-mode approach

Charge-mode amplifier approach will also be investigated because it has advantages in handling interconnect parasitics and the convenience of adding signals from different rows of the MEMS device together. Inspired by existing works in neural recording [1], the team will use MOS-bipolar pseudo-resistors as the feedback resistors in the charge-mode amplifier. As shown in Fig. 2, two back-to-back connected PMOS transistors (T1 and T2) that can easily achieve resistance of GOhm will be implemented as the feedback resistor of the charge-mode amplifier, enabling processing brain signals with a frequency as low as 0.025 Hz. With negative V_{GS}, T1 and T2 function as diode-connected PMOS transistors. With positive V_{GS}, the parasitic source–well–drain p-n-p bipolar junction transistor (BJT) is activated, such that T1 and T2 act as diode-connected BJTs. For small voltages across the pseudo-resistors, the small-signal resistance is extremely high and thus moves the corner frequency to low enough for bio-signal processing. On the other hand, a large voltage across the pseudo-resistors will reduce the small-signal resistance and result in a fast settling time for the amplifier. As a result, this pseudo-resistor-based design can amplify low-frequency signals down to the millihertz range while properly rejecting large DC offsets. The theoretical noise–power tradeoff limit, i.e., the noise efficiency factor, have already been derived and demonstrated by selectively operating MOS transistors in either weak or strong inversion [1]. The only potential drawback of this configuration is that the amplifier cannot have a large output swing, because otherwise the pseudo-resistors may become two diodes. However, this is not a concern for this work as the amplifier is implemented as pre-amplifier in the front-end, where signal to be handled is very weak.

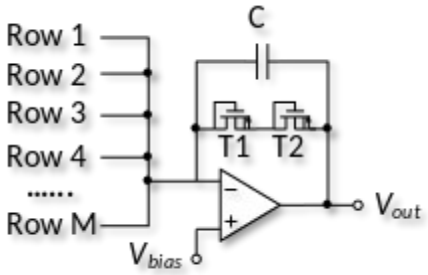

Figure 2. Charge-mode amplifier with pseudo-resistor feedback and summing capability.

3. Re-configurable summing and difference amplifiers

After the piezoelectric signal is captured by arrays of preamplifiers located near the MEMS devices, the obtained voltage signals will be further processed by a re-configurable summing and difference amplifier. This amplifier will be digitally controlled in real-time to either add or subtract signals coming from different regions of the fabricated device. This will enable both common-mode detection, which senses the total field, and differential-mode detection, which senses the field gradient.

One potential challenge for the summing and difference amplifier is the tradeoff between high sensitivity and large dynamic range. Being able to perform both summing and difference detection, as well as the existence of strong earth field, requires the amplifier to have a very large dynamic range. However, the

DARPA specification also mandate high sensitivity for brain signal recovery. To this end, a 3-op-amp topology will be customized and implemented in GlobalFoundries 180-nm SiGe BiCMOS 7WL process for both low-noise and high-linearity operation. Bipolar PNP transistors will be utilized as the input buffer to minimize the input-referred noise. A programmable resistor array will be implemented between the outputs of the two first-stage amplifiers to provide a large tunable gain range. In a previous DARPA project (MELD – Mind Electromagnetic Localization Device), the team has evaluated various topologies and different semiconductor processes (e.g., SOI versus BiCMOS) for the amplifier of brain magnetic field detector, and verified through both Cadence simulation and fabricated chip measurement that the 3-op-amp topology with bipolar transistor input buffer offers the best combined sensitivity and linearity performance.

4. Solution to low-frequency noise and device mismatch in electronics

Because the magnetic field induced by brain activities not only is extremely weak, but also has very low frequencies (below 100 Hz), 1/f noise and device mismatch have significant impact to the success of the proposed work. To resolve the challenge, the bio-inspired MEMS device will operate at a resonant frequency which “carries” the signal of interest. A double-balanced demodulator featuring low noise at the baseband output, high rejection to harmonic distortion, and low LO/RF leakage will be implemented after the summing/difference amplifier to recover the field information of interest.

After the signal is demodulated to the baseband, circuit techniques including dynamic offset cancellation, dynamic element matching (DEM), and chopping will be applied extensively to the remaining signal processing circuits to cancel the mismatch errors and low-frequency noises. On the data acquisition side, the analog-to-digital converter (ADC) is an important component for correctly interpreting the field information. Nyquist ADC accuracy is limited by the matching of components in ADCs, while oversampling ADCs, such as sigma-delta ADC, trade speed for resolution. Because brain signals have low frequencies, sigma-delta ADC is a very good candidate for precision sensing. Another advantage of sigma-delta ADC is that chopping technology and dynamic element matching are suitable for its architecture to minimize the impact of low-frequency noise and offset errors.

References

[1] R. R. Harrison, C. Charles, "A low-power low-noise CMOS amplifier for neural recording applications," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 6, pp. 958-965, June 2003.