ECEN 438/738 – Power Electronics Spring 2025

Lab 2: Linear Regulator with Feedback Control

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The goal of this lab is to investigate the properties and the response of the error amplifier, which generates the MOSFET gate driver voltage in linear regulators. First, we will review the architecture and the simplified equations describing an error amplifier in DC and AC operation. Next, we will use the simplified error amplifier model to predict its AC gain. Then, we will simulate the response of the error amplifier to the perturbations of the output voltage with respect to the desired nominal value, in a linear regulator. Finally, we will perform experimental tests with a real error amplifier, and will compare the results of simulations and measurements to verify their consistency.

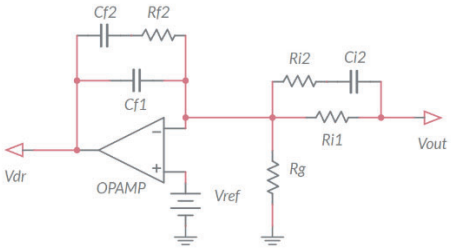

Figure 1-1. Error Amplifier.

Learning Objectives

After completing this lab, you should be able to complete the following activities.

1. Given a MOSFET operating as linear regulator, a load resistance, a DC source, a gate driver generator, and an error amplifier, you will calculate the magnitude of the error amplifier voltage determined by DC deviations and AC perturbations on the output voltage of the linear regulator, with specified units and decimal digits, by applying the appropriate theoretical formulae.
2. Given a MOSFET operating as linear regulator, a load resistance, a DC source, a gate driver generator, and an error amplifier, you will simulate the operation of the error amplifier to analyze the sensitivity of its voltage with respect to AC perturbations of the linear regulator output voltage, with specified units and decimal digits, to verify the consistency of theoretical predictions.
3. Given a real MOSFET operating as linear regulator, a DC power supply, a load resistor of given resistance, a function generator, and a real error amplifier, you will measure the DC and AC components of the error amplifier voltage determined by DC and AC perturbations of the linear regulator output voltage, with specified units and decimal digits, to verify the consistency of simulations and correct the model parameters.

Required Tools and Technology

Platform: NI ELVIS III Instruments used in this lab: ● Function generator ● Digital multimeter ● Oscilloscope ● Power Supply **Note**: The NI ELVIS III Cables and Accessories Kit (purchased separately) is required for using the instruments.	✓ Access Instruments https://measurementslive.ni.com/ ✓ View User Manual http://www.ni.com/en-us/support/model.ni-elvis-iii.html ✓ View Tutorials https://www.youtube.com/watch?v=TwvbRUpEpJU&list=PLvcPIuVaUMIWm8ziaSxv0gwtshBA2dh_M
Hardware: TI Power Electronics Board	✓ View User Manual http://www.ni.com/en-us/support/model.ti-power-electronics-board-for-ni-elvis-iii.html
Software: NI Multisim Live	✓ Access https://www.multisim.com/ ✓ View Tutorial https://www.multisim.com/get-started/
Software: TI Power Electronics Configuration Utility	✓ Download (Windows OS Only) http://download.ni.com/support/acadcw/PowerElectronics/TIPowerElectronicsBoardUtility-Windows.zip Note: Mac Version will be available soon

Expected Deliverables

In this lab, you will collect the following deliverables:

- ✓ Calculations based on equations provided in the Theory and Background Section
- ✓ Results of circuit simulations performed by means of Multisim Live
- ✓ Results of experiments performed by means of TI Power Electronics Board for NI ELVIS III
- ✓ Observations on simulations and experiments
- ✓ Answers to questions

Your instructor may expect you complete a lab report. Refer to your instructor for specific requirements or templates.

1 Theory and Background

1-1 Introduction.

In this section, we review the fundamental equations used to analyze the DC and AC response of an error amplifier. The error amplifier is a fundamental part of linear regulators, as it drives the MOSFET gate voltage and regulates the output voltage.

1-2 Error Amplifier Architecture and Function

Figure 1-2 shows a linear regulator under open loop operation. The *error amplifier* consists of an operational amplifier (OPAMP), a voltage reference V_{ref}, and a group of capacitors $\{C_{f1},C_{f2},C_{i2}\}$ and resistors $\{R_g,R_{i1},R_{i2},R_{f2}\}$. The function of the error amplifier is to sense the output voltage V_{out} and compare it to a desired DC nominal value $V_{outDC,nom}$, to generate a gate driver voltage V_{drEA} ensuring that V_{out} = $V_{outDC,nom}$. The capacitors $\{C_{f1},C_{f2},C_{i2}\}$ and the resistors $\{R_g,R_{i1},R_{i2},R_{f2}\}$ determine the sensitivity of the error amplifier to the output voltage perturbations, and its capability to reject the effects of noise or undesired signals on the linear regulator output voltage.

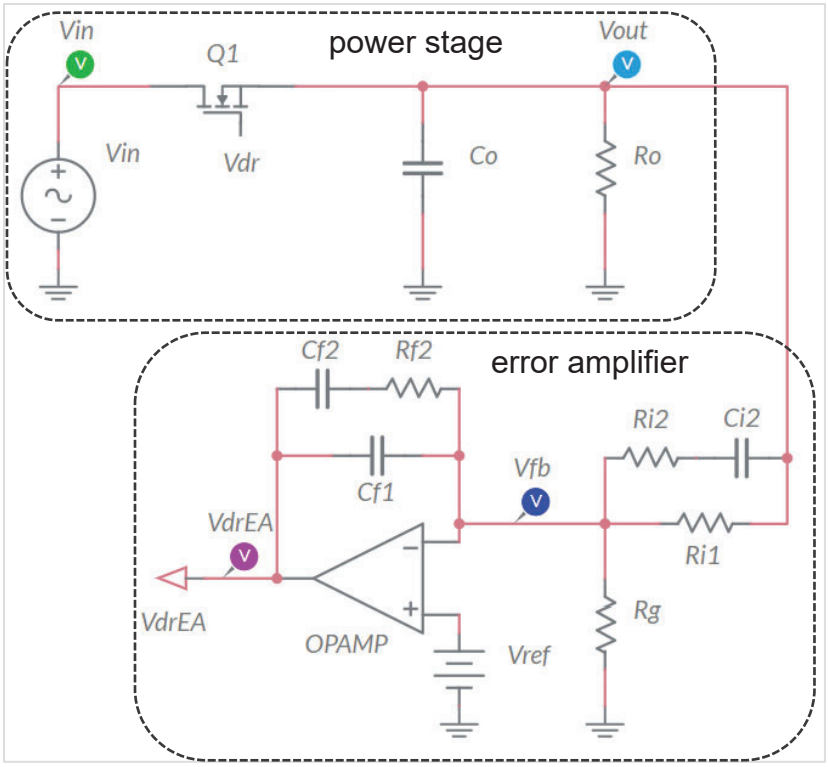

Figure 1-2. Error Amplifier in Open Loop Operation.

1-3 DC Analysis of the Error Amplifier

The MOSFET of the linear regulator shown in Figure 1-2 is driven by the generator V_{dr}. The DC output voltage V_{outDC} is determined by the DC source voltage V_{inDC} and by the DC gate driver voltage V_{drDC} (see **Lab1**). In DC steady-state operation, the capacitors C_{i2}, C_{f1} and C_{f2} are open, and the resistors R_g and R_{i1} form a *voltage divider sensor*, generating the feedback signal V_{fbDC}. If the OPAMP operates in its linear region, we have $V_{fbDC} \cong V_{ref}$, thus the DC output voltage fulfills Equation 1-1:

Equation 1-1

$$V_{outDC} = \left[1 + \frac{R_{i1}}{R_g}\right] V_{ref} = \frac{V_{ref}}{H}$$

where $H=R_g/(R_g+R_{i1})$. According to Equation 1-1, we can achieve a desired nominal DC output voltage $V_{outDC,nom} > V_{ref}$ with two resistances R_g and R_{i1} fulfilling Equation 1-2:

Equation 1-2

$$\frac{R_{i1}}{R_g} = \frac{V_{outDC,nom}}{V_{ref}} - 1$$

In DC operation, the error amplifier generates the MOSFET gate driver voltage $V_{drEA,DC}$ required to achieve the nominal value $V_{outDC,nom}$ (see **Lab1**):

Equation 1-3

$$V_{drDC,nom} = V_{th} + V_{outDC,nom} + \sqrt{\frac{2V_{outDC,nom}}{R_o \beta}}$$

If the DC output voltage deviates from the value $V_{outDC,nom}$, the error amplifier will generate a voltage given by

Equation 1-4

$$V_{drEA} = V_{drDC,nom} - G_{EA,DC}(V_{outDC} - V_{outDC,nom})$$

The coefficient $G_{EA,DC}$ is the error amplifier *open loop DC gain*. Based on Equation 1-4, if $V_{outDC} > V_{outDC,nom}$ the error amplifier decreases V_{drEA}, whereas if $V_{outDC} < V_{outDC,nom}$ the error amplifier increases V_{drEA}. We can achieve $V_{outDC} = V_{outDC,nom}$ only if $G_{EA,DC} = \infty$. In reality, $G_{EA,DC} = A_{dc}H$, where A_{dc} is the OPAMP DC open loop gain. An OPAMP with a higher DC open loop gain A_{dc} ensures a smaller steady-state error V_{outDC} - $V_{outDC,nom}$. The output voltage V_{dr} of the error amplifier is upper bounded by the OPAMP positive supply rail voltage V_{cc+}, and lower bounded by the negative supply rail voltage V_{cc-}. Therefore, Equation 1-4 is valid only if the OPAMP operates in the linear region, which happens when $V_{cc-} < A_{dc}H(V_{outDC,nom} - V_{outDC}) < V_{cc+}$.

1-4 AC Analysis of the Error Amplifier

An AC perturbation $V_{inAC}sin(2\pi fOt)$ injected on the source voltage generates an AC perturbation $V_{outAC}sin(2\pi fOt+\varphi)$ on the output voltage (see **Lab2**). The error amplifier

senses the output voltage AC perturbation and generates a signal $V_{drAC}sin(2\pi fOt+\theta)$. The amplitude V_{drAC} depends on the amplitude V_{outAC} and frequency f of the AC output voltage perturbation. The AC gain $G_{EA,AC} = V_{drAC}/V_{outAC}$ of the error amplifier is given by:

Equation 1-5

$$G_{EA,AC} = \frac{V_{drAC}}{V_{outAC}} = \begin{cases} \frac{f_0}{f}\frac{1+f^2/f_Z^2}{1+f^2/f_P^2} & f > f_{LPF} \\ A_{dc}H & f < f_{LPF} \end{cases}$$

where $f_{LPF} = f_0/A_{dc}$. The pole frequencies f_0, f_P and the zero frequency f_Z influence the sensitivity of the error amplifier with respect to output voltage AC perturbations, and impact the stability of the regulator. They are set by means of the capacitors $\{C_{f1},C_{f2},C_{i2}\}$, and the resistors $\{R_g,R_{i1},R_{i2},R_{f2}\}$. Equation 1-5 highlights that the parameters f_0, f_P and f_Z are not influential on the error amplifier sensitivity at very low frequency. Normally, $f_Z < f_P$, and Equation 1-5 can be simplified as follows:

Equation 1-6

$$\frac{V_{drAC}}{V_{outAC}} \cong \begin{cases} [f < f_{LPF}] & [f_{LPF} < f < f_Z] & [f_Z < f < f_P] & [f > f_P] \\ A_{dc}H & \frac{f_0}{f} & \frac{f_0 f}{f_Z^2} & \frac{f_0 f_P^2}{f_Z^2 f} \end{cases}$$

The frequency f_0 determines the sensitivity of the error amplifier. A higher f_0 expands the range of frequency where the error amplifier is more sensitive to the output voltage AC perturbations. For the error amplifier shown in Figure 1-1 (known as *Type III* error amplifier) $f_0 = 1/(R_{i1}(C_{f1}+C_{f2}))$. The sensitivity of the error amplifier decreases as the frequency f of the AC perturbation increases, except in the frequency range $[f_Z,f_P]$. The ratio f_P/f_Z is fixed based on *stability* requirements, and it is typically higher if f_0 is higher. The phase θ of the error amplifier output voltage $V_{drAC}sin(2\pi fOt+\theta)$ is correlated to the phase φ of the linear regulator output voltage $V_{outAC}sin(2\pi fOt+\varphi)$ by Equation 1-7:

Equation 1-7

$$\theta - \varphi = \begin{cases} -180° + 2\left[\arctan\left(f/f_Z\right) - \arctan\left(f/f_P\right)\right] - 90° & f > f_{LPF} \\ -180° & f < f_{LPF} \end{cases}$$

Based on Equations 1-5 and 1-7, if $f < f_{LPF}$ we have an *inverting error amplifier* with a very high gain, whereas if $f > f_{LPF}$ the gain decreases and the error amplifier voltage is expected to be delayed 270° with respect to the output voltage perturbation, except for $0.3f_Z<f<3f_P$.

Check Your Understanding

Note: The following questions are meant to help you self-assess your understanding so far. You can view the answer key for all "Check your Understanding" questions at the end of the lab.

1-1 What are the error amplifier parameters determining the nominal DC output voltage of a linear regulator?

A. the frequencies of zero and poles
B. the source voltage of the regulator
C. the reference voltage and the resistors of the voltage divider sensor

1-2 What parameter of the OPAMP determines the magnitude of the linear regulator output voltage DC error?

A. the DC open loop gain
B. the positive supply voltage
C. the low frequency pole

1-3 What is the amplitude of the error amplifier AC voltage correlated to the frequency of the linear regulator AC output voltage perturbations?

A. it is not correlated
B. it increases as the frequency increases
C. it decreases as the frequency increases

1-4 What parameter of the error amplifier majorly impacts its sensitivity with respect to the linear regulator AC output voltage perturbations?

A. the frequency of zero f_Z
B. the frequency of pole f_0
C. the reverence voltage V_{ref}

1-5 Based on your answer to Question 1-4, say what actions you would make to improve the sensitivity of the error amplifier:

_____

_____

_____

_____

2 Exercise

The error amplifier of the **Discrete Linear Section** in the TI Power Electronics Board for NI ELVIS III uses the TI's OPA835IDBVR OPAMP) and has the following nominal parameters (http://www.ti.com/lit/ds/symlink/opa835.pdf):

- $A_{dc}=10^6$, $V_{cc+}=5.5V$, $V_{cc-}=0V$.
- $R_g=26.1k\Omega$, $R_{i1}=39.2k\Omega$, $V_{ref}=1.024V$.
- f_0 = 3.28kHz, f_Z = 5.44kHz, f_P = 172.95kHz, f_{LPF} = 3.28mHz.

2-1 Given the parameters of the error amplifier, calculate the expected nominal value of the DC output voltage $V_{outDC,nom}$:

$V_{outDC,nom}$ = _____

2-2 What are the values of resistances R_g and R_{i1} required to achieve a nominal DC output voltage $V_{outDC,nom}$ = 3.3V?

Given $R_g=26.1k\Omega$, $R_{i1,nominal}$ = _____

Given $R_{i1}=39.2k\Omega$, $R_{g,nominal}$ = _____

2-3 You have an AC perturbation $V_{outAC}sin(2\pi fOt)$ on the output voltage of the linear regulator, which has an amplitude V_{outAC} = 10mV and frequency f listed in Table 2-1. Calculate the ratio V_{drAC}/V_{outAC} and the expected value of the amplitude V_{drAC}, in milli Volts with one decimal digit, of the AC voltage $V_{drAC}sin(2\pi fOt+\theta)$ generated by the error amplifier.

Table 1-1 Analysis of error amplifier voltage in AC operation.

f [Hz]	1	10	100	1000	10000	100000
V_{drAC}/V_{outAC}						
V_{drAC} [mV]						

2-4 Is the OPAMP able to generate all the V_{drAC} values you have collected in Table 2-1?

A. yes
B. no
if your answer is B, when? why?: _____

_____

_____

3 Simulate

The simulations you will perform in this section will allow you to analyze the open loop behavior of an error amplifier. First, you will observe the voltage generated by the error amplifier, under different conditions determined by the deviations of the linear regulator output voltage with respect to the desired nominal value. Then, you will compare the results of the simulations with the results of calculations performed in the **Exercise** section, to verify the consistency of theoretical calculations and simulations.

3.1 Simulation 1: Instructions

1. Open *Lab3 – Error Amplifier Operation* from the file path: https://www.multisim.com/content/QQ7QQ7drTxXe82G5zYttqc/lab-3-error-amplifier-operation/.
   The circuit is shown in Figure 3-1.

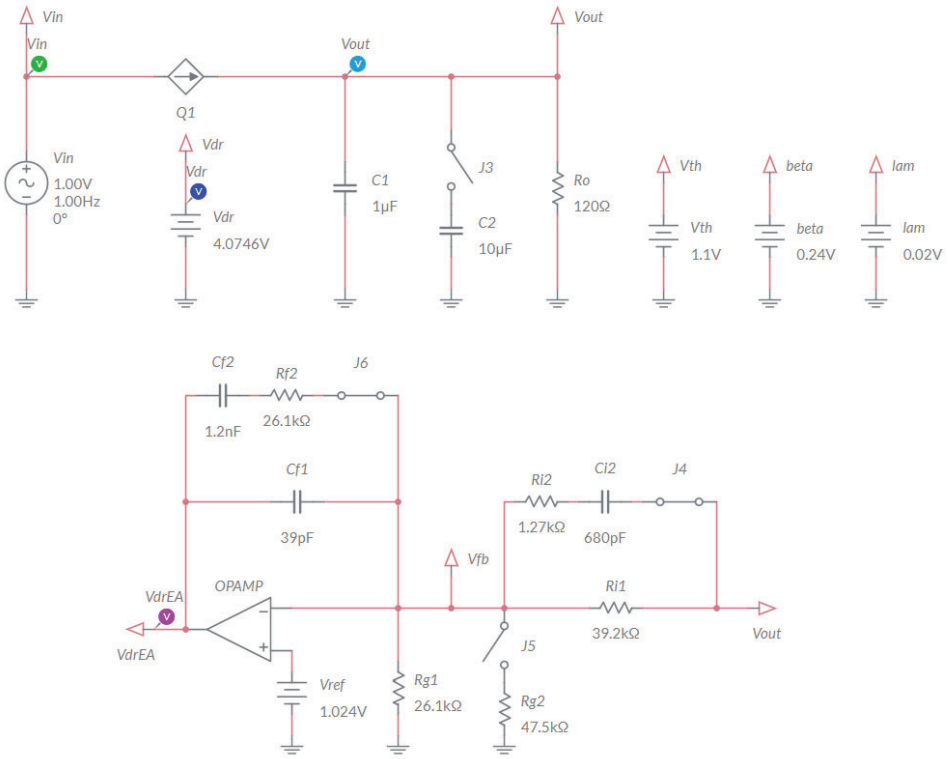

Figure 3-1. Multisim Live Circuit Schematic for the Analysis of Error Amplifier Operation.

In this simulation, you will observe the response of the error amplifier to deviations of the output voltage of the linear regulator with respect to the nominal value. For this purpose, the error amplifier voltage V_{drEA} is not used directly as gate driver voltage. The generator V_{dr} is used indeed to set the desired DC output voltage V_{outDC} (see

Lab1). Injecting an AC perturbation $V_{inAC}sin(2\pi fOt)$ on source voltage V_{in} generates an AC perturbation $V_{outAC}sin(2\pi fOt+\varphi)$ on the output voltage (see **Lab2**).The auxiliary generators *Vth*, *beta* and *lam* allow to set the MOSFET parameters {V_{th}, β, λ}, respectively. The parameters {*VA*, *Freq*, *VO*} of generators V_{in} and V_{dr} correspond to the parameters {V_{inAC}, *f*, V_{inDC}}, and {V_{drAC}, *f*, V_{drDC}}, respectively, as defined in the **Theory and Background** section. The capacitors {C_{f1},C_{f2},C_{i2}}, and the resistors {R_g,R_{i1},R_{i2},R_{f2}} are set so that the resulting error amplifier zero and poles are approximately f_0 = 3.28kHz, f_Z = 5.44kHz, f_P = 172.95kHz. The OPAMP parameters are A_{dc}=10^6, f_{OPAMP} = 30Hz, V_{cc+}=5.5V, V_{cc-}=0V.

2. Set the switches J3 and J5 to be OPEN, and the switches J4 and J6 to be CLOSED in the simulation schematic.
3. Select the *Interactive* simulation option and the *Split* visualization option.
4. Set the *Maximum Time Step* and *Maximum Initial Step* at 1e-6, in the *Simulation settings* menu;
5. Check the *Instantaneous* option box for voltage probes V_{in}, V_{out}, and V_{drEA} in the *Measurement labels* menu.
6. Calculate the nominal value $V_{outDC,nom}$ in Volts with three decimal digits, and report the result in Table 3-1.
7. Set *VA*=0, *Freq*=100Hz, *VO*=5V for the generator V_{in}, and *DC_mag* = 4.05V for the generator V_{dr}.
8. For each value of *DC_mag* of the DC voltage generator V_{dr} listed in Table 3-1, run the simulation, read the measurements of voltage probes V_{out} and V_{drEA} in Volts with three decimal digits and report the results in Table 3-1.

Table 3-1 Error Amplifier voltage as function of linear regulator output voltage V_{out}.

V_{drDC} (DC_mag) [V]	4.050	4.060	4.070	4.080	4.090	4.100
$V_{outDC,nom}$ [V]						
V_{outDC} [V]						
V_{outDC} - $V_{outDC,nom}$ [V]						
V_{drEA} [V]						

3-1-1 How does the error V_{outDC} - $V_{outDC,nom}$ vary as V_{dr} increases?

A. it increases
B. it decreases
other: _____

_____

3-1-2 How does the error amplifier voltage V_{drEA} vary as V_{dr} increases?

A. it increases
B. it decreases
other: _____

_____

3-1-3 Discuss the results of the error amplifier voltage V_{drEA}, based on the equations and relevant comments provided in the **Theory and Background** section:

_____

_____

_____

3-1-4 Set the values of the auxiliary generators *Vth* = 1.35, *beta* = 0.33 and *lam* = 0.05 in the circuit schematic, run the simulation and find the threshold value of V_{drDC} determining the transition of the error amplifier voltage V_{drEA} from V_{cc+} to V_{cc-}. Is this value greater or smaller than the threshold value of V_{drDC} from the Table 3-1?

A. greater
B. smaller
why?: _____

_____

3.2 Simulation 2: Instructions

1. Open *Lab3 – Error Amplifier Operation* from the file path:

https://www.multisim.com/content/QQ7QQ7drTxXe82G5zYttqc/lab-3-error-amplifier-operation/

2. Set the switches J3 and J5 OPEN, and the switches J4 and J6 to be CLOSED.
3. Select the *Interactive* simulation option and the *Split* visualization option.
4. Set the *Maximum Time Step* and *Maximum Initial Step* at 1e-6, in the *Simulation settings* menu;
5. Check the *Periodic* option box for voltage probes V_{in}, V_{out}, and V_{drEA} in the *Measurement labels* menu.
6. Set *VA*=1V, *Freq*=1Hz, *VO*=5V for the generator V_{in}, and *DC_mag* = 4.0746V for the generator V_{dr} and run the simulation.
7. Read the DC average measurement V_{AV} and the AC peak-to-peak measurement V_{pp} of V_{out} voltage probe and report the values of V_{outDC} = V_{AV} (in Volts with three decimal digits) and V_{outAC} (in milli Volts with three decimal digits) in Table 3-2
8. Read the DC average measurement V_{AV} and the AC peak-to-peak measurement V_{pp} of V_{drEA} voltage probe and report the values of $V_{drEA,DC}$ = V_{AV} (in Volts with three decimal digits) and $V_{drEA,AC}$ (in milli Volts with three decimal digits) in Table 3-2
9. Repeat steps 7-8 under V_{in} frequency and amplitude listed in Table 3-2.
10. Import in Table 3-2 the values of V_{drAC}/V_{outAC} recorded in Table 2-1 of **Exercise** section, for the corresponding frequencies.

Table 3-2 Error Amplifier response with C_o=1μF.

f [Hz] (V_{in} Freq)	1	10	100	1000	10000	100000
V_{inAC} [V] (V_{in} VA)	0.5	1	1	1	1	1
V_{drDC} [V] (V_{dr} DC_mag)	4.0746					
ML Simulation Max. Time Step	1e-5	1e-5	1e-5	1e-6	1e-7	1e-8
ML Grapher Horizontal Axis	500ms/div	50ms/div	5ms/div	500us/div	50us/div	5us/div
$V_{outDC,nom}$ [V]						
V_{outDC} [V]						
V_{outAC} [mV]						
$V_{drEA,DC}$ [V]						
$V_{drEA,AC}$ [mV]						
$V_{drEA,AC}/V_{outAC}$						
V_{drAC}/V_{outAC} from Table 2-1						

3-2-1 Do the values of $V_{drEA,AC}$ obtained with simulations show the same trend of V_{drAC} results obtained with calculations?

A. yes
B. no

if your answer is B, highlight and discuss the differences: _____

_____

_____

3-2-2 How does the ratio V_{drAC}/V_{outAC} vary with the frequency?

A. it increases
B. it decreases
C. other

if your answer is C, describe and discuss what you observe: _____

_____

_____

3-2-3 Should the error amplifier exhibit a different ratio V_{drAC}/V_{outAC} if the MOSFET parameters V_{th}, β and λ are changed?

A. yes
B. no

why?: _____

_____

If you are not able to answer Question 3-2-3, change the value of the generators *Vth*, *lam* and *beta* in the circuit schematic and run the simulation. Analyze the results, read the **Theory and Background** section and then answer the question.

Troubleshooting tips:

- If the simulation does not run and you get some error message, reload *Lab3 – Error Amplifier Operation* from this file path: https://www.multisim.com/content/QQ7QQ7drTxXe82G5zYttqc/lab-3-error-amplifier-operation/ and restart the simulation, following the instructions.

4 Implement

The experiments of this section allow you to observe the behavior of a real error amplifier, and to verify the response of the error amplifier to DC and AC deviations of the output voltage of a linear regulator with respect to the desired nominal value. You will compare the experimental measurements with simulations, to verify their consistency and determine possible adjustments of MOSFET model parameters to improve the accuracy of simulations. The experiments are performed by means of the **Discrete Linear Section** of the TI Power Electronics Board for NI ELVIS III shown in Figure 4-1, which uses the TI's CSD15380F3 MOSFET (pass device) and OPA835IDBVR OPAMP (error amplifier). The linear regulator is powered by a TI's TPS40303DRCR Integrated Buck regulator, generating a 5V DC voltage. The AC disturbance on the output voltage of the Discrete Linear regulator is generated by applying an AC signal to the linear regulator gate driver voltage. The error amplifier pole frequency f_0 is 3.3kHz when jumpers J60 and J62 are shorted, and 104kHz when jumpers J60 and J62 are open. The output capacitance C_o is 1µF with jumper J59 open, and 11µF with jumper J59 shorted. The nominal output voltage of the linear regulator is set at 2.5V with jumper J61 open, and at 3.3V with jumper J61 shorted.

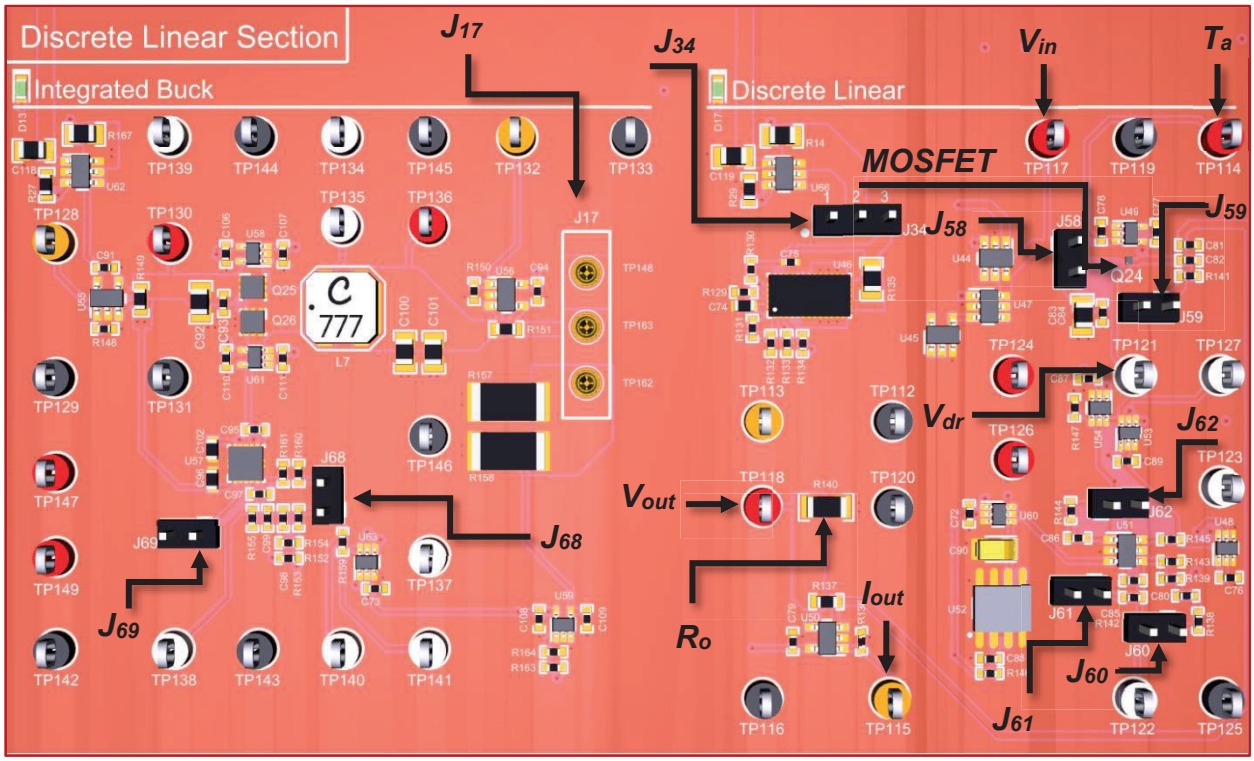

Figure 4-1. TI Power Electronics Board for NI ELVIS III - Discrete Linear Section Used for the Analysis of Error Amplifier Operation

TI's devices datasheets are available at the following links:

CSD15380F3 MOSFET: http://www.ti.com/lit/ds/symlink/csd15380f3.pdf
OPA835IDBVR OPAMP: http://www.ti.com/lit/ds/symlink/opa835.pdf
TPS40303DRCR Buck Regulator: http://www.ti.com/lit/ds/symlink/tps40303.pdf

[**Note:** the parameters provided in the following instructions for instruments setup may require some adjustment due to thermal effects and tolerances of TI Power Electronics Board components]

4-1 General Instructions

1. Open *Power Supply*, *Function Generator* and *Oscilloscope* using Measurements Live. For help on launching instruments, refer to this help document: http://www.ni.com/documentation/en/ni-elvis-iii/latest/getting-started/launching-soft-front-panels/
2. Open the *User Manual* of TI Power Electronics Board for NI ELVIS III from this file path: http://www.ni.com/en-us/support/model.ti-power-electronics-board-for-ni-elvis-iii.html
3. Read the *User Manual* sections *Description*, *Warnings* and *Recommendations* regarding *Discrete Linear Section*.
4. Open the *TI Top Board RT Configuration Utility* of TI Power Electronics Board for NI ELVIS III (See Required Tools and Technology section for download instructions), and select *Lab3 – Error Amplifier Operation*.
5. Configure the jumpers of the board as indicated in Table 4-1.
6. Connect the instruments as indicated in Table 4-2.

Table 4-1 Jumpers setup

J17	J34	J58	J59	J60	J61	J62	J68	J69
short TP148-TP163	short 2-3	open	open	short	open	short	short	open

Table 4-2 Instruments connections

Power Supply	connect to red and black banana connectors
Oscilloscope	connect CH-1 to TP117 (input voltage V_{in}) connect CH-2 to TP118 (output voltage V_{out}) connect CH-3 to TP121 (gate driver voltage V_{dr}) connect CH-4 to TP123 (error amplifier voltage V_{drEA})
Function Generator	connect Ch-2 to FGEN2 BNC connector (→TP121 = gate driver voltage V_{dr})

4-2 Experiment 1: Instructions

1. Use the instruments configuration and setup shown in Table 4-2-1.
2. Run *Power Supply*, *Function Generator* and *Oscilloscope*.

Table 4-2-1 Instruments initial configuration and setup

<table>
<tr><td>Power Supply</td><td colspan="5">CH "+": Static, 7.00V, CH "-": Inactive</td></tr>
<tr><td rowspan="2">Oscilloscope</td><td>Trigger:
Immediate</td><td>Horizontal:
100us/div</td><td>Acquisition:
average</td><td>Measurements:
show</td><td>Probe Attenuation:
10x</td></tr>
<tr><td colspan="2">CH-1: ON
• DC coupling
• 2V/div
• offset 0V</td><td>CH-2: ON
• DC coupling
• 20mV/div
• offset -2.55V</td><td>CH-3: ON
• DC coupling
• 20mV/div
• offset -4.35V</td><td>CH-4: ON
• DC coupling
• 2V/div
• offset 0V</td></tr>
<tr><td>Function Generator</td><td colspan="5">CH-1: Inactive
CH-2: Sine, DC offset 3.9V, Amplitude 0mV, Frequency 1kHz</td></tr>
</table>

3. Using horizontal cursors in Manual mode, read the average DC values of the *Oscilloscope* CH-2 (V_{out}), CH-3 (V_{dr}) and CH-4 (V_{drEA}), in Volts with all decimal digits shown by the instrument, and report the values in Table 4-2-2.

Table 4-2-2 Error Amplifier voltage as function of linear regulator output voltage V_{out}.

V_{drDC} [V] (Function Generator CH2 DC offset)	3.90	4.00	4.10	4.20	4.30	4.40
$V_{outDC,nom}$ [V]						
V_{dr} [V]						
V_{out} [V]						
V_{drEA} [V]						

4. Repeat the measurement for all the values of the driver voltage V_{drDC} indicated in Table 4-2-2, by changing the DC offset of *Function Generator* CH-2.
5. Stop *Oscilloscope*, *Function Generator* and *Power Supply*.

4-2-1 Do you observe a transition in the measured values of V_{drEA} from V_{cc+} to V_{cc-} like the one you have observed with the simulations?

A. yes
B. no
what is you comment? _____

_____

4-2-2 If your answer to Question 4-2-1 is A, does the threshold value of the gate driver voltage V_{dr} determine the transition of V_{drEA} of V_{drEA} from V_{cc+} to V_{cc-} the same you have observed with the simulations?

A. yes
B. no
what is you comment? _____

_____

4-2-3 Based on your answer to Question 4-2-2, what parameter of the MOSFET model would you change to improve the accuracy of simulations? How and why?

A. V_{th}: _____

B. β: _____

C. λ: _____

4-2-4 Run again the simulation by changing the parameters of MOSFET model and verify your predictions based on your answers to Question 4-2-3. Are the new simulation results closer to experimental ones? Do you infer a rule or a procedure to obtain the parameters of a MOSFET from experimental measurements?

_____

_____

_____

_____

4-3 Experiment 2: Instructions

1. Open *Power Supply*, *Function Generator* and *Oscilloscope* and use the instruments configuration and setup shown in Table 4-3-1.
2. Run *Power Supply*, *Function Generator* and *Oscilloscope*.

Table 4-3-1 Instruments initial configuration and setup

Power Supply	*CH "+"*: Static, 7.00V, *CH "-"*: Inactive				
Oscilloscope	*Trigger*: Immediate	*Horizontal*: 200ms/div	*Acquisition*: average	*Measurements*: show	*Probe Attenuation*: 10x
	CH-1: ON • DC coupling • 1V/div • offset -4V	*CH-2*: ON • DC coupling • 10mV/div • offset -2.55V	*CH-3*: ON • DC coupling • 10mV/div • offset -4.175V	*CH-4*: ON • DC coupling • 1V/div • offset -3.5V	
Function Generator	*CH-1*: Inactive *CH-2*: Sine, DC offset 4.175V, Amplitude 20mV, Frequency 1Hz				

3. Using horizontal cursors in Manual mode, read the DC average values of the *Oscilloscope* CH-2 (V_{out}), CH-3 (V_{dr}) and CH-4 (V_{drEA}), in Volts with all decimal digits shown by the instrument, and report the values in Table 4-3-2.
4. Using cursors in Track mode, read the peak-peak values of the *Oscilloscope* CH-2 (V_{out}), CH-3 (V_{dr}) and CH-4 (V_{drEA}), in Volts with all decimal digits shown by the instrument, calculate the ratio $V_{drEA,AC}/V_{outAC}$, and report the values in Table 4-3-2.

Table 4-3-2 Error Amplifier response.

f [Hz] (FG CH-2 Frequency)	1	10	100	1000	10000	100000
suggested oscilloscope time/division	200ms/div	20ms/div	2ms/div	200µs/div	20µs/div	2µs/div
suggested oscilloscope CH-4 volt/division	1V/div	1V/div	100mV/div	10mV/div	10mV/div	10mV/div
suggested oscilloscope CH-4 offset	-3.5V	-3.5V	-5.54V	-5.54V	-5.54V	-5.54V
V_{drDC} [V] (FG CH-2 DC offset)	4.175	4.182	4.182	4.182	4.175	4.175
V_{drACpp} [mV] (FG CH-2 Amplitude)	20	20	20	20	20	20
V_{drACpp} [mV] (Scope CH-3 Volts pk-pk)						
$V_{outDC,nom}$ [V]						
V_{outDC} [V] (Scope CH-2 Average)						
$V_{outACpp}$ [mV] (Scope CH-2 Volts pk-pk)						
$V_{drEA,DC}$ [V] (Scope CH-4 Average)						
$V_{drEA,ACpp}$ [mV] (Scope CH-4 Volts pk-pk)						
$V_{drEA,ACpp}/V_{outACpp}$						
V_{drAC}/V_{outAC} from Table 3-2 (simulations)						

5. Repeat the measurement for all the values of Frequency, DC Offset and Amplitude of the driver voltage V_{dr} shown in Table 4-3-2, by changing the setup of *Function Generator* CH-2. [**Notes: 1)** if you don't see the CH-4 trace in the scope frame, decrease the DC offset V_{drDC}, with respect to the values shown in Table 4-3-2, in

steps of -1mV, until the CH-4 sets in the frame; **2)** while measuring peak-peak voltage values, do not consider the high-frequency noise appearing as a rapid up-and-down swinging signal around the main sinusoidal waveform].

6. Enter in Table 4-3-2 the V_{drAC}/V_{outAC} values collected in Table 3-2.
7. Stop *Oscilloscope*, *Function Generator* and *Power Supply*.

4-3-1 Do you observe the same trend in the measured and simulated ratio V_{outAC}/V_{inAC} as the frequency increases?

A. yes
B. no
if your answer is B, why? _____

_____

4-3-2 Should the error amplifier exhibit a different ratio V_{drAC}/V_{outAC} with C_o = 11μF?

A. yes
B. no
why?: _____

_____

_____

Troubleshooting tips:

- If the simulated and measured results do not match, verify the setup and connections of instruments, and restart the experiment.

5 Analyze

5-1 Using the results collected in Table 4-3-2, calculate the ratios $G_{dr} = V_{outAC}/V_{drAC}$, $G_{EA} = V_{drEA,AC}/V_{outAC}$ and $T_{loop} = G_{EA}G_{dr} = V_{drEA,AC}/V_{drAC}$, report the results in Table 5-1, and graph the values of ratios G_{dr}, G_{EA} and T_{loop} as a function of the frequency f using a logarithmic scale for the horizontal axis and decibel scale for the vertical axis, including a legend that indicates which line style corresponds to which series (calculations, measurements).

Table 5-1 Error Amplifier response.

f [Hz]	1	10	100	1000	10000	100000
$G_{dr} = V_{outAC}/V_{drAC}$						
$G_{EA} = V_{drEA,AC}/V_{outAC}$						
$T_{loop} = V_{drEA,AC}/V_{drAC}$						

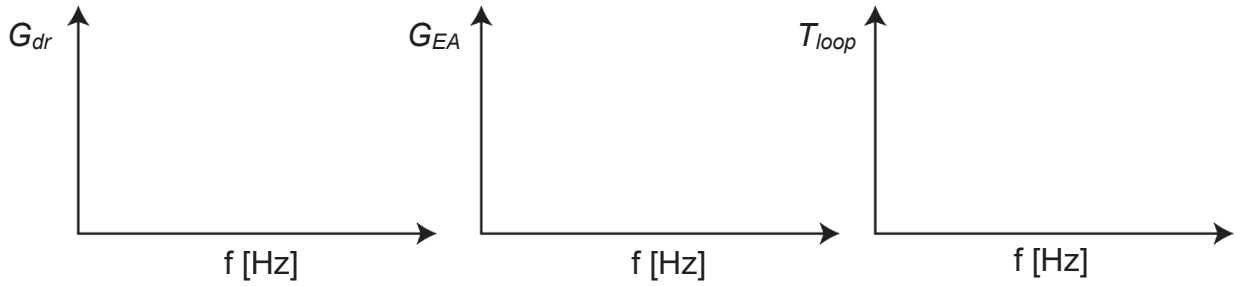

Figure 5-1 Calculated and measured values of ratios V_{outAC}/V_{inAC} and V_{outAC}/V_{drAC} obtained while varying the frequency, with the MOSFET operating in the saturation region

The ratio G_{dr} is the open loop *control-to-output* gain of the linear regulator, which expresses the sensitivity of the output voltage with respect to the gate driver voltage perturbations (see **Lab2**). The ratio G_{EA} is the gain of the error amplifier, which expresses the sensitivity of the error amplifier voltage with respect to the output voltage perturbations (see **Theory and Background** section). The ratio T_{loop} is the loop gain of the linear regulator, which expresses the global sensitivity of the linear regulator to AC perturbations. A higher value of the loop gain involves a higher reactivity of the linear regulator to disturbances, which results in a more effective suppression of the disturbances and in a better output voltage regulation capability.

5-2 Based on the loop gain plot T_{loop} you have plotted in Figure 5-1, for what of the frequency values is the linear regulator better suppressing the disturbance effects?

A. 60Hz
B. 6kHz

C. 60kHz

5-3 Based on your observations and on the equations provided in the **Theory and Background** section, how would you modify the parameters f_0, f_Z, f_P and A_{dc} of the error amplifier to improve the disturbance suppression capability of the linear regulator?

_____

_____

_____

6 Conclusion

6-1 Summary

Write a summary of what you observed and learned about the AC response of the error amplifier of a linear regulator, regarding its sensitivity with respect to output voltage AC perturbations. Discuss the parameters influencing the AC response of the error amplifier, in what frequency range is it important to have a high error amplifier gain, why, and how you can achieve it.

6-2 Expansion Activities

6-2-1. Using the Multisim Live schematic of Figure 3-1, determine the frequency response of the linear regulator and of the error amplifier, by means of the *AC Sweep* option:

a. Set the switches J4 and J6 to be closed.
b. Replace the V_{dr} DC generator with an AC generator and set VO=4.0746V, Freq=1Hz, VA=0.1V.
c. Set AC_mag = 0.1V in the *AC analysis value* menu option of the voltage generator V_{dr}.
d. Set AC_mag = 0 V in the *AC analysis value* menu option of the voltage generator V_{in}.
e. Set Start freq. = 1Hz and Stop freq. = 1MHz in the *Configuration Panel*.
f. Set *Show plots* box unchecked on probe V_{in}.
g. Run the simulation and watch the resulting AC Sweep plots (Bode plots). The continuous lines are the magnitudes of the ratios $G_{dr} = V_{outAC}/V_{drAC}$, $T_{loop} = G_{EA}G_{dr} = V_{drEA,AC}/V_{drAC}$, while the dashed line is the phase shift between V_{outAC} and $V_{drEA,AC}$ with respect to V_{drAC} over the selected frequency range.
h. Verify that the plots follow the trend of results of Tables 3-2, 4-3-2 and 5-1.

6-2-2. Observe the behavior of an error amplifier with a higher gain, using the circuit schematic of Figure 3-1.

a. Open the switches J4 and J6. The resulting gain of the error amplifier will be:

Equation 6-2-1

$$G_{EA} = \frac{V_{drAC}}{V_{outAC}} = \begin{cases} \frac{f_0}{f} & f > f_{LPF} \\ A_{dc}H & f < f_{LPF} \end{cases}$$

The pole frequency f_0 of the error amplifier is now given by $f_0 = 1/(R_{i1}C_{f1})$ = 104kHz (*Type I* error amplifier), and consequently f_{LPF} = 10.4Hz.

b. Open switches J4 and J6.
c. Repeat the simulations in the test conditions listed in Table 3-2 (use *VA*=100mV with *Freq* = 1Hz, 10Hz, 100Hz, for generator V_{in}).
d. Compare and discuss the results of simulations obtained with the two different error amplifier setup.

6-2-1. Verify experimentally the effect of a higher error amplifier gain

a. Open the jumpers J60 and J62 in the **Discrete Linear Section** of TI Power Electronics Board for NI ELVIS III shown in Figure 4-1.
b. Test the regulator with Frequency = 10kHz, Amplitude = 30mVpp and DC offset = 4.328V on *Function Generator* CH-2, set the *Oscilloscope* CH-4 with AC coupling, 500mV/div, 0V offset, 50us/div.
c. Compare the error amplifier gain with the corresponding result reported in Table 4-3-2.

6-3 Resources for learning more

- This book provides the fundamentals of linear regulators control:
  C.Basso, *Designing Control Loops for Linear and Switching Power Supplies: A Tutorial Guide*, Artech House