Pre-Lab #2

#1) Truth Table

Input bits				Output bits		
S	I	H	C	P_2	P_1	P_0
0	0	0	0	0	0	0
0	0	0	1	1	0	0
0	0	1	0	0	1	1
0	0	1	1	1	1	1
0	1	0	0	0	0	1
0	1	0	1	0	1	1
0	1	1	0	0	1	1
0	1	1	1	X	X	X
1	0	0	0	0	1	0
1	0	0	1	1	1	1
1	0	1	0	1	0	1
1	0	1	1	X	X	X
1	1	0	0	1	1	1
1	1	0	1	X	X	X
1	1	1	0	X	X	X
1	1	1	1	X	X	X

#2) K-maPS

P_0:

CH \ SI	00	01	11	10
00		1	1	
01	1	1	X	1
11	1	X	X	X
10		1	X	1

P_1:

CH \ SI	00	01	11	10
00			1	1
01	1	1	X	
11	1	X	X	X
10		1	X	1

$P_0 = I + H + CS$

$P_1 = HS' + CI + H'S$

P_2:

CH \ SI	00	01	11	10
00				
01			X	1
11	1	X	X	X
10	1		X	1

$P_2 = CI' + HS$

#3) Minimized Expression

$P_0 = I + H + CS$

$P_1 = HS' + CI + H'S$

$P_2 = CI' + HS$

4.) Schematic / Gate