

ECEN 248 - Lab Report

Laboratory Exercise #3

Rudimentary Adder Circuits

ECEN-248-509

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Objectives:

The purpose of this lab is to introduce students to the design of simple combinational adder circuits. In the lab, students will breadboard and test the adder circuits as well as introduce students to simple arithmetic logic. Also, we will be using Karnaugh Maps.

Design:

Experiment Part 1:

This lab will be separated into three sections, the first being a half-adder design. I had to learn and understand the concept and logic behind a half-adder. After bread-boarding the first part of the experiment, we moved on to using the half adder's logic expression to create the lab's second part. To minimize the number of gates used in the circuit to reduce delay, I incorporated an XOR gate for the “S” output and an AND gate for the “Cout” in the integrated circuit.

Experiment Part 2:

I placed all needed gates on the breadboard and proceeded to put VCC and GND to all gates as well as the power to the breadboard. Since the breadboard only supplies power to certain areas, I used jumper wires to move VCC and GND to the parts that were needed. I moved on to setting my inputs which were only three for the full adder. Following the logic expression and the circuit, The main difference between the half adder and full adder was that one extra input was required named “Cin.” The full adder required an OR gate, which the half adder did not. I had drawn, I placed wires to each gate from the inputs accordingly and set my outputs as “Cout” and “S.” After the circuit was wired and debugging was complete, I checked my combinations of inputs with the results of the outputs with the truth table.

Experiment Part 3:

For the third part of the experiment, two full adders were required to make a Ripple Carry Address. To accomplish this, I took the approach of just rebuilding another full adder circuit right next to the one I had already completed, I added a_1 , b_1 , c_1 , inputs for the second full adder, and instead of having a “Cout” from the first adder it was the input for the second full adder, meaning there was a total of 5 inputs and a total of 3 outputs. After completing the breadboarded circuit and debugging it, I created a truth table and checked it with Sri to be completely correct. This concluded my experiment.

Results:

The results of my experiment showed that the half adder, full adder, and Ripple Carry Address followed any combinations of input values on the truth table to light up the correct corresponding output values. After testing several different inputs and checking with the output truth table, all combinations were correct and they were observed by my TA, Sri.

Conclusion:

The result of completing the pre-lab and conducting this experiment gave me the ability to understand the concept behind half adders, full adders, and Ripple Carry Address by using logic expressions to wire these on a breadboard. The experiment further showed me about creating truth tables and utilizing Karnaugh Maps to further simplify circuits to minimize the number of gates used in the circuit to prevent complex log expressions and propagation delay.

Post-lab Deliverables:

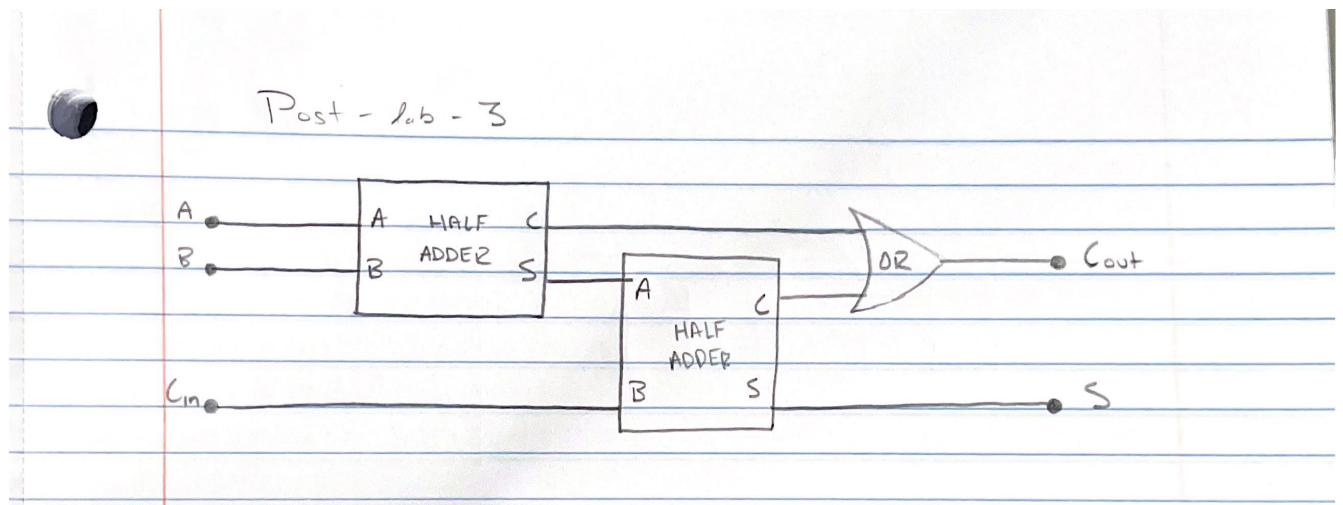
1. Provide all design items found in the pre-lab deliverables. If you found that a design needed corrections while executing the lab, supply the updated version of that material.

The items used in this lab for the half adder were minimal, including a variety of different colored wires, power supply, VCC and GND cables, breadboard, AND gate, XOR gate, and LEDs. For the full adder, I used different colored wires, power supply, VCC and GND cables, breadboard, AND gate, XOR gate, OR gate, and LEDs. The Ripple Carry Address used the same design as the full adder just twice as many gates except for the OR gate and more wires to implement more inputs and jumping from gate to gate.

2. Determine the worst-case propagation delay for your full adder design. Assume each gate has the same delay of 1 unit. Show the maximum delay path in your schematic. The maximum delay path is known as the critical path for that particular combinational block.

The worst-case propagation for the full adder circuit would be when all the inputs are at “1” or true, this would cause a propagation delay for every gate the path goes through.

3. Design a 2-bit carry ripple adder assuming you only have half adder circuits and OR gates to work with. Draw up a schematic for your design using half adder building blocks and OR gates. Be sure to clearly label all inputs and outputs of your blocks.



Important Student Feedback

1. What did you like most about the lab assignment and why? What did you like least about it and why?

I believe this lab was simple and straightforward. The way the lab is set up in a row with the TA in front is a bad system in my opinion. The people further back in the row are not able to hear the TA speaking at the front of the row.

2. Were there any sections of the lab manual that were unclear? If so, what was unclear? Do you have any suggestions for improving the clarity?

All sections on the lab manual were clear, if there was anything I was confused about it was because of my under-preparedness for the lab. I did not read over the lab the night prior, so I was confused at first but with help of classmates and the TA, I was luckily able to figure it out well.

3. What suggestions do you have to improve the overall lab assignment?

I have noticed a lot of the smaller components used to perform the lab are broken or defective, and it makes building the circuit a hassle since the students don't know if the wiring is at fault or the components are.