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ECEN 248

Section 509

Pre-lab #8

1. **Supposed we want to build a 32-bit counter using the circuit in Figure 1. If the gates used to construct the half-adders in the circuit are assumed to have a 2ns delay each, and the flip-flop overhead is assumed to be negligible, what is the maximum clock frequency we could use to drive our counter? Given the clock frequency you just calculated, how long would it take this counter to roll over (i.e. return to 0). Please show your calculations.**

Delay = 2ns x 32bits = 64ns

Clock frequency = 1 / Delay = 1 / 64ns = 0.015625 GHz → 15MHz

For time roll over : 2^{32} = 4.3 seconds

2. **Consider the use of a counter to divide an incoming clock. If our incoming clock signal is 32.768 kHz and we need a 64 Hz signal, how many bits would our counter need to have (i.e. what is n) to divide the incoming clock correctly?**

$F_2 = F_1 / 2^n$ → 64Hz = 32768 Hz / 2^n → 2^n = 512 → n = 9

3. **If the Seconds per Division setting for Figure 3 was set to 1 ms/div (ie. the time between axis markings is 1 millisecond), what do you think would be a good bit width for the counter in Figure 4, assuming a 50 MHz clock signal was driving the counter? Explain your answer.**

A good pulse width for the counter in the figure would be 40ns, this is because 1/50 is equal to 20 ns and the formula for pulse width is a change in time plus the frequency of clock signal and they both happen to be 20ns. This means the answer would be 40 ns for pulse width.