Lab 1: Digital Logic Gates

ECEN-248 Section 509

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Objectives:

In this lab I will become introduced to breadboards, DIP, breadboarding techniques, and components and equipment I will be using this semester for ECEN 248. In parts 1 and 2 of the lab I will be looking at the behavior of logic gates and recording voltages that I conclude.

Design:

Experiment Part 1:

To begin the lab, start by setting up the DC power supply and multi-meter. Connect the red cable to the red input and the black cable to the black for the area marked under “voltage.” Repeat the same steps for the power supply and place them at the top of the breadboard.

Turn on the multimeter and the power supply and turn the coarse adjustment clockwise until the multimeter reads 5V. Make sure the multimeter also reads 5V to make sure there is no short on the circuit.

Now to test the first gate, start by wiring a 74ALS04 gate, refer to the datasheet given to ensure the connections, and place it down onto the breadboard. Identify the power (VCC) and the ground (GND) pins for the 74ALS04 gate shown in the datasheet. Connect power and ground to said connections by jumping from the positive column where the power cable comes in and another from the negative column where the ground cable comes in. Also, make connections from the red lead of the multimeter to the gate output, the black lead of the multimeter should stay connected to the black lead of the power supply. Now connect a wire from either the VCC pin to the input for high voltage or from the GND input for low voltage. However, connecting both at the same time will cause a short. Turn on the power supply and record the gate outputs for low and high voltages and record this data in the tables shown on the lab manual.

Experiment Part 2:

Now, repeat the same experiment with the 74LS00 (NAND), 74LS02 (NOR), 74LS08 (AND), 74LS32 (OR), 74LS86 (XOR). Each gate has two inputs and one output according to the datasheets, fill in the tables shown in the lab manual to attach to the post-lab to show observed responses of the gates.

Results:

***Table 1**: Truth Table for Inverter (NOT Gate)*

A (High/Low)	Y (Volts)	Y (High/Low)
Low	4.2	High
High	.059	Low

***Table 2**: Truth Table for AND & OR Gates*

A (H/L)	B (H/L)	AND2 (V)	AND2 (H/L)	OR2 (V)	OR2 (H/L)
L	L	.098	L	.114	L
L	H	.097	L	4.2	H
H	L	.936	L	4.23	H
H	H	4.27	H	4.25	H

***Table 3**: Truth Table for NAND, NOR, & XOR Gates*

A (H/L)	B (H/L)	NAND2 (V)	NAND2 (H/L)	NOR2 (V)	NOR2 (H/L)	XOR2 (V)	XOR2 (H/L)
L	L	1.1	H	4.2	H	0.15	L
L	H	1.2	H	.069	L	4.2	H
H	L	1.06	H	.069	L	4.2	H
H	H	0.12	L	.068	L	.16	L

Conclusion:

From this lab, I was able to observe what each logic gate does by setting it up with the instructions shown above. I was able to correctly fill out the truth tables as I checked them on the datasheets after conducting the experiment. I am now more confident with the role that each logic gate does in a circuit.

Post-lab Deliverables:

1. What did you like most about the lab assignment and why? What did you like least about it and why?

I believe this lab was a simple and straightforward activity to introduce the students to logic gates and get familiarized with the breadboard and the multimeter. The way the lab is set up in a row with the TA in front is a very bad system in my opinion. The people further back in the row are not able to hear the TA speaking at the front of the row.

2. Were there any sections of the lab manual that were unclear? If so, what was unclear? Do you have any suggestions for improving the clarity?

All sections on the lab manual were clear, if there was anything I was confused about it was because of my under-preparedness for the lab. I did not read over the lab the night prior, so I was confused at first but with help of classmates and the TA, I was luckily able to figure it out well.

3. What suggestions do you have to improve the overall lab assignment?

I have noticed a lot of the smaller components used to perform the lab are broken or defective, and it makes building the circuit a hassle since the students don't know if the wiring is at fault or the components are.