Joaquin
Salas

Pre-lab 3

Half-Adder

A	B	C_{out}	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

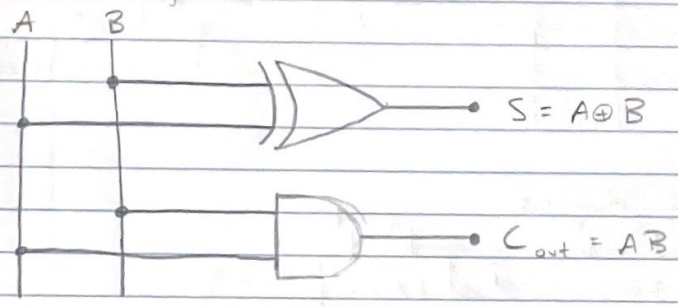
A \ B	0	1
0	0	0
1	0	1

$C_{out} = AB$

A \ B	0	1
0	0	1
1	1	0

$S = A \oplus B$

Logic Diagram -



The total gates needed would be 1, There is an advantage to using XOR GATES, it will simplify the circuit.

Full-Adder

A	B	C_{in}	C_{out}	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

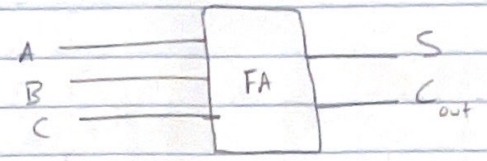
A \ BC_{in}	00	01	11	10
0	0	(1)	0	(1)
1	(1)	0	(1)	0

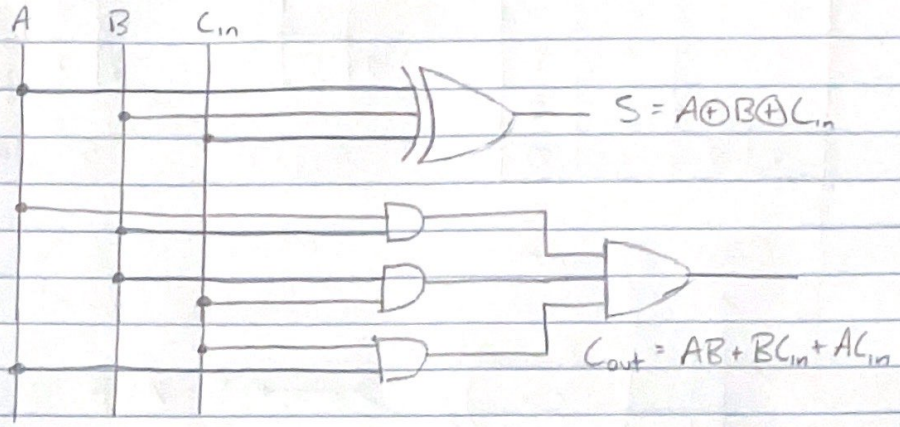
$S = A + B + C_{in}$

A \ BC_{in}	00	01	11	10
0	0	0	1	
1	0	1	1	1

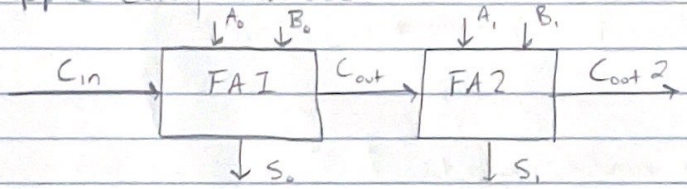
$C_{in} = AB + AC_{in} + BC_{in}$

Gate Schematic





Ripple Carry Adress



Input 1		Input 2				
A_1	A_0	B_1	B_0	S_2	S_1	C_{out}
0	0	0	0	0	0	0
0	0	0	1	0	1	0
0	0	1	0	1	0	0
0	0	1	1	1	1	0
0	1	0	0	0	1	0
0	1	0	1	1	0	0
0	1	1	0	1	1	0
0	1	1	1	0	0	1
1	0	0	0	0	1	0
1	0	0	1	1	0	0
1	0	1	0	1	1	0
1	0	1	1	0	0	1
1	1	0	0	0	1	0
1	1	0	1	1	0	0
1	1	1	0	1	1	0
1	1	1	1	0	0	1