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ECEN 248 – 509

Lab 7 Prelab

Pre-lab Deliverables

1. Create a new Verilog source file named "adder 2bit.v" with the module named "adder 2bit". You can use your full adder module created in lab6.

```
`timescale 1ns / 1 ps
`default_nettype none
/*This module describes the gate-level model of *
*a full-adder in Verilog  */

module adder_2bit(S, Cout, A, B, Cin);

    /*declare output and input ports*/
    //1-bit wires
    input wire A, B, Cin;  //1-bit wires
    output wire S, Cout;

    /*declare internal nets*/
    wire andBCin, andACin, andAB;

    /*use dataflow to describe the gate-level activity */
    assign S = A ^ B ^ Cin; //the hat (^) is for XOR
    assign andAB = A & B;
    assign andBCin = B & Cin;
    assign andACin = A & Cin;
    //filled out the code for andBC and andAC
    assign Cout = andAB | andBCin | andACin; //pipe (|) is for or

endmodule
```

2. If the circuit in Figure 7 utilizes the 2-bit carry ripple adder designed in Lab 3, what would be the maximum clock rate f given that each gate delay is 4ns? You can refer to your post-lab deliverable answer.

Gate delay = 2 * 2n = 2 * 2 * (4*10^-9) = 16*10^-9s.
Fmax = 1/gatedelay = 1 / (16*10^-9s) = 62.5*10^-6 Hz.
The max clock rate f given each gate delay 62.5*10^-6 Hz.

3. Compare all the three memory components discussed in the background part in the same table. Explain their differences and improvements.

Here we are comparing three memory components in the background part, the latch is a level–sensitive memory device. The latch depends on the value of the input, except it cannot be synchronous. In a set and reset latch, you can't have both buttons pressed at the same time. Flip flops apply the edge case, they will continue taking inputs and saving the previous input. The clock must be activated for the flip-flop to function.