

# **ECEN 248 - Lab Report**

## **Laboratory Exercise #4**

### **Simple Arithmetic Logic Unit**

**ECEN-248-509**

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**10-05-2022**

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## **Objectives:**

In this lab, I designed, implemented, and tested a simple 4-bit Arithmetic Logic Unit (ALU) that executes elementary computations like addition and subtraction for Boolean numbers and bit-wise AND. To do this we needed to learn about 2's complement arithmetic and multiplexers.

## **Design:**

In this lab, I breadboarded the 3 steps to getting to the Arithmetic Logic Unit. Addition and subtraction both utilize an adder circuit. We will create separate adders for both addition and subtraction. The circuit will work like figure 6 in the lab report, there are 4 full adders lined up and 2 inputs going into each with an XOR gate on the "b" input. And the carry goes on to the next. The sum is carried out to the output and the last carry out will go to any overflow needed.

### **Experiment Part 1:**

In the first part, I had breadboarded and tested the addition/subtraction unit. To do this we used the 4-bit carry ripple adder component 74283. A DIP switch is recommended, but since the need for many resistors on the switch, I personally decided to skip off on this part. We wired the inputs through the adding and subtraction unit and displayed the outputs to the LEDs.

### **Experiment Part 2:**

In this part, I followed the same steps but instead did it with the 4-bit 2:1 MUX chip 74257. I proceeded with the same steps and wired the outputs to the LED again. After debugging and testing this circuit we proceeded to move on to the next step.

### **Experiment Part 3:**

To begin this point of the lab experiment, we will begin by connecting the outputs of the AND units and addition/subtraction units to the "A" and "B" inputs from the 4-bit 2:1 MUX. The second step was to connect the OE of the MUX to the ground on the breadboard. Wire the MUX outputs to the LEDs display. The last step is to vary the control signals  $c_0$  and  $c_1$  by connecting them to the power or the ground. We began to debug the circuit and checking it with the table created in our pre-lab.

## Results:

After completing all three parts of this experiment, we checked several inputs for each part and showed these results to our TA, Sri. This lab worked very well and I believe we did well on this lab and got it done in a short amount of time which made me very confident with my newly learned skills about breadboards.

## Conclusion:

In this lab, I was able to learn about implementing half and full adders along with a MUX and adder/subtractor to create a complex but simple adding and subtracting circuit, basically a calculator. This was a very interesting lab that I really enjoyed.

## Post-lab Deliverables:

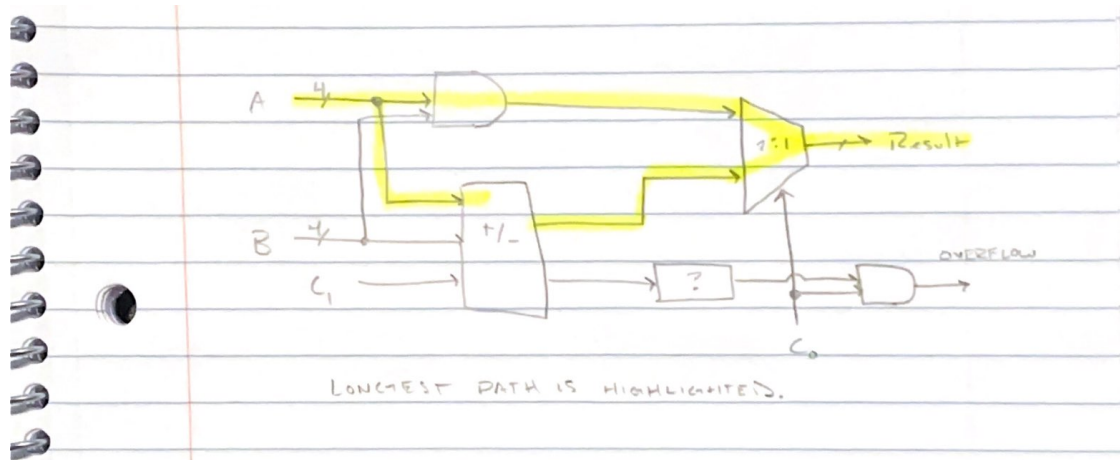
1. Observe and fill in Table 1. Both A and B are two's complement numbers. The result should be a 4-bit binary number. Determine whether overflow occurs or not.

Table 1: c0 and c1 operation.

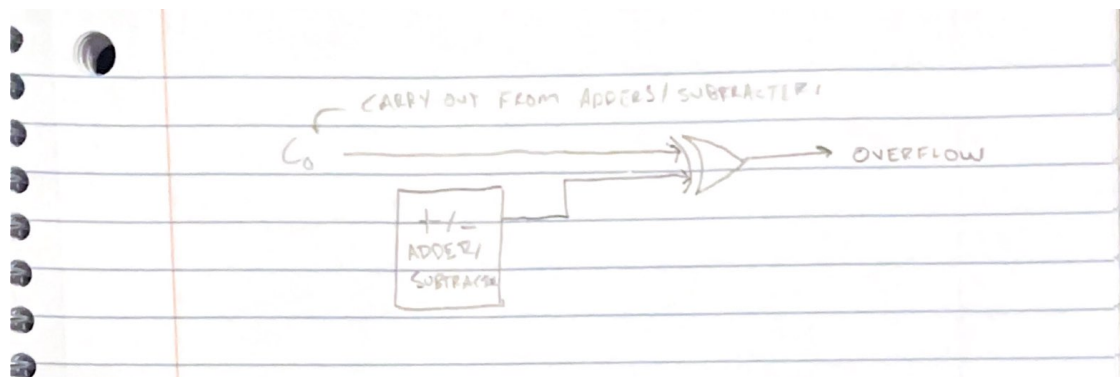
C <sub>0</sub>	C <sub>1</sub>	Operation	A	B	Result	Overflow
0	0	AND	0100	0110	0110	none
0	1	AND	0110	1101	0110	none
1	0	ADD	0100	0110	1010	yes
1	0	ADD	0100	1101	0001	none
1	0	ADD	1101	1001	0110	yes
1	1	SUB	0100	0111	1000	none
1	1	SUB	0110	1001	0001	yes

2. Determine the maximum gate delay through your final ALU circuit assuming each gate has a delay of 1 unit. Highlight the critical path on the gate-level schematic.

According to my circuit design in my pre-lab, the maximum gate delay will be 3 since it goes through 3 logic gates.



3. Please design the overflow detecting unit in Figure 6. You can use all available signals except the signals inside the chip package. Show your process and draw a gate-level schematic.



## **Important Student Feedback**

1. What did you like most about the lab assignment and why? What did you like least about it and why?

I believe this lab was simple and straightforward. The way the lab is set up in a row with the TA in front is a bad system in my opinion. The people further back in the row are not able to hear the TA speaking at the front of the row.

2. Were there any sections of the lab manual that were unclear? If so, what was unclear? Do you have any suggestions for improving the clarity?

All sections on the lab manual were clear, if there was anything I was confused about it was because of my under-preparedness for the lab. I did not read over the lab the night prior, so I was confused at first but with help of classmates and the TA, I was luckily able to figure it out well.

3. What suggestions do you have to improve the overall lab assignment?

I have noticed a lot of the smaller components used to perform the lab are broken or defective, and it makes building the circuit a hassle since the students don't know if the wiring is at fault or the components are.