Prelab 7: Buck Converter: Closed Loop

1 Theory and Background

Check Your Understanding

- 1-1 What parameters of a buck regulator determine the nominal value of its DC output voltage?
    - A. the inductance and capacitance of the L-C filter
    - B. the reference voltage and the voltage sensor gain
    - C. the error amplifier pole and OPAMP dc gain Adc
- 1-2 What parameter of a buck regulator determines its DC output voltage offset error?
    - A. the inductance L
    - B. the OPAMP open loop dc gain Adc
    - C. the error amplifier pole frequency f0
- 1-3 What parameter of a buck regulator determines the open loop output impedance of the buck regulator at low frequency?
    - A. the inductance of the inductor
    - B. the capacitance pf the capacitor
    - C. the resistance of the inductor
- 1-4 What parameters majorly influence the closed loop output impedance of the buck regulator at low frequency?
    - A. the error amplifier pole frequency f0 and OPAMP dc gain Adc
    - B. the MOSFET half-bridge gate driver voltage
    - C. the reference voltage and the voltage sensor gain

- 1-5 Based on your answers to Questions 1-1 to 1-4, what would you do to design a buck regulator with higher DC accuracy and low output impedance? Find a correct voltage sensor gain H to improve DC accuracy, also from equation 1-3-5, increasing the OPAMP DC gain (Adc) will reduce the DC offset error.

2 Exercise

The **Discrete Buck Section** in the TI Power Electronics Board for NI ELVIS III is based on the following setup:

- MOSFETs: TI's CSD15380F3, assume V_{th} = 1.35V, β = 0.24A/V^2, λ =0.05V^{-1}
- OPAMP: TI's OPA835IDBVR, assume A_{dc}=10^6, V_{cc+}=5.5V, V_{cc-}=0V.
- VOLTAGE REFERENCE: TI's LM4140, assume V_{ref}=1.024V.
- ERROR AMPLIFER SETUP: f_0 = 4.06kHz.

The TI's devices datasheets are available at the following links:

- CSD15380F3 MOSFET: http://www.ti.com/lit/ds/symlink/csd15380f3.pdf
- OPA835IDBVR OPAMP: http://www.ti.com/lit/ds/symlink/opa835.pdf
- LM4140 VOLTAGE REFERENCE: http://www.ti.com/lit/ds/symlink/lm4140.pdf

The voltage divider is configurable as follows:

- (a) R_{i1}=39.2kΩ, R_g=18.2kΩ; (b) R_{i1}=39.2kΩ, R_g=10.2kΩ

The L-C filter is configurable as follows:

- (a) L = 15µH, R_L = 140mΩ; (b) L = 48µH, R_L = 400mΩ;
- (a) C = 10µF, R_c = 5mΩ; (b) C = 100µF, R_c = 55mΩ.

2-1 Calculate the nominal value of the DC output voltage VoutDC,nom, in Volts with three decimal digits, and the DC offset error, in microvolts with one decimal digit, with voltage divider options (a) and (b) :

- (a): VoutDC,nom = _3.230_V_____; ERRDC = 10.2µV_____
- (b): VoutDC,nom = _____4.959V_____; ERRDC = 24.0µV_____

2-2 You have a buck regulator powered by a 7V DC source voltage and generating a 5V DC output voltage for a 120 DC load resistance Ro. The load is subjected to an AC perturbation IoutACsin(2ft), where the frequency f can have the values listed in Table 2-1. Assume the inductor configuration (b) and the capacitor configuration (a). Calculate the open and closed loop output impedance Zout,OL and Zout,CL in Ohms with three decimal digits, and report the results in Table 2-1.

f [Hz]	1	10	100	1000	10k
Zout,OL	0.400	0.400	0.400	0.507	3.190
Zout,CL	0.000	0.001	0.010	0.125	2.270

2-3 Based on the results of your calculations, do you see an improvement in the AC load current perturbation rejection capability of the buck regulator in closed loop operation compared to open loop operation? A. yes B. no Please provide your comments: ____**Yes Closed-loop operation significantly reduces the output impedance at frequencies below the crossover frequency, improving perturbation rejection.**_____

_____

2-4 What parameter would you change to further improve the low frequency rejection capability, and how? ___**Increase the feedback factor by adjusting the voltage divider resistors This enhances the loop gain at low frequencies, further reducing Zout,CL**

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3 Simulate

3.1

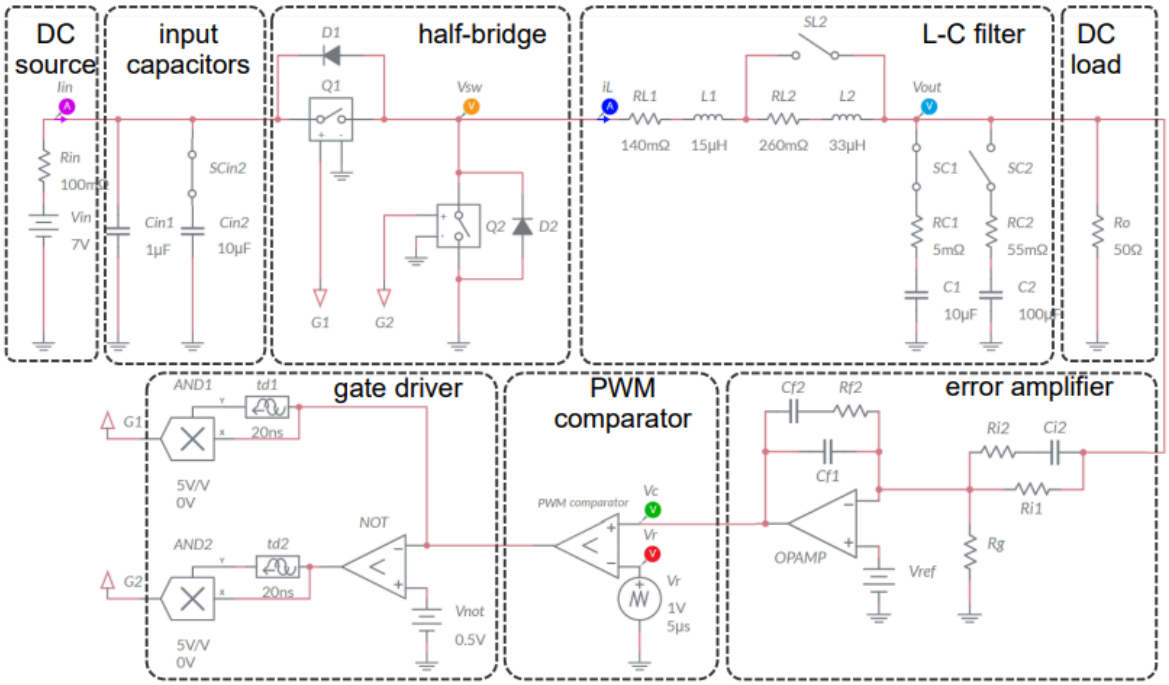

Figure 3-1. Multisim Live Circuit Schematic for the Analysis of Buck Regulator in Closed Loop Operation.

Vin DC	6.0	6.5	7.0	7.5	8.0	8.5	9.0
Vout DC nom [V]	4.959	4.959	4.959	4.959	4.959	4.959	4.959
Vout DC [V]	4.961	4.960	4.960	4.961	4.962	4.959	4.960
Vc DC /	0.835	0.771	0.716	0.668	0.627	0.590	0.558

Vrpp [V]							
VoutDC / VinDC	0.819	0.763	0.709	0.661	0.620	0.583	0.551

- 3-1-1 Does the DC output voltage VoutDC change as VinDC increases? A. yes **B. no**

  Discuss the results based on the Theory and Background section equations: **Based on the equations, the output voltage is on the duty cycle and the efficiency. Since D = VcDC/Vrpp, and that ratio decreases as the input voltage increases, the output voltage is expected to remain the same.**

- 3-1-2 Does the PWM control voltage VcDC change as VinDC increases? **A. yes** B. no

  Discuss the results based on the Theory and Background section equations: **If we rearrange Equation 1-3-1 to solve for VcDC, then as VinDC increases VcDC should decrease because they have a ratio of 1/Vin = VcDC.**

- 3-1-3 How is the ratio VcDC/Vrpp correlated to the ratio VoutDC/VinDC? why?

  The ratios both change decrease as the input voltage increases, and the values of both measurements are generally close together.

- 3-1-4 What change do you expect in the simulation results if you close the switch SC2 and open the switch SC1? why? **I expect the simulation values should not change much compared to the values when SC1 is closed.**