

ATtiny24A/44A/84A

Silicon Errata and Data Sheet Clarification

Introduction

The ATtiny24A/44A/84A devices you have received conform functionally to the current device data sheet (www.microchip.com/DS40002269), except for the anomalies described in this document. The errata described in this document will likely be addressed in future revisions of the ATtiny24A/44A/84A devices.

Note:

· This document summarizes all the silicon errata issues from all revisions of silicon, previous and current.

1. Silicon Issue Summary

Legend

- Erratum is not applicable.
- **X** Erratum is applicable.

		Valid for Silicon Revision				
Peripheral	Short Description	ATtiny24A	ATtiny44A		ATtiny84A	
		Rev. H ⁽¹⁾	Rev. F ⁽¹⁾	Rev. G	Rev. C ⁽¹⁾	
Device	No known errata					

Note:

1. This revision is the initial release of the silicon.

2. Silicon Errata Issues

2.1 Errata Details

- Erratum is not applicable.
- **X** Erratum is applicable.

2.2 None

There are no known errata as of this publication date.

3. **Data Sheet Clarifications**

Note the following typographic corrections and clarifications for the latest version of the device data sheet (www.microchip.com/DS40002269).

Note: Corrections are shown in bold. Where possible, the original bold text formatting has been removed for clarity.

3.1 Appendix B – ATtiny24A/44A/84A Specification at 125°C

A clarification for the Supply Current Power-Down Mode maximum limits in Appendix B - ATtiny24A/44A/84A Specification at 125°C (https://ww1.microchip.com/downloads/en/DeviceDoc/Atmel-8183-AVR-8-bit-Microcontroller-ATtiny24A-ATtiny44A-ATtiny84A-Appendix-B-125C_Datasheet.pdf) has been made.

Table 3-1. Table 2-1. DC Characteristics. $T_A = -40$ °C to +125°C

Symbol	Parameter	Condition	Min.	Typ. <u>⁽¹⁾</u>	Max.	Units
	Input low voltage	V _{CC} = 1.8-2.4V	-0.5		0.2V _{CC} ⁽³⁾	V
.,	Input low voltage	$V_{CC} = 2.4-5.5V$	-0.5		0.3V _{CC} ⁽³⁾	V
V _{IL}	Input high voltage RESET pin as Reset ⁽⁴⁾	V _{CC} = 1.8-5.5	-0.5		0.2V _{CC} ⁽³⁾	
	Input high voltage	V _{CC} = 1.8-2.4V	0.7 V _{CC} ⁽²⁾		V _{CC} +0.5	V
.,	RESET pin as Reset	V _{CC} = 2.4-5.5V	0.6 V _{CC} ⁽²⁾		V _{CC} +0.5	V
V _{IH}	Input high voltage RESET pin as Reset ⁽⁴⁾	V _{CC} = 1.8-5.5V	0.9 V _{CC} ⁽²⁾		V _{CC} +0.5	V
.,	Output low voltage	I _{OL} = 10 mA, V _{CC} = 5V			0.6	V
V _{OL}	(5) except RESET pin(7)	I_{OL} = 5 mA, V_{CC} = 3V			0.5	V
.,	Output high voltage	I_{OH} = -10 mA, V_{CC} = 5V	4.3			V
V _{OH}	(6) except RESET pin(7)	I_{OH} = -5 mA, V_{CC} = 3V	2.5			V
I _{LIL}	Input leakage current I/O pin	V _{CC} = 5.5V, pin low (absolute value)		< 0.05	1 ⁽⁸⁾	μA
I _{LIH}	Input leakage current I/O pin	V _{CC} = 5.5V, pin high (absolute value)		< 0.05	1 ⁽⁸⁾	μΑ
Б	Pull-up resistor, I/O pin	V_{CC} = 5.5V, input low	20		50	kΩ
R _{PU}	Pull-up resistor, Reset pin	V _{CC} = 5.5V, input low	30		60	kΩ

Errata

continued						
Symbol	Parameter	Condition	Min.	Typ. <u>(1)</u>	Max.	Units
	Supply current, Active mode ⁽⁹⁾	f = 1 MHz, V _{CC} = 2V		0.25	0.5	mA
		f = 4 MHz, V _{CC} = 3V		1.2	2	mA
		f = 8 MHz, V _{CC} = 5V		4.4	7	mA
		f = 1 MHz, V _{CC} = 2V		0.04	0.2	mA
I _{CC}	Supply current, Idle mode ⁽⁹⁾	f = 4 MHz, V _{CC} = 3V		0.25	0.6	mA
		f = 8 MHz, V _{CC} = 5V		1.3	2	mA
	Supply current, Power-Down mode ⁽¹⁰⁾	WDT enabled, V _{CC} = 3V		4	30	μA
		WDT disabled, V _{CC} = 3V		0.2	20	μΑ

Notes:

- 1. Typical values at 25°C.
- 2. "Min" means the lowest value where the pin is guaranteed to be read as high.
- 3. "Max" means the highest value where the pin is guaranteed to be read as low.
- 4. Not tested in production.
- 5. Although each I/O port can sink more than the test conditions (10 mA at V_{CC} = 5V, 5 mA at VCC = 3V) under steady-state conditions (non-transient), the sum of all I_{OL} (for all ports) should not exceed 60 mA. If I_{OL} exceeds the test conditions, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current higher than the listed test condition.
- 6. Although each I/O port can source more than the test conditions (10 mA at V_{CC} = 5V, 5 mA at V_{CC} = 3V) under steady-state conditions (non-transient), the sum of all I_{OH} (for all ports) should not exceed 60 mA. If I_{OH} exceeds the test condition, V_{OH} may exceed the related specification. Pins are not guaranteed to source current higher than the listed test condition.
- 7. The RESET pin must tolerate high voltages when entering and operating in programming modes and, as a consequence, has a weak drive strength as compared to regular I/O pins. See the figures for ATtiny24A: From Figure 3-22 on page 21 to Figure 3-25 on page 23. The figures for ATtiny44A: From Figure 3-67 on page 44 to Figure 3-70 on page 45.
- 8. These are test limits, accounting for leakage currents of the test environment. Actual device leakage currents are lower.
- 9. Values are with an external clock using methods described in "Minimizing Power Consumption". Power reduction is enabled (PRR = 0xFF), and there is no I/O drive.
- 10. BOD disabled.

4. Document Revision History

Note: The document revision is independent of the silicon revision.

4.1 Revision History

Doc Rev.	Date	Comments
В	03/2022	Data sheet clarification added. • 3.1. Appendix B – ATtiny24A/44A/84A Specification at 125°C
A	10/2020	Initial release of this document. Content moved from the data sheet and restructured to the new document template Updated the die revision list to reflect die revisions in production

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