Design of Low-Voltage and Low-Power Cryogenic CMOS Voltage Reference Circuits

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***Abstract*—This paper presents the design of low-voltage and low-power cryogenic CMOS voltage reference circuits. This cryo-optimized circuit uses low-threshold devices to compensate for the transistors' threshold increase in ultra-low temperatures. Similarly, the PTAT factor is increased three times from its optimal value as compensation for the current decrease in cryogenic temperatures. A family of reference circuits was implemented in standard 65-nm CMOS. The silicon results show temperature coefficients of 419, 350, and 229 ppm/K in the ultra-wide temperature range from 4 to 295 K, with power consumptions at 4 K of only 5.3 μW, 22.7 μW, and 410 nW, respectively.**

***Index Terms*—Quantum-Computing, Cryogenic, Bulk CMOS, Reference, Circuit, Design, Cryo-optimized.**

I. Introduction

Quantum computers use quantum bits (Qubits) as the basic unit of information. Qubits are not limited to a binary (on or off) state similar to conventional bits, but instead, they possess an infinite number of states significantly advancing computing power [1]. Cryogenic temperatures (CT) are typically required to realize a Qubit, minimizing the thermal noise that would otherwise jeopardize the fragile Qubit states [2]–[5]. On the other hand, the electronic circuits that control the Qubits usually operate at room temperatures (RT) [6]. This imposes integration limitations due to the gap in operating temperatures and the number of wires required in and out of the cryostat.

Recently, Cryogenic (Cryo) CMOS circuits, operating at 4 degrees Kelvin (K), have been proposed as a way to reduce the temperature gap and facilitate the integration of the Qubits and the associated circuits within the cryostat [7]. Digital-to-Analogue Converters (DACs) and Analogue-to-Digital Converters (ADCs) are at the heart of Qubit interfaces [6], controlling (requires DACs) and reading (requires both ADCs and DACs) the Qubit states, respectively. Several DACs and ADCs designs performing at 4 K have been summarized in the literature [8]. DACs and ADCs rely on a solid voltage reference to define the conversion least significant bit (LSB). Therefore, it is vital to design voltage references that can operate at CT with low power dissipation.

In recent years, in the literature, there have been presented a number of voltage references for cryo-temperatures [9]–[11]. In [9], it was demonstrated that the traditional bandgap voltage reference using bipolar devices becomes unreliable at temperatures below 100 K. Also in [9], the authors used dynamic threshold (DT) PMOS devices as a replacement for bipolar devices, producing an all-CMOS voltage reference circuit operable at 4 K. A refined version of [9] was presented in [11], using fewer stacked transistors and thus reducing the required supply voltage and associated power dissipation. In [10], fully depleted silicon on insulator (FDSOI) process was used, in order to control the transistor characteristics and fine-tune the reference voltage. At this point, it is important to mention that the two main challenges in the design of low-voltage Cryo-CMOS circuits are the limited temperature coverage of foundry models and the increase in the transistor's threshold voltage (V_{TH}) [12], [13].

This paper presents the design of low-voltage (1.2 V) low-power voltage reference circuits. The cryo-optimized voltage reference circuit presented here is a modified version of [9], where all the transistors are replaced with low V_{TH} (LVT) devices, and the PTAT coefficient is over-designed by three times to compensate for the increase in V_{TH} at CT. As a result, one of the voltage reference circuits in this paper achieves a temperature coefficient of 350 ppm/K in the wide temperature range from 4 to 295 K and 135 ppm/K explicitly optimized from 4 to 20 K for deep-cryogenic application, with lower power consumption than [9]. The rest of the paper is organized as follows. Section II introduces the modified low-voltage, low-power voltage reference and the adopted circuit design methodology. Section III presents the silicon measurements, and conclusions are drawn in Section IV.

II. Cryo-Optimized Voltage References Circuits and Design Methodology

As the operating temperature decreases, CMOS transistor characteristics change. Notably, from the I-V curves, V_{TH} and carrier mobility are increased [12]–[14]. From the literature, it can be seen that the increase in the V_{TH} has a more dominant impact on the circuit performance than the increase in the carrier mobility [9]–[11]. Therefore, it becomes necessary to account for this effect in the design phase of cryogenic circuits.

The introduced low-power voltage reference circuit is presented in Fig. 1. This reference circuit is similar to that in [9], but it has all the transistors replaced with their LVT devices.

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	W/L
$T_{1,2,3}$	$3\mu m/0.5\mu m$
$T_{4,5}$	$2\mu m/0.5\mu m$
$T_{6,8}$	$4\mu m/0.5\mu m$
T_7	$144\mu m/0.5\mu m$
R_1	$6.5k\Omega$
R_2	$8k\Omega$
α	1.23

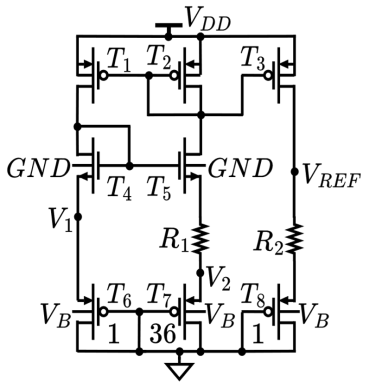

Fig. 1: Schematic of the voltage reference circuit with all LVT devices and overdesigned α factor.

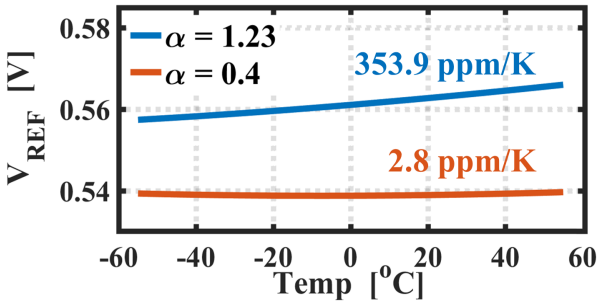

Fig. 2: LVT voltage reference circuit simulation in the temperature range from -50 to +50 ^{o}C with optimum α = 0.4 (red) and overdesigned α = 1.2 (blue) for cryogenic applications.

Furthermore, the bulk terminal (V_B) of the core-PMOS devices was configured to evaluate the circuit performance with V_B tied to the supply (V_{DD}) and to the ground (GND). For the sake of completeness and comparison, the reference circuit is also implemented with standard V_{TH} (SVT) devices.

Circuit simulators and foundry device models are at the heart of integrated circuit design. Unfortunately, foundry device models have limited temperature coverage and are yet to be calibrated for cryo-CMOS design. To bridge this gap, initial works have investigated modeling techniques that can be used to perform simulations at 4 K [14]–[16]. However, these results are mostly technology-dependent and typically require single or multiple test chips from which key parameters can be empirically extracted, significantly increasing the design and development time. To overcome this limitation, the reference circuit presented here is first designed and simulated to operate in the temperature range from -50 to +50 ^{o}C to be then modified to account for the dominant effects at cryo-temperatures.

The reference circuit generates a Proportional To Absolute Temperature (PTAT) voltage through the difference ΔV = V_1 - V_2, forcing a PTAT current on R_1. This current is then mirrored to the output branch stage, generating the PTAT voltage $\Delta V \cdot (R_2 \ / \ R_1)$, which is then combined with the Complementary To Absolute Temperature (CTAT) voltage generated in the diode-connected PMOS. This creates a first-order compensation of the PTAT and CTAT components at the output of the reference circuit. The resistor ratio R_2 / R_1 controls the PTAT voltage's slope, usually referred to as the α factor. In the -50 to +50 ^{o}C range, the optimal α = 0.4, which can be achieved with R_1 = 20 kΩ and R_2 = 8 kΩ. This optimal value produces an approximately first-order temperature-independent voltage, as depicted in Fig. 2.

In cryogenic temperature, however, the increase in V_{TH} reduces the current sourcing capability of the floating current mirror [17]. This causes the ΔV curve to be flattened as the temperature decreases [9], i.e., the PTAT slope decreases, equivalent to having a smaller α. In other words, an optimal α for the temperature range -50 to +50 ^{o}C, becomes sub-optimal at CT due to the current starvation of the current mirror as a result of the V_{TH} increase. Therefore, to optimize the voltage reference circuit for its use in CT, the designer can intentionally over-design α to compensate for the PTAT slope decrease.

From [9], [10], and [11], it can be seen that the current consumption at CT reduces by at least a factor of two with respect to RT. Therefore, α should be made at least two times larger for a cryo-optimized design. In this design, α was made three times larger from the optimal value, i.e., 1.2, to account for any other effects reducing the PTAT slope in CT. As expected, this change deteriorates the temperature coefficient in the -50 to +50 ^{o}C, as depicted in Fig. 2, but it will ensure a more temperature-independent performance at CT. Similarly, it will prevent the temperature curve from shifting between PTAT and CTAT slopes [9].

The resistors were implemented with polysilicon for the physical implementation of the circuits, whose resistance variation with temperature is less than 10% [9]. Deep N^- well (DNW) with associated guard rings were used to isolate the bulk-connected-to-ground PMOSs in the circuits, preventing other devices from latch-up.

III. Measurement Results

Utilizing LVT and SVT devices, the cryo-optimized voltage references were designed and fabricated in a 65-nm bulk CMOS process. Along with the voltage references, stand-alone transistors and resistors were also fabricated to obtain the I-V curves of these devices at CT. QFN32 packaging was employed, which is directly soldered on the test Printed Circuit Board (PCB). The PCB is directly attached to the 4K flange of a Bluefors LD-4K dilution refrigerator by using brass screws. A copper heat sink is placed between the QFN packaging and the 4K flange to minimize temperature variations between them. Details on the chip micrograph and the cryogenic test setup are shown in Fig. 3. The used cryostat maintains a 1 K/min rate during its cooling down (RT to CT) and a 0.2 K/min rate during its heating up (CT to RT). As no temperature sensor was designed in the chip, measurements were mainly taken using the slower 0.2 K/min rate in order to give enough

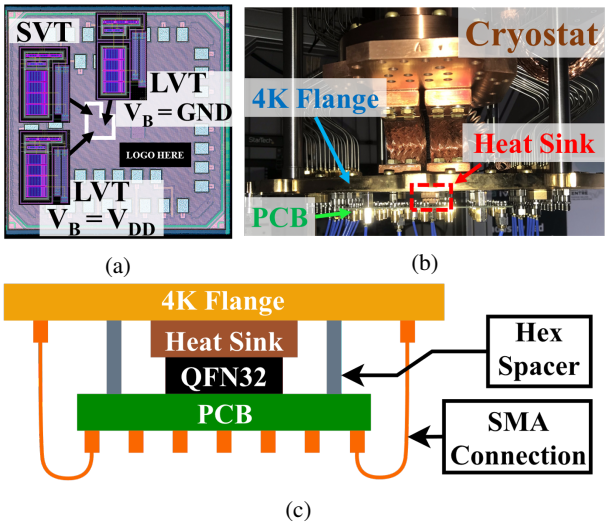

Fig. 3: (a) Chip Photograph; (b) Cryogenic Measurement Set-Up; (c) Sketch of Thermal Bridge.

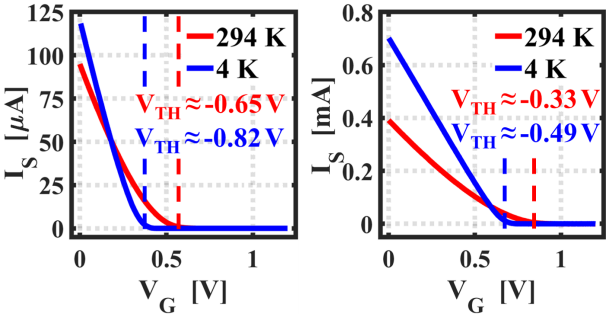

Fig. 4: I_S-V_G Measurements for (a) SVT and (b) LVT PMOS.

time for the chip to reach thermal equilibrium with the 4K flange.

A. Threshold voltage at 4K

The PMOS transistor devices of SVT and LVT have been characterized at RT and CT. Tested transistors have 4 μm width (W) and 0.5 μm length (L). Both sources and bulks of the transistors have been tied to V_{DD}, 1.2 V, and the drains have been connected to GND. Measurements are taken every 50 mV decrease of gate voltage (V_G) from 1.2 V. For each measurement, 20000 samples are collected over 2 min and averaged to produce the final result. Fig. 4 shows the source current (I_S) as a function of the gate voltage (V_G), where it can be seen that V_{TH} increases by more than 150 mV in both cases. The low V_{TH} nature of LVT PMOS has been maintained at CT.

B. LVT PMOS with Body Effect

The tested DTPMOS, with W / L = 4 μm / 0.5 μm, had its source connected to V_{DD} while its drain was connected to GND. Source current has been measured with the change of

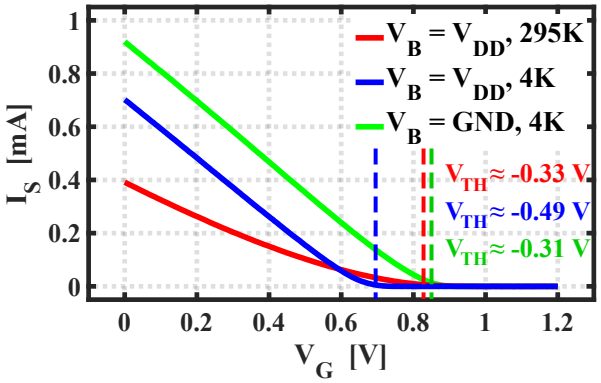

Fig. 5: I_S-V_G Measurements for LVT PMOS.

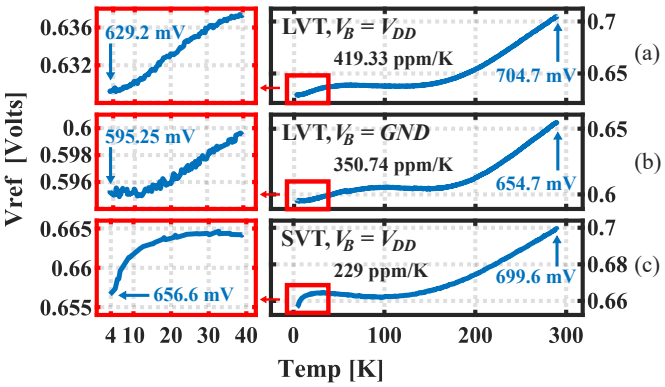

Fig. 6: Reference Voltage versus. Temperature constructed by: (a) LVT, $V_B = V_{DD}$; (b) LVT, $V_B = GND$; and (c) SVT.

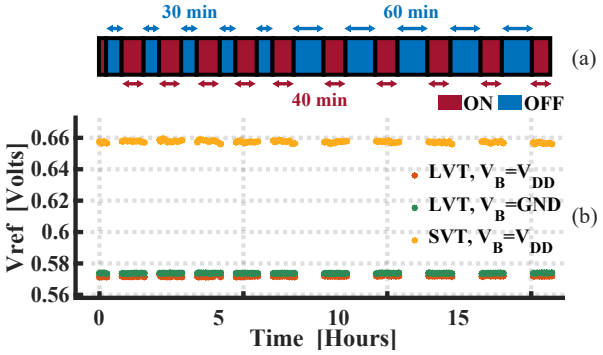

Fig. 7: ON OFF Cycle at 4 K. (a) Schedule; (b) Results.

V_G at two different levels of body bias (V_B), V_{DD} and GND, which is illustrated in Fig. 5. Similarly, results are constructed by measuring every 50 mV of V_G, with 20000 samples collected and averaged for each. From the results, the V_{TH} of the LVT device reduces when biasing its bulk to GND. Additionally, similar to the 40nm bulk process [18], the 65nm bulk process demonstrates its FDSOI-comparable capability for bulk control at CT due to the suppressed forward-bias current leakage, resulting from the increased ON-resistance of source-bulk PN junction [19].

TABLE I: PERFORMANCE COMPARISON OF CRYOGENIC VOLTAGE REFERENCE CIRCUIT IN CMOS

		This work			**2018 [9]**	**2020 [10]**	**2024 [11]**		
CMOS Process		65 nm Bulk			40nm Bulk	28nm FDSOI	40nm Bulk		
Core Device		SVT PMOS (V_B = V_{DD})	LVT PMOS (V_B = V_{DD})	LVT PMOS (V_B = GND)	Thick Oxide DTPMOS	NMOS	NMOS	PMOS	DTPMOS
Temperature Range [K]		4-295			4-300	4-300	4.2-300		
Supply Voltage [V]		1.2-1.3[a]	1.1-1.3[a]	1.1-1.4[a]	1.8-3.3	1.2-1.8	0.96-1.1	0.99-1.1	0.98-1.1
Power [μW]	RT	20.8	65.04	77.4	368	15.8[b]	13.7	14.9	15.1
	CT	0.41	5.3	22.73	132	13.9[b]	5.1	8.2	7.8
Reference Voltage [V]	RT	0.699	0.705	0.655	1.02	0.485	N.A.	N.A.	N.A.
	CT	0.656	0.629	0.595	0.81	0.658	N.A.	N.A.	N.A.
Temperature Coefficient [ppm/K]		229[c] (744.3[d])	419.3[c] (377.5[d])	350.7[c] (135[d])	833[c] (123[a])	1214[c] (195[e])	111[f]	547[c]	475[c]
PSRR [dB] (@ 1 MHz)	RT	-12.25	-11.79	-11.82	-23.1	-51	N.A.	N.A.	N.A.
	CT	-8.25	-11.85	-12.65	-23.4	-51.1			
Chip Area [μm^2]		725	725	836.5	445	40920	6000	9000	9000

[a]At 4 K; [b]Simulation results; [c]From CT to RT; [d]From 4 to 20 K; [e]From 4 to 19 K; [f]Trimmed and averaged, from CT to RT;

C. Cryo-Optimized Voltage Reference Circuits

The fabricated voltage reference circuits were tested in the ultra-wide temperature range from 4 to 295 K. Measurements are taken at 4 K intervals, with results averaged from 20,000 samples collected over 2 minutes. Fig. 6 (a) shows the measured reference voltage generated by the circuit with LVT devices and V_B = V_{DD}, showing a temperature coefficient of 419.33 ppm/K in the ultra-wide temperature range. The power consumption at RT is 65 μW, while at 4 K, it is only 5 μW. The measured performance is summarised in the comparison Table I. In Fig. 6 (b), the result corresponds to the reference circuit with LVT devices but with V_B = GND, producing a lower temperature coefficient of 350.74 ppm/K. In this case, the power consumption is 77.4 μW at RT and 22.73 μW at CT. This increment in power is associated with larger currents being sourced by the current mirror due to the reduced V_{TH} of the core devices by the V_B = GND connection.

From the above results, it can be observed that the approximately flat first-order temperature compensation, achieved with α = 0.4 in the range from -50 to +50 ^{o}C has now shifted down to temperatures in the range of around 50 to 150 K with α = 1.2. Shifting of the flat validates the optimized approach of increasing α by a 3$\times$ factor to compensate for increased V_{TH} at low temperatures. However, note that the overall responses are of the PTAT type, with a steeper slope from 150 to 295 K, due to the larger than necessary α in this range. Furthermore, biasing the bulk voltage of core devices to GND could achieve better output temperature independence from 4 to 50 K, similar to [9].

The result from the voltage reference circuit with SVT device is shown in Fig. 6 (c), but only for V_B = V_{DD}, as no version with V_B = GND was implemented. The temperature coefficient of only 229 ppm/K is the lowest among the three designed and tested reference circuits. The power consumption is also the lowest, with only 410 nW. Similarly, in the 50 to 150 K temperature region, the response is also the flatlets, but it shows a temperature coefficient inversion from 4 to 20 K. The inversion indicates that the sourced current by the mirror is too weak to maintain the PTAT contribution strong enough. Although this design offers the best performance characteristics, multi-chip testing has revealed that it is susceptible to process variations, and its use is less recommended for deep-cryogenic applications.

Considering the start-up circuit is not included in the design, the reference circuits are powered periodically at 4 K to verify their cryogenic robustness. As demonstrated in Fig. 7 (a), each circuit is scheduled to be powered off and kept in 4 K for 30 minutes, followed by 40 minutes of power-on. After repeating this cycle five times, the power-off time is then extended to 60 minutes for the subsequent five cycles. Measurements take every 5 minutes once the circuits have been powered on, with 20000 samples averaged for each. As described in Fig. 7 (b), all three designs can be powered on and produce relatively stable voltage references after either 30 or 60 minutes of being powered off at 4 K. This primarily demonstrates the designs' cryogenic capability without a start-up circuit.

The fabricated reference circuit with LVT devices and V_B = GND represents the best compromise of all the designed and tested circuits. Compared to the works in state of the art [9]–[11], the modified reference circuit achieves the best temperature coefficient across the wide temperature range among works that utilize PMOS as core devices. It also shows reduced power consumption compared to [9], which is mainly due to the reduction in supply voltage but also to the prevention of forward-biased source-bulk junction of the DTPMOS.

IV. Conclusions

Maintaining temperature independence among wide temperature ranges is critical for advanced QC development. This work achieves low-power and cryogenic-optimized design by utilizing LVT CMOSs with the combination of over-designed α factor. The achieved wide-range temperature dependency of 350.7 ppm/K is outstanding among PMOS-based designs. Repeated circuit ON-OFF cycles at 4 K ensure the circuits' cryogenic capability even without start-up circuits.

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