A Self-Cascoding CMOS Circuit for Low-Power Applications

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ABSTRACT

A self-cascoding CMOS circuit for operation in weak inversion is presented. The self-cascoding MOSFET circuit has been shown to exhibit greater than twenty-fold increase in the output resistance, without paying virtually any penalty in real estate and power consumption. The circuit has been used to increase the gain in the front stage of operational amplifiers, and to obtain improved performance from analog current copier circuits.

I. INTRODUCTION

A conventional cascode circuit is shown in fig. 1. The cascode circuit consists of two transistors (M_m, M_c) connected in series and are usually biased to operate in saturation. The bias level of the cascode transistor (M_c) is usually generated on-chip at the cost of increased power and real-estate. Furthermore, the performance of certain class of cascode circuits called regulated cascode circuits depends critically on the bias currents [1].

There are two main reasons for the use of cascode circuits [2]. First, the output resistance of a cascode circuit is higher than that of an ordinary MOSFET. Secondly, the input capacitance can be kept low due to reduced miller effect. In several applications, such as current memory circuits [3, 4] and capacitive transimpedance amplifiers, low input capacitance may not be required. However, the availability of large output resistances is important to the operation of these circuits. Specifically, increased output resistance translates to higher gain in amplifiers and lower error in current copier circuits.

In this brief, an alternate cascode circuit consisting of a double gate MOSFET called self-cascoding FET (SCFET) is presented. The SCFET features increased output resistance compared to a single FET biased under similar operating conditions and is intended for use in applications where low-power and small real-estate are important. The cell design is simple, and unlike existing cascode

circuits, does not require additional real-estate and power for its operation. The brief is organized as follows. First, the operation of SCFET is described. Then the results from SCFET test-chips are presented and discussed, and the enhancements in performance of amplifier and current memory circuits by the use of SCFET are demonstrated.

Double gate structures have previously been used for enhancement of analog circuit performance. One such circuit is a twin gate SOI MOSFET, which can also be used in MOSFET circuits operating at cryogenic temperatures [5]. However, the SCFET and the twin gate SOI MOSFET are functionally different. The increase in the output resistance of a SOI MOSFET is the result of the suppression of the kink and the parasitic bipolar effects that are important in SOI structures and cryogenic MOSFETs, whereas the SCFET is essentially a cascode circuit implemented with conventional CMOS technology.

II. OPERATION OF A SCFET

An SCFET consists of two appropriately scaled transistors (M_m, M_c), with both their gates tied to a common input voltage, as shown in fig. 2. The resultant structure is very similar to a conventional cascode circuit shown in fig. 1, with the exception that the cascode transistor (M_c) does not require additional external bias. The circuit operates in the self-cascoding mode only when M_c is biased in weak inversion, (M_m may operate in weak or moderate inversion). This is made possible by two reasons. First, in weak or moderate inversion, for the main transistor (M_m) to operate in saturation, its drain-to-source bias is required to be larger than only a few times the thermal voltage, $V_T = kT/q$. Since the thermal voltage at room temperature is only 26 mV, M_m can operate in saturation only with a few tenths of a volt. Secondly, when a MOSFET is biased in weak inversion, it does not require a threshold drop across its gate and source for channel conduction. These two factors allow both the transistors to remain approximately in saturation if M_c can be biased in weak or moderate inversion.

When the two transistors are biased in saturation, the circuit operates essentially as a conventional cascode circuit, with the increase in output resistance being given by g_{m2}/g_{ds2}, where g_{m2} is the transconductance of M_c, and g_{ds2} is its output impedance. On the other hand, when the circuit is biased in strong inversion, the gate to source voltage of M_c is greater than a threshold drop, causing the main transistor to operate as a switch (low output resistance), and the net output resistance is lowered, being equal to the output resistance of M_c.

The W/L ratios of the two transistors are scaled in order to ensure that both the transistors are biased in or near saturation, so that a large output resistance is obtained. For typical values of sub-threshold range, the main transistor (M_m) is biased near saturation. Therefore, it is desirable to keep the gate-to-source voltage drop in the cascoding transistor as small as possible. This can be achieved by making the W/L ratio of M_c to be larger than the W/L ratio of M_m. For a SCFET circuit this ratio

$R=(W/L)_c/(W/L)_m$ is the main design parameter. The SCFET circuit was simulated in PSPICE for different values of R. The results of the simulation, shown in fig. 2, exhibit the expected dependence of the output resistance on R. The output resistance was found to increase with an increase in R, the increase tailing off for $R > 6$.

III. RESULTS and DISCUSSION

SCFET circuits were fabricated using commercially available standard 2 μm CMOS process through MOSIS. The test chip contained differential amplifiers and current memory circuits, constructed with SCFETs and regular MOSFETs of similar dimensions, as well as test structures to measure the d.c. characteristics and noise performance of the SCFET and a regular MOSFET of same dimensions. The MOSFET dimensions were W/L=3/10 μm. The dimensions of the main transistor of the SCFET were chosen to be W/L=3/8 μm, and that of the cascode transistor was W/L=3/2 μm.

The d.c. characteristics of the SCFET and the MOSFET were measured using a HP 4145 dynamic signal analyzer. In order to carry out meaningful comparison, both the devices were biased in weak inversion at a nominal drain current of 225 nA. The results of the test are shown in fig. 3. It can be easily seen from the figure that the SCFET exhibits lower output conductance compared to an ordinary MOSFET. From fig. 3, the output conductance of the SCFET was calculated to be 3.675 nA/V at a drain current of 225 nA, and is 22.5 times smaller than the MOSFET of same dimension. The calculated output conductance is however larger than that predicted by PSPICE simulation, because of the inaccuracy of PSPICE model in weak inversion. The increase in the output resistance is less than expected because for the channel dimensions chosen, the main transistor is biased at the edge of saturation, causing its output resistance to be lower than expected. The output resistance was also found to be dependent on the channel lengths and widths of the two transistors. Further work is under way to optimize the channel lengths and widths of the two transistors for largest output resistance and minimum real-estate.

A similar experiment was carried out using n-channel SCFETs of same dimensions as the p-channel devices. The output conductance of the n-channel SCFET biased at 210 nA was measured to be 3.162 nA/V, and is 18 times smaller than the ordinary n-channel MOSFET.

The SCFET circuits were used to construct CMOS differential amplifiers. The single stage differential amplifier was biased at a relatively large current of 500 nA. Even at these increased currents, the low frequency amplifier gain was found to be 56.75 dB, which is twelve times greater than that of an amplifier constructed with ordinary MOSFETs and biased at same current level. Thus, the output resistance of the SCFET differential amplifier is increased twelve times, which corroborates the data on the measured output resistance of a p-channel SCFET. The increase in SCFET output

resistance is more pronounced at smaller current levels, as the transistors are biased deeper in weak inversion. For a 1 nA nominal bias on a SCFET differential amplifier, gains larger than 120 dB has been achieved from a single stage amplifier. Therefore, an SCFET is ideally suited for use in ultra low-power circuits required in large format analog VLSI.

The SCFET circuits were also used in current copier cells, in which the gate voltage corresponding to the drain current flowing through a MOSFET is stored on its gate. The finite output resistance of the cell causes an error between the current memorized and the current read out due to a change in the output voltage during readout. The current copier cells built with SCFET circuits were operated with less than 0.1% absolute error, indicating that the increase in the output resistance has been sufficient to render the error due to finite output resistance insignificantly small.

The noise in the SCFETs and the MOSFETs were measured using a HP 3541 dynamic signal analyzer. No difference in the noise power spectrum was noticed between a SCFET and a MOSFET of same dimensions.

IV. CONCLUSION

A new self-cascoding FET circuit is presented. Compared to a single transistor, the SCFET adds minimal area to the unit cell and does not require extra power dissipation or additional bias supply lines for operation. In the SCFET device under test, the output resistance was found to be more than 20 times larger compared to that of a MOSFET of same dimensions, operating under similar bias conditions. The SCFETs circuits have been employed in a variety of situations -- from increasing the gain in amplifiers to enhancing the performance of current copiers. The channel lengths and widths of the two transistors can be optimized for the largest increase in the output resistance.

V. ACKNOWLEDGMENTS

The authors wish to thank T. Cunningham of Jet Propulsion Laboratory for helping in testing the circuits and Robert Nixon of Jet Propulsion Laboratory for facilitating the fabrication of the test chips.

The research described in this paper was carried out at the Center for Space Microelectronics Technology, Jet Propulsion Laboratory, California Institute of Technology, and was sponsored by the Defense Advanced Research Projects Agency and the National Aeronautics and Space Administration.

VI. REFERENCE

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FIGURE CAPTIONS

Fig. 1a Schematic of a cascode circuit.

Fig. 1b Schematic of a SCFET circuit.

Fig. 2 Simulated output resistance of p-SCFET (normalized to the output resistance of a p-FET of same dimensions) vs. the ratio between the main transistor length (L_m) to cascode transistor length (L_c).

Fig. 3 Measured I-V characteristics of a p-SCFET and a p-FET of same dimensions (W/L=3/10).

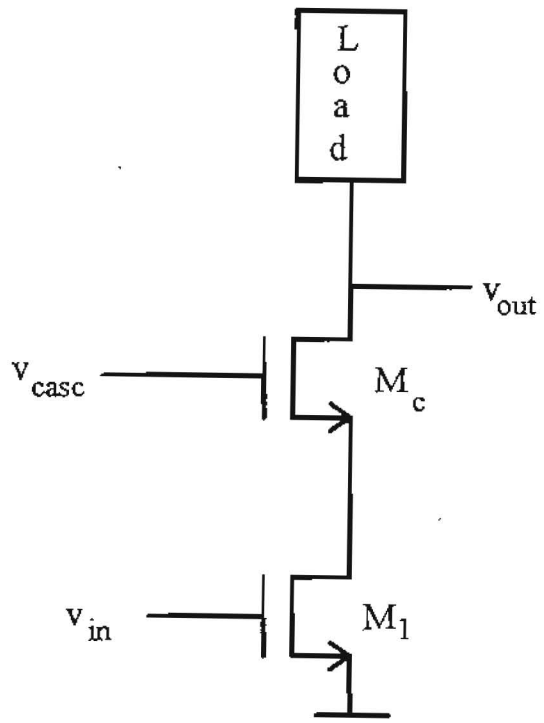


Fig . 1a Schematic of a cascode circuit.

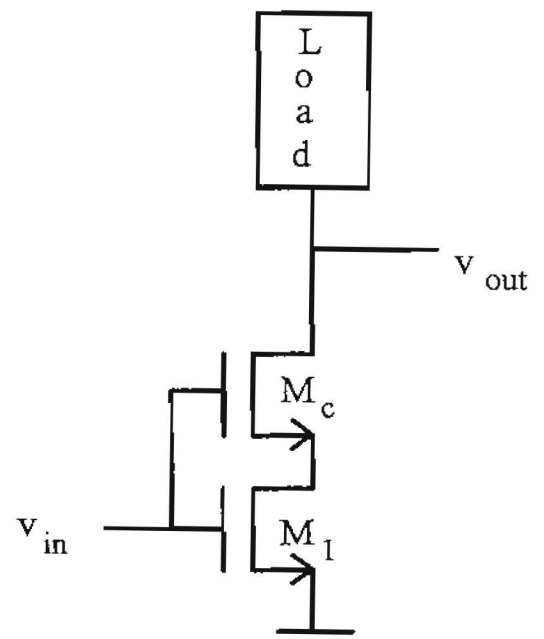
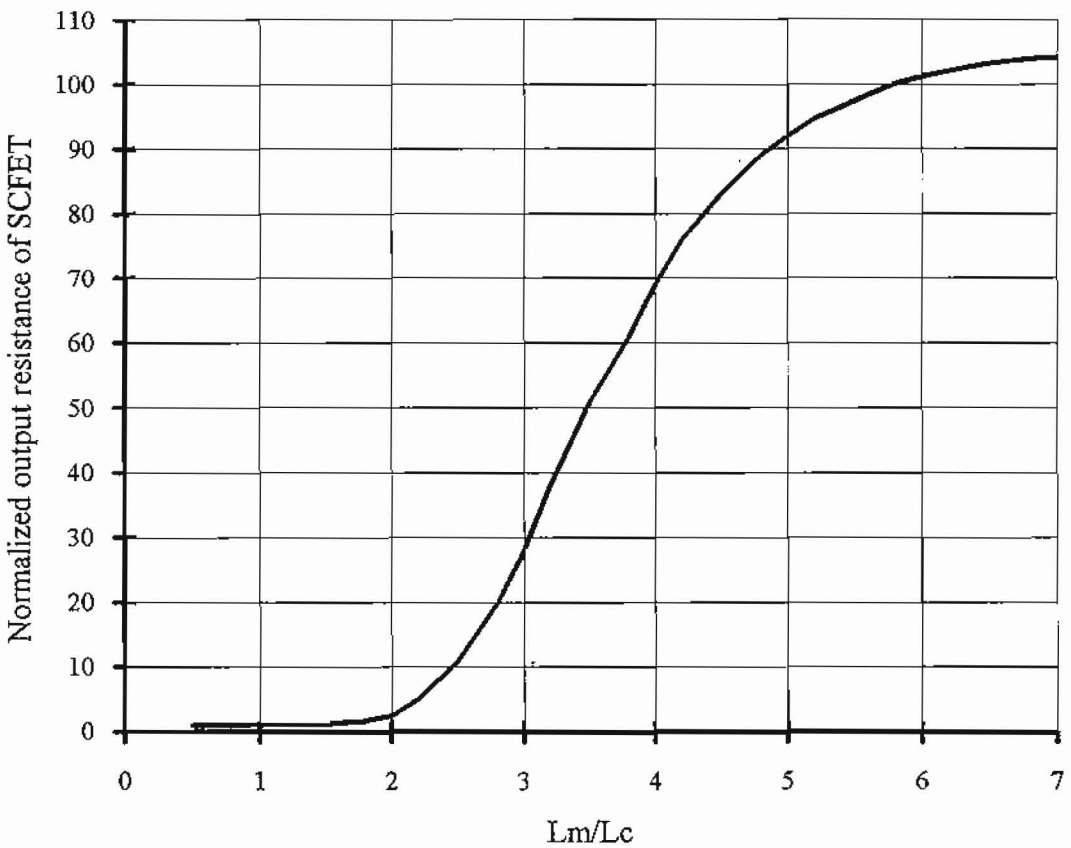


Fig . 1b Schematic of a SCFET circuit.



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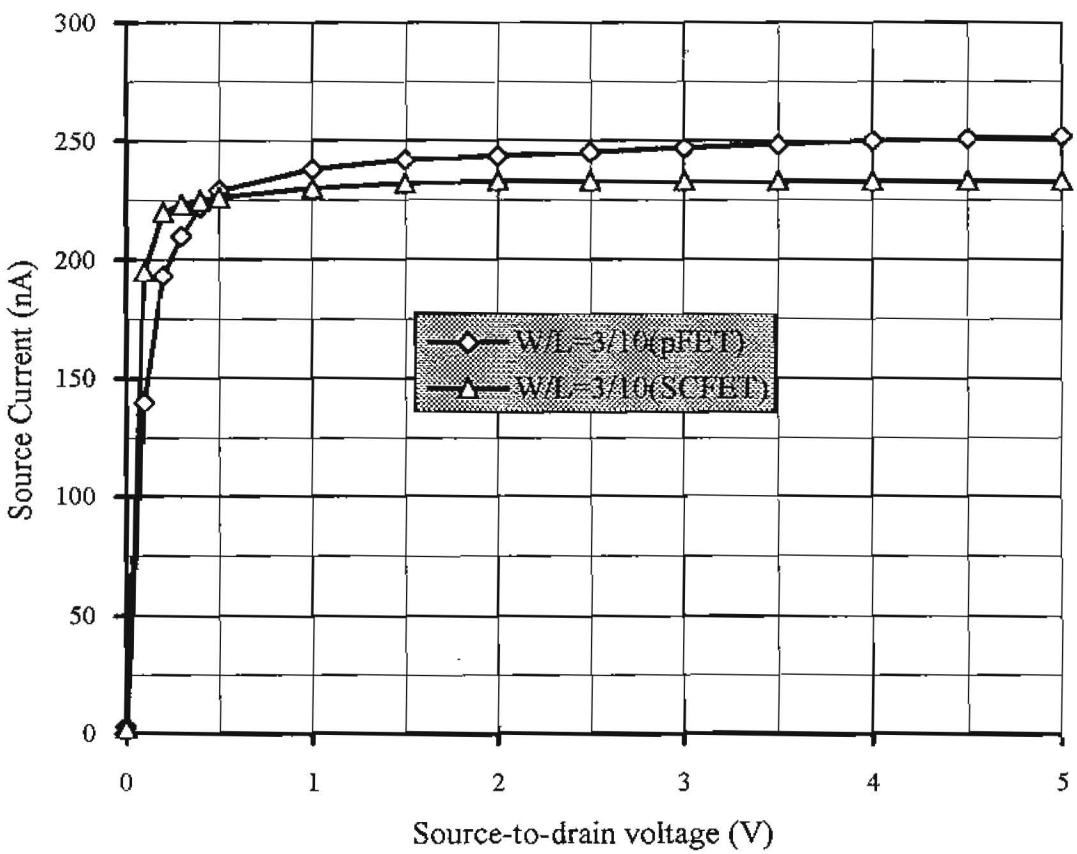

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