

# ECE385

## DIGITAL SYSTEMS LABORATORY

### Instantiation Megafunctions (IP modules)

Megafunctions are what Intel calls their reconfigurable Intellectual Property (IP) modules. These modules are pre-designed FPGA components (such as interfaces, memory controllers, computation accelerators, etc.) which can be licensed from Intel or third parties and instantiated into an FPGA design. Typically, these can be configured graphically through a GUI, or through code via SystemVerilog parameters. For Experiment 5, you will configure an on-chip memory Megafunction for use as your main memory.

To start, open your existing Experiment 5 project that you have created. You can then expand the IP Catalog panel (by default located on the right side). Select RAM: 1-PORT and name your “IP Variant” as *ram*.

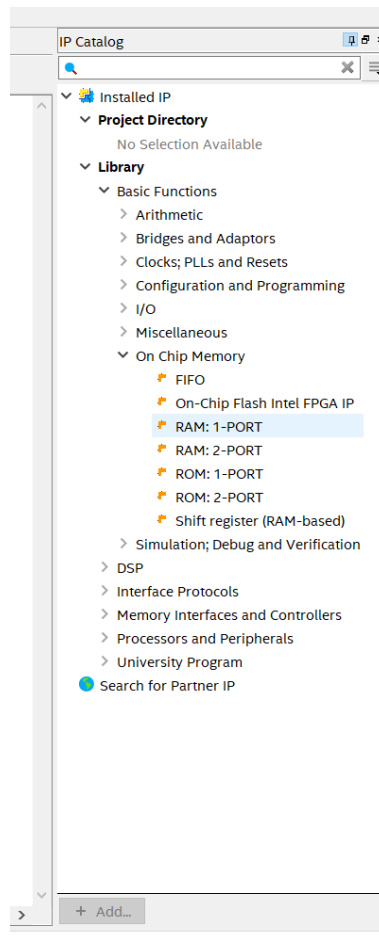


Figure 1 IP Catalog

## IMF.2

You will then be presented with the following GUI tool. Populate the following according to the screenshots and click Finish.

The screenshots show the MegaWizard Plug-In Manager GUI for the RAM: 1-PORT wizard. The wizard is divided into four pages:

- Page 1 of 6:** Shows the initial configuration. The device family is MAX 10. The block type is M9K. The width is 16 bits, and the depth is 1024 words. The clocking method is Single clock.
- Page 2 of 6:** Shows the 'Which ports should be registered?' section. The 'data' and 'wren' input ports are checked. The 'address' input port is checked. The 'q' output port is checked. The 'rden' read enable signal is checked.
- Page 3 of 6:** Shows the 'Single Port Read-During-Write Option' section. The 'What should the q output be when reading from a memory location being written to?' is set to 'Don't Care'.
- Page 4 of 6:** Shows the 'Do you want to specify the initial content of the memory?' section. The 'No, leave it blank' option is selected.

Although it is possible to populate the memory contents from the Megafunction GUI, we provide a module called `instantiatiram.sv` which initializes the on-chip memory from the FPGA logic on reset. This is so the memory contents can be restored during a reset, rather than requiring a full FPGA reprogramming to restore.