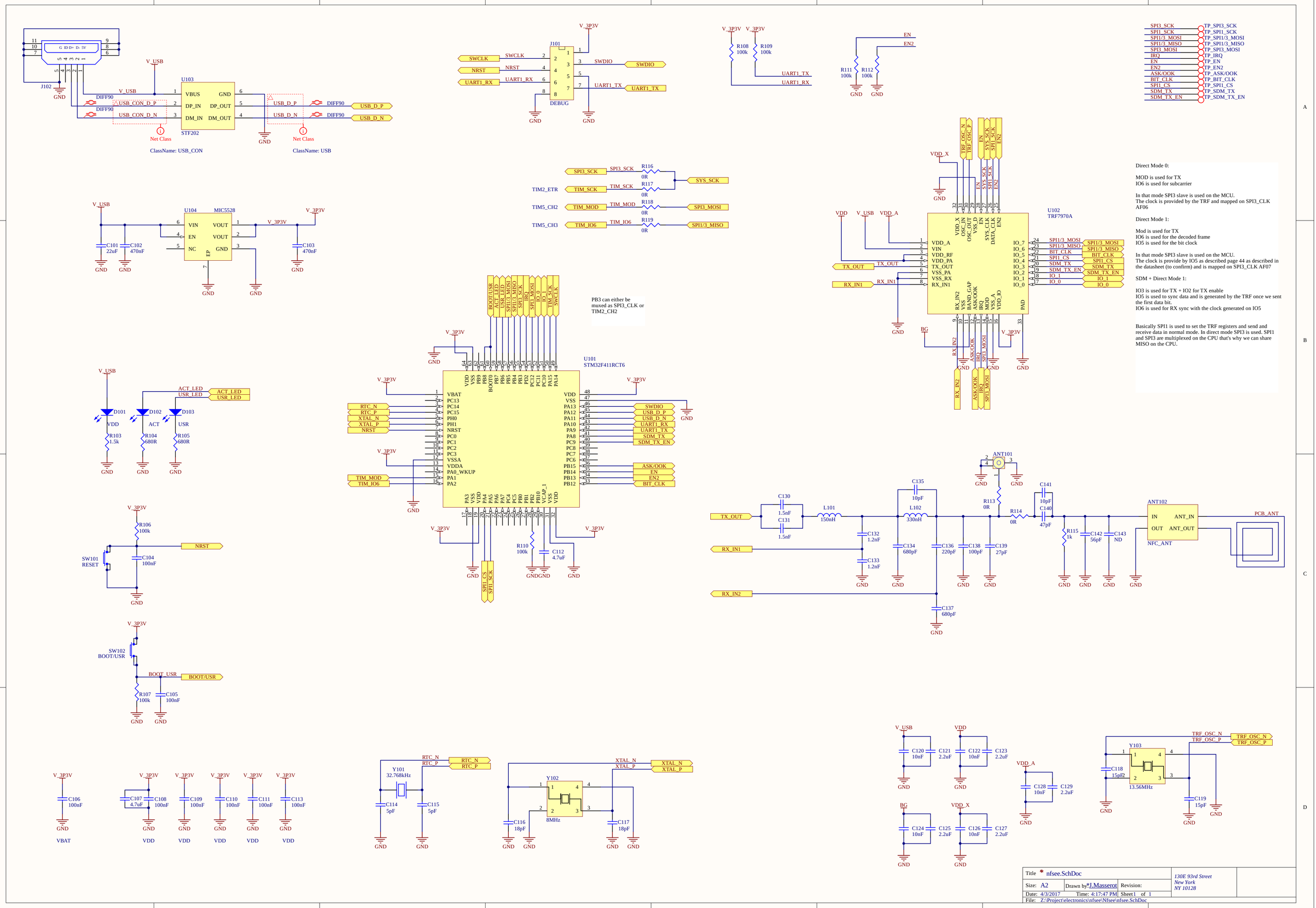
J102
U103
STF202
V_USB
DIFF90
USB_CON_D_P
USB_CON_D_N
USB_D_P
USB_D_N
Net Class
ClassName: USB_CON
ClassName: USB
J101
DEBUG
SWCLK
NRST
UART1_RX
SWDIO
UART1_TX
V_3P3V
R108 100k
R109 100k
EN
EN2
R111 100k
R112 100k
TP_SPI3_SCK
TP_SPI1_SCK
TP_SPI1/3_MOSI
TP_SPI1/3_MISO
TP_SPI3_MOSI
TP_IRQ
TP_EN
TP_EN2
TP_ASK/OOK
TP_BIT_CLK
TP_SPI1_CS
TP_SDM_TX
TP_SDM_TX_EN
U104
MIC5528
C101 22uF
C102 470nF
C103 470nF
SPI3_SCK
TIM2_ETR
TIM_SCK
TIM5_CH2
TIM_MOD
TIM5_CH3
TIM_IO6
R116 0R
R117 0R
R118 0R
R119 0R
SYS_SCK
SPI3_MOSI
SPI1/3_MISO
U102
TRF7970A
VDD_X
VDD
VDD_A
TX_OUT
RX_IN1
RX_IN2
BG
IO_7
IO_6
IO_5
IO_4
IO_3
IO_2
IO_1
IO_0
BIT_CLK
SPI1_CS
SDM_TX
SDM_TX_EN
Direct Mode 0:
MOD is used for TX
IO6 is used for subcarrier
In that mode SPI3 slave is used on the MCU.
The clock is provided by the TRF and mapped on SPI3_CLK AF06
Direct Mode 1:
Mod is used for TX
IO6 is used for the decoded frame
IO5 is used for the bit clock
In that mode SPI3 slave is used on the MCU.
The clock is provide by IO5 as described page 44 as described in the datasheet (to confirm) and is mapped on SPI3_CLK AF07
SDM + Direct Mode 1:
IO3 is used for TX + IO2 for TX enable
IO5 is used to sync data and is generated by the TRF once we sent the first data bit.
IO6 is used for RX sync with the clock generated on IO5
Basically SPI1 is used to set the TRF registers and send and receive data in normal mode. In direct mode SPI3 is used. SPI1 and SPI3 are multiplexed on the CPU that's why we can share MISO on the CPU.
PB3 can either be muxed as SPI3_CLK or TIM2_CH2
U101
STM32F411RCT6
BOOT/USR
ACT_LED
USR_LED
SPI1/3_MOSI
SPI1/3_MISO
SPI3_SCK
IRQ
IO_1
IO_0
TIM_SCK
SWCLK
RTC_N
RTC_P
XTAL_N
XTAL_P
ASK/OOK
BIT_CLK
SPI1_CS
SPI1_SCK
D101
D102
D103
VDD
ACT
USR
R103 1.5k
R104 680R
R105 680R
R106 100k
SW101 RESET
C104 100nF
SW102 BOOT/USR
BOOT_USR
R107 100k
C105 100nF
R110 100k
C112 4.7uF
ANT101
C130 1.5nF
C131 1.5nF
L101 150nH
C132 1.2nF
C133 1.2nF
C135 10pF
L102 330nH
C134 680pF
C136 220pF
C137 680pF
C138 100pF
C139 27pF
R113 0R
R114 0R
C141 10pF
C140 47pF
R115 1k
C142 56pF
C143 ND
ANT102
IN
OUT
ANT_IN
ANT_OUT
NFC_ANT
PCB_ANT
C106 100nF
C107 4.7uF
C108 100nF
C109 100nF
C110 100nF
C111 100nF
C113 100nF
VBAT
Y101 32.768kHz
C114 5pF
C115 5pF
Y102 8MHz
C116 18pF
C117 18pF
C120 10nF
C121 2.2uF
C122 10nF
C123 2.2uF
C124 10nF
C125 2.2uF
C126 10nF
C127 2.2uF
C128 10nF
C129 2.2uF
Y103 13.56MHz
C118 15pF
C119 15pF
Title * nfsee.SchDoc
Size: A2
Drawn by: J.Masserot
Revision:
Date: 4/3/2017
Time: 4:17:47 PM
Sheet 1 of 1
File: Z:\Project\electronics\nfsee\Nfsee\nfsee.SchDoc
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