HDL Week 2

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Self Test Chapter 3

```
ARCHITECTURE x OF gate_network IS
BEGIN
    -- concurrent assignment statements operate in parallel
    -- D(1) selects bit 1 of standard logic vector D
    X <= A AND NOT(B OR C) AND (D(1) XOR D(2));
    -- Process must declare a sensitivity list
    -- Sensitivity list includes all signals which can change the outputs
    PROCESS (A,B,C,D)
    BEGIN
        -- Statements inside a process execute in sequential order
        Y <= A AND NOT(B OR C) AND (D(1) XOR D(2));
    END PROCESS;
END x;
```

1. *Is this a structural, behavioral, or RTL description?*

   This is a RTL description cause the circuit is described in the input/output relationship of signals.

2. *What is the purpose of a generic?*

   The purpose of generics is to create flexible components.

3. *What is the purpose of a configuration statement?*

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4. *In our tutorial there is an adder, is this a structural, behavioral, or RTL description?*

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5. *Draw the schematics of a full adder and make a structural VHDL description*

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Self Test Chapter 4