HDL Week 2

Jochem Arends (485637)

Self Test Chapter 3

```
architecture arch of gate_network is
begin
-- concurrent assignment statements operate in parallel
-- d(1) selects bit 1 of standard logic vector D
    x <= a and not(b or c) and (d(1) xor d(2));
-- srocess must declare a sensitivity list
-- sensitivity list includes all signals which can change the outputs
    process (a, b, c, d)
    begin
    -- statements inside a process execute in sequential order
        y <= a and not(b OR c) and (d(1) xor d(2));
    end process;
end arch;
```

1. *Is this a structural, behavioral, or RTL description?*

   This is a RTL description cause the circuit is described in the relationship between signals.

2. *What is the purpose of a generic?*

   The purpose of generics is to create flexible components.

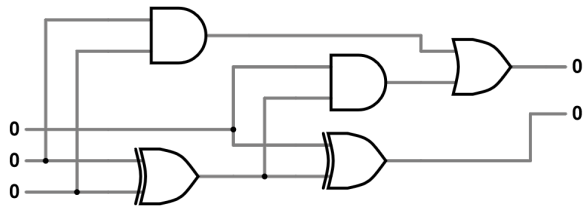
3. *What is the purpose of a configuration statement?*

   TODO

4. *In our tutorial there is an adder, is this a structural, behavioral, or RTL description?*

   The adder from the tutorial uses a RTL description because the behaviour is described in terms of relationships between signals.

5. *Draw the schematics of a full adder and make a structural VHDL description*



Exercises Chapter 3

1. *Simulate in Quartus the behavioral VHDL of a 3-bit adder.*

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;

entity adder is
port (
    a, b:  in  std_logic_vector(2 downto 0);
    sum:   out std_logic_vector(2 downto 0);
    carry: out std_logic
);
end adder;

architecture arch of adder is
begin
    process (a, b)
    -- intermediate carry
    variable int_carry: std_logic;
    begin
        -- reset carry
        int_carry := '0';

        for i in 0 to a'length-1 loop
            -- set sum bit
            if (a(i) = '0' and b(i) = '0' and int_carry = '1')
            or (a(i) = '0' and b(i) = '1' and int_carry = '0')
            or (a(i) = '1' and b(i) = '0' and int_carry = '0')
            or (a(i) = '1' and b(i) = '1' and int_carry = '1') then
                sum(i) <= '1';
            else
                sum(i) <= '0';
            end if;

            -- determine carry out
            if (a(i) = '0' and b(i) = '1' and int_carry = '1')
            or (a(i) = '1' and b(i) = '1' and int_carry = '0')
            or (a(i) = '1' and b(i) = '0' and int_carry = '1')
            or (a(i) = '1' and b(i) = '1' and int_carry = '1') then
                int_carry := '1';
            else
                int_carry := '0';
            end if;
        end loop;

        -- set final carry out
        carry <= int_carry;
    end process;
end arch;
```

1. *Implement the 3-bit adder on the MAX 10 board.*

I have no access to such board at the moment.

2. *Simulate in Quartus a structural description of a half adder.*

   I have pasted an image of the simulation at the end of this document.

Self Test Chapter 4

```
architecture arch of gate_network is
begin
    x <= a and not(b or c) and (d(1) xor d(2));
    y <= (d(1) xor d(2));
end
```

1. *Which value,* `x` *or* `y` *is first evaluated?*

   They are executed simultaneously since signal assignment is concurrent.

2. *Give the behavioral description of a 2 to 4 decoder.*

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;

entity decoder is
port (
    a: in  std_logic_vector(1 downto 0);
    d: out std_logic_vector(3 downto 0)
);
end decoder;

architecture arch of decoder is
begin
    process (a)
    begin
        case a is
            when "00" => d <= "0001";
            when "01" => d <= "0010";
            when "10" => d <= "0100";
            when "11" => d <= "1000";
        end case;
    end process;
end arch;
```

Exercises Chapter 4

1. *Simulate the behavioral description of a 2 to 4 decoder in Quartus.*

   I have pasted an image of the simulation at the end of this document.

2. *Implement the 2 to 4 decoder on the Danjel board*

   I have no access to such board at the moment.

Self Test Chapter 5

1. *What does a concurrent assignment mean?*

   Concurrent assignment means that the assignment is happening at the same time to something else.

Exercises Chapter 5

1. *Simulate the 7 segments display model.*

   TODO

2. *Design a 4-bit even parity checker (structured) and simulate it.*

   The source code is put below and the simulation results can be found at the end of this document.

3. *Implement the parity checker and the 7 segm display on the max 10 board*

   I have no access to such board at the moment.

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;

entity parity_checker is
port (
    data:   in  std_logic_vector(3 downto 0);
    output: out std_logic
);
end parity_checker;

architecture arch of parity_checker is
    component xor_gate is
    port (
        a, b:   in  std_logic;
        output: out std_logic
    );
    end component;
    -- intermediate results
    signal a, b: std_logic;
begin
    u1: xor_gate port map (data(0), data(1), a);
    u2: xor_gate port map (data(2), a, b);
    u3: xor_gate port map (data(3), b, output);
end arch;
```

Simulation Results

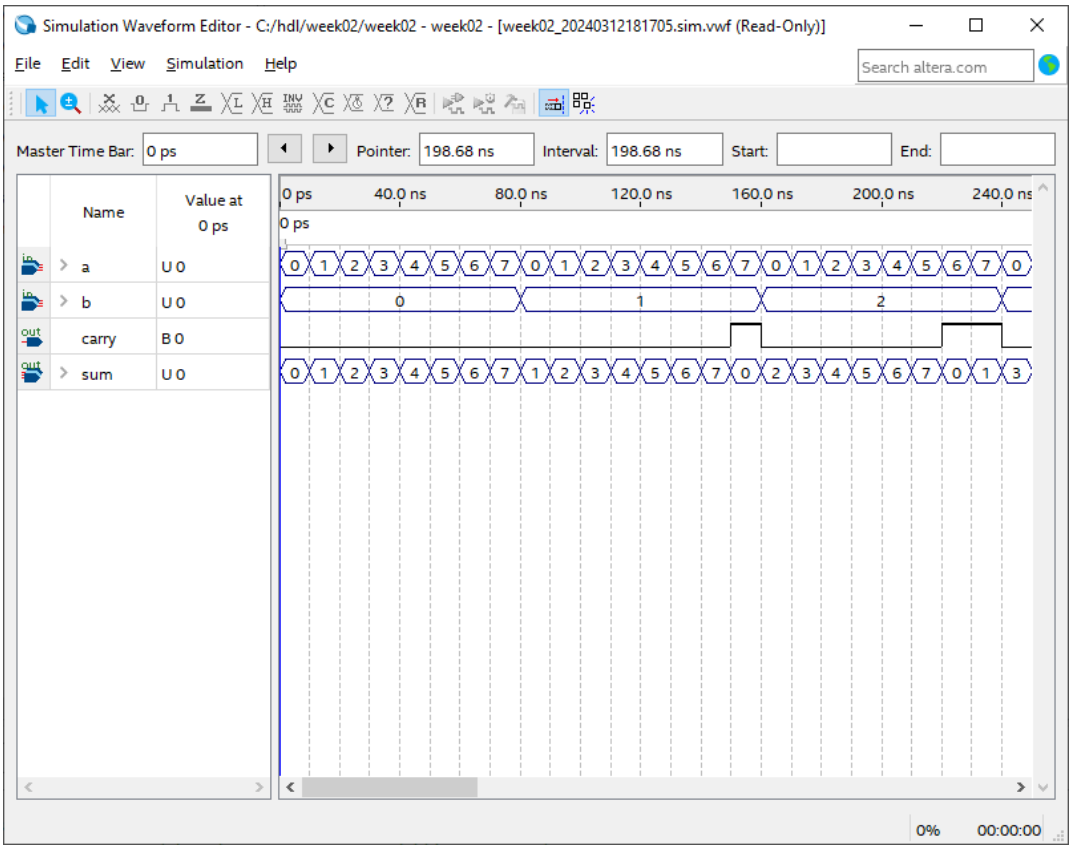


Figure 1. Simulation of Behavioral Half Adder

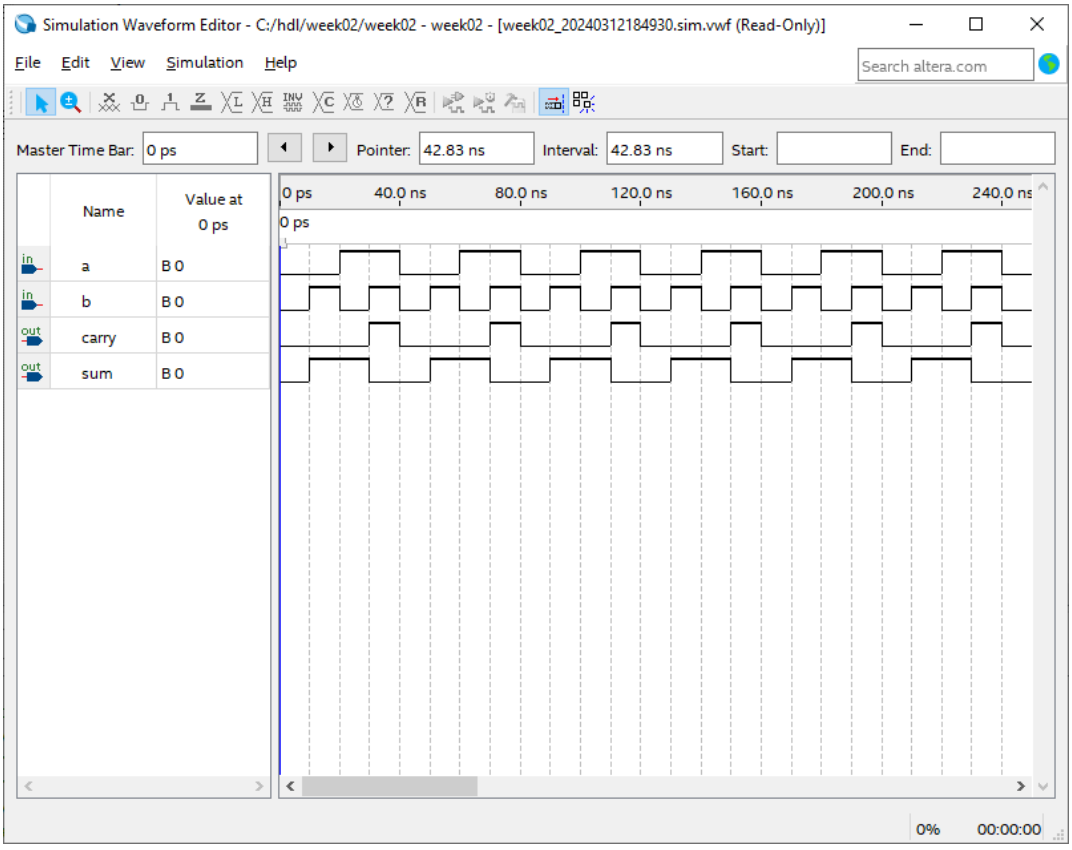


Figure 2. Simulation of Structural Half Adder

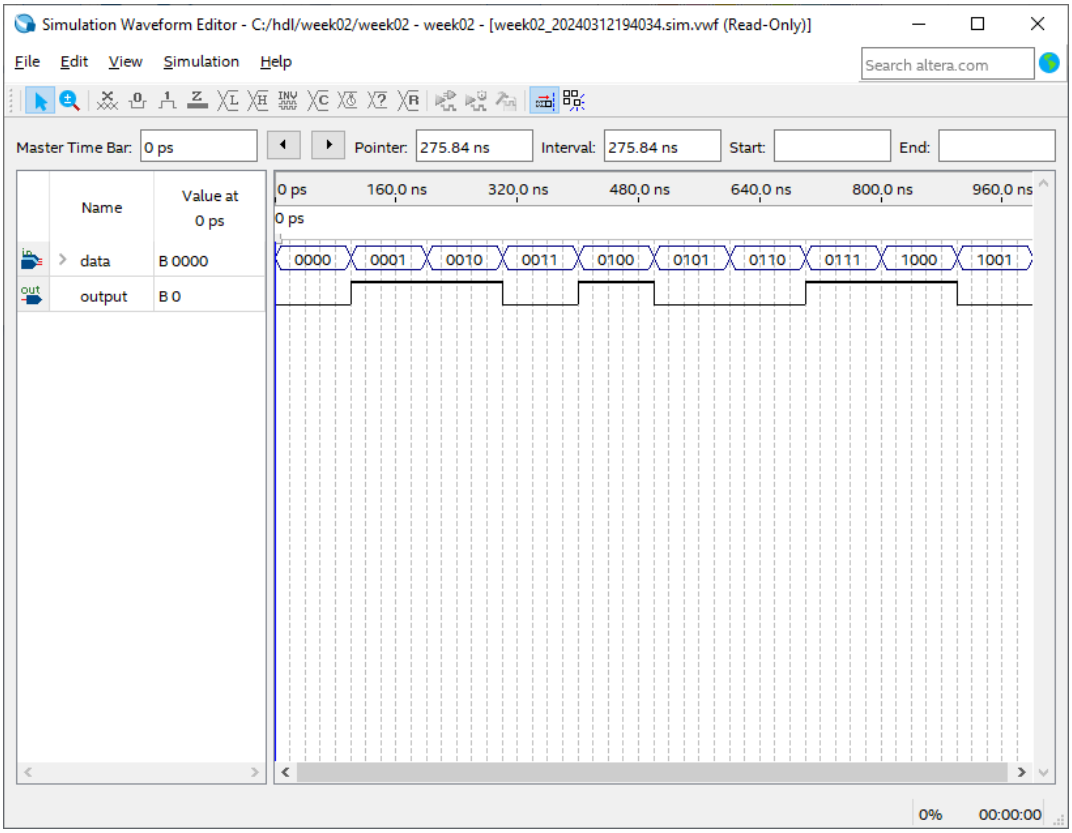


Figure 3. Simulation of Even Parity Checker