LMX2572 6.4-GHz Low power wideband RF synthesizer with phase synchronization and JESD204B support

1 Features

- Output frequency: 12.5 MHz to 6.4 GHz
- Low power consumption: 75 mA at 3.3-V supply
- –106-dBc/Hz Phase noise at 100-kHz offset with 6.4-GHz carrier
- PLL figure of merit: –232 dBc/Hz
- PLL normalized 1/f noise: –123.5 dBc/Hz
- 32-Bit Fractional-N divider
- Remove integer boundary spurs with programmable input multiplier
- Synchronization of output phase across multiple devices
- Support for JESD204B SYSREF with programmable delay
- Support for ramp and chirp functions
- Support for FSK direct digital modulation
- Two programmable output power level differential outputs
- Fast VCO calibration speed: < 20 µs
- Single 3-V to 3.5-V power supply

2 Applications

- Test and measurement equipment
- Digital 2-way radios
- Low power radio communication systems
- Satellite communication
- Wireless microphones
- Propriety wireless connectivity
- MIMO
- RADAR
- High-speed data converter clocking

3 Description

The LMX2572 is a low-power, high-performance wideband synthesizer that can generate any frequency from 12.5 MHz to 6.4 GHz without using an internal doubler. The PLL delivers excellent performance while consuming just 75 mA from a single 3.3-V supply.

For applications like digital mobile radio (DMR) and wireless microphones, the LMX2572 supports FSK modulation. Discrete level FSK and pulse-shaping FSK are supported. Direct digital FSK modulation is achievable through programming or pins.

The LMX2572 allows users to synchronize the output of multiple devices and also enables applications that need deterministic delay between input and output. The LMX2572 provides an option to adjust the phase with fine granularity to account for delay mismatch on the board or within devices. A frequency ramp generator can synthesize up to two segments of ramp in an automatic ramp generation option or a manual option for maximum flexibility. The fast calibration algorithm allows the user to change frequencies faster than 20 µs. The LMX2572 also supports generating or repeating SYSREF (compliant to JESD204B standard) making it an ideal low-power, low-noise clock source for clocking high-speed data converters. Fine delay adjustment is provided in this configuration to account for delay differences of board traces.

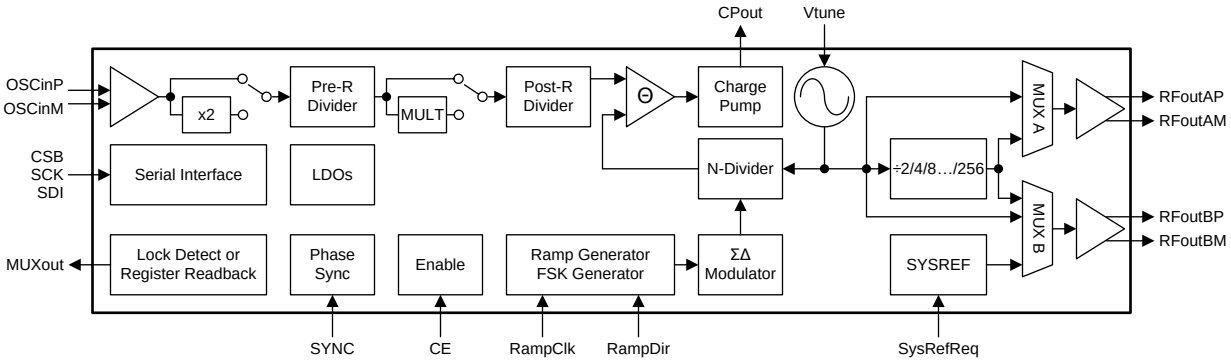
The LMX2572 integrates LDOs from a single 3.3-V supply, thus eliminating the need for onboard low-noise LDOs.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMX2572	VQFN (40)	6.00 mm × 6.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Functional Block Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (October 2017) to Revision B	Page

- Changed RampDir pin description from: …ramp size selection… to: …ramp segment selection… ... 4
- Changed RFoutAM pin description from: High impedance… to: Low impedance… ... 4
- Changed RFoutAP pin description from: High impedance… to: Low impedance… ... 4
- Changed RFoutBM pin description from: High impedance… to: Low impedance… ... 4
- Changed RFoutBP pin description from: High impedance… to: Low impedance… ... 4
- Changed VbiasVCO pin decoupling capacitor requirement ... 5
- Changed VbiasVCO2 pin decoupling capacitor requirement ... 5
- Changed VccMASH pin decoupling capacitor requirement ... 5
- Changed VccVCO pin decoupling capacitor requirement ... 5
- Changed VccVCO2 pin decoupling capacitor requirement ... 5
- Changed VregVCO pin decoupling capacitor requirement ... 5
- Added Vtune pin shunt capacitor requirement ... 5
- Changed V_{OH} and V_{OL} data in Electrical Characteristics ... 8
- Changed SCK to CSB low time symbol ... 8
- Changed Figure 28 ... 13
- Added charge pump gain table ... 16
- Deleted sentence 'When the device comes out of the powered down state, either by resuming the POWERDOWN bit to zero or by pulling back CE pin HIGH (if it was powered down by CE pin), it is required that register R0 with FCAL_EN = 1 be programmed again to re-calibrate the device.' from the *Powerdown* section ... 18
- Added sentence 'The wake-up time for the device to come out of the powered state is adjustable.' to the *Powerdown* section ... 18
- Changed *Programming Sequence* step from: Wait 100 µs… to: Wait 500 µs… ... 21
- Changed R6 initial programming from: No to: Depends ... 21
- Changed R52 initial programming from: No to: Yes ... 22

Revision History (continued)

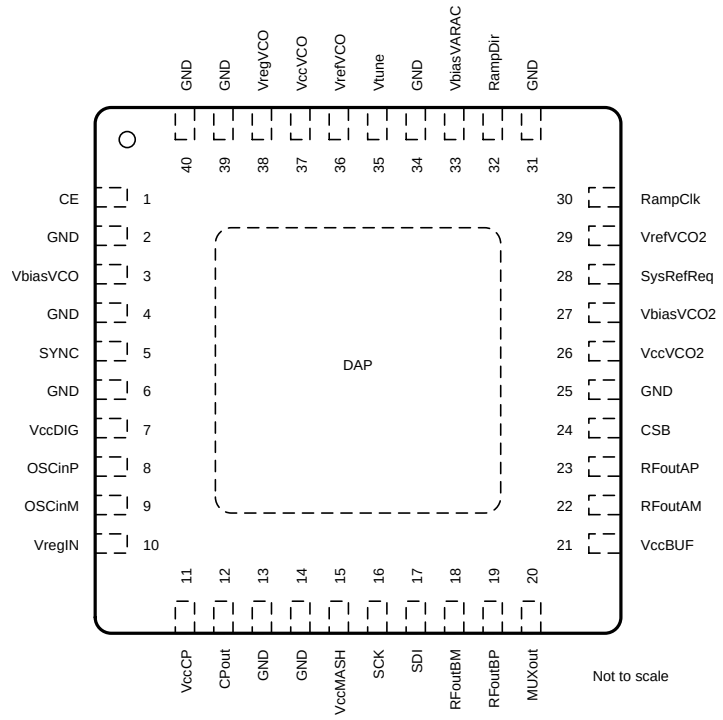
- Added LDO_DLY in register R6 24
- Changed R15[0] from: 1 to: 0 24
- Changed R15 POR value 24
- Changed R20[14] from: 0 to: 1 24
- Changed R52[0] from: 0 to: 1 25
- Changed register R0, FCAL_HPFD_ADJ value definition 28
- Added sentence 'Writing 0 to this field is prohibited.' to FCAL_EN bit description 28
- Added LDO_DLY in register R6 30
- Changed MULT bit description from: …30 MHz… to: …40 MHz… 32
- Changed register R14 default value 33
- Changed R15[0] from: 1 to: 0 33
- Changed register R20 default value 35
- Deleted VCO_SEL_STRT_EN = 1 in Register 20 Field Descriptions 35
- Changed register R46, OUTB_MUX value definition 42
- Changed register R52 programming value 44
- Changed register R58, INPIN_LVL value definition 45
- Changed from: MASH reset count… to: This register… 48
- Changed VCO_CAPCTRL_STRT reset value 51
- Changed register R114, FSK_MODE_SEL value definition 61
- Changed Figure 165 and Figure 166 65
- Changed setup procedure step from: …divide N… to: …set N = N' / 2… 68
- Changed RAMP_MODE = 1 to RAMP_MANUAL = 1 in the *Manual Ramping Mode* section 69
- Changed RAMP_THRESH value suggestion 69
- Deleted paragraph 'For ramping that are not calibration free, the ramp waveform is more like a staircase ramp. For all automatic ramping waveforms, be aware that there is a very small phase disturbance as the VCO crosses over the integer boundary, so one might consider using the input Multiplier to avoid these or timing the VCO calibration at integer boundaries.' from the *Automatic Ramping Mode* section 70
- Changed ADR_HOLD = 1 to ADD_HOLD = 1 74
- Added an application section for external loop filter 75
- Added an application section for powerup wake up time 75

Changes from Original (August 2017) to Revision A **Page**

- Changed Advance Information to Production Data Release 1

5 Pin Configuration and Functions

RHA Package
40-Pin VQFN
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
CE	1	Input	Chip enable. High impedance CMOS input. 1.8-V to 3.3-V logic. Active HIGH powers on the device.
CPout	12	Output	Charge pump output. Place C1 of loop filter close to this pin.
CSB	24	Input	SPI latch. High impedance CMOS input. 1.8-V to 3.3-V logic.
DAP	—	Ground	RF ground.
GND	2, 4, 25, 31, 34, 39	Ground	VCO ground.
	6, 14, 40	Ground	Digital ground.
	13	Ground	Charge pump ground.
MUXout	20	Output	Multiplexed output pin. Configurable between lock detect and register readback.
OSCinM	9	Input	Reference input clock (–). High impedance self-biasing pin. Requires AC-coupling.
OSCinP	8	Input	Reference input clock (+). High impedance self-biasing pin. Requires AC-coupling.
RampClk	30	Input	Ramp trigger in automatic ramping mode or ramp clock in manual ramping mode. High impedance CMOS input. 1.8-V to 3.3-V logic.
RampDir	32	Input	Ramp trigger in automatic ramping mode or ramp segment selection in manual ramping mode. High impedance CMOS input. 1.8-V to 3.3-V logic.
RFoutAM	22	Output	Differential output A (–). Low impedance output. Requires AC-coupling.
RFoutAP	23	Output	Differential output A (+). Low impedance output. Requires AC-coupling.
RFoutBM	18	Output	Differential output B (–). Low impedance output. Requires AC-coupling. Configurable between RF output or SYSREF output.
RFoutBP	19	Output	Differential output B (+). Low impedance output. Requires AC-coupling. Configurable between RF output or SYSREF output.

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
SCK	16	Input	SPI clock. High impedance CMOS input. 1.8-V to 3.3-V logic.
SDI	17	Input	SPI data. High impedance CMOS input. 1.8-V to 3.3-V logic.
SYNC	5	Input	Phase synchronization trigger. Configurable to accept CMOS input (1.8-V to 3.3-V logic) or differential input.
SysRefReq	28	Input	SYSREF request for JESD204B support. Configurable to accept CMOS input (1.8-V to 3.3-V logic) or differential input.
VbiasVARAC	33	Bypass	VCO Varactor bias. Connect a 10-µF decoupling capacitor to VCO ground.
VbiasVCO	3	Bypass	VCO bias. Connect a 470-nF (X7R) decoupling capacitor to VCO ground as close to this pin as possible.
VbiasVCO2	27	Bypass	VCO bias. Connect a 100-nF (X7R) decoupling capacitor to VCO ground.
VccBUF	21	Supply	Supply for output buffers. Connect a 0.1-µF decoupling capacitor to RF ground.
VccCP	11	Supply	Supply for charge pump. Connect a 0.1-µF decoupling capacitor to charge pump ground.
VccDIG	7	Supply	Digital power supply. Connect a 0.1-µF decoupling capacitor to digital ground.
VccMASH	15	Supply	Digital power supply. Connect a 1-µF decoupling capacitor to digital ground.
VccVCO	37	Supply	Supply for VCO. Connect a 1-µF decoupling capacitor to VCO ground.
VccVCO2	26	Supply	Supply for VCO. Connect a 1-µF decoupling capacitor to VCO ground.
VrefVCO	36	Bypass	VCO supply reference. Connect a 10-µF decoupling capacitor to VCO ground.
VrefVCO2	29	Bypass	VCO supply reference. Connect a 10-µF decoupling capacitor to VCO ground.
VregIN	10	Bypass	Input reference path regulator output. Connect a 1-µF decoupling capacitor to RF ground as close to this pin as possible.
VregVCO	38	Bypass	VCO regulator node. Connect a 10-nF decoupling capacitor to VCO ground.
Vtune	35	Input	VCO tuning voltage input. Connect a 1.5-nF or more capacitor to VCO ground. See *External Loop Filter* for details.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Power supply voltage	–0.3	3.6	V
V_{IN}	Digital IO input voltage		V_{CC} + 0.3	V
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
T_A	Ambient temperature	–40		85	°C
T_J	Junction temperature			125	°C

6.4 Thermal Information

THERMAL METRIC(1)		LMX2572 RHA (VQFN) 40 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	25.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	14.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	8.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	7.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

3.0 V ≤ V_{CC} ≤ 3.5 V, –40°C ≤ T_A ≤ 85°C. Typical values are at V_{CC} = 3.3 V, 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER SUPPLY							
V_{CC}	Supply voltage			3	3.3	3.5	V
I_{CC}	Supply current	f_{PD} = 20 MHz; I_{CPout} = 1.25 mA	Direct VCO output(1)		75		mA
		f_{PD} = 100 MHz; I_{CPout} = 2.5 mA			79		
		f_{PD} = 20 MHz; I_{CPout} = 1.25 mA	Divided down output(2)		82		
		f_{PD} = 100 MHz; I_{CPout} = 2.5 mA			86		
$I_{CC}PD$	Power down current				2.5		
INPUT SIGNAL PATH							
f_{OSCin}	OSCin input frequency	OSC_2X = 0 (Doubler bypassed)		5		250	MHz
		OSC_2X = 1 (Doubler enabled)		5		125	
V_{OSCin}	OSCin input voltage(3)	Single-ended input buffer		0.3		3.6	V
		Differential input buffer		0.15		1	
f_{MULTin}	Multiplier input frequency	MULT ≥ 3		10		40	MHz
$f_{MULTout}$	Multiplier output frequency			60		150	
PLL							
f_{PD}	Phase detector frequency(4)	Integer channel		0.25		250	MHz
		1st and 2nd order modulator		5		200	
		3rd order modulator		5		160	
		4th order modulator		5		120	
I_{CPout}	Charge pump current	CPG = 1			625		µA
		CPG = 2			1250		
		CPG = 3			1875		
		…			…		
		CPG = 15			6875		

(1) f_{OSCin} = 100 MHz; f_{VCO} = f_{OUT} = 6.4 GHz; P_{OUT} = 0 dBm; OSC_2X = 0; MULT = 1; one RF output.
(2) f_{OSCin} = 100 MHz; f_{VCO} = 6.4 GHz; f_{OUT} = 3.2 GHz; P_{OUT} = 0 dBm; OSC_2X = 0; MULT = 1; one RF output.
(3) See OSCin Configuration for definition of OSCin input voltage.
(4) For lower VCO frequencies, the N-divider minimum value can limit the phase detector frequency.

Electrical Characteristics (continued)

3.0 V ≤ V_{CC} ≤ 3.5 V, –40°C ≤ T_A ≤ 85°C. Typical values are at V_{CC} = 3.3 V, 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$PN_{PLL\_1/f}$	Normalized PLL 1/f noise(5)				–123.5		dBc/Hz
PN_{PLL_Flat}	Normalized PLL noise floor(5)	Integer channel(6)			–232		dBc/Hz
		Fractional channel(7)			–232		dBc/Hz
VCO							
f_{VCO}	VCO frequency			3200		6400	MHz
PN_{VCO}	Open loop VCO phase noise	f_{VCO} = 3.4 GHz	10 kHz		–88		dBc/Hz
			100 kHz		–111		dBc/Hz
			1 MHz		–131		dBc/Hz
			10 MHz		–150		dBc/Hz
		f_{VCO} = 3.9 GHz	10 kHz		–87.5		dBc/Hz
			100 kHz		–111		dBc/Hz
			1 MHz		–131.5		dBc/Hz
			10 MHz		–150		dBc/Hz
		f_{VCO} = 4.4 GHz	10 kHz		–86.5		dBc/Hz
			100 kHz		–111		dBc/Hz
			1 MHz		–131		dBc/Hz
			10 MHz		–150		dBc/Hz
		f_{VCO} = 4.9 GHz	10 kHz		–85		dBc/Hz
			100 kHz		–110		dBc/Hz
			1 MHz		–130.5		dBc/Hz
			10 MHz		–149.5		dBc/Hz
		f_{VCO} = 5.4 GHz	10 kHz		–84.5		dBc/Hz
			100 kHz		–109		dBc/Hz
			1 MHz		–129.5		dBc/Hz
			10 MHz		–149		dBc/Hz
		f_{VCO} = 5.9 GHz	10 kHz		–84		dBc/Hz
			100 kHz		–108.5		dBc/Hz
			1 MHz		–129		dBc/Hz
			10 MHz		–148		dBc/Hz
K_{VCO}	VCO gain	f_{VCO} = 3.4 GHz			39		MHz/V
		f_{VCO} = 3.9 GHz			44		MHz/V
		f_{VCO} = 4.4 GHz			55		MHz/V
		f_{VCO} = 4.9 GHz			60		MHz/V
		f_{VCO} = 5.4 GHz			69		MHz/V
		f_{VCO} = 5.9 GHz			62		MHz/V
t_{VCOcal}	VCO calibration-time(8)	f_{OSCin} = f_{PD} = 100 MHz; Switch between 3.2 GHz and 6.4 GHz	No assist		130		µs
			Partial assist		50		µs
			Full assist		5		µs
$\lvert\Delta_{TCL}\rvert$	Allowable temperature drift(9)	VCO not being re-calibrated, –40°C ≤ T_A ≤ 85°C				125	°C

(5) Measured with a clean OSCin signal with a high slew rate using a wide loop bandwidth. The noise metrics model the PLL noise for an infinite loop bandwidth as: PLL_Total = 10*log[$10^{(PLL\_Flat/10)}$+$10^{(PLL\_Flicker/10)}$]; PLL_Flat = PN1 Hz + 20*log(N) + 10*log(f_{PD}); PLL_Flicker = PN10 kHz - 10*log(Offset/10 kHz) + 20*log(f_{OUT}/1 GHz)
(6) f_{OSCin} = 200 MHz; f_{PD} = 100 MHz; f_{VCO} = f_{OUT} = 6 GHz
(7) f_{OSCin} = 200 MHz; f_{PD} = 100 MHz; f_{VCO} = f_{OUT} = 6.001 GHz; Fractional denominator = 1000.
(8) See VCO Calibration for details.
(9) Not tested in production. Ensured by characterization. Allowable temperature drift refers to programming the device at an initial temperature and allowing this temperature to drift WITHOUT reprogramming the device, and still have the device stay at lock. This change could be up or down in temperature and the specification does not apply to temperatures that go outside the recommended operating temperatures of the device.

Electrical Characteristics (continued)

3.0 V ≤ V_{CC} ≤ 3.5 V, –40°C ≤ T_A ≤ 85°C. Typical values are at V_{CC} = 3.3 V, 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
RF OUTPUT							
f_{OUT}	RF output frequency			12.5		6400	MHz
P_{OUT}	Single-ended output power	f_{OUT} = 6.4GHz	OUTx_PWR = 50		4.5		dBm
$H2_{OUT}$	Second harmonic	f_{VCO} = f_{OUT} = 6.4 GHz			–20		dBc
		f_{VCO} = 6.4 GHz, f_{OUT} = 3.2 GHz			–37		
$H3_{OUT}$	Third harmonic	f_{VCO} = f_{OUT} = 6.4 GHz			–25		
		f_{VCO} = 6.4 GHz, f_{OUT} = 3.2 GHz			–13		
$\lvert t_{skew}CH \rvert$	Channel to channel skew	f_{OUT} = 3.2 GHz			14		ps
PHASE SYNCHRONIZATION							
$f_{OSCin}SYNC$	OSCin input frequency with SYNC	Category 3		5		100	MHz
		Categories 1 and 2		5		200	
$\lvert t_{skew}SYNC \rvert$	OSCin to RFout skew	After phase synchronization; $f_{OSCin}SYNC$ = f_{OUT} = 100 MHz			2		ns
DIGITAL INTERFACE							
V_{IH}	High-level input voltage			1.4		V_{CC}	V
V_{IL}	Low-level input voltage					0.4	
I_{IH}	High-level input current			–25		25	µA
I_{IL}	Low-level input current			–25		25	
V_{OH}	High-level output voltage	Load current = –5 mA	MUXout pin	V_{CC} – 0.5			V
V_{OL}	Low-level output voltage	Load current = 5 mA				0.5	

6.6 Timing Requirements

3.0 V ≤ V_{CC} ≤ 3.5 V, –40°C ≤ T_A ≤ 85°C. Typical values are at V_{CC} = 3.3 V, 25°C (unless otherwise noted)

			MIN	NOM	MAX	UNIT
SERIAL INTERFACE WRITE TIMING						
f_{SCK}	SCK frequency	1 / (t_{CWL}+ t_{CWH})			75	MHz
t_{CE}	SCK to CSB low time	Figure 1	5			ns
t_{CS}	SDI to SCK setup time		2			ns
t_{CH}	SDI to SCK hold time		2			ns
t_{CWH}	SCK pulse width high		5			ns
t_{CWL}	SCK pulse width low		5			ns
t_{CES}	CSB to SCK setup time		5			ns
t_{EWH}	CSB pulse width high		2			ns
SERIAL INTERFACE READ TIMING						
f_{SCK}	SCK frequency	1 / (t_{CWL}+ t_{CWH})			50	MHz
t_{CE}	SCK to CSB low time	Figure 1	10			ns
t_{CS}	SDI to SCK setup time		10			ns
t_{CH}	SDI to SCK hold time		10			ns
t_{CWH}	SCK pulse width high		10			ns
t_{CWL}	SCK pulse width low		10			ns
t_{CES}	CSB to SCK setup time		10			ns
t_{EWH}	CSB pulse width high		10			ns
SYNC AND SYSREFREQ TIMING						
t_{CS}	Pin to OSCin setup time	Figure 2	2.5			ns
t_{CH}	Pin to OSCin hold time		2			ns

6.7 Timing Diagrams

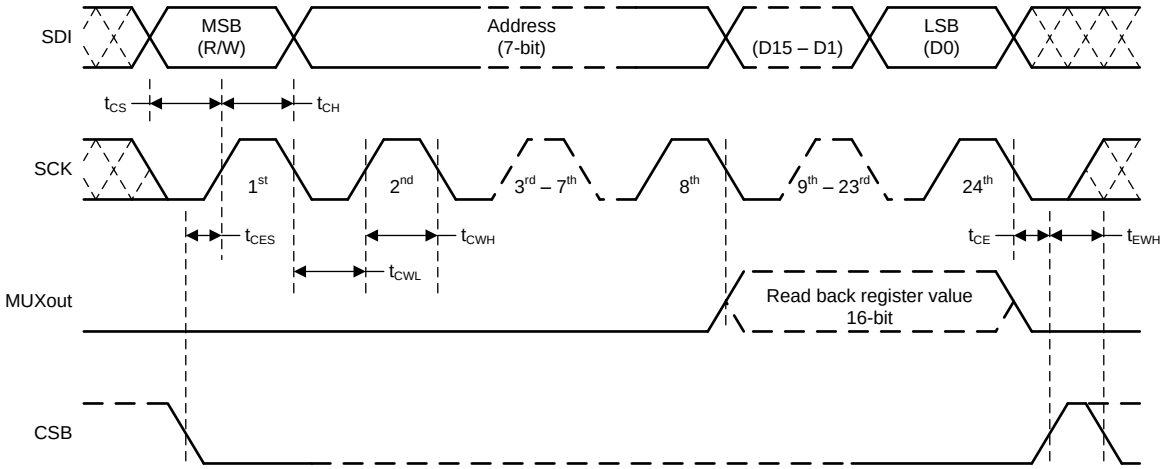


Figure 1. Serial Interface Timing Diagram

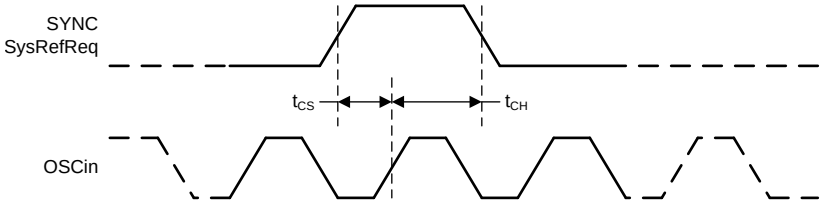


Figure 2. Trigger Signals Timing Diagram

6.8 Typical Characteristics

At T_A = 25°C, unless otherwise noted

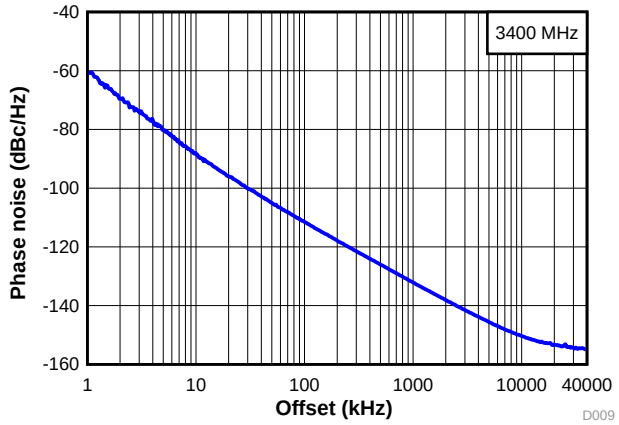


Figure 3. Open-Loop VCO Phase Noise at 3.4 GHz

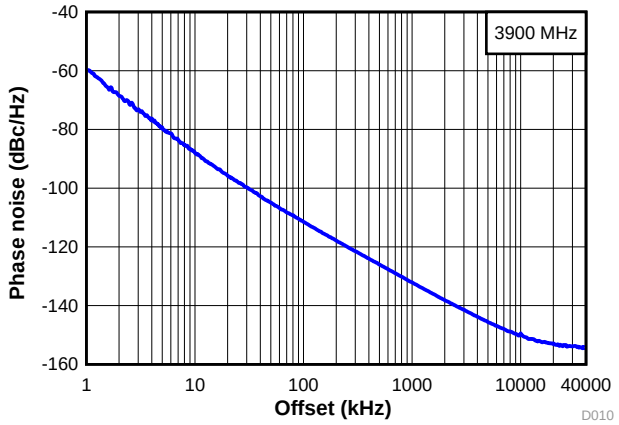


Figure 4. Open-Loop VCO Phase Noise at 3.9 GHz

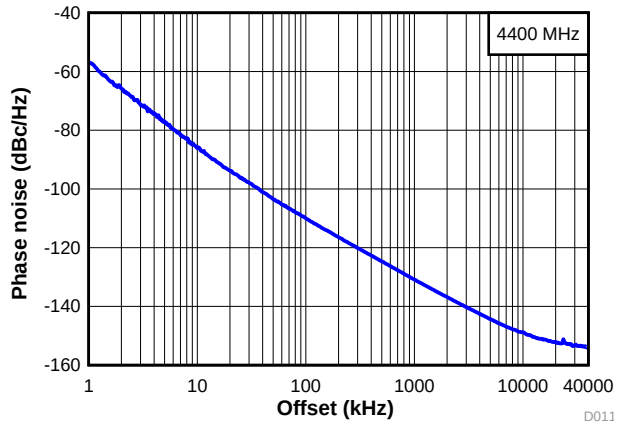


Figure 5. Open-Loop VCO Phase Noise at 4.4 GHz

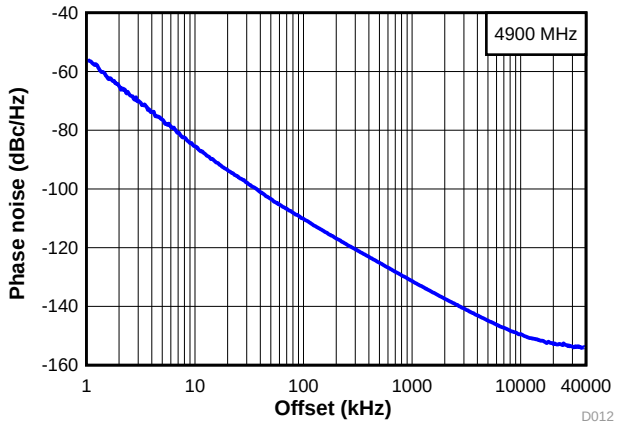


Figure 6. Open-Loop VCO Phase Noise at 4.9 GHz

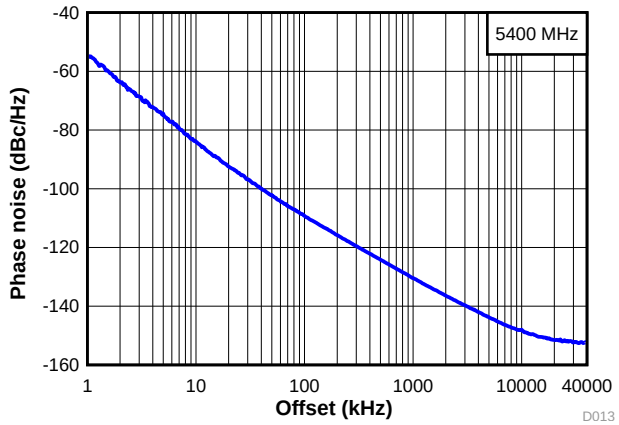


Figure 7. Open-Loop VCO Phase Noise at 5.4 GHz

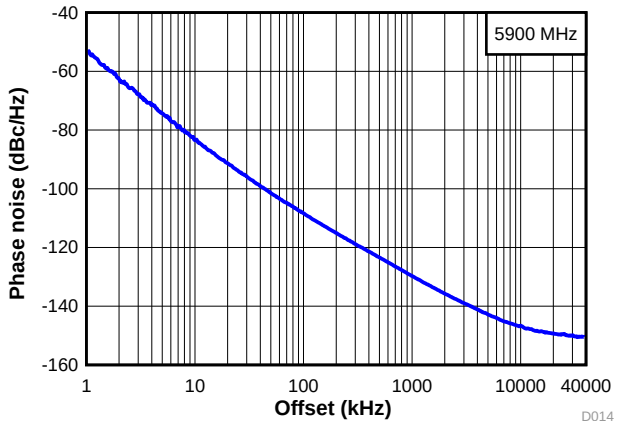


Figure 8. Open-Loop VCO Phase Noise at 5.9 GHz

Typical Characteristics (continued)

At T_A = 25°C, unless otherwise noted

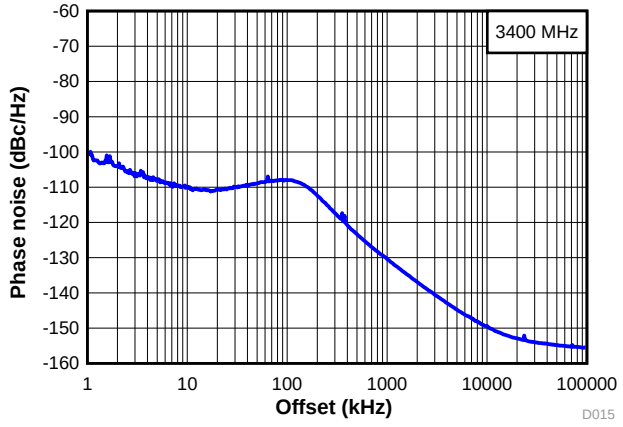


Figure 9. Wide Band Phase Noise at 3.4 GHz

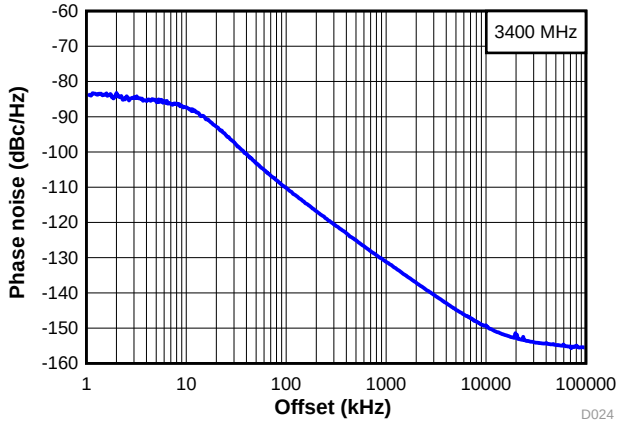


Figure 10. Narrow Band Phase Noise at 3.4 GHz

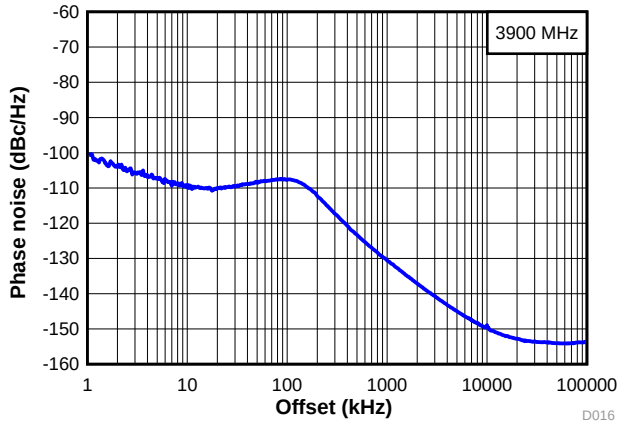


Figure 11. Wide Band Phase Noise at 3.9 GHz

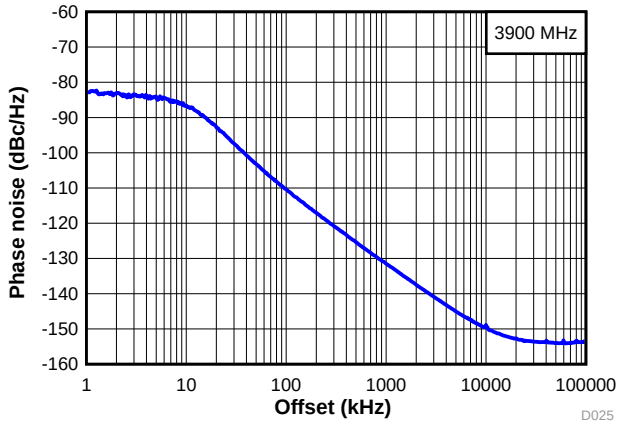


Figure 12. Narrow Band Phase Noise at 3.9 GHz

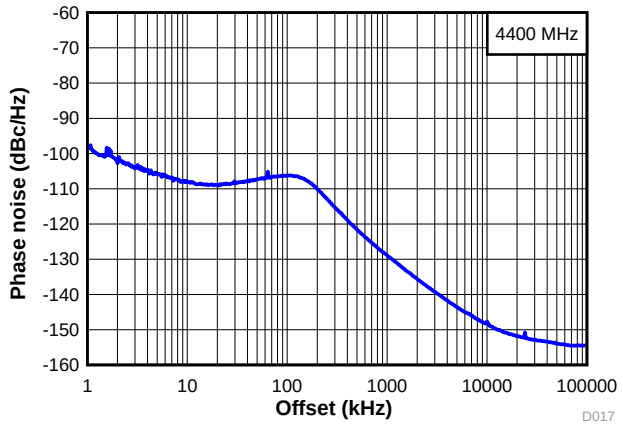


Figure 13. Wide Band Phase Noise at 4.4 GHz

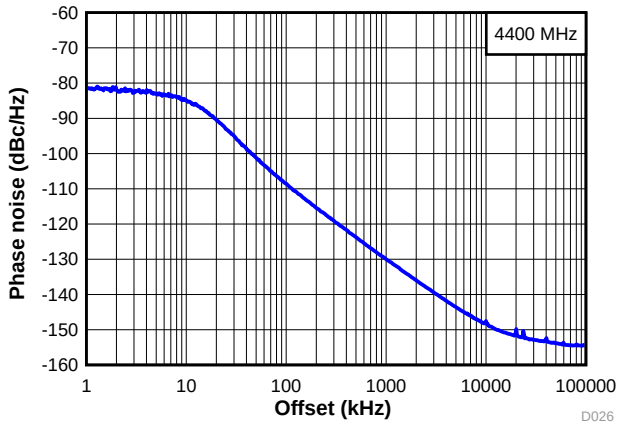


Figure 14. Narrow Band Phase Noise at 4.4 GHz

Typical Characteristics (continued)

At T_A = 25°C, unless otherwise noted

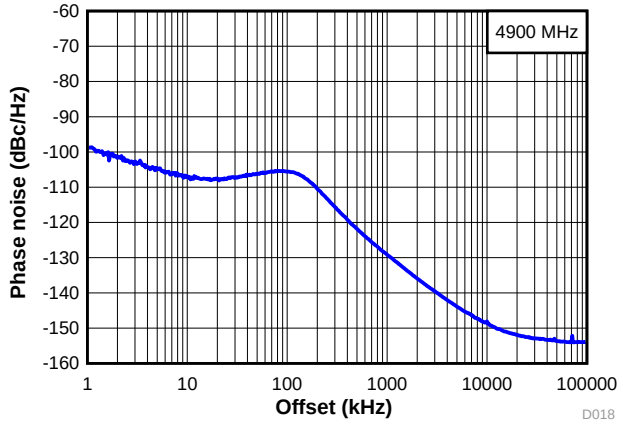


Figure 15. Wide Band Phase Noise at 4.9 GHz

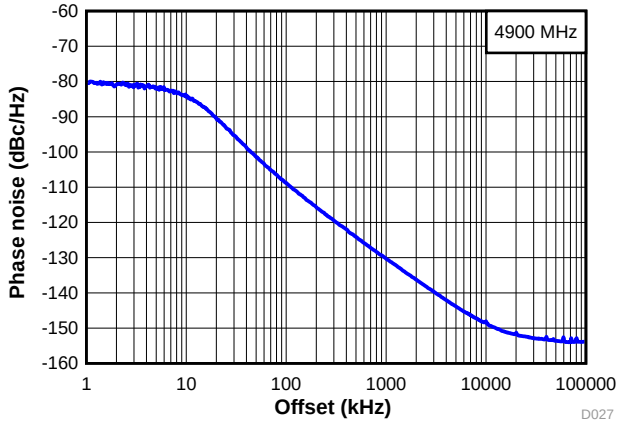


Figure 16. Narrow Band Phase Noise at 4.9 GHz

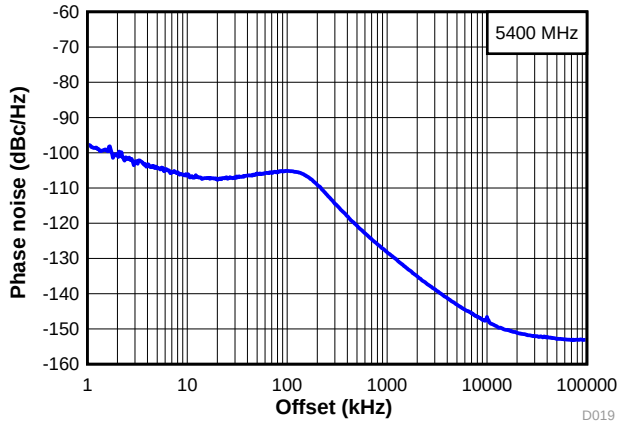


Figure 17. Wide Band Phase Noise at 5.4 GHz

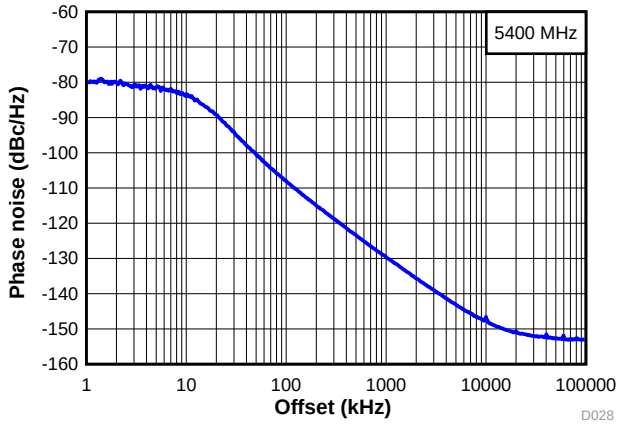


Figure 18. Narrow Band Phase Noise at 5.4 GHz

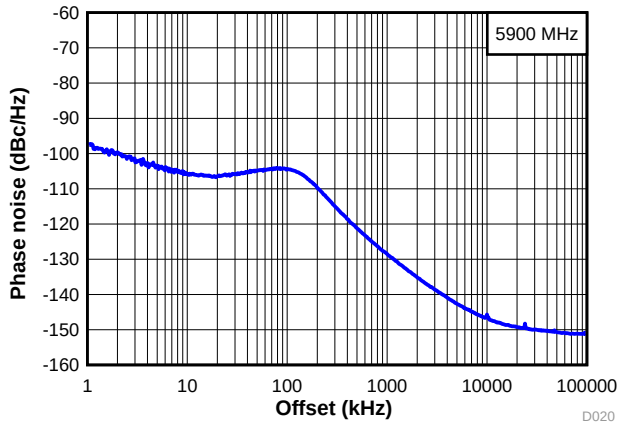


Figure 19. Wide Band Phase Noise at 5.9 GHz

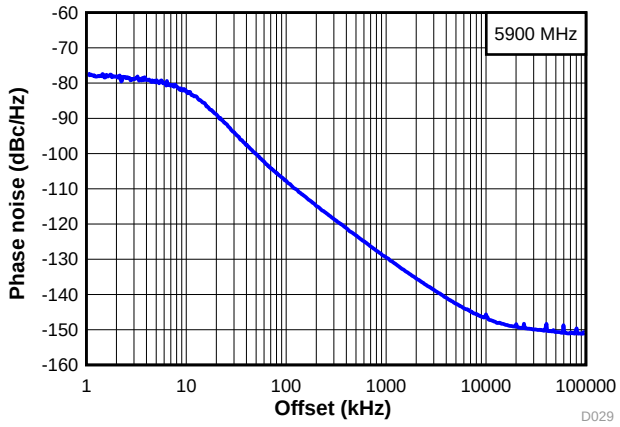


Figure 20. Narrow Band Phase Noise at 5.9 GHz

Typical Characteristics (continued)

At T_A = 25°C, unless otherwise noted

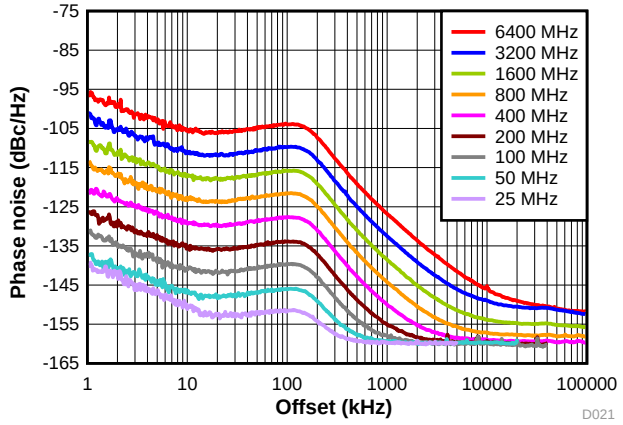


Figure 21. Direct and Divided Down Outputs

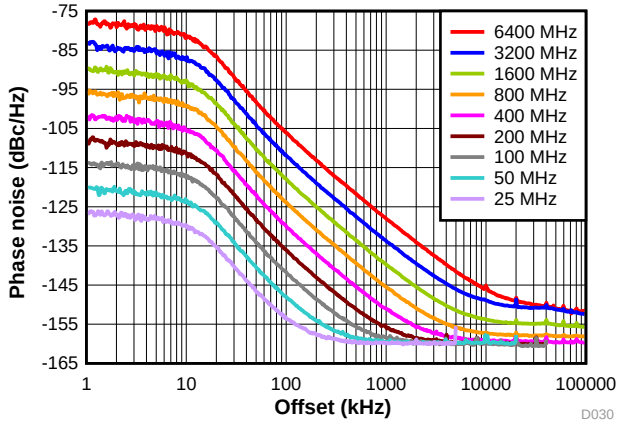
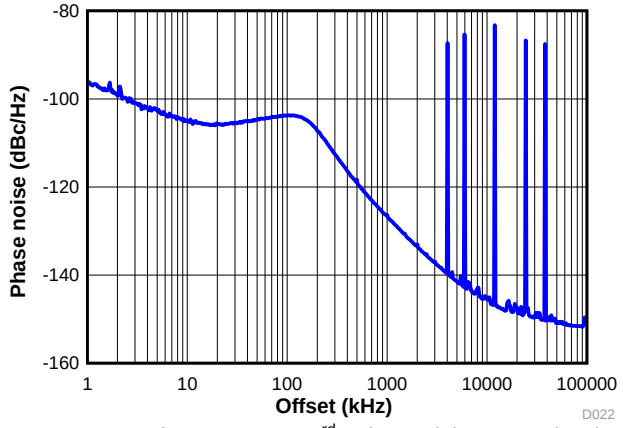
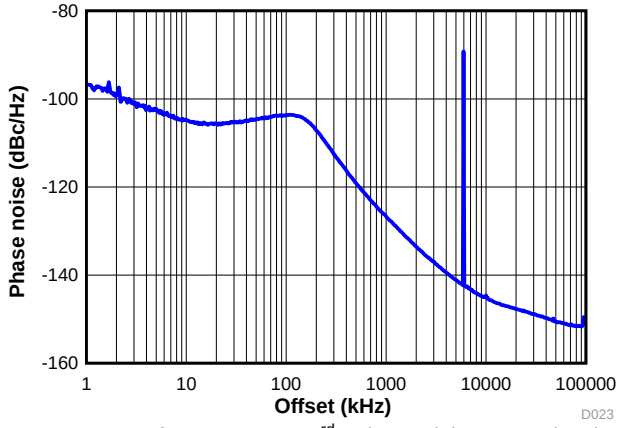


Figure 22. Direct and Divided Down Outputs



f_{VCO} = 6397 MHz; f_{PD} = 100 MHz; 3rd order modulator; Fractional denominator = 1000; Loop filter bandwidth = 115 kHz

Figure 23. Wide Band Fractional Spurs



f_{VCO} = 6397 MHz; f_{PD} = 100 MHz; 3rd order modulator; Fractional denominator = 2^{32} – 1; Loop filter bandwidth = 115 kHz

Figure 24. Wide Band Fractional Spurs

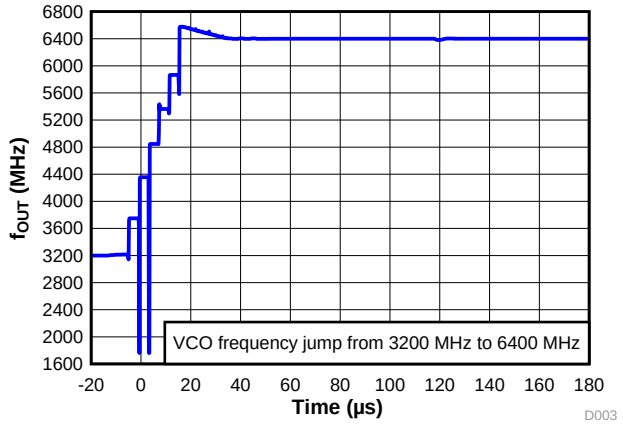


Figure 25. VCO Calibration Time

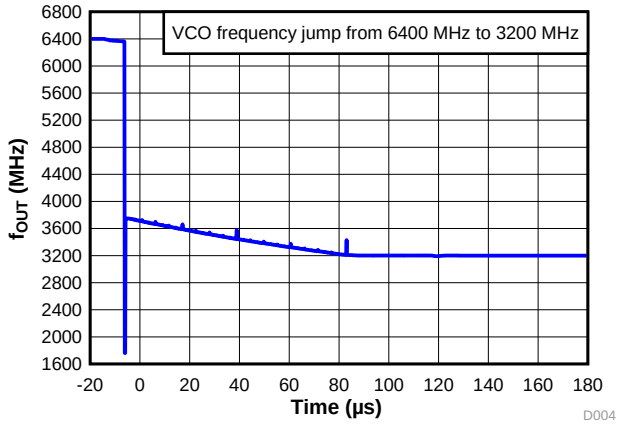


Figure 26. VCO Calibration Time

Typical Characteristics (continued)

At T_A = 25°C, unless otherwise noted

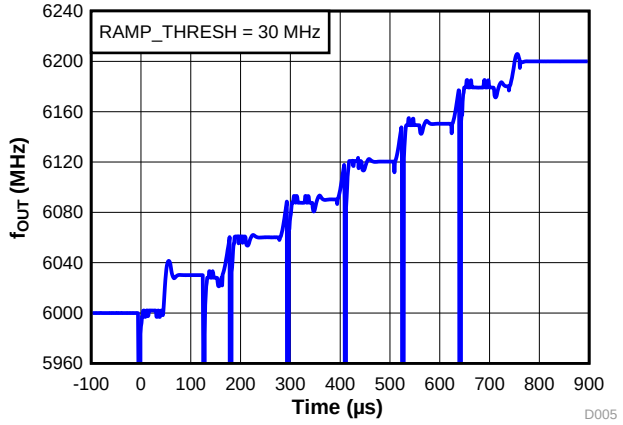


Figure 27. Automatic Ramping

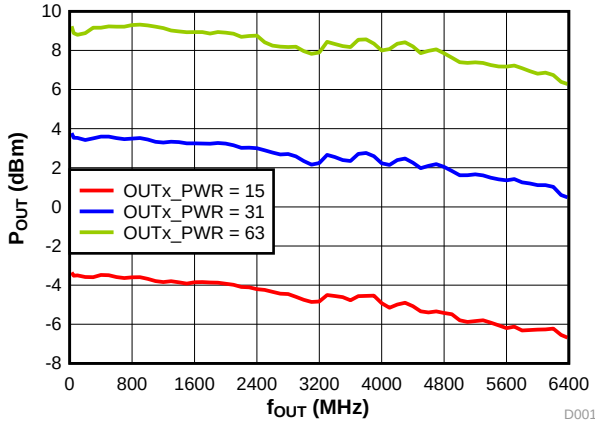


Figure 28. Output Power vs Frequency

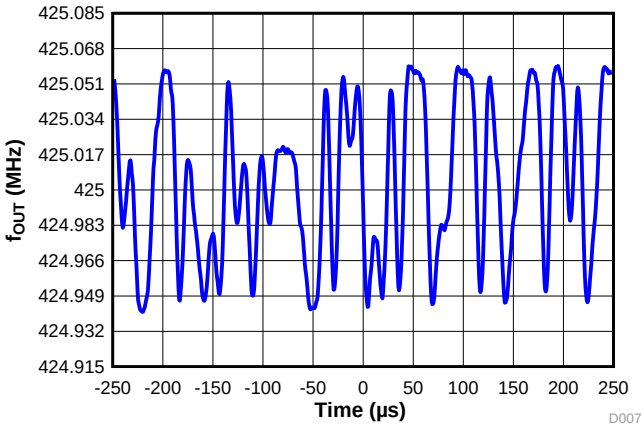


Figure 29. 4-Level GFSK Modulation

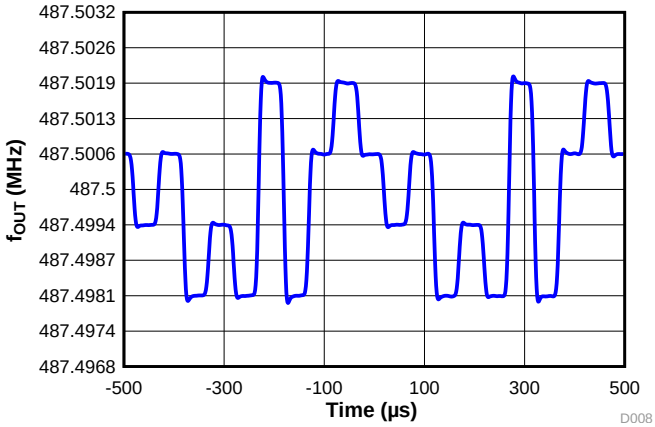


Figure 30. Discrete-Level FSK Modulation

7 Detailed Description

7.1 Overview

The LMX2572 is a low-power, high-performance, wideband frequency synthesizer with integrated VCO and output divider. The VCO operates from 3.2 to 6.4 GHz, and this can be combined with the output divider to produce any frequency in the range of 12.5 MHz to 6.4 GHz. Within the input path, there are two dividers and a multiplier for flexible frequency planning. The multiplier also allows reduction of spurs by moving the frequencies away from the integer boundary.

The PLL is a fractional-N PLL with a programmable delta-sigma modulator up to 4th order. The fractional denominator is a programmable 32-bit long that can supply fine frequency steps easily below the 1-Hz resolution. The denominator can also be used to do exact fractions like 1/3, 7/1000, and many others.

For applications where deterministic or adjustable phase is desired, the SYNC pin can be used to get the phase relationship between the OSCin and RFout pins deterministic. Once this is done, the phase can be adjusted in very fine steps of the VCO period divided by the fractional denominator.

The ultra-fast VCO calibration is ideal for applications where the frequency must be swept or abruptly changed. The frequency can be manually programmed, or the device can be set up to do ramps and chirps.

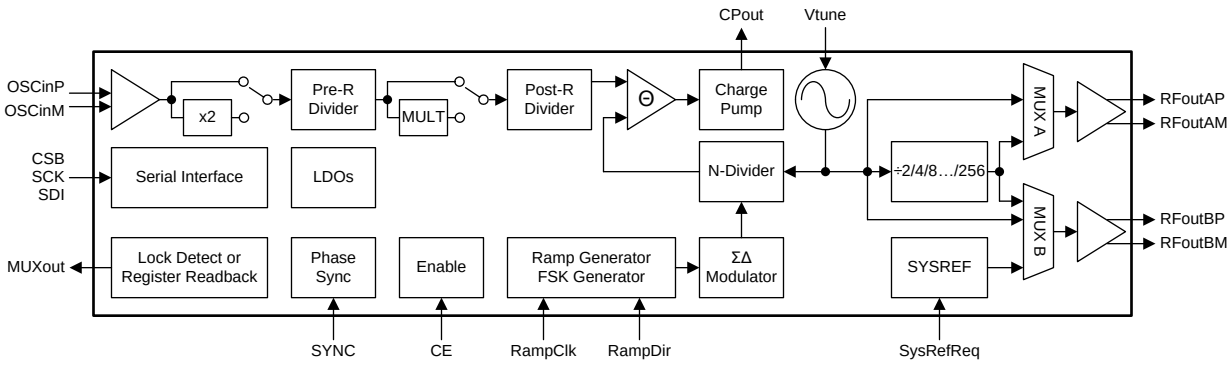
The JESD204B support includes using the RFoutB output to create a differential SYSREF output that can be either a single pulse, series of pulse, or a continuous stream of pulses. These pulses are synchronous with the RFoutA signal with an adjustable delay.

The FSK generator can support FSK generation in discrete 2-, 4-, or 8-level FSK, or it can any arbitrary level FSK making it ideal to support pulse-shaped FSK modulation such as GFSK.

The LMX2572 device requires only a single 3.3-V power supply and uses very low current. The internal power supplies are provided by integrated LDOs, eliminating the need for high performance external LDOs.

Digital logic interface is compatible with 1.8-V input. The user can program the device through the serial interface. The device can be powered down through register programming or by toggling the Chip Enable (CE) pin.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Reference Oscillator Input

The OSCin pins are used as a frequency reference input to the device. The input is high impedance and requires AC-coupling capacitors at the pin. The OSCin pins can be driven single-ended with a CMOS clock, XO, or single-ended differential clock. Differential clock input is also supported, which makes the device easier to interface with high-performance system clock devices such as TI's LMK series clock devices. As the OSCin signal is used as a clock for the VCO calibration, a proper reference signal must be applied at the OSCin pin at the time of programming FCAL_EN.

Feature Description (continued)

7.3.2 Reference Path

The reference path consists of an OSCin doubler (OSC_2X), Pre-R divider (PLL_R_PRE), Multiplier (MULT), and a Post-R divider (PLL_R).

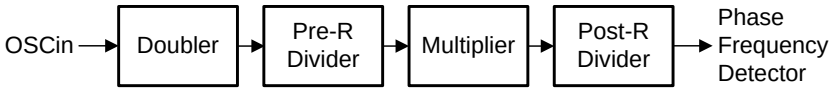


Figure 31. Reference Path

The Doubler allows one to double the input reference frequency up to 250 MHz. The Doubler adds minimal noise and is useful for raising the phase detector frequency for better phase noise. The Doubler can also be used to avoid spurs. The Doubler uses both the rising and falling edges of the input signal, so the input signal must have 50% duty cycle if the Doubler is enabled. Note that the Multiplier cannot be used if the Doubler is engaged.

The Pre-R divider can help reduce input frequency so that the Multiplier can be used and the maximum 200-MHz input frequency limitation of the Post-R divider can be met.

The Multiplier multiplies the frequency up under the allowable multiplications of 3, 4, 5, 6, and 7. In combination with the Pre-R and Post-R dividers, the Multiplier offers the flexibility to shift the phase detector frequency away from frequencies that may create integer boundary spurs with the VCO and the output frequencies. Be aware that unlike the Doubler, the Multiplier degrades the PLL figure of merit. This degradation would only matter, however, for a very clean reference oscillator input and if the loop bandwidth was wide. The user should not use the Doubler while using the Multiplier. The Multiplier is bypassed if its value is set to 1.

The Post-R divider can be used to further divide down the frequency to the phase detector frequency. When it is used (PLL_R > 1), the input frequency to this divider is limited to 200 MHz.

Use Equation 1 to calculate the phase detector frequency, f_{PD}.

$$f_{PD} = f_{OSCin} \times OSC\_2X \times MULT / (PLL\_R\_PRE \times PLL\_R) \quad (1)$$

Table 1 summarizes the usage boundaries of these functional blocks in the reference path.

Table 1. Reference Path Boundaries

PARAMETER	VALUE	INPUT FREQUENCY (MHz)		OUTPUT FREQUENCY (MHz)		NOTES
		MIN	MAX	MIN	MAX	
OSCin	N/A	5	250			
Doubler	0 (Bypassed), 1 (x2)	5	125	10	250	When OSC_2X = 1, Multiplier cannot be used at the same time.
Pre-R divider	1 (Bypassed), 2, 3, …, 254, 255	5	200	0.25	200	Keep it equals 1 unless when necessary.
Multiplier	1 (Bypassed), 3, 4, 5, 6, 7	10	40	60	150	When the output frequency is greater than 100MHz, set MULT_HI = 1.
Post-R divider	1 (Bypass), 2, 3, …, 254, 255	5	200	0.25	200	

7.3.3 PLL Phase Detector and Charge Pump

The phase detector compares the outputs of the Post-R divider and N divider and generates a correction current corresponding to the phase error until the two signals are aligned in phase. This charge-pump current is software programmable to many different levels, allowing modification of the closed-loop bandwidth of the PLL.

Table 2. Charge Pump Gain

CGP	0	1	2	3	4 or 8	5 or 9	6 or 10	7 or 11	12	13	14	15	UNIT
Gain	Tri-state	625	1250	1875	2500	3125	3750	4375	5000	5625	6250	6875	µA

7.3.4 PLL N Divider and Fractional Circuitry

The N divider includes fractional compensation and can achieve any fractional denominator (PLL_DEN) from 1 to (2^{32} – 1). The integer portion of N (PLL_N) is the whole part of the N divider value, and the fractional portion, N_{frac} = PLL_NUM / PLL_DEN, is the remaining fraction. PLL_N, PLL_NUM and PLL_DEN are software programmable. The higher the denominator, the finer the resolution step of the output. For example, even when using f_{PD} = 200 MHz, the output can increment in steps of 200 MHz / (2^{32} – 1) = 0.0466 Hz. Equation 2 shows the relationship between the phase detector and VCO frequencies. Note that in SYNC mode, there is an extra divider that is not shown in Equation 2.

$$f_{VCO} = f_{PD} \times [PLL\_N + (PLL\_NUM / PLL\_DEN)] \quad (2)$$

The multi-stage noise-shaping (MASH) sigma-delta modulator that controls the fractional division is also programmable from integer mode to fourth order. All of these settings work for integer channel where PLL_NUM = 0. To make the fractional spurs consistent, the modulator is reset any time that the R0 register is programmed.

The N divider has minimum value restrictions based on the modulator order. Furthermore, the PFD_DLY_SEL bit must be programmed in accordance to Table 3.

Table 3. Minimum N Divider Restrictions

VCO FREQUENCY (GHz)	MASH ORDER									
	INTEGER		FIRST ORDER		SECOND ORDER		THIRD ORDER		FOURTH ORDER	
	N	PFD_DLY_SEL	N	PFD_DLY_SEL	N	PFD_DLY_SEL	N	PFD_DLY_SEL	N	PFD_DLY_SEL
$f_{VCO} < 4$	20	0	25	1	26	1	32	2	44	4
$4 \le f_{VCO} < 4.9$	24	1	29	2	30	2	32	2	44	4
$4.9 \le f_{VCO} \le 6.4$	24	1	29	2	30	2	36	3	48	5

7.3.5 Voltage-Controlled Oscillator

The LMX2572 includes a fully integrated VCO. The VCO generates a frequency which varies with the tuning voltage from the loop filter. The entire VCO frequency range, 3.2 to 6.4 GHz, covers an octave that allows the channel divider to take care of frequencies below the lower bound.

To reduce the VCO tuning gain, thus improving the VCO phase noise performance, the VCO frequency range is divided into 6 different frequency bands. This creates the need for frequency calibration to determine the correct frequency band given in a desired output frequency. The VCO is also calibrated for amplitude to optimize phase noise. These calibration routines are activated any time that the R0 register is programmed with the FCAL_EN bit equals one. It is important that a valid OSCin signal must present before VCO calibration begins. This device will support a full sweep of the valid temperature range of 125°C (–40°C to 85°C) without having to re-calibrate the VCO. This is important for continuous operation of the synthesizer under the most extreme temperature variation.

7.3.6 Channel Divider

To go below the VCO lower bound of 3.2 GHz, the channel divider can be used. The channel divider consists of several segments, and the total division value is equal to the multiplication of them. Therefore, not all values are valid.

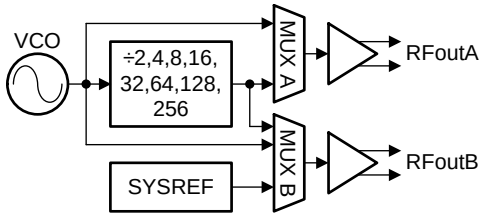


Figure 32. Channel Divider

The channel divider is automatically powered up whenever the MUXs have selected divided down output or SYSREF output, regardless of whether the RF output buffers are turned on or not. When an output is not used, TI recommends selecting the VCO output (OUTx_MUX = 1) to ensure that the channel divider is not unnecessarily powered up.

Table 4. Channel Divider

OUTA_MUX	OUTB_MUX	CHANNEL DIVIDER
0: Channel divider output	Don't care	Powered up
Don't care	0: Channel divider output 2: SYSREF output	
All other cases		Powered down

7.3.7 Output Buffer

The output buffers are differential push-pull type buffers, thus no external pullup to V_{CC} is required. The output impedance of the buffer is very small, and as such, the buffer can be AC-coupled to drive a 50-Ω load. Output power of the buffer can be programed to various levels. The buffer can be disabled while still keeping the PLL in lock. Buffer A supports direct VCO output or divided down output. Buffer B supports direct VCO output, divided down output or SYSREF output.

7.3.8 Lock Detect

The MUXout pin can be configured to output a signal that gives an indication for the PLL being locked. If the MUXout pin is configured as a lock detect output (MUXOUT_LD_SEL = 1), the MUXout pin output is a logic HIGH voltage when the device is locked. When the device is unlocked, the MUXout pin output is a logic LOW voltage.

There are options to select the definition of PLL being locked. If LD_TYPE = 0, lock detect asserts a HIGH output after the VCO has finished calibration and the LD_DLY timeout counter is finished. If LD_TYPE = 1, in addition to the VCO calibration and counter check, lock detect will assert a HIGH output if the VCO tuning voltage is also within an acceptable limits.

7.3.9 Register Readback

The MUXout pin can also be configured to read back useful information from the device. Common uses for readback are:

- Read back registers to ensure that they have been programmed to the correct value. LMX2572 allows any of its registers to be read back.
- Read back the lock detect status to determine if the PLL is in lock.
- Read back VCO calibration information so that it can be used to improve the lock time.

7.3.10 Powerdown

The LMX2572 can be powered up and down using the CE pin or the POWERDOWN bit. All registers are preserved in memory while the device is powered down.

The wake-up time for the device to come out of the powered state is adjustable. See Power-Up, Wake-Up Time for details.

7.3.11 Phase Synchronization

The SYNC pin allows the user to synchronize the LMX2572 such that the delay from the rising edge of th OSCin signal to the RF output signal is deterministic. Phase synchronization is especially useful if there are multiple LMX2572 devices in a system and it is desirable to have all the RF outputs aligned in phase.

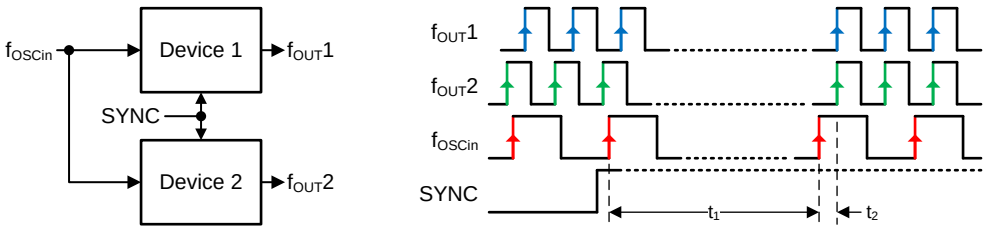


Figure 33. Phase Synchronization

Initially, the devices are locked to the input but are not synchronized. The user sends a synchronization pulse that is re-clocked to the next rising edge of the OSCin pulse. After a given time, t_1, the devices are synchronized. This time is dominated by the sum of the VCO calibration time, the analog settling time of the PLL loop, and the MASH_RST_COUNT, if used in fractional mode. After synchronization, both devices will have a deterministic delay of t_2, related to OSCin.

7.3.12 Phase Adjustment

The LMX2572 can use the sigma-delta modulator to adjust the output signal phase with respect to the input reference. The phase shift every time you write the value of MASH_SEED is Equation 3:

Phase shift in degree = 360° × (MASH_SEED / PLL_DEN) × (P / CHDIV)

where

- P = 2 when VCO_PHASE_SYNC_EN = 1, else P = 1 (3)

For example, if

- MASH_SEED = 800
- PLL_DEN = 1000
- CHDIV = 32
- VCO_PHASE_SYNC_EN = 0

Phase shift = 360° × (800 / 1000) × (1 / 32) = 9°. If we write 800 to MASH_SEED 40 times, then we will shift the phase by 360°.

There are a couple of restrictions when using phase adjustment:

- Phase adjustment does not work with MASH_ORDER equals 0 (Integer mode) or 1 (First order).
- Phase adjustment is possible with integer channels (PLL_NUM = 0) as long as MASH_ORDER is greater than 1.
- PLL_DEN must be greater than PLL_NUM + MASH_SEED.

7.3.13 Ramping Function

The LMX2572 supports the ability to make frequency ramping waveforms using manual mode or automatic mode.

In manual ramping mode, the user defines a step and uses the RampClk and RampDir pins to create the ramp. The output frequency jumps from one frequency to another frequency on each ramp.

In automatic ramping mode, the user sets up the ramp with up to two linear segments in advance and the device automatically creates this ramp. The output waveform is a continuous frequency sweep between the start and end frequencies. If the frequency ramping range is small (approximately 10 MHz), no VCO calibration break is necessary in the middle of the ramp.

When using ramp, the following must be set accordingly:

- Phase detector frequency must be between f_{OSCin} / $2^{CAL\_CLK\_DIV}$ and 125 MHz.
- OUT_FORCE = 1 to force the RF outputs not to be automatically muted during VCO calibration.
- LD_DLY = 0 to avoid interfering with VCO calibration.
- PLL_DEN = 2^{32} – 1. The actual denominator value being used in ramping mode is 2^{24}.

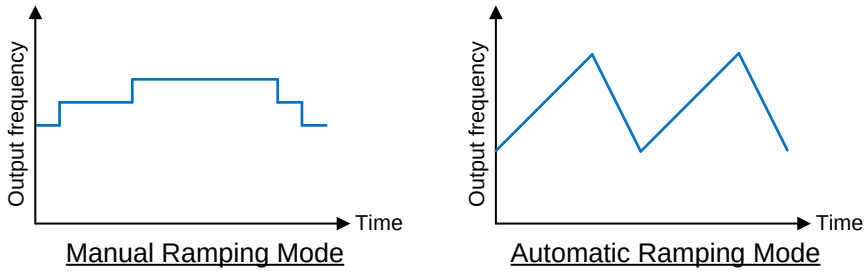


Figure 34. Ramping Modes

7.3.14 SYSREF

RFoutB of LMX2572 can be used to generate or duplicate SYSREF signal. The output of RFoutB can be a single pulse, series of pulse, or a continuous stream of pulses. These pulses are synchronous with the RFoutA signal with an adjustable delay. To use the SYSREF capability, the PLL must be in SYNC mode with VCO_PHASE_SYNC_EN = 1. SYSREF output is triggered when there is a 0 → 1 transition at the SysRefReq pin. In SYSREF Pulsed mode, a maximum of 15 consecutive pulses can be generated at a time.

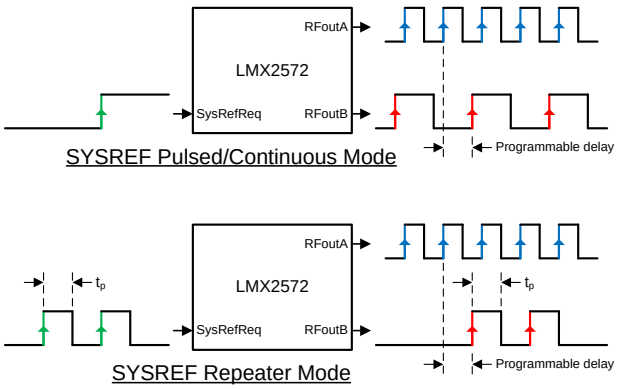


Figure 35. SYSREF Modes

7.3.15 FSK Modulation

Direct digital FSK modulation is supported in LMX2572. FSK modulation is achieved by changing the output frequency by changing the N divider value. The LMX2572 supports two different types of FSK operation.

1. FSK SPI mode. This mode supports discrete 2-, 4- and 8-level FSK modulation. There are eight dedicated registers used to pre-store the desired FSK frequency deviations. Program FSK_SPI_DEV_SEL to select one of the FSK deviations at a time.
2. FSK SPI FAST mode. In this mode, instead of selecting one of the pre-stored FSK deviations, change the FSK deviation directly by writing to FSK_SPI_FAST_DEV. As a result, this mode supports arbitrary-level FSK, which is useful to construct pulse-shaping or analog-FM modulation.

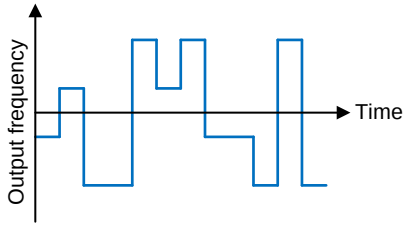


Figure 36. FSK Modulation

7.4 Device Functional Modes

Table 5 lists the device functional modes of the LMX2572.

Table 5. Device Functional Modes

MODE	DESCRIPTION
Normal operation mode	The device is used as a high frequency signal source without any addition features.
FSK mode	Generates discrete-level FSK or arbitrary-level pulse-shaped FSK modulation.
SYNC mode	This mode is used to ensure deterministic phase between OSCin and RFout.
SYSREF mode	The device is used as a JESD204B SYSREF clock generator or repeater.
Ramping mode	Automatic frequency sweeping without the need of continuous SPI programming.

7.5 Programming

The LMX2572 is programmed using several 24-bit shift registers. The shift register consists of a data field, an address field, and a R/W bit. The MSB is the R/W bit. 0 means register write while 1 means register read. The following seven bits, ADDR[6:0], form the address field which is used to decode the internal register address. The remaining 16 bits form the data field DATA[15:0]. Serial data is shifted MSB first into the shift register. See Figure 1 for timing diagram details.

To write registers:

- The R/W bit must be set to 0.
- The data on SDI pin is clocked into the shift register upon the rising edge of the clocks on SCK pin. On the rising edge of the 24th clock cycle, the data is transferred from the data field into the selected register bank.
- The CSB pin may be held high after programming, which causes the LMX2572 to ignore clock pulses.
- If the SCK and SDI lines are toggled while the VCO is in lock, as is sometimes the case when these lines are shared between devices, the phase noise may be degraded during the time of this programming.

To read back registers:

- The R/W bit must be set to 1.
- The data field contents on the SDI line are ignored.
- The read back data on MUXout pin is clocked out starting from the falling edge of the 8th clock cycle.

7.5.1 Recommended Initial Power-On Programming

7.5.1.1 Programming Sequence

When the device is first powered up, it must be initialized, and the ordering of this programming is important. The sequence is listed below. After this sequence is completed, the device should be running and locked to the proper frequency.

1. Apply power to the device and ensure all the supply pins are at the proper levels.
2. If CE is low, pull it high.
3. Wait 500 µs for the internal LDOs to become stable.
4. Ensure that a valid reference clock is applied to the OSCin pins.
5. Program register R0 with RESET = 1. This will ensure all the registers are reset to their default values. This bit is self-clearing.
6. Program in sequence registers R125, R124, R123, ..., R1 and then R0.

7.5.1.2 Programming Register

There are altogether 126 programmable registers. However, not every register is required to be programmed at initial power-on.

For example, most of the registers have fixed field value which is also equal to their silicon default value. After programming R0 with RESET = 1, these register fields have returned to their silicon default values. As such, it is not necessary to program these registers again. Similarly, for those registers having configurable fields, if the desired field values are equal to the silicon default values, again it is not necessary to program these registers again after programming R0 with RESET = 1.

In Table 6, *Depends* means it is up to the user's decision of whether programming the register or not based upon the application need.

Table 6. Suggested Register Programming

REGISTER	PROGRAM	REGISTER	PROGRAM	REGISTER	PROGRAM	REGISTER	PROGRAM	REGISTER	PROGRAM	REGISTER	PROGRAM
0	Yes	21	No	42	Yes	63	No	84	Depends	105	Depends
1	Depends	22	No	43	Yes	64	No	85	Depends	106	Depends
2	No	23	No	44	Depends	65	No	86	Depends	107	No
3	No	24	No	45	Depends	66	No	87	No	108	No
4	No	25	No	46	Depends	67	No	88	No	109	No
5	Depends	26	No	47	No	68	No	89	No	110	No
6	Depends	27	No	48	No	69	Depends	90	No	111	No

Programming (continued)

Table 6. Suggested Register Programming (continued)

REGISTER	PROGRAM	REGISTER	PROGRAM	REGISTER	PROGRAM	REGISTER	PROGRAM	REGISTER	PROGRAM	REGISTER	PROGRAM
7	Depends	28	No	49	No	70	Depends	91	No	112	No
8	Depends	29	Yes	50	No	71	Yes	92	No	113	No
9	Depends	30	Yes	51	No	72	Depends	93	No	114	Depends
10	Depends	31	No	52	Yes	73	Depends	94	No	115	Depends
11	Depends	32	No	53	No	74	Depends	95	No	116	Depends
12	Depends	33	No	54	No	75	Depends	96	Depends	117	Depends
13	No	34	Depends	55	No	76	No	97	Depends	118	Depends
14	Depends	35	No	56	No	77	No	98	Depends	119	Depends
15	No	36	Yes	57	Yes	78	Yes	99	Depends	120	Depends
16	Depends	37	Yes	58	Depends	79	Depends	100	Depends	121	Depends
17	Depends	38	Yes	59	Depends	80	Depends	101	Depends	122	Depends
18	No	39	Yes	60	Depends	81	Depends	102	Depends	123	Depends
19	Depends	40	Depends	61	No	82	Depends	103	Depends	124	Depends
20	Depends	41	Depends	62	Depends	83	Depends	104	Depends	125	No

7.5.2 Recommended Sequence for Changing Frequencies

The recommended sequence for changing frequencies in different scenarios is as follows:

1. If the N divider is changing, program the relevant registers and then program R0 with FCAL_EN = 1.
2. In FSK and Ramp mode, the fractional numerator is changing; program the relevant registers only.

7.5.3 Double Buffering

Some register fields support double buffering. That is, the change to these fields would not be effective immediately. To latch the new values into the device requires programming R0 again with FCAL_EN = 1. The following register fields support double buffering, see Table 70 for details.

- MASH order (MASH_ORDER)
- Fractional numerator (PLL_NUM)
- N divider (PLL_N)
- Doubler (OSC_2X); Pre-R divider (PLL_R_PRE); Multiplier (MULT); Post-R divider (PLL_R)

For example,

1. Program PLL_R and PLL_N to new values. If double buffering for these fields is enabled, the PLL will remain unchanged.
2. Program R0 with FCAL_EN = 1. The PLL will calibrate and lock using the new PLL_R and PLL_N values.

7.5.4 Block Programming

In a register write sequence, instead of sending 24 bits (one W/R bit, seven address bits, and 16 data bits) of payload for each register (with Block Programming), only the first register write requires the W/R bit and the address bits. The succeeding registers require sending only the 16-bit of data. However, the succeeding registers must be in descending order. For example, if the first register is R20, then all 24 bits of payload must be sent for R20. The next register must be R19, but only the 16-bit data is required. The programming sequence is as follows:

1. Pull CSB pin LOW.
2. Write 0x14aaaa for R20.
3. Write 0xbbbb for R19, followed by 0xcccc for R18, and so on.
4. After the last register write is completed, pull CSB pin HIGH to finish Block Programming.

Since there is no CSB pulse between each register, the 16-bit of data field of each register can be sent immediately after the previous one.

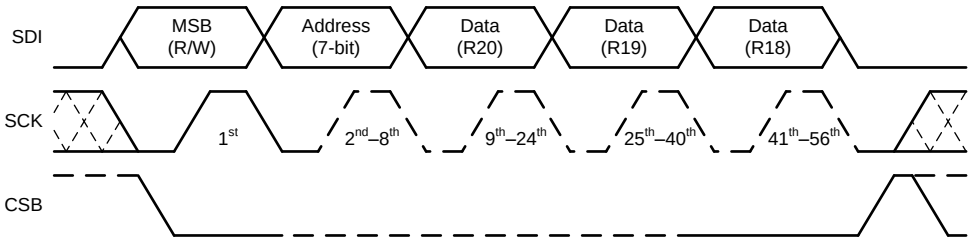


Figure 37. Block Programming Timing Example

Block Programming applies to both register write and read.

7.6 Register Maps

REG.	DATA[15:0]																POR
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
R0	RAMP_EN	VCO_PHASE_SYNC_EN	1	0	ADD_HOLD	0	OUT_MUTE	FCAL_HPFD_ADJ		FCAL_LPFD_ADJ		1	FCAL_EN	MUXOUT_LD_SEL	RESET	POWER DOWN	00221Ch
R1	0	0	0	0	1	0	0	0	0	0	0	0	1	CAL_CLK_DIV			010808h
R2	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	020500h
R3	0	0	0	0	0	1	1	1	1	0	0	0	0	0	1	0	030782h
R4	0	0	0	0	1	0	1	0	0	1	0	0	0	0	1	1	040A43h
R5	0	0	1	IPBUF_TYPE	IPBUF_TERM	0	0	0	1	1	0	0	1	0	0	0	0530C8h
R6	LDO_DLY					0	0	0	0	0	0	0	0	0	1	0	06C802h
R7	0	OUT_FORCE	0	0	0	0	0	0	1	0	1	1	0	0	1	0	0700B2h
R8	0	VCO_DACISET_FORCE	1	0	VCO_CAPCTRL_FORCE	0	0	0	0	0	0	0	0	0	0	0	082000h
R9	0	MULT_HI	0	OSC_2X	0	0	0	0	0	0	0	0	0	1	0	0	090004h
R10	0	0	0	1	MULT					1	1	1	1	0	0	0	0A10F8h
R11	1	0	1	1	PLL_R								1	0	0	0	0BB018h
R12	0	1	0	1	PLL_R_PRE												0C5001h
R13	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0D4000h
R14	0	0	0	1	1	0	0	0	0	CPG				0	0	0	0E1840h
R15	0	0	0	0	0	1	1	0	0	0	0	0	1	1	1	0	0F060Eh
R16	0	0	0	0	0	0	0	VCO_DACISET									100080h
R17	0	0	0	0	0	0	0	VCO_DACISET_STRT									110096h
R18	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0	120064h
R19	0	0	1	0	0	1	1	1	VCO_CAPCTRL								1327B7h
R20	0	1	VCO_SEL			VCO_SEL_FORCE	0	0	0	1	0	0	1	0	0	0	143048h
R21	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	1	150409h
R22	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	160001h
R23	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	0	17007Ch
R24	0	0	0	0	0	1	1	1	0	0	0	1	1	0	1	0	18071Ah
R25	0	0	0	0	0	1	1	0	0	0	1	0	0	1	0	0	190624h
R26	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	1A0808h
R27	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1B0002h
R28	0	0	0	0	0	1	0	0	1	0	0	0	1	0	0	0	1C0488h
R29	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1D18C6h
R30	0	0	0	1	1	0	0	0	1	0	1	0	0	1	1	0	1E18C6h
R31	1	1	0	0	0	0	1	1	1	1	1	0	0	1	1	0	1FC3E6h
R32	0	0	0	0	0	1	0	1	1	0	1	1	1	1	1	1	2005BFh
R33	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	1	211E01h
R34	0	0	0	0	0	0	0	0	0	0	0	1	0	PLL_N[18:16]			220010h

Register Maps (continued)

REG.	DATA[15:0]																POR
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
R35	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	230004h
R36	PLL_N																240028h
R37	MASH_ SEED_EN	0	PFD_DLY_SEL						0	0	0	0	0	1	0	1	250205h
R38	PLL_DEN[31:16]																26FFFFh
R39	PLL_DEN[15:0]																27FFFFh
R40	MASH_SEED[31:16]																280000h
R41	MASH_SEED[15:0]																290000h
R42	PLL_NUM[31:16]																2A0000h
R43	PLL_NUM[15:0]																2B0000h
R44	0	0	OUTA_PWR						OUTB_ PD	OUTA_ PD	MASH_ RESET_N	0	0	MASH_ORDER			2C22A2h
R45	1	1	0	OUTA_MUX		1	1	0	0	0	OUTB_PWR						2DC622h
R46	0	0	0	0	0	1	1	1	1	1	1	1	0	0	OUTB_MUX		2E07F0h
R47	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	2F0300h
R48	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	3003E0h
R49	0	1	0	0	0	0	0	1	1	0	0	0	0	0	0	0	314180h
R50	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	320080h
R51	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	330080h
R52	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	1	340420h
R53	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	350000h
R54	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	360000h
R55	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	370000h
R56	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	380000h
R57	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	390000h
R58	INPIN_ IGNORE	INPIN_ HYST	INPIN_LVL		INPIN_FMT			0	0	0	0	0	0	0	0	1	3A8001h
R59	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	LD_TYPE	3B0001h
R60	LD_DLY																3C03E8h
R61	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0	3D00A8h
R62	DBLBUF_ EN_5	DBLBUF_ EN_4	DBLBUF_ EN_3	DBLBUF_ EN_2	DBLBUF_ EN_1	DBLBUF_ EN_0	0	0	1	0	1	0	1	1	1	1	3E00AFh
R63	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	3F0000h
R64	0	0	0	1	0	0	1	1	1	0	0	0	1	0	0	0	401388h
R65	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	410000h
R66	0	0	0	0	0	0	0	1	1	1	1	1	0	1	0	0	4201F4h
R67	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	430000h
R68	0	0	0	0	0	0	1	1	1	1	1	0	1	0	0	0	4403E8h
R69	MASH_RST_COUNT[31:16]																450000h
R70	MASH_RST_COUNT[15:0]																46C350h

Register Maps (continued)

REG.	DATA[15:0]																POR
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
R71	0	0	0	0	0	0	0	0	SYSREF_DIV_PRE			SYSREF_ PULSE	SYSREF_ EN	SYSREF_ REPEAT	0	1	470080h
R72	0	0	0	0	0	SYSREF_DIV											480001h
R73	0	0	0	0	JESD_DAC2_CTRL						JESD_DAC1_CTRL						49003Fh
R74	SYSREF_PULSE_CNT				JESD_DAC4_CTRL						JESD_DAC3_CTRL						4A0000h
R75	0	0	0	0	1	CHDIV					0	0	0	0	0	0	4B0800h
R76	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	4C000Ch
R77	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	4D0000h
R78	0	0	0	0	RAMP_ THRESH[32]	0	QUICK_ RECAL_EN	VCO_CAPCTRL_STRT								1	4E0064h
R79	RAMP_THRESH[31:16]																4F0000h
R80	RAMP_THRESH[15:0]																500000h
R81	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	RAMP_LIMIT_ HIGH[32]	510000h
R82	RAMP_LIMIT_HIGH[31:16]																520000h
R83	RAMP_LIMIT_HIGH[15:0]																530000h
R84	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	RAMP_LIMIT_ LOW[32]	540000h
R85	RAMP_LIMIT_LOW[31:16]																550000h
R86	RAMP_LIMIT_LOW[15:0]																560000h
R87	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	570000h
R88	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	580000h
R89	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	590000h
R90	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	5A0000h
R91	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	5B0000h
R92	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	5C0000h
R93	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	5D0000h
R94	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	5E0000h
R95	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	5F0000h
R96	RAMP_ BURST_EN	RAMP_BURST_COUNT													0	0	600000h
R97	RAMP0_RST	0	0	0	0	RAMP_TRIGB				RAMP_TRIGA				0	RAMP_BURST_TRIG		610000h
R98	RAMP0_INC[29:16]														0	RAMP0_DLY	620000h
R99	RAMP0_INC[15:0]																630000h
R100	RAMP0_LEN																640000h
R101	0	0	0	0	0	0	0	0	0	RAMP1_ DLY	RAMP1_ RST	RAMP0_ NEXT	0	0	RAMP0_NEXT_TRIG		650000h
R102	0	0	RAMP1_INC[29:16]														660000h
R103	RAMP1_INC[15:0]																670000h
R104	RAMP1_LEN																680000h

Register Maps (continued)

REG.	DATA[15:0]																POR
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
R105	RAMP_DLY_CNT										RAMP_ MANUAL	RAMP1_ NEXT	0	0	RAMP1_NEXT_TRIG		694440h
R106	0	0	0	0	0	0	0	0	0	0	0	RAMP_ TRIG_CAL	0	RAMP_SCALE_COUNT			6A0007h
R107	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	6B0000h
R108	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	6C0000h
R109	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	6D0000h
R110	0	0	0	0	0	rb_LD_VTUNE		0	rb_VCO_SEL			0	0	0	0	0	6E0000h
R111	0	0	0	0	0	0	0	0	rb_VCO_CAPCTRL								6F0000h
R112	0	0	0	0	0	0	0	rb_VCO_DACISET									700000h
R113	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	710000h
R114	0	1	1	1	1	FSK_EN	0	0	0	FSK_SPI_LEVEL		FSK_SPI_DEV_SEL			FSK_MODE_SEL		727800h
R115	0	0	0	0	0	0	0	0	FSK_DEV_SCALE					0	0	0	730000h
R116	FSK_DEV0																740000h
R117	FSK_DEV1																750000h
R118	FSK_DEV2																760000h
R119	FSK_DEV3																770000h
R120	FSK_DEV4																780000h
R121	FSK_DEV5																790000h
R122	FSK_DEV6																7A0000h
R123	FSK_DEV7																7B0000h
R124	FSK_SPI_FAST_DEV																7C0000h
R125	0	0	1	0	0	0	1	0	1	0	0	0	1	0	0	0	7D2288h

Table 7 lists the access codes for the LMX2572 registers.

Table 7. Access Type Codes

ACCESS TYPE	CODE	DESCRIPTION
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset

7.6.1 Register R0 (offset = 00h) [reset = 221Ch]

Figure 38. Register R0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RAMP_EN	VCO_PHASE_SYNC_EN	1	0	ADD_HOLD	0	OUT_MUTE	FCAL_HPFD_ADJ		FCAL_LPFD_ADJ		1	FCAL_EN	MUXOUT_LD_SEL	RESET	POWER DOWN
R/W-0h	R/W-0h	R/W-2h		R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h		R/W-1h	R/W-1h	R/W-1h	R/W-0h	R/W-0h

Table 8. Register R0 Field Descriptions

Bit	Field	Type	Reset	Description
15	RAMP_EN	R/W	0h	Enables frequency ramping. The action of programming register R0 with RAMP_EN = 1 starts the ramping. Be aware that this is in the same register as FCAL_EN, so toggling this bit also can active the ramping if RAMP_EN = 1. RAMP_EN applies to both automatic and manual ramping modes. 0: Normal operation 1: Starts frequency ramping
14	VCO_PHASE_SYNC_EN	R/W	0h	Enables phase sync mode. In this state, part of the channel divider is put in the feedback path to ensure deterministic phase. The action of toggling this bit from 0 to 1 also sends an asynchronous SYNC pulse. 0: Normal operation 1: Phase sync mode
13 - 12		R/W	2h	Program 2h to this field.
11	ADD_HOLD	R/W	0h	Freeze the register address in Block Programming. See Block Programming for details.
10		R/W	0h	Program 0h to this field.
9	OUT_MUTE	R/W	1h	Mutes RF outputs (RFoutA and RFoutB) when the VCO is calibrating. 0: Disabled 1: Muted
8 - 7	FCAL_HPFD_ADJ	R/W	0h	Set this field in accordance to the phase detector frequency for optimal VCO calibration. 0: $f_{PD} \leq 37.5$ MHz 1: 37.5 MHz < $f_{PD} \leq 75$ MHz 2: 75 MHz < $f_{PD} \leq 100$ MHz 3: $f_{PD} > 100$ MHz
6 - 5	FCAL_LPFD_ADJ	R/W	0h	Set this field in accordance to the phase detector frequency for optimal VCO calibration. 0: $f_{PD} \geq 10$ MHz 1: 10 MHz > $f_{PD} \geq 5$ MHz 2: 5 MHz > $f_{PD} \geq 2.5$ MHz 3: $f_{PD} < 2.5$ MHz
4		R/W	1h	Program 1h to this field.
3	FCAL_EN	R/W	1h	Enables and activates VCO frequency calibration. Writing register R0 with this bit set to a 1 enables and triggers the VCO frequency calibration. Writing 0 to this field is prohibited. 0: Invalid 1: Enabled

Table 8. Register R0 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	MUXOUT_LD_SEL	R/W	1h	Selects the functionality of the MUXout pin. 0: Register readback 1: Lock detect
1	RESET	R/W	0h	Resets all registers to silicon default values. This bit is self-clearing. 0: Normal operation 1: Reset
0	POWERDOWN	R/W	0h	Powers down the device. 0: Normal operation 1: Power down

7.6.2 Register R1 (offset = 01h) [reset = 0808h]

Figure 39. Register R1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1	0	0	0	0	0	0	0	1	CAL_CLK_DIV		
R/W-101h													R/W-0h		

Table 9. Register R1 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 3		R/W	101h	Program 101h to this field.
2 - 0	CAL_CLK_DIV	R/W	0h	Divides down the state machine clock during VCO calibration. Maximum state machine clock frequency is 200 MHz. State machine clock frequency = f_{OSCin} / ($2^{CAL\_CLK\_DIV}$). 0: $f_{OSCin} \leq 200$ MHz 1: 200 MHz < $f_{OSCin} \leq 250$ MHz All other values are not used.

7.6.3 Register R2 (offset = 02h) [reset = 0500h]

Figure 40. Register R2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0
R/W-500h															

Table 10. Register R2 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0		R/W	500h	Program 500h to this field. After programming R0 with RESET = 1, no need to program this register.

7.6.4 Register R3 (offset = 03h) [reset = 0782h]

Figure 41. Register R3

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	1	1	1	1	0	0	0	0	0	1	0
R/W-782h															

Table 11. Register R3 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0		R/W	782h	Program 782h to this field. After programming R0 with RESET = 1, no need to program this register.

7.6.5 Register R4 (offset = 04h) [reset = 0A43h]

Figure 42. Register R4

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1	0	1	0	0	1	0	0	0	0	1	1
R/W-A43h															

Table 12. Register R4 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0		R/W	A43h	Program A43h to this field. After programming R0 with RESET = 1, no need to program this register.

7.6.6 Register R5 (offset = 05h) [reset = 30C8h]

Figure 43. Register R5

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	IPBUF_TYPE	IPBUF_TERM	0	0	0	1	1	0	0	1	0	0	0
R/W-1h			R/W-1h	R/W-0h	R/W-C8h										

Table 13. Register R5 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 13		R/W	1h	Program 1h to this field.
12	IPBUF_TYPE	R/W	1h	Selects OSCin input type. 0: Differential input 1: Single-ended input
11	IPBUF_TERM	R/W	0h	Enables internal 50-Ω terminations on both OSCin and OSCin* pins. This function is valid even if OSCin input is configured as single-ended input. 0: Normal operation 1: OSCin and OSCin* pins are internally 50-Ω terminated
10 - 0		R/W	C8h	Program C8h to this field.

7.6.7 Register R6 (offset = 06h) [reset = C802h]

Figure 44. Register R6

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LDO_DLY					0	0	0	0	0	0	0	0	0	1	0
R/W-19h					R/W-2h										

Table 14. Register R6 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 11	LDO_DLY	R/W	19h	LDO start up delay. Delay duration is a function of state machine clock. See Power-Up, Wake-Up Time for details.
10 - 0		R/W	2h	Program 2h to this field.

7.6.8 Register R7 (offset = 07h) [reset = 00B2h]

Figure 45. Register R7

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	OUT_FORCE	0	0	0	0	0	0	1	0	1	1	0	0	1	0
R/W-0h	R/W-0h	R/W-B2h													

Table 15. Register R7 Field Descriptions

Bit	Field	Type	Reset	Description
15		R/W	0h	Program 0h to this field.
14	OUT_FORCE	R/W	0h	Forces the RF outputs not to be automatically muted during VCO calibration. This bit should be enabled during frequency ramping. 0: Mute setting depends on OUT_MUTE 1: No mute during VCO calibration
13 - 0		R/W	B2h	Program B2h to this field.

7.6.9 Register R8 (offset = 08h) [reset = 2000h]

Figure 46. Register R8

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	VCO_DACISET_FORCE	1	0	VCO_CAPCTRL_FORCE	0	0	0	0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-2h		R/W-0h	R/W-0h										

Table 16. Register R8 Field Descriptions

Bit	Field	Type	Reset	Description
15		R/W	0h	Program 0h to this field.
14	VCO_DACISET_FORCE	R/W	0h	Forces VCO_DACISET value. Useful for fully-assisted VCO calibration and debugging purposes. 0: Normal operation 1: Use VCO_DACISET value instead of the value obtained from VCO calibration
13 - 12		R/W	2h	Program 2h to this field.
11	VCO_CAPCTRL_FORCE	R/W	0h	Forces VCO_CAPCTRL value. Useful for fully-assisted VCO calibration and debugging purposes. 0: Normal operation 1: Use VCO_CAPCTRL value instead of the value obtained from VCO calibration
10 - 0		R/W	0h	Program 0h to this field.

7.6.10 Register R9 (offset = 09h) [reset = 0004h]

Figure 47. Register R9

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	MULT_HI	0	OSC_2X	0	0	0	0	0	0	0	0	0	1	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-4h											

Table 17. Register R9 Field Descriptions

Bit	Field	Type	Reset	Description
15		R/W	0h	Program 0h to this field.
14	MULT_HI	R/W	0h	Sets this bit to 1 if the output frequency of the Multiplier is greater than 100 MHz. 0: Multiplier output ≤ 100 MHz 1: Multiplier output > 100 MHz
13		R/W	0h	Program 0h to this field.
12	OSC_2X	R/W	0h	Enables reference path Doubler. 0: Disabled 1: Enabled
11 - 0		R/W	4h	Program 4h to this field.

7.6.11 Register R10 (offset = 0Ah) [reset = 10F8h]

Figure 48. Register R10

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	MULT					1	1	1	1	0	0	0
R/W-1h				R/W-1h					R/W-78h						

Table 18. Register R10 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 12		R/W	1h	Program 1h to this field.
11 - 7	MULT	R/W	1h	Reference path frequency Multiplier. Input frequency to the Multiplier: 10 to 40 MHz. Multiplier output frequency: 60 to 150 MHz. 0: Not used 1: Bypassed 2: Not recommended. Use OSC_2X instead of MULT 3: 3X ….. 7: 7X 8 - 31: Not recommended
6 - 0		R/W	78h	Program 78h to this field.

7.6.12 Register R11 (offset = 0Bh) [reset = B018h]

Figure 49. Register R11

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1	1	PLL_R								1	0	0	0
R/W-Bh				R/W-1h								R/W-8h			

Table 19. Register R11 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 12		R/W	Bh	Program Bh to this field.
11 - 4	PLL_R	R/W	1h	Reference path Post-R divider. It is the divider after the frequency Multiplier.
3 - 0		R/W	8h	Program 8h to this field.

7.6.13 Register R12 (offset = 0Ch) [reset = 5001h]

Figure 50. Register R12

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	1	PLL_R_PRE											
R/W-5h				R/W-1h											

Table 20. Register R12 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 12		R/W	5h	Program 5h to this field.
11 - 0	PLL_R_PRE	R/W	1h	Reference path Pre-R divider. It is the divider before the frequency Multiplier.

7.6.14 Register R13 (offset = 0Dh) [reset = 4000h]

Figure 51. Register R13

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W-4000h															

Table 21. Register R13 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0		R/W	4000h	Program 4000h to this field. After programming R0 with RESET = 1, no need to program this register.

7.6.15 Register R14 (offset = 0Eh) [reset = 1840h]

Figure 52. Register R14

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	1	0	0	0	0	CPG				0	0	0
R/W-30h									R/W-8h				R/W-0h		

Table 22. Register R14 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 7		R/W	30h	Program 30h to this field.
6 - 3	CPG	R/W	8h	Effective charge pump gain. This is the sum of the up and down currents. Each increment represents 625 µA. 0: Tri-state 1: 625 µA 2: 1250 µA 3: 1875 µA ….. 15: 6875 µA
2 - 0		R/W	0h	Program 0h to this field.

7.6.16 Register R15 (offset = 0Fh) [reset = 060Eh]

Figure 53. Register R15

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	1	1	0	0	0	0	0	1	1	1	0
R/W-60Eh															

Table 23. Register R15 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0		R/W	60Eh	Program 60Eh to this field. After programming R0 with RESET = 1, no need to program this register.

7.6.17 Register R16 (offset = 10h) [reset = 0080h]

Figure 54. Register R16

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	VCO_DACISET								
R/W-0h							R/W-80h								

Table 24. Register R16 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 9		R/W	0h	Program 0h to this field.
8 - 0	VCO_DACISET	R/W	80h	Programmable current setting for the VCO that is applied when VCO_DACISET_FORCE = 1. Useful for fully-assisted VCO calibration.

7.6.18 Register R17 (offset = 11h) [reset = 0096h]

Figure 55. Register R17

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	VCO_DACISET_STRT								
R/W-0h							R/W-96h								

Table 25. Register R17 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 9		R/W	0h	Program 0h to this field.
8 - 0	VCO_DACISET_STRT	R/W	96h	Starting calibration value for VCO_DACISET.

7.6.19 Register R18 (offset = 12h) [reset = 0064h]

Figure 56. Register R18

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0
R/W-64h															

Table 26. Register R18 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0		R/W	64h	Program 64h to this field. After programming R0 with RESET = 1, no need to program this register.

7.6.20 Register R19 (offset = 13h) [reset = 27B7h]

Figure 57. Register R19

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	0	0	1	1	1	VCO_CAPCTRL							
R/W-27h								R/W-B7h							

Table 27. Register R19 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8		R/W	27h	Program 27h to this field.
7 - 0	VCO_CAPCTRL	R/W	B7h	Programmable band within VCO core that applies when VCO_CAPCTRL_FORCE = 1. Valid values are 183 to 0, where the higher number is a lower frequency.

7.6.21 Register R20 (offset = 14h) [reset = 3048h]

Figure 58. Register R20

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	VCO_SEL			VCO_SEL_FORCE	0	0	0	1	0	0	1	0	0	0
R/W-0h		R/W-6h			R/W-0h	R/W-48h									

Table 28. Register R20 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 14		R/W	0h	Program 1h to this field.
13 - 11	VCO_SEL	R/W	6h	User specified start VCO for calibration. This sets the VCO that is used when VCO_SEL_FORCE = 1. 1: VCO1 2: VCO2 ….. 6: VCO6 All other values are not used.
10	VCO_SEL_FORCE	R/W	0h	Forces the VCO to use the core specified by VCO_SEL. 0: Disabled 1: Enabled
9 - 0		R/W	48h	Program 48h to this field.

7.6.22 Register R21 (offset = 15h) [reset = 0409h]

Figure 59. Register R21

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	1
R/W-409h															

Table 29. Register R21 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0		R/W	409h	Program 409h to this field. After programming R0 with RESET = 1, no need to program this register.

7.6.23 Register R22 (offset = 16h) [reset = 0001h]

Figure 60. Register R22

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W-1h															

Table 30. Register R22 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0		R/W	1h	Program 1h to this field. After programming R0 with RESET = 1, no need to program this register.

7.6.24 Register R23 (offset = 17h) [reset = 007Ch]

Figure 61. Register R23

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	0
R/W-7Ch															

Table 31. Register R23 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0		R/W	7Ch	Program 7Ch to this field. After programming R0 with RESET = 1, no need to program this register.

7.6.25 Register R24 (offset = 18h) [reset = 071Ah]

Figure 62. Register R24

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	1	1	1	0	0	0	1	1	0	1	0
R/W-71Ah															

Table 32. Register R24 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0		R/W	71Ah	Program 71Ah to this field. After programming R0 with RESET = 1, no need to program this register.

7.6.26 Register R25 (offset = 19h) [reset = 0624h]

Figure 63. Register R25

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	1	1	0	0	0	1	0	0	1	0	0
R/W-624h															

Table 33. Register R25 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0		R/W	624h	Program 624h to this field. After programming R0 with RESET = 1, no need to program this register.

7.6.27 Register R26 (offset = 1Ah) [reset = 0808h]

Figure 64. Register R26

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0
R/W-808h															

Table 34. Register R26 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0		R/W	808h	Program 808h to this field. After programming R0 with RESET = 1, no need to program this register.

7.6.28 Register R27 (offset = 1Bh) [reset = 0002h]

Figure 65. Register R27

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
R/W-2h															

Table 35. Register R27 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0		R/W	2h	Program 2h to this field. After programming R0 with RESET = 1, no need to program this register.

7.6.29 Register R28 (offset = 1Ch) [reset = 0488h]

Figure 66. Register R28

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	1	0	0	1	0	0	0	1	0	0	0
R/W-488h															

Table 36. Register R28 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0		R/W	488h	Program 488h to this field. After programming R0 with RESET = 1, no need to program this register.

7.6.30 Register R29 (offset = 1Dh) [reset = 18C6h]

Figure 67. Register R29

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W-18C6h															

Table 37. Register R29 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0		R/W	18C6h	Program 0h to this field.

7.6.31 Register R30 (offset = 1Eh) [reset = 18C6h]

Figure 68. Register R30

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	1	0	0	0	1	0	1	0	0	1	1	0
R/W-18C6h															

Table 38. Register R30 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0		R/W	18C6h	Program 18A6h to this field.

7.6.32 Register R31 (offset = 1Fh) [reset = C3E6h]

Figure 69. Register R31

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	0	0	0	1	1	1	1	1	0	0	1	1	0
R/W-C3E6h															

Table 39. Register R31 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0		R/W	C3E6h	Program C3E6h to this field. After programming R0 with RESET = 1, no need to program this register.

7.6.33 Register R32 (offset = 20h) [reset = 05BFh]

Figure 70. Register R32

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	1	0	1	1	0	1	1	1	1	1	1
R/W-5BFh															

Table 40. Register R32 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0		R/W	5BFh	Program 5BFh to this field. After programming R0 with RESET = 1, no need to program this register.

7.6.34 Register R33 (offset = 21h) [reset = 1E01h]

Figure 71. Register R33

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	1
R/W-1E01h															

Table 41. Register R33 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0		R/W	1E01h	Program 1E01h to this field. After programming R0 with RESET = 1, no need to program this register.

7.6.35 Register R34 (offset = 22h) [reset = 0010h]

Figure 72. Register R34

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	1	0	PLL_N[18:16]		
R/W-2h													R/W-0h		

Table 42. Register R34 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 3		R/W	2h	Program 2h to this field.
2 - 0	PLL_N[18:16]	R/W	0h	Upper 3 bits of N-divider.

7.6.36 Register R35 (offset = 23h) [reset = 0004h]

Figure 73. Register R35

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
R/W-4h															

Table 43. Register R35 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0		R/W	4h	Program 4h to this field. After programming R0 with RESET = 1, no need to program this register.

7.6.37 Register R36 (offset = 24h) [reset = 0028h]

Figure 74. Register R36

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PLL_N															
R/W-28h															

Table 44. Register R36 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	PLL_N	R/W	28h	Lower 16 bits of N-divider.

7.6.38 Register R37 (offset = 25h) [reset = 0205h]

Figure 75. Register R37

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASH_SEED_EN	0	PFD_DLY_SEL						0	0	0	0	0	1	0	1
R/W-0h	R/W-0h	R/W-2h						R/W-5h							

Table 45. Register R37 Field Descriptions

Bit	Field	Type	Reset	Description
15	MASH_SEED_EN	R/W	0h	Enables the MASH_SEED value to be used. This can be used for programmable phase stepping or fractional spur optimization. 0: Disabled 1: Enabled
14		R/W	0h	Program 0h to this field.
13 - 8	PFD_DLY_SEL	R/W	2h	PFD_DLY_SEL must be adjusted in accordance to the N-divider value. See Table 3 for details.
7 - 0		R/W	5h	Program 5h to this field.

7.6.39 Register R38 (offset = 26h) [reset = FFFFh]

Figure 76. Register R38

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PLL_DEN[31:16]															
R/W-FFFFh															

Table 46. Register R38 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	PLL_DEN[31:16]	R/W	FFFFh	Upper 16 bits of fractional denominator (DEN).

7.6.40 Register R39 (offset = 27h) [reset = FFFFh]

Figure 77. Register R39

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PLL_DEN[15:0]															
R/W-FFFFh															

Table 47. Register R39 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	PLL_DEN[15:0]	R/W	FFFFh	Lower 16 bits of fractional denominator (DEN).

7.6.41 Register R40 (offset = 28h) [reset = 0000h]

Figure 78. Register R40

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASH_SEED[31:16]															
R/W-0h															

Table 48. Register R40 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	MASH_SEED[31:16]	R/W	0h	Upper 16 bits of MASH_SEED. MASH_SEED sets the initial state of the fractional engine. Useful for producing a phase shift and fractional spur optimization.

7.6.42 Register R41 (offset = 29h) [reset = 0000h]

Figure 79. Register R41

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASH_SEED[15:0]															
R/W-0h															

Table 49. Register R41 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	MASH_SEED[15:0]	R/W	0h	Lower 16 bits of MASH_SEED. MASH_SEED sets the initial state of the fractional engine. Useful for producing a phase shift and fractional spur optimization.

7.6.43 Register R42 (offset = 2Ah) [reset = 0000h]

Figure 80. Register R42

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PLL_NUM[31:16]															
R/W-0h															

Table 50. Register R42 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	PLL_NUM[31:16]	R/W	0h	Upper 16 bits of fractional numerator (NUM).

7.6.44 Register R43 (offset = 2Bh) [reset = 0000h]

Figure 81. Register R43

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PLL_NUM[15:0]															
R/W-0h															

Table 51. Register R43 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	PLL_NUM[15:0]	R/W	0h	Lower 16 bits of fractional numerator (NUM).

7.6.45 Register R44 (offset = 2Ch) [reset = 22A2h]

Figure 82. Register R44

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	OUTA_PWR						OUTB_PD	OUTA_PD	MASH_RESET_N	0	0	MASH_ORDER		
R/W-0h		R/W-22h						R/W-1h	R/W-0h	R/W-1h	R/W-0h		R/W-2h		

Table 52. Register R44 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 14		R/W	0h	Program 0h to this field.
13 - 8	OUTA_PWR	R/W	22h	Adjusts RFoutA output power. Higher numbers give more output power.
7	OUTB_PD	R/W	1h	Powers down RF output B. 0: Normal operation 1: Power down
6	OUTA_PD	R/W	0h	Powers down RF output A. 0: Normal operation 1: Power down
5	MASH_RESET_N	R/W	1h	Resets MASH. 0: Reset 1: Normal operation
4 - 3		R/W	0h	Program 0h to this field.
2 - 0	MASH_ORDER	R/W	2h	Sets the MASH order. 0: Integer mode 1: First order modulator 2: Second order modulator 3: Third order modulator 4: Fourth order modulator 5 - 7: Not used

7.6.46 Register R45 (offset = 2Dh) [reset = C622h]

Figure 83. Register R45

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	OUTA_MUX		1	1	0	0	0	OUTB_PWR					
R/W-6h			R/W-0h				R/W-18h			R/W-22h					

Table 53. Register R45 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 13		R/W	6h	Program 6h to this field.
12 - 11	OUTA_MUX	R/W	0h	Selects the input source to RFoutA. 0: Channel divider 1: VCO 2: Not used 3: High impedance
10 - 6		R/W	18h	Program 18h to this field.
5 - 0	OUTB_PWR	R/W	22h	Adjusts RFoutB output power. Higher numbers give more output power.

7.6.47 Register R46 (offset = 2Eh) [reset = 07F0h]

Figure 84. Register R46

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	1	1	1	1	1	1	1	0	0	OUTB_MUX	
R/W-1FCh														R/W-0h	

Table 54. Register R46 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 2		R/W	1FCh	Program 1FCh to this field.
1 - 0	OUTB_MUX	R/W	0h	Selects the input source to RFoutB. 0: Channel divider 1: VCO 2: SYSREF 3: High impedance

7.6.48 Register R47 (offset = 2Fh) [reset = 0300h]

Figure 85. Register R47

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0
R/W-300h															

Table 55. Register R47 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0		R/W	300h	Program 300h to this field. After programming R0 with RESET = 1, no need to program this register.

7.6.49 Register R48 (offset = 30h) [reset = 03E0h]

Figure 86. Register R48

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0
R/W-3E0h															

Table 56. Register R48 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0		R/W	3E0h	Program 3E0h to this field. After programming R0 with RESET = 1, no need to program this register.

7.6.50 Register R49 (offset = 31h) [reset = 4180h]

Figure 87. Register R49

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	0	0	0	0	1	1	0	0	0	0	0	0	0
R/W-4180h															

Table 57. Register R49 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0		R/W	4180h	Program 4180h to this field. After programming R0 with RESET = 1, no need to program this register.

7.6.51 Register R50 (offset = 32h) [reset = 0080h]

Figure 88. Register R50

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
R/W-80h															

Table 58. Register R50 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0		R/W	80h	Program 80h to this field. After programming R0 with RESET = 1, no need to program this register.

7.6.52 Register R51 (offset = 33h) [reset = 0080h]

Figure 89. Register R51

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
R/W-80h															

Table 59. Register R51 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0		R/W	80h	Program 80h to this field. After programming R0 with RESET = 1, no need to program this register.

7.6.53 Register R52 (offset = 34h) [reset = 0420h]

Figure 90. Register R52

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	1
R/W-420h															

Table 60. Register R52 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0		R/W	420h	Program 421h to this field.

7.6.54 Register R53 (offset = 35h) [reset = 0000h]

Figure 91. Register R53

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W-0h															

Table 61. Register R53 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0		R/W	0h	Program 0h to this field. After programming R0 with RESET = 1, no need to program this register.

7.6.55 Register R54 (offset = 36h) [reset = 0000h]

Figure 92. Register R54

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W-0h															

Table 62. Register R54 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0		R/W	0h	Program 0h to this field. After programming R0 with RESET = 1, no need to program this register.

7.6.56 Register R55 (offset = 37h) [reset = 0000h]

Figure 93. Register R55

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W-0h															

Table 63. Register R55 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0		R/W	0h	Program 0h to this field. After programming R0 with RESET = 1, no need to program this register.

7.6.57 Register R56 (offset = 38h) [reset = 0000h]

Figure 94. Register R56

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W-0h															

Table 64. Register R56 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0		R/W	0h	Program 0h to this field. After programming R0 with RESET = 1, no need to program this register.

7.6.58 Register R57 (offset = 39h) [reset = 0000h]

Figure 95. Register R57

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
R/W-0h															

Table 65. Register R57 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0		R/W	0h	Program 20h to this field.

7.6.59 Register R58 (offset = 3Ah) [reset = 8001h]

Figure 96. Register R58

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INPIN_IGNORE	INPIN_HYST	INPIN_LVL		INPIN_FMT			0	0	0	0	0	0	0	0	1
R/W-1h	R/W-0h	R/W-0h		R/W-0h			R/W-1h								

Table 66. Register R58 Field Descriptions

Bit	Field	Type	Reset	Description
15	INPIN_IGNORE	R/W	1h	Ignore SYNC and SysRefReq pins when VCO_PHASE_SYNC = 0. This bit should be set to 1 unless VCO_PHASE_SYNC = 1.
14	INPIN_HYST	R/W	0h	Enables high hysteresis for LVDS input to SysRefReq and SYNC pin. 0: Disabled 1: Enabled
13 - 12	INPIN_LVL	R/W	0h	Sets bias level for LVDS input to SysRefReq and SYNC pin. 0: Vin / 4 1: Vin 2: Vin / 2 3: Invalid
11 - 9	INPIN_FMT	R/W	0h	Defines the input format of SysRefReq and SYNC pin. 0: SYNC = SysRefReq = CMOS 1: SYNC = LVDS; SysRefReq = CMOS 2: SYNC = CMOS; SysRefReq = LVDS 3: SYNC = SysRefReq = LVDS 4: SYNC = SysRefReq = CMOS 5: SYNC = LVDS (filtered); SysRefReq = CMOS 6: SYNC = CMOS; SysRefReq = LVDS (filtered) 7: SYNC = SysRefReq = LVDS (filtered)
8 - 0		R/W	1h	Program 1h to this field.

7.6.60 Register R59 (offset = 3Bh) [reset = 0001h]

Figure 97. Register R59

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	LD_TYPE
R/W-0h															R/W-1h

Table 67. Register R59 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 1		R/W	0h	Program 0h to this field.
0	LD_TYPE	R/W	1h	Defines lock detect type. 0: VCOCal. Lock detect asserts a HIGH output after the VCO has finished calibration and the LD_DLY timeout counter is finished. 1: Vtune and VCOCal. Lock detect asserts a HIGH output when VCOCal lock detect would assert a HIGH signal and the tuning voltage to the VCO is within acceptable limits.

7.6.61 Register R60 (offset = 3Ch) [reset = 03E8h]

Figure 98. Register R60

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LD_DLY															
R/W-3E8h															

Table 68. Register R60 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	LD_DLY	R/W	3E8h	For the VCOCal lock detect, this is the delay in ¼ f_{PD} cycles that is added after the calibration is finished before the VCOCal lock detect is asserted HIGH.

7.6.62 Register R61 (offset = 3Dh) [reset = 00A8h]

Figure 99. Register R61

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0
R/W-A8h															

Table 69. Register R61 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0		R/W	A8h	Program A8h to this field. After programming R0 with RESET = 1, no need to program this register.

7.6.63 Register R62 (offset = 3Eh) [reset = 00AFh]

Figure 100. Register R62

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DBLBUF_EN_5	DBLBUF_EN_4	DBLBUF_EN_3	DBLBUF_EN_2	DBLBUF_EN_1	DBLBUF_EN_0	0	0	1	0	1	0	1	1	1	1
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-AFh									

Table 70. Register R62 Field Descriptions

Bit	Field	Type	Reset	Description
15	DBLBUF_EN_5	R/W	0h	Enables double buffering for the MASH order. 0: Disabled 1: Enabled
14	DBLBUF_EN_4	R/W	0h	Enables double buffering for fractional numerator NUM. 0: Disabled 1: Enabled
13	DBLBUF_EN_3	R/W	0h	Enables double buffering for the integer portion of the N-divider. 0: Disabled 1: Enabled
12	DBLBUF_EN_2	R/W	0h	Enables double buffering for the Pre-R and Post-R dividers in the reference path. Effective only if DBL_BUF_EN_3 = 1. 0: Disabled 1: Enabled
11	DBLBUF_EN_1	R/W	0h	Enables double buffering for the Multiplier in the reference path. Effective only if DBL_BUF_EN_3 = 1. 0: Disabled 1: Enabled
10	DBLBUF_EN_0	R/W	0h	Enables double buffering for the Doubler in the reference path. Effective only if DBL_BUF_EN_3 = 1. 0: Disabled 1: Enabled
9 - 0		R/W	AFh	Program AFh to this field.

7.6.64 Register R63 (offset = 3Fh) [reset = 0000h]

Figure 101. Register R63

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W-0h															

Table 71. Register R63 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0		R/W	0h	Program 0h to this field. After programming R0 with RESET = 1, no need to program this register.

7.6.65 Register R64 (offset = 40h) [reset = 1388h]

Figure 102. Register R64

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	0	0	1	1	1	0	0	0	1	0	0	0
R/W-1388h															

Table 72. Register R64 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0		R/W	1388h	Program 1388h to this field. After programming R0 with RESET = 1, no need to program this register.

7.6.66 Register R65 (offset = 41h) [reset = 0000h]

Figure 103. Register R65

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W-0h															

Table 73. Register R65 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0		R/W	0h	Program 0h to this field. After programming R0 with RESET = 1, no need to program this register.

7.6.67 Register R66 (offset = 42h) [reset = 01F4h]

Figure 104. Register R66

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	1	1	1	1	1	0	1	0	0
R/W-1F4h															

Table 74. Register R66 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0		R/W	1F4h	Program 1F4h to this field. After programming R0 with RESET = 1, no need to program this register.

7.6.68 Register R67 (offset = 43h) [reset = 0000h]

Figure 105. Register R67

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W-0h															

Table 75. Register R67 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0		R/W	0h	Program 0h to this field. After programming R0 with RESET = 1, no need to program this register.

7.6.69 Register R68 (offset = 44h) [reset = 03E8h]

Figure 106. Register R68

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	1	1	1	1	0	1	0	0	0
R/W-3E8h															

Table 76. Register R68 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0		R/W	3E8h	Program 3E8h to this field. After programming R0 with RESET = 1, no need to program this register.

7.6.70 Register R69 (offset = 45h) [reset = 0000h]

Figure 107. Register R69

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASH_RST_COUNT[31:16]															
R/W-0h															

Table 77. Register R69 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	MASH_RST_COUNT [31:16]	R/W	0h	Upper 16 bits of MASH_RST_COUNT. This register is used to add a delay when using phase SYNC. The delay should be set at least four times the PLL lock time. This delay is expressed in state machine clock periods. One of these periods is equal to $2^{CAL\_CLK\_DIV}$ / f_{OSCin}.

7.6.71 Register R70 (offset = 46h) [reset = C350h]

Figure 108. Register R70

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASH_RST_COUNT[15:0]															
R/W-C350h															

Table 78. Register R70 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	MASH_RST_COUNT [15:0]	R/W	C350h	Lower 16 bits of MASH_RST_COUNT.

7.6.72 Register R71 (offset = 47h) [reset = 0080h]

Figure 109. Register R71

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	SYSREF_DIV_PRE			SYSREF_PULSE	SYSREF_EN	SYSREF_REPEAT	0	1
R/W-0h								R/W-4h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	

Table 79. Register R71 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8		R/W	0h	Program 0h to this field.
7 - 5	SYSREF_DIV_PRE	R/W	4h	This divider is used to get the frequency input to the Post-SR divider within acceptable limits. See Application for SYSREF for details. 2: Divide by 2 4: Divide by 4 All other values are invalid.
4	SYSREF_PULSE	R/W	0h	When in master mode (SYSREF_REPEAT = 0), this allows multiple pulses (as determined by SYSREF_PULSE_CNT) to be sent out whenever the SysRefReq pin goes high. 0: Disabled 1: Enabled
3	SYSREF_EN	R/W	0h	Enables SYSREF mode. 0: Disabled 1: Enabled
2	SYSREF_REPEAT	R/W	0h	Defines SYSREF mode. 0: Master mode. In this mode, SYSREF pulses are generated continuously at the output. 1: Repeater Mode. In this mode, SYSREF pulses are generated in response to the SysRefReq pin.
1 - 0		R/W	0h	Program 1h to this field.

7.6.73 Register R72 (offset = 48h) [reset = 0001h]

Figure 110. Register R72

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	SYSREF_DIV										
R/W-0h					R/W-1h										

Table 80. Register R72 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 11		R/W	0h	Program 0h to this field.
10 - 0	SYSREF_DIV	R/W	1h	This divider further divides the output frequency for the SYSREF. See Application for SYSREF for details.

7.6.74 Register R73 (offset = 49h) [reset = 003Fh]

Figure 111. Register R73

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	JESD_DAC2_CTRL						JESD_DAC1_CTRL					
R/W-0h				R/W-0h						R/W-3Fh					

Table 81. Register R73 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 12		R/W	0h	Program 0h to this field.
11 - 6	JESD_DAC2_CTRL	R/W	0h	Programmable delay adjustment for SYSREF mode.
5 - 0	JESD_DAC1_CTRL	R/W	3Fh	Programmable delay adjustment for SYSREF mode.

7.6.75 Register R74 (offset = 4Ah) [reset = 0000h]

Figure 112. Register R74

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYSREF_PULSE_CNT				JESD_DAC4_CTRL						JESD_DAC3_CTRL					
R/W-0h				R/W-0h						R/W-0h					

Table 82. Register R74 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 12	SYSREF_PULSE_CNT	R/W	0h	Used in SYSREF_REPEAT mode to define how many pulses are sent.
11 - 6	JESD_DAC4_CTRL	R/W	0h	Programmable delay adjustment for SYSREF mode.
5 - 0	JESD_DAC3_CTRL	R/W	0h	Programmable delay adjustment for SYSREF mode.

7.6.76 Register R75 (offset = 4Bh) [reset = 0800h]

Figure 113. Register R75

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1	CHDIV					0	0	0	0	0	0
R/W-1h					R/W-0h					R/W-0h					

Table 83. Register R75 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 11		R/W	1h	Program 1h to this field.
10 - 6	CHDIV	R/W	0h	Channel divider. 0: Divide by 2 1: Divide by 4 3: Divide by 8 5: Divide by 16 7: Divide by 32 9: Divide by 64 12: Divide by 128 14: Divide by 256 All other values are not used.
5 - 0		R/W	0h	Program 0h to this field.

7.6.77 Register R76 (offset = 4Ch) [reset = 000Ch]

Figure 114. Register R76

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0
R/W-Ch															

Table 84. Register R76 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0		R/W	Ch	Program Ch to this field. After programming R0 with RESET = 1, no need to program this register.

7.6.78 Register R77 (offset = 4Dh) [reset = 0000h]

Figure 115. Register R77

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W-0h															

Table 85. Register R77 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0		R/W	0h	Program 0h to this field. After programming R0 with RESET = 1, no need to program this register.

7.6.79 Register R78 (offset = 4Eh) [reset = 0064h]

Figure 116. Register R78

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	RAMP_THRESH[32]	0	QUICK_RECAL_EN	VCO_CAPCTRL_STRT								1
R/W-0h				R/W-0h	R/W-0h	R/W-0h	R/W-32h								R/W-0h

Table 86. Register R78 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 12		R/W	0h	Program 0h to this field.
11	RAMP_THRESH[32]	R/W	0h	The 33rd bit of RAMP_THRESH. RAMP_THRESH sets how much the ramp can change the VCO frequency before a VCO calibration is required. If the frequency is chosen to be Δf, then RAMP_THRESH = $(\Delta f / f_{PD}) \times 2^{24}$.
10		R/W	0h	Program 0h to this field.
9	QUICK_RECAL_EN	R/W	0h	This sets the initial VCO starting calibration values. Especially useful if the frequency change is smaller, say < 50 MHz or so. 0: Calibration starts with VCO_SEL, VCO_CAPCTRL_START, VCO_DACISET_START 1: Calibration starts with the current value
8 - 1	VCO_CAPCTRL_STRT	R/W	32h	This sets the starting VCO_CAPCTRL value that is used for VCO frequency calibration. Smaller values yield a higher frequency band within a VCO core. Valid number range is 0 to 183.
0		R/W	0h	Program 1h to this field.

7.6.80 Register R79 (offset = 4Fh) [reset = 0000h]

Figure 117. Register R79

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RAMP_THRESH[31:16]															
R/W-0h															

Table 87. Register R79 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RAMP_THRESH[31:16]	R/W	0h	Upper 16 bits of RAMP_THRESH. See Table 86 for description.

7.6.81 Register R80 (offset = 50h) [reset = 0000h]

Figure 118. Register R80

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RAMP_THRESH[15:0]															
R/W-0h															

Table 88. Register R80 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RAMP_THRESH[15:0]	R/W	0h	Lower 16 bits of RAMP_THRESH. See Table 86 for description.

7.6.82 Register R81 (offset = 51h) [reset = 0000h]

Figure 119. Register R81

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	RAMP_LIMIT_HIGH[32]
R/W-0h															R/W-0h

Table 89. Register R81 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 1		R/W	0h	Program 0h to this field.
0	RAMP_LIMIT_HIGH[32]	R/W	0h	The 33rd bit of RAMP_LIMIT_HIGH. RAMP_LIMIT_HIGH sets a maximum frequency that the ramp cannot exceed so that the VCO does not get set beyond a valid frequency range. Suppose f_{HIGH} is this frequency and f_{VCO} is the starting VCO frequency, then: $f_{HIGH} \geq f_{VCO}$; RAMP_LIMIT_HIGH = $2^{24} \times (f_{HIGH} - f_{VCO}) / f_{PD}$

7.6.83 Register R82 (offset = 52h) [reset = 0000h]

Figure 120. Register R82

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RAMP_LIMIT_HIGH[31:16]															
R/W-0h															

Table 90. Register R82 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RAMP_LIMIT_HIGH [31:16]	R/W	0h	Upper 16 bits of RAMP_LIMIT_HIGH. See Table 89 for description.

7.6.84 Register R83 (offset = 53h) [reset = 0000h]

Figure 121. Register R83

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RAMP_LIMIT_HIGH[15:0]															
R/W-0h															

Table 91. Register R83 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RAMP_LIMIT_HIGH[15:0]	R/W	0h	Lower 16 bits of RAMP_LIMIT_HIGH. See Table 89 for description.

7.6.85 Register R84 (offset = 54h) [reset = 0000h]

Figure 122. Register R84

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	RAMP_LIMIT_LOW[32]
R/W-0h															R/W-0h

Table 92. Register R84 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 1		R/W	0h	Program 0h to this field.
0	RAMP_LIMIT_LOW[32]	R/W	0h	The 33rd bit of RAMP_LIMIT_LOW. RAMP_LIMIT_LOW sets a minimum frequency that the ramp cannot exceed so that the VCO does not get set beyond a valid frequency range. Suppose f_{LOW} is this frequency and f_{VCO} is the starting VCO frequency, then: $f_{LOW} \leq f_{VCO}$; RAMP_LIMIT_LOW = $2^{33} - 2^{24} \times (f_{VCO} - f_{LOW}) / f_{PD}$

7.6.86 Register R85 (offset = 55h) [reset = 0000h]

Figure 123. Register R85

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RAMP_LIMIT_LOW[31:16]															
R/W-0h															

Table 93. Register R85 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RAMP_LIMIT_LOW [31:16]	R/W	0h	Upper 16 bits of RAMP_LIMIT_LOW. See Table 92 for description.

7.6.87 Register R86 (offset = 56h) [reset = 0000h]

Figure 124. Register R86

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RAMP_LIMIT_LOW[15:0]															
R/W-0h															

Table 94. Register R86 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RAMP_LIMIT_LOW[15:0]	R/W	0h	Lower 16 bits of RAMP_LIMIT_LOW. See Table 92 for description.

7.6.88 Register R87 (offset = 57h) [reset = 0000h]

Figure 125. Register R87

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W-0h															

Table 95. Register R87 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0		R/W	0h	Program 0h to this field. After programming R0 with RESET = 1, no need to program this register.

7.6.89 Register R88 (offset = 58h) [reset = 0000h]

Figure 126. Register R88

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W-0h															

Table 96. Register R88 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0		R/W	0h	Program 0h to this field. After programming R0 with RESET = 1, no need to program this register.

7.6.90 Register R89 (offset = 59h) [reset = 0000h]

Figure 127. Register R89

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W-0h															

Table 97. Register R89 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0		R/W	0h	Program 0h to this field. After programming R0 with RESET = 1, no need to program this register.

7.6.91 Register R90 (offset = 5Ah) [reset = 0000h]

Figure 128. Register R90

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W-0h															

Table 98. Register R90 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0		R/W	0h	Program 0h to this field. After programming R0 with RESET = 1, no need to program this register.

7.6.92 Register R91 (offset = 5Bh) [reset = 0000h]

Figure 129. Register R91

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W-0h															

Table 99. Register R91 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0		R/W	0h	Program 0h to this field. After programming R0 with RESET = 1, no need to program this register.

7.6.93 Register R92 (offset = 5Ch) [reset = 0000h]

Figure 130. Register R92

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W-0h															

Table 100. Register R92 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0		R/W	0h	Program 0h to this field. After programming R0 with RESET = 1, no need to program this register.

7.6.94 Register R93 (offset = 5Dh) [reset = 0000h]

Figure 131. Register R93

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W-0h															

Table 101. Register R93 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0		R/W	0h	Program 0h to this field. After programming R0 with RESET = 1, no need to program this register.

7.6.95 Register R94 (offset = 5Eh) [reset = 0000h]

Figure 132. Register R94

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W-0h															

Table 102. Register R94 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0		R/W	0h	Program 0h to this field. After programming R0 with RESET = 1, no need to program this register.

7.6.96 Register R95 (offset = 5Fh) [reset = 0000h]

Figure 133. Register R95

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W-0h															

Table 103. Register R95 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0		R/W	0h	Program 0h to this field. After programming R0 with RESET = 1, no need to program this register.

7.6.97 Register R96 (offset = 60h) [reset = 0000h]

Figure 134. Register R96

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RAMP_BURST_EN	RAMP_BURST_COUNT													0	0
R/W-0h	R/W-0h													R/W-0h	

Table 104. Register R96 Field Descriptions

Bit	Field	Type	Reset	Description
15	RAMP_BURST_EN	R/W	0h	This enables ramp burst mode. In this mode, a number of ramps equal to RAMP_BURST_COUNT is sent out whenever RAMP_EN is set to 1. This is intended to produce a finite pattern of ramps, instead of a continuous pattern. 0: Disabled 1: Enabled
14 - 2	RAMP_BURST_COUNT	R/W	0h	When RAMP_BURST_EN = 1, this sets the number of ramps that is sent out.
1 - 0		R/W	0h	Program 0h to this field.

7.6.98 Register R97 (offset = 61h) [reset = 0000h]

Figure 135. Register R97

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RAMP0_RST	0	0	0	0	RAMP_TRIGB				RAMP_TRIGA				0	RAMP_BURST_TRIG	
R/W-0h	R/W-0h				R/W-0h				R/W-0h				R/W-0h	R/W-0h	

Table 105. Register R97 Field Descriptions

Bit	Field	Type	Reset	Description
15	RAMP0_RST	R/W	0h	Resets RAMP0 at start of ramp to eliminate round-off errors. Applies to automatic ramping mode only. 0: Disabled 1: Reset
14 - 11		R/W	0h	Program 0h to this field.
10 - 7	RAMP_TRIGB	R/W	0h	Definition of ramp trigger B. 0: Disabled 1: RampClk pin rising edge 2: RampDir pin rising edge 4: Always triggered 9: RampClk pin falling edge 10: RampDir pin falling edge All other values are not used.
6 - 3	RAMP_TRIGA	R/W	0h	Definition of ramp trigger A. Options are same as RAMP_TRIGB.
2		R/W	0h	Program 0h to this field.
1 - 0	RAMP_BURST_TRIG	R/W	0h	Sets what triggers the next ramp in burst mode. 0: Ramp transition 1: Trigger A 2: Trigger B 3: Not used

7.6.99 Register R98 (offset = 62h) [reset = 0000h]

Figure 136. Register R98

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RAMP0_INC[29:16]														0	RAMP0_DLY
R/W-0h														R/W-0h	R/W-0h

Table 106. Register R98 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 2	RAMP0_INC[29:16]	R/W	0h	Upper 14 bits of RAMP0_INC. RAMP0_INC sets the 2's compliment of the number added to the fractional numerator on every ramp cycle.
1		R/W	0h	Program 0h to this field.
0	RAMP0_DLY	R/W	0h	When enabled, increases RAMP0 length by basing the ramp clock on two phase detector cycles instead of one. 0: Ramp clock = 1 f_{PD} cycle 1: Ramp clock = 2 f_{PD} cycles

7.6.100 Register R99 (offset = 63h) [reset = 0000h]

Figure 137. Register R99

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RAMP0_INC[15:0]															
R/W-0h															

Table 107. Register R99 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RAMP0_INC[15:0]	R/W	0h	Lower 16 bits of RAMP0_INC. See Table 106 for description.

7.6.101 Register R100 (offset = 64h) [reset = 0000h]

Figure 138. Register R100

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RAMP0_LEN															
R/W-0h															

Table 108. Register R100 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RAMP0_LEN	R/W	0h	Length of the ramp in phase detector cycles.

7.6.102 Register R101 (offset = 65h) [reset = 0000h]

Figure 139. Register R101

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	RAMP1_DLY	RAMP1_RST	RAMP0_NEXT	0	0	RAMP0_NEXT_TRIG	
R/W-0h									R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h	

Table 109. Register R101 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 7		R/W	0h	Program 0h to this field.
6	RAMP1_DLY	R/W	0h	When enabled, increases RAMP1 length by basing the ramp clock on two phase detector cycles instead of one. 0: Ramp clock = 1 f_{PD} cycle 1: Ramp clock = 2 f_{PD} cycles
5	RAMP1_RST	R/W	0h	Resets RAMP1 at start of ramp to eliminate round-off errors. Applies to automatic ramping mode only. 0: Disabled 1: Reset
4	RAMP0_NEXT	R/W	0h	Defines what ramp comes after RAMP0. 0: RAMP0 1: RAMP1
3 - 2		R/W	0h	Program 0h to this field.
1 - 0	RAMP0_NEXT_TRIG	R/W	0h	Defines what triggers the next ramp. 0: RAMP0_LEN timeout counter 1: Trigger A 2: Trigger B 3: Not used

7.6.103 Register R102 (offset = 66h) [reset = 0000h]

Figure 140. Register R102

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	RAMP1_INC[29:16]													
R/W-0h		R/W-0h													

Table 110. Register R102 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 14		R/W	0h	Program 0h to this field.
13 - 0	RAMP1_INC[29:16]	R/W	0h	Upper 14 bits of RAMP1_INC. RAMP1_INC sets the 2's compliment of the number added to the fractional numerator on every ramp cycle.

7.6.104 Register R103 (offset = 67h) [reset = 0000h]

Figure 141. Register R103

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RAMP1_INC[15:0]															
R/W-0h															

Table 111. Register R103 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RAMP1_INC[15:0]	R/W	0h	Lower 16 bits of RAMP1_INC. See Table 110 for description.

7.6.105 Register R104 (offset = 68h) [reset = 0000h]

Figure 142. Register R104

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RAMP1_LEN															
R/W-0h															

Table 112. Register R104 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RAMP1_LEN	R/W	0h	Length of the ramp in phase detector cycles.

7.6.106 Register R105 (offset = 69h) [reset = 4440h]

Figure 143. Register R105

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RAMP_DLY_CNT										RAMP_MANUAL	RAMP1_NEXT	0	0	RAMP1_NEXT_TRIG	
R/W-111h										R/W-0h	R/W-0h	R/W-0h		R/W-0h	

Table 113. Register R105 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 6	RAMP_DLY_CNT	R/W	111h	For ramping mode, RAMP_DLY_CNT and RAMP_SCALE_COUNT determine the minimum necessary time taken for VCO calibration during the ramp. Min. VCOCal time = (1 / f_{smc}) / (RAMP_DLY_CNT × $2^{RAMP\_SCALE\_COUNT}$), where f_{smc} = f_{OSCin} / $2^{CAL\_CLK\_DIV}$.
5	RAMP_MANUAL	R/W	0h	Selects the ramping mode. 0: Automatic ramping mode 1: Manual (Pin) ramping mode
4	RAMP1_NEXT	R/W	0h	Defines what ramp comes after RAMP1. 0: RAMP0 1: RAMP1
3 - 2		R/W	0h	Program 0h to this field.
1 - 0	RAMP1_NEXT_TRIG	R/W	0h	Defines what triggers the next ramp. 0: RAMP1_LEN timeout counter 1: Trigger A 2: Trigger B 3: Not used

7.6.107 Register R106 (offset = 6Ah) [reset = 0007h]

Figure 144. Register R106

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	RAMP_TRIG_CAL	0	RAMP_SCALE_COUNT		
R/W-0h											R/W-0h	R/W-0h	R/W-7h		

Table 114. Register R106 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 5		R/W	0h	Program 0h to this field.
4	RAMP_TRIG_CAL	R/W	0h	Enabling this bit causes VCO calibration to occur in automatic ramping mode at the beginning of each ramp. 0: Disabled 1: Enabled
3		R/W	0h	Program 0h to this field.
2 - 0	RAMP_SCALE_COUNT	R/W	7h	For ramping mode, RAMP_DLY_CNT and RAMP_SCALE_COUNT determine the minimum necessary time taken for VCO calibration during the ramp. Min. VCOCal time = (1 / f_{smc}) / (RAMP_DLY_CNT × $2^{RAMP\_SCALE\_COUNT}$), where f_{smc} = f_{OSCin} / $2^{CAL\_CLK\_DIV}$.

7.6.108 Register R107 (offset = 6Bh) [reset = 0000h]

Figure 145. Register R107

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R-0h															

Table 115. Register R107 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0		R	0h	Not used. (Read back only)

7.6.109 Register R108 (offset = 6Ch) [reset = 0000h]

Figure 146. Register R108

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R-0h															

Table 116. Register R108 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0		R	0h	Not used. (Read back only)

7.6.110 Register R109 (offset = 6Dh) [reset = 0000h]

Figure 147. Register R109

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R-0h															

Table 117. Register R109 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0		R	0h	Not used. (Read back only)

7.6.111 Register R110 (offset = 6Eh) [reset = 0000h]

Figure 148. Register R110

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	rb_LD_VTUNE		0	rb_VCO_SEL			0	0	0	0	0
R-0h															

Table 118. Register R110 Field Descriptions

Bit	Field	Type	Reset	Description
10 - 9	rb_LD_VTUNE	R	0h	Readback of Vtune lock detect. 0: Unlocked 1: Unlocked 2: Locked 3: Invalid
7 - 5	rb_VCO_SEL	R	0h	Reads back the actual VCO that the calibration has selected. 1: VCO1 2: VCO2 ….. 6: VCO6 All other values are not used.

7.6.112 Register R111 (offset = 6Fh) [reset = 0000h]

Figure 149. Register R111

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	rb_VCO_CAPCTRL							
R-0h															

Table 119. Register R111 Field Descriptions

Bit	Field	Type	Reset	Description
7 - 0	rb_VCO_CAPCTRL	R	0h	Reads back the actual CAPCTRL value that the VCO calibration has chosen.

7.6.113 Register R112 (offset = 70h) [reset = 0000h]

Figure 150. Register R112

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	rb_VCO_DACISET								
R-0h															

Table 120. Register R112 Field Descriptions

Bit	Field	Type	Reset	Description
8 - 0	rb_VCO_DACISET	R	0h	Reads back the actual DACISET value that the VCO calibration has chosen.

7.6.114 Register R113 (offset = 71h) [reset = 0000h]

Figure 151. Register R113

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R-0h															

Table 121. Register R113 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0		R	0h	Not used. (Read back only)

7.6.115 Register R114 (offset = 72h) [reset = 7800h]

Figure 152. Register R114

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	1	1	FSK_EN	0			FSK_SPI_LEVEL		FSK_SPI_DEV_SEL			FSK_MODE_SEL	
R/W-Fh					R/W-0h	R/W-0h			R/W-0h		R/W-0h			R/W-0h	

Table 122. Register R114 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 11		R/W	Fh	Program Fh to this field.
10	FSK_EN	R/W	0h	Enables all FSK modes. 0: Disabled 1: Enabled
9 - 7		R/W	0h	Program 0h to this field.
6 - 5	FSK_SPI_LEVEL	R/W	0h	Defines the desired FSK level in FSK SPI mode. When this bit is zero, FSK operation in this mode is disabled even if FSK_EN = 1. 0: Disabled 1: 2FSK 2: 4FSK 3: 8FSK
4 - 2	FSK_SPI_DEV_SEL	R/W	0h	In FSK SPI mode, these bits select one of the FSK deviations as defined in registers R116 - R123. 0: FSK_DEV0 1: FSK_DEV1 ….. 7: FSK_DEV7
1 - 0	FSK_MODE_SEL	R/W	0h	Defines FSK mode. 0: Not used 1: Not used 2: FSK SPI 3: FSK SPI FAST

7.6.116 Register R115 (offset = 73h) [reset = 0000h]

Figure 153. Register R115

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	FSK_DEV_SCALE					0	0	0
R/W-0h								R/W-0h					R/W-0h		

Table 123. Register R115 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8		R/W	0h	Program 0h to this field.
7 - 3	FSK_DEV_SCALE	R/W	0h	The FSK deviation will be scaled by $2^{FSK\_DEV\_SCALE}$.
2 - 0		R/W	0h	Program 0h to this field.

7.6.117 Register R116 (offset = 74h) [reset = 0000h]

Figure 154. Register R116

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FSK_DEV0															
R/W-0h															

Table 124. Register R116 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	FSK_DEV0	R/W	0h	Defines the desired frequency deviation in FSK SPI mode.

7.6.118 Register R117 (offset = 75h) [reset = 0000h]

Figure 155. Register R117

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FSK_DEV1															
R/W-0h															

Table 125. Register R117 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	FSK_DEV1	R/W	0h	Defines the desired frequency deviation in FSK SPI mode.

7.6.119 Register R118 (offset = 76h) [reset = 0000h]

Figure 156. Register R118

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FSK_DEV2															
R/W-0h															

Table 126. Register R118 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	FSK_DEV2	R/W	0h	Defines the desired frequency deviation in FSK SPI mode.

7.6.120 Register R119 (offset = 77h) [reset = 0000h]

Figure 157. Register R119

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FSK_DEV3															
R/W-0h															

Table 127. Register R119 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	FSK_DEV3	R/W	0h	Defines the desired frequency deviation in FSK SPI mode.

7.6.121 Register R120 (offset = 78h) [reset = 0000h]

Figure 158. Register R120

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FSK_DEV4															
R/W-0h															

Table 128. Register R120 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	FSK_DEV4	R/W	0h	Defines the desired frequency deviation in FSK SPI mode.

7.6.122 Register R121 (offset = 79h) [reset = 0000h]

Figure 159. Register R121

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FSK_DEV5															
R/W-0h															

Table 129. Register R121 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	FSK_DEV5	R/W	0h	Defines the desired frequency deviation in FSK SPI mode.

7.6.123 Register R122 (offset = 7Ah) [reset = 0000h]

Figure 160. Register R122

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FSK_DEV6															
R/W-0h															

Table 130. Register R122 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	FSK_DEV6	R/W	0h	Defines the desired frequency deviation in FSK SPI mode.

7.6.124 Register R123 (offset = 7Bh) [reset = 0000h]

Figure 161. Register R123

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FSK_DEV7															
R/W-0h															

Table 131. Register R123 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	FSK_DEV7	R/W	0h	Defines the desired frequency deviation in FSK SPI mode.

7.6.125 Register R124 (offset = 7Ch) [reset = 0000h]

Figure 162. Register R124

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FSK_SPI_FAST_DEV															
R/W-0h															

Table 132. Register R124 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	FSK_SPI_FAST_DEV	R/W	0h	Defines the desired frequency deviation in FSK SPI FAST mode.

7.6.126 Register R125 (offset = 7Dh) [reset = 2288h]

Figure 163. Register R125

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	0	0	0	1	0	1	0	0	0	1	0	0	0
R/W-2288h															

Table 133. Register R125 Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0		R/W	2288h	Program 2288h to this field. After programming R0 with RESET = 1, no need to program this register.

8 Application and Implementation

NOTE

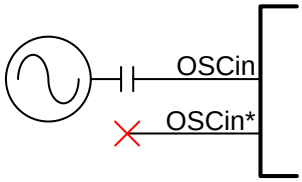
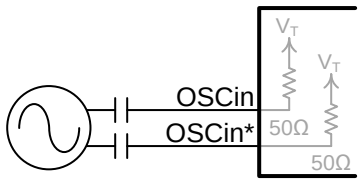
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 OSCin Configuration

OSCin supports single-ended and differential clock. Register R5 defines OSCin configuration.

Table 134. OSCin Configuration

OSCin TYPE	SINGLE-ENDED CLOCK	DIFFERENTIAL CLOCK
Configuration Diagram		
Register Setting	IPBUF_TYPE = 1	IPBUF_TYPE = 0 IPBUF_TERM = 1

Single-ended and differential input clock definitions are shown in Figure 164.

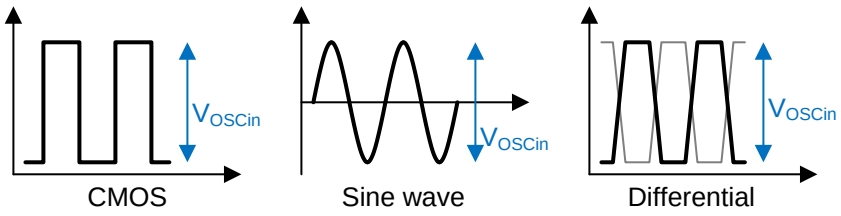


Figure 164. Input Clock Definition

8.1.2 OSCin Slew Rate

The slew rate of the OSCin signal can have an impact on the spurs and phase noise of the LMX2572 if it is too low. In general, the best performance is for a high slew rate but a lower amplitude signal, such as LVDS.

8.1.3 VCO Gain

The VCO gain varies between the six VCO cores and is the lowest at the lowest end of the band and highest at the highest end of each band. The typical VCO gain over each VCO core is listed in Table 135.

Table 135. VCO Gain

VCO CORE	f_{Min} (MHz)	f_{Max} (MHz)	$K_{VCO}Min$ (MHz/V)	$K_{VCO}Max$ (MHz/V)
VCO1	3200	3650	32	47
VCO2	3650	4200	35	54
VCO3	4200	4650	47	64
VCO4	4650	5200	50	73
VCO5	5200	5750	61	82
VCO6	5750	6400	57	79

For an arbitrary VCO frequency, the VCO gain can be estimated as Equation 4:

$$K_{VCO} = K_{VCO}Min + (K_{VCO}Max - K_{VCO}Min) \times (f_{VCO} - f_{Min}) / (f_{Max} - f_{Min}) \quad (4)$$

8.1.4 VCO Calibration

The purpose of VCO calibration is to find out: (1) the correct VCO core, (2) the best band within the core, and (3) the best VCO amplitude setting. The LMX2572 allows the user to assist the VCO calibration. In general, there are three kinds of assistance.

8.1.4.1 Partial Assist

Upon every frequency change, before the FCAL_EN bit is checked, the user provides a good estimate of the initial starting point for the VCO core (VCO_SEL), band (VCO_CAPCTRL_STRT), and amplitude (VCO_DACISET_STRT). To do the partial assist for the VCO calibration, follow this procedure:

1. Pick a VCO core that includes the desired VCO frequency. If at the boundary of two cores, choose based on phase noise or performance.
2. Use Equation 5 to find the approximate band:

$$VCO\_CAPCTRL\_STRT = Round[C_{Min} - (f_{VCO} - f_{Min}) \times (C_{Min} - C_{Max}) / (f_{Max} - f_{Min})] \quad (5)$$

3. Use Equation 6 to find the approximate amplitude setting.

$$VCO\_DACISET\_STRT = Round[A_{Min} - (f_{VCO} - f_{Min}) \times (A_{Min} - A_{Max}) / (f_{Max} - f_{Min})] \quad (6)$$

Table 136. VCO Core Parametric

VCO CORE	f_{Min} (MHz)	f_{Max} (MHz)	C_{Min}	C_{Max}	A_{Min}	A_{Max}
VCO1	3200	3650	131	19	138	137
VCO2	3650	4200	143	25	162	142
VCO3	4200	4650	135	34	126	114
VCO4	4650	5200	136	25	195	172
VCO5	5200	5750	133	20	190	163
VCO6	5750	6400	151	27	256	204

8.1.4.2 Close Frequency Assist

Upon initialization of the device, the user enables the QUICK_RECAL_EN bit. The next VCO calibration will use the current VCO core, band, and amplitude settings as the initial starting point. This approach is useful if the frequency change is small, say 50 MHz or so.

8.1.4.3 Full Assist

The user forces the VCO core (VCO_SEL), band (VCO_CAPCTRL), and amplitude (VCO_DACISET) and manually sets the value. No VCO calibration will be performed. To force the set values, set VCO_SEL_FORCE, VCO_CAPCTRL_FORCE, and VCO_DACISET_FORCE equal 1. First do a VCO calibration and then read back the values to obtain the set values.

8.1.5 Output Buffer Control

8.1.5.1 Output Power

The OUTA_PWR and OUTB_PWR registers can be used to control the output power of the output buffers. The change in output power becomes not obvious when these registers values are over 35.

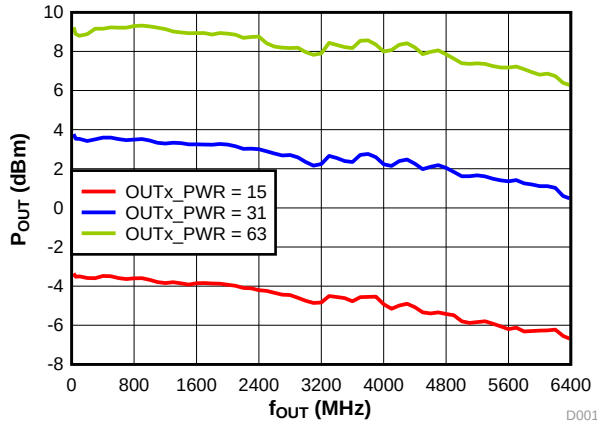


Figure 165. Output Power vs Frequency

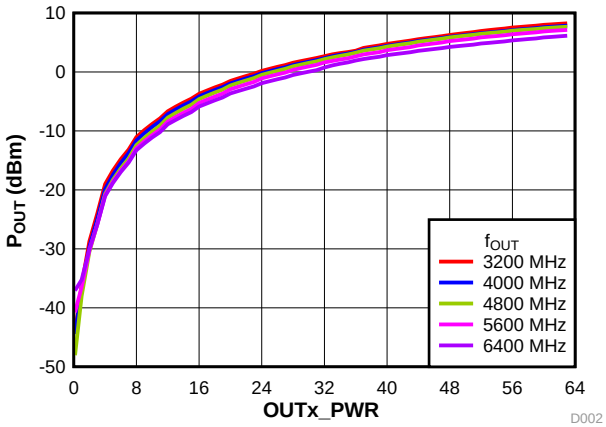


Figure 166. Output Power vs Power Control Bits

8.1.5.2 Power-Up Response

Use the OUTx_PD bits to power up or power down the output buffers. The RF output will vanish immediately when the buffer is powered down. However, it takes some tiny amount of time for it to power up. The response time is shorter if the output frequency is lower.

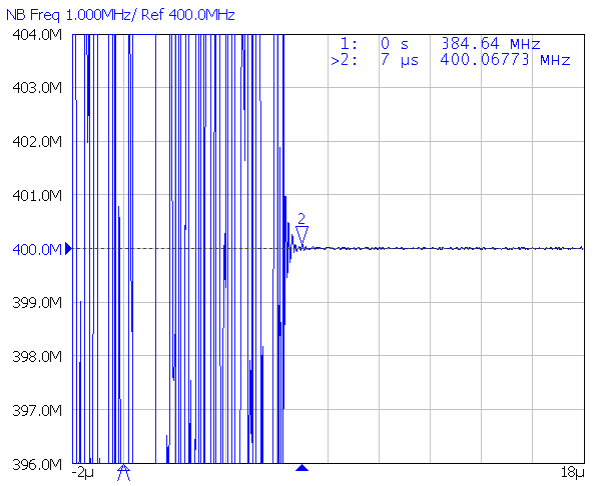


Figure 167. Buffer Power Up at 400-MHz Output

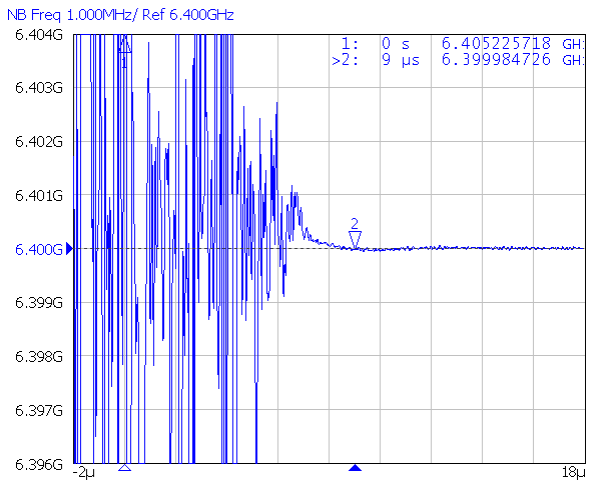


Figure 168. Buffer Power Up at 6400-MHz Output

8.1.5.3 Unused Output Pin

Each output buffer has two differential pair pins. The buffer can be used as a single differential output or two single-ended outputs. If only one single-ended output is necessary, the unused pin cannot be left open. The pin should be terminated properly as shown in Figure 169.

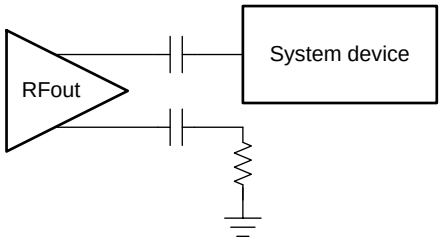


Figure 169. Unused Output Buffer Differential Pin

8.1.6 Application for SYNC

The requirements for SYNC depend on certain setup conditions. In cases where the SYNC is not timing critical, the setup can be done through software by toggling the VCO_PHASE_SYNC_EN bit from 0 to 1. When the SYNC is timing critical, then setup must be done through the SYNC pin and the setup and hold times for the OSCin pin are critical.

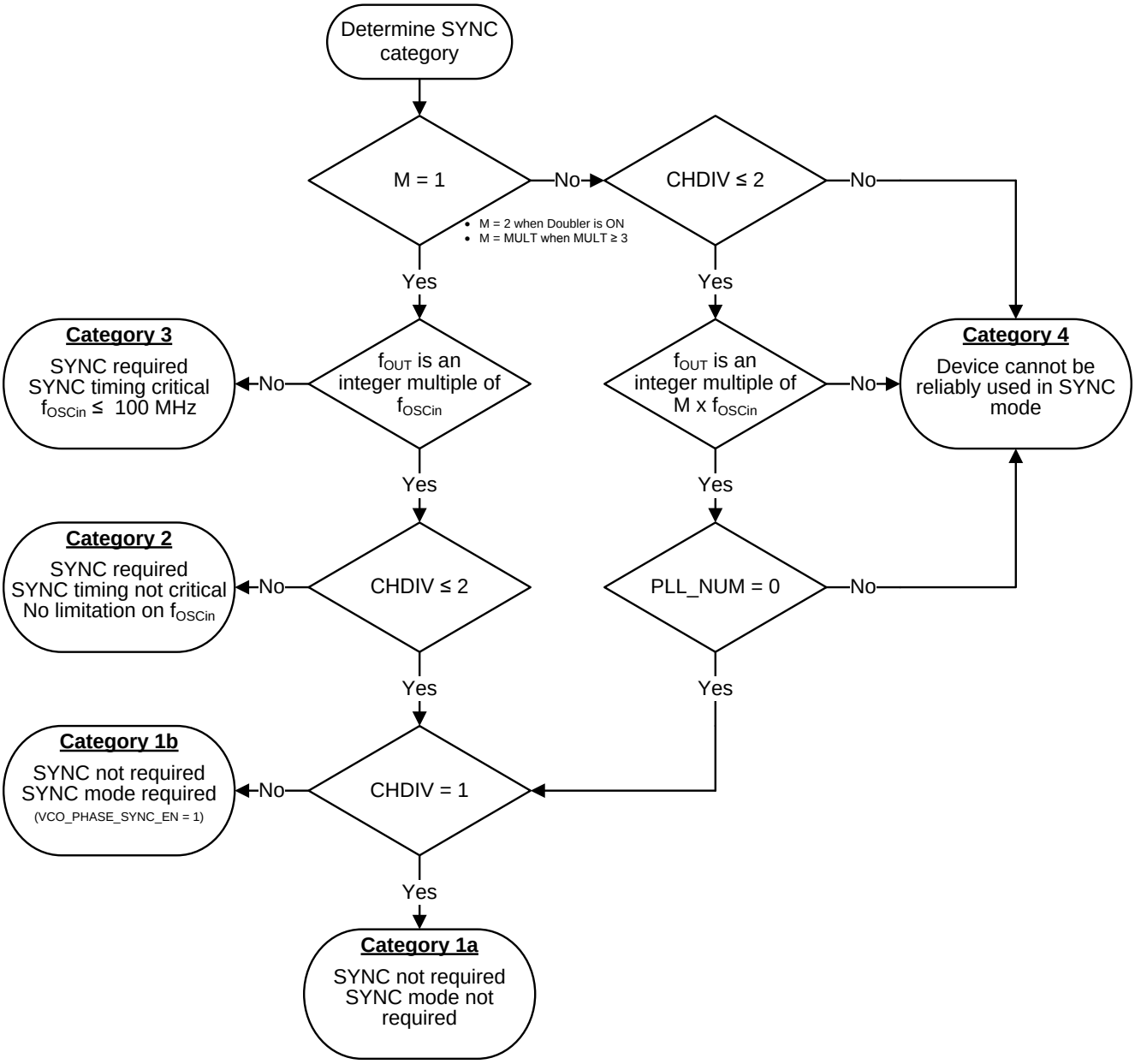


Figure 170. SYNC Category

The procedure for using SYNC in different SYNC categories is shown in Table 137.

Table 137. Procedure for Using SYNC

CATEGORY	CHARACTERISTIC	SETUP PROCEDURE
1a	• SYNC not required. • SYNC mode not required.	1. Setup as usual. 2. Program all the registers as usual. The phase relationship between OSCin and f_{OUT} will always be deterministic.
1b	• SYNC not required. • SYNC mode required.	1. Set N = N' / 2, where N' is the normal N divider value. 2. Program all the registers with R0 VCO_PHASE_SYNC_EN = 1.
2	• SYNC required. • SYNC timing not critical. • No limitation on f_{OSCin}.	1. Setup as usual. 2. Program all the registers as usual. The device is now locked. 3. Program N = N' / 2, where N' is the normal (original) N divider value. 4. Program R0 with VCO_PHASE_SYNC_EN = 1. 5. Program N = N'. 6. Program R0 with VCO_PHASE_SYNC_EN = 0. 7. Alternatively, step 3 to 6 can be replaced by applying a SYNC signal (0 → 1 transition) to the SYNC pin and the timing on this in not critical.
3	• SYNC required. • SYNC timing critical. • $f_{OSCin} \leq 100$ MHz	1. Ensure that the maximum f_{OSCin} for SYNC is not violated and there are hardware accommodations to use the SYNC pin. 2. If neither OUTA_MUX nor OUTB_MUX is equal to 0 (Channel divider output), program N divider as usual. 3. If one of the OUTA_MUX or OUTB_MUX is equal to 1, set N = N' / 2, where N' is the normal N divider (integer + fraction) value. 4. Program all the registers with R0 VCO_PHASE_SYNC_EN = 1. 5. Apply a SYNC signal (0 → 1 transition) to the SYNC pin. The timing of the SYNC signal as shown in Timing Requirements must be obey.

Set these bits to drive the SYNC pin with a LVDS signal:

- Set INPIN_FMT to 1 or 3 to enable LVDS input
- Set INPIN_LVL to one of the options
- Set INPIN_HYST, if necessary

The LVDS driver that is driving the SYNC pin should be configured as shown in Figure 171:

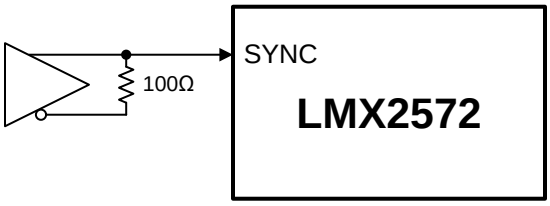


Figure 171. Driving SYNC Pin With Differential Signal

8.1.7 Application for Ramp

8.1.7.1 Manual Ramping Mode

Manual ramping is enabled when the user sets RAMP_EN = 1 and RAMP_MANUAL = 1. In this mode, the ramp is clocked by the rising edges applied to the RampClk pin. The size of the frequency change is defined by RAMP0_INC and RAMP1_INC. If a LOW is seen at the RampDir pin on the rising edge of RampClk, the output frequency will be incremented by RAMP0_INC. On the contrary, the output frequency will be incremented by RAMP1_INC if a HIGH is captured. If a rising edge is seen on the RampClk pin while the VCO is calibrating, then this rising edge is ignored. The frequency for the RampClk must be limited to a frequency of 250 kHz or less, and the rising edge of the RampDir signal must be targeted to the falling edge of the RampClk pin. The necessary register fields for use in manual ramping mode are shown in Table 138.

Table 138. Manual Ramping Mode Programming

REGISTER FIELD	VALUE	DESCRIPTION
RAMP_EN	1 = Enable ramp	Set this bit to 1 to enable frequency ramping.
RAMP_MANUAL	1 = Manual ramping mode	To select manual ramping mode, set this bit to 1.
RAMP_LIMIT_HIGH	Greater than the highest VCO ramp frequency	This sets the upper ramp limit that the ramp cannot go above. Suppose f_{High} is this frequency and f_{Start} is the starting VCO ramp frequency, then, for $f_{High} > f_{Start}$, RAMP_LIMIT_HIGH = $2^{24} \times (f_{High} - f_{Start}) / f_{PD}$
RAMP_LIMIT_LOW	Smaller than the lowest VCO ramp frequency	This sets the lower ramp limit that the ramp cannot go below. Suppose f_{Low} is this frequency and f_{Start} is the starting VCO ramp frequency, then, for $f_{Start} > f_{Low}$, RAMP_LIMIT_LOW = $2^{33} - 2^{24} \times (f_{Start} - f_{Low}) / f_{PD}$
RAMP0_INC RAMP1_INC	Equal to the ramp size	Suppose the ramp size is Δf, then RAMPx_INC = $(\Delta f / f_{PD}) \times 2^{24}$ or = $2^{30} - (\Delta f / f_{PD}) \times 2^{24}$ if Δf is a negative number.
RAMP_THRESH	Suggest less than 50 MHz	If the amount of frequency ramp exceeds this threshold, a VCO calibration will be initiated. For example, if the ramp size is 50 MHz while this threshold is 30 MHz, then VCO calibration will be executed every time it ramps. Suppose the threshold frequency is f_{TH}, then RAMP_THRESH = $(f_{TH} / f_{PD}) \times 2^{24}$
RAMP_TRIGA RAMP_TRIGB	1 = RampClk rising edge trigger	In manual ramping mode, the ramp is triggered by the rising edges applied to the RampClk pin. Either RAMP_TRIGA or RAMP_TRIGB can be selected as the trigger source for the next ramp.
RAMP0_NEXT_TRIG RAMP1_NEXT_TRIG	Equal to the selected RAMP_TRIGx	These fields define what triggers the next ramp. They must be set to the same trigger source selected above.

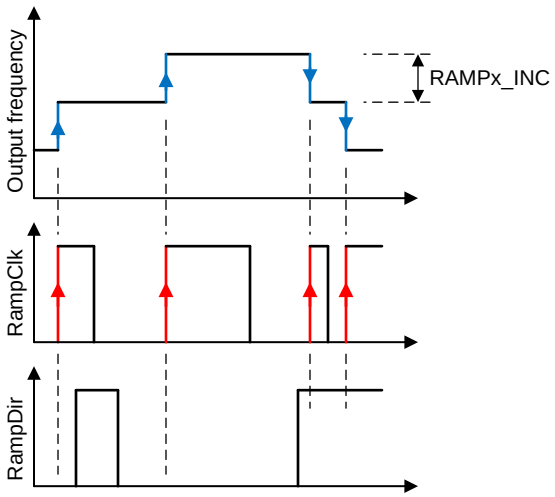


Figure 172. Manual Ramp Waveform

8.1.7.2 Automatic Ramping Mode

Automatic ramping mode is enabled when RAMP_EN = 1 with RAMP_MANUAL = 0. In this mode, there are two ramps profiles that one can use to set the length and frequency change. In addition to this, there are ramp limits that can be used to create more complicated waveforms. The output frequency will ramp once on each phase detector cycle.

Automatic ramping can really be divided into two classes depending on whether the VCO must calibrate in the middle of the ramping or not. If the VCO can go the entire range without calibrating, this is calibration-free ramping. Note that this range is less at hot temperatures and less for lower frequency VCOs. This range is not ensured, so margin must be built into the design.

For ramping that are not calibration free, the ramp waveform is more like a staircase ramp.

Table 139. Automatic Ramping Mode Programming

REGISTER FIELD	VALUE	DESCRIPTION
RAMP_EN	1 = Enable ramp	Set this bit to 1 to enable frequency ramping.
RAMP_MANUAL	0 = Automatic ramping mode	To select automatic ramping mode, set this bit to 0.
RAMP_LIMIT_HIGH	Greater than the highest VCO ramp frequency	This sets the upper ramp limit that the ramp cannot go above. Suppose f_{High} is this frequency and f_{Start} is the starting VCO ramp frequency, then, for $f_{High} > f_{Start}$, RAMP_LIMIT_HIGH = $2^{24} \times (f_{High} - f_{Start}) / f_{PD}$
RAMP_LIMIT_LOW	Smaller than the lowest VCO ramp frequency	This sets the lower ramp limit that the ramp cannot go below. Suppose f_{Low} is this frequency and f_{Start} is the lowest VCO ramp frequency, then, for $f_{Start} > f_{Low}$, RAMP_LIMIT_LOW = $2^{33} - 2^{24} \times (f_{Start} - f_{Low}) / f_{PD}$
RAMP0_INC RAMP1_INC	Equal to the ramp size	Suppose the ramp size is Δf, then RAMPx_INC = $(\Delta f / f_{PD}) \times 2^{24}$ or = $2^{30} - (\Delta f / f_{PD}) \times 2^{24}$ if Δf is a negative number.
RAMP_THRESH	Suggest less than 50 MHz	If the amount of frequency ramp exceed this threshold, a VCO calibration will be initiated. For example, if the ramp size is 15 MHz while this threshold is 20 MHz, then VCO calibration will be executed every two ramps. Suppose the threshold frequency is f_{TH}, then RAMP_THRESH = $(f_{TH} / f_{PD}) \times 2^{24}$
RAMP0_LEN RAMP1_LEN	0 to 2^{16}	Set the number of ramp required in each ramp profile. Maximum value is 2^{16}. If this number is exceeded, enable the RAMPx_DLY bit or reduce the phase detector frequency. RAMPx_LEN = Ramp duration of a ramp profile × f_{PD}
RAMP0_DLY RAMP1_DLY	0 or 1	If this bit is set to 1, the output frequency will ramp every two f_{PD} cycles.
RAMP0_NEXT RAMP1_NEXT	Equal to the next ramp	Set the next ramping profile when the present profile is finished.
RAMP0_NEXT_TRIG RAMP1_NEXT_TRIG	0 = RAMP_LENx time out counter	Set these bits to 0 in order to start the next ramp immediately after the previous ramp.
RAMP0_RST RAMP1_RST	0 or 1	If the stop frequency of the present ramp profile is different from the start frequency of the next ramp profile, set this bit to 1.
RAMP_SCALE_COUNT RAMP_DLY_CNT	Suggest a minimum pause time of 50 µs	These two register fields set the minimum pause time when RAMP_THRESH is hit. This pause time must be sufficient to allow the VCO to complete a calibration, otherwise it will be overwritten by the actual VCO calibration time. Minimum pause time = RAMP_DLY_CNT × $2^{RAMP\_SCALE\_COUNT}$ × $2^{CAL\_CLK\_DIV}$ / f_{OSCin}

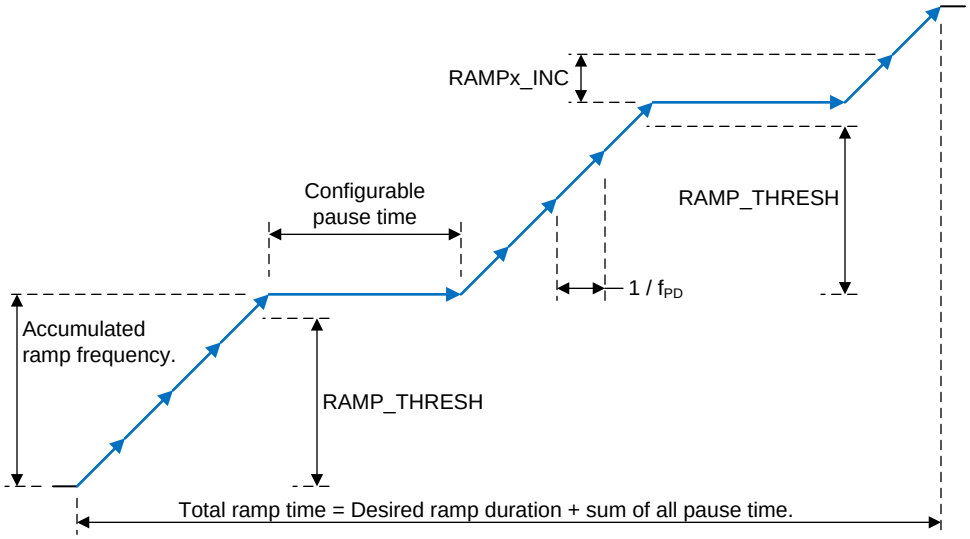


Figure 173. Auto Ramp Waveform

8.1.8 Application for SYSREF

SYSREF consists of multiple dividers and a delay circuitry. The dividers include two fixed value dividers, a Pre-SR divider (SYSREF_DIV_PRE), and a Post-SR divider (SYSREF_DIV).

Figure 174. SYSREF

SYSREF output frequency, f_{SYSREF}, is calculated by Equation 7:

$$f_{SYSREF} = f_{VCO} / (4 \times SYSREF\_DIV\_PRE \times SYSREF\_DIV) \quad (7)$$

The delay circuitry is consist of 4 counters (JESD_DAC1_CTRL, JESD_DAC2_CTRL, JESD_DAC3_CTRL, and JESD_DAC4_CTRL). Altogether, there are 200 useful programmable steps and each step is approximately a 5 ps (Pre-SR divider = 2) or 10 ps (Pre-SR divider = 4) delay. The values of the counters must be set in accordance to Table 140.

Table 140. SYSREF Delay Step

DELAY STEP NUMBER	JESD_DAC1_CTRL	JESD_DAC2_CTRL	JESD_DAC3_CTRL	JESD_DAC4_CTRL
0	36	27	0	0
…				
36	0	63	0	0
37	0	62	1	0
…				
99	0	0	63	0
100	0	0	62	1
…				
162	0	0	0	63
163	1	0	0	62
…				
200	38	0	0	25
> 200	Invalid	Invalid	Invalid	Invalid

Table 141 summarizes the usage boundaries of all functional blocks in SYSREF.

Table 141. SYSREF Boundaries

PARAMETER	VALUE	NOTES
Pre-SR divider	1 (Bypassed), 2, 4	
Post-SR divider	4, 6, 8, 10, …, 4096, 4098	Input frequency range: 400 to 2300 MHz
Number of SYSREF pulse in Pulsed mode	1, 2, 3, …, 14, 15	
Number of delay step	0 (No additional delay), 1, 2, 3, …, 199, 200	

Since SYSREF operation requires enabling the VCO_PHASE_SYNC_EN bit, during programming, set N = N' / 2, where N' is the normal N divider value.

8.1.8.1 Driving SysRefReq Pin With Differential Signal

By default, the SysRefReq pin is configured as CMOS type input. V_{IO} and V_{IH} as shown in the Electrical Specifications apply. In Repeater mode (SYSREF_REPEAT = 1), there is an option to program this pin to support LVDS input signal.

- Set INPIN_FMT to 2 or 3 to enable LVDS input
- Set INPIN_LVL to one of the options
- Set INPIN_HYST if necessary

The LVDS driver that is driving the SysRefReq pin should be configured like Figure 175:

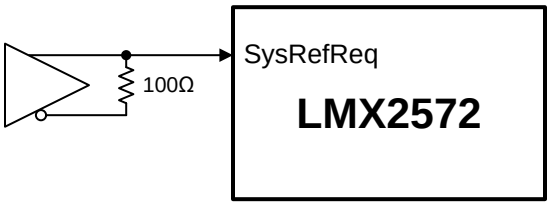


Figure 175. Driving SysRefReq Pin With Differential Signal

8.1.8.2 SYSREF Output

The SYSREF output comes in differential format through RFoutB. The common mode output voltage of this driver is between 1.9 V to 2.3 V. If DC-coupling to the receiving device is not possible, there are two strategies for AC-coupling.

1. Send a series of pulses to establish a DC-bias level across the AC-coupling capacitor.
2. Establish a bias voltage at the receiving device that is below the threshold voltage by using a resistive divider.

8.1.9 Application for FSK

In fractional mode, the finest delta frequency difference between two programmable output frequencies is equal to Equation 8:

$$f_1 - f_2 = \Delta f_{min} = f_{PD} \times \{[(PLL\_N + 1) / PLL\_DEN] - (PLL\_N / PLL\_DEN)\} = f_{PD} / PLL\_DEN \quad (8)$$

In other words, when the fractional numerator is incremented by 1 (one step), the output frequency will change by Δf_{min}. A two steps increment will therefore change the frequency by $2 \times \Delta f_{min}$.

In FSK operation, the instantaneous carrier frequency is kept changing among some pre-defined frequencies. In general, the instantaneous carrier frequency is defined as a certain frequency deviation from the nominal carrier frequency. The frequency deviation could be positive and negative.

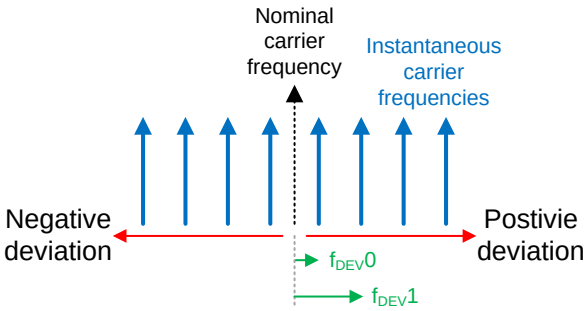


Figure 176. General FSK Definition

Equation 9 and Equation 10 define the number of steps required for the desired frequency deviation with respect to the nominal carrier frequency output. Assume Δf_{DEV} is the frequency deviation,

For positive deviation, FSK step = Round[(Δf_{DEV} × PLL_DEN x CHDIV) / (f_{PD} × $2^{FSK\_DEV\_SCALE}$)] (9)

For negative deviation, FSK step = 2^{16} – the positive deviation, FSK step answer (10)

In FSK SPI mode, registers R116 – R123 are used to store the desired FSK steps as defined in Equation 9 and Equation 10. The order of the registers, 0 to 7, depends on the application system. A typical 4FSK definition is shown in Figure 177. In this case, the FSK_DEV0 and FSK_DEV1 are calculated using Equation 9, while the FSK_DEV2 and FSK_DEV3 are calculated using Equation 10.

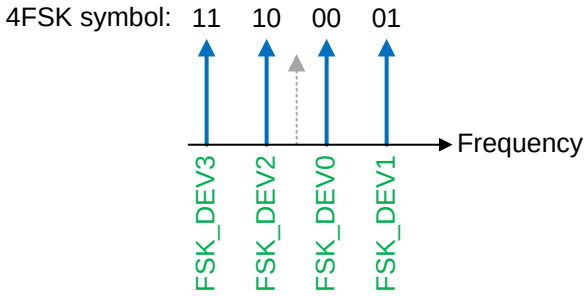


Figure 177. Typical 4FSK Definition

FSK SPI mode assumes the user knows which symbol to send. The user can directly write to FSK_SPI_DEV_SEL to select the desired frequency deviation. For example, to enable the device to support 4FSK modulation in FSK SPI mode, set:

- FSK_MODE_SEL = 2 (FSK SPI)
- FSK_SPI_LEVEL = 2 (4FSK)
- FSK_EN = 1

Table 142. FSK SPI Mode Example

DESIRED SYMBOL	WRITE REGISTER FSK_SPI_DEV_SEL	REGISTER SELECTED
10	2	FSK_DEV2
11	3	FSK_DEV3
10	2	FSK_DEV2
11	3	FSK_DEV3
01	1	FSK_DEV1
00	0	FSK_DEV0
…	…	…

FSK SPI mode supports up to eight levels of FSK. To support an arbitrary-level FSK, use FSK SPI FAST mode. Constructing pulse-shaping FSK modulation by over-sampling the FSK modulation waveform is one of the used cases of this mode.

Analog-FM modulation can also be produced in this mode. For example, with a 1-kHz sine wave modulation signal with peak frequency deviation of ±2 kHz, the signal can be oversampled, say 10 times. Each sample point corresponding to a scaled frequency deviation.

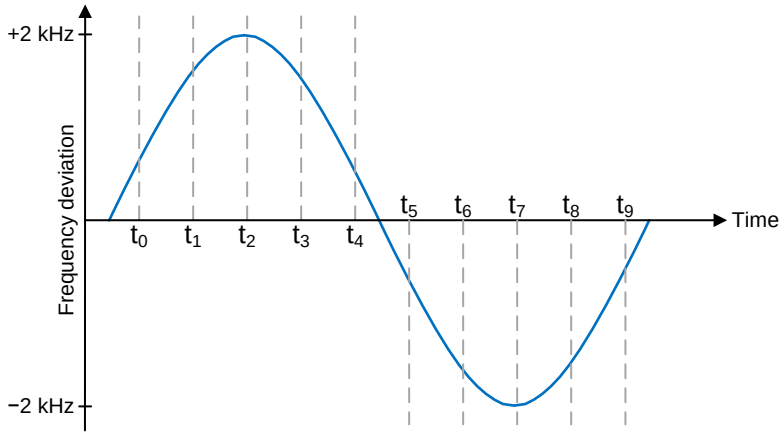


Figure 178. Oversampling Modulation Signal

In FSK SPI FAST mode, write the desired FSK steps directly to FSK_SPI_FAST_DEV. To enable this mode, set:

- FSK_MODE_SEL = 3 (FSK SPI FAST)
- FSK_EN = 1

Table 143. FSK SPI FAST Mode Example

TIME	FREQUENCY DEVIATION (Hz)	CORRESPONDING FSK STEPS(1)	WRITE TO FSK_SPI_FAST_DEV
t_0	618.034	396	396
t_1	1618.034	1036	1036
t_2	2000	1280	1280
…	…	…	…
t_6	–1618.034	64500	64500
t_7	–2000	64256	64256
…	…	…	…

(1) f_{VCO} = 3840 MHz, f_{OUT} = 480 MHz, f_{PD} = 100 MHz, CHDIV = 8, PLL_DEN = 8000000, FSK_DEV_SCALE = 0.

Block Programming is possible with FSK SPI FAST mode programming as long as ADD_HOLD = 1, which will freeze the register address after the first register write. The same programming sequent as shown in Figure 37 applies.

8.1.10 Unused Pins

TI recommends to pull these pins low if they are not used:

- Pin 5, SYNC
- Pin 28, SysRefReq
- Pin 30, RampClk
- Pin 32, RampDir

8.1.11 External Loop Filter

The LMX2572 requires an external loop filter that is application-specific and can be configured by PLLatinum Sim. For the LMX2572, it matters what impedance is seen from the Vtune pin looking outwards. This impedance is dominated by the component C3 for a third order filter or C1 for a second order filter. If there is at least 1.5 nF for the capacitance that is shunt with this pin, the VCO phase noise will be close to the best it can be. If there is less, the VCO phase noise in the 100-kHz to 1-MHz region will degrade. This capacitor should be placed close to the Vtune pin.

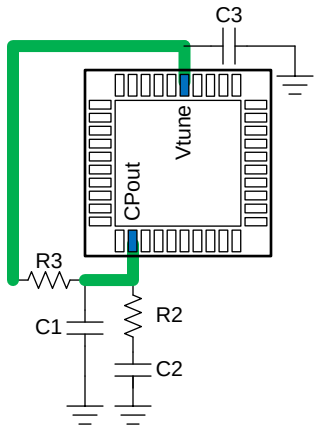


Figure 179. External Loop Filter

8.1.12 Power-Up, Wake-Up Time

When the device comes out of the powered-down state, either by resuming the POWERDOWN bit to zero or by pulling back CE pin HIGH (if it was powered down by CE pin), it takes time for the device to acquire lock again. This wake-up time depends on LDO_DLY setting, loop bandwidth, and the state machine clock frequency (= f_{OSCin} / $2^{CAL\_CLK\_DIV}$). If the loop bandwidth is greater than 20 kHz, the wake-up time could be adjusted to less than 1.5 ms with the LDO_DLY setting listed in Table 144.

Table 144. LDO_DLY Setting

STATE MACHINE CLOCK FREQUENCY	LDO_DLY
130 MHz ≤ f ≤ 200MHz	8
80 MHz ≤ f < 130 MHz	5
50 MHz ≤ f < 80 MHz	3
30 MHz ≤ f < 50 MHz	2
f < 30 MHz	1

8.2 Typical Application

This application example demonstrates how to set up the LMX2572 in FSK SPI FAST mode to synthesize 4-level GFSK modulation.

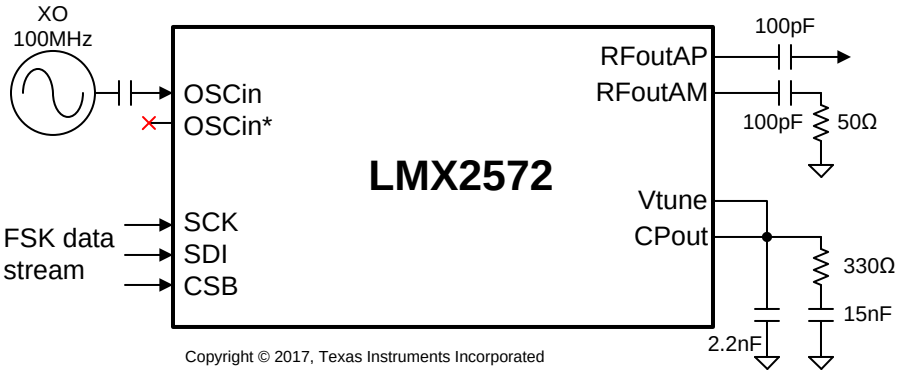


Figure 180. Application Example Schematic

8.2.1 Design Requirements

Table 145 lists the design parameters for this example.

Table 145. Design Parameters

PARAMETER	EXAMPLE VALUE
OSCin frequency	100 MHz
RFout frequency	490 MHz
4FSK modulation baud rate	125 kSps
BT of Gaussian filter	0.4
FSK frequency deviation	±17 kHz and ±51 kHz
Fractional denominator	8000000

8.2.2 Detailed Design Procedure

First, determine all the elementary blocks of a synthesizer.

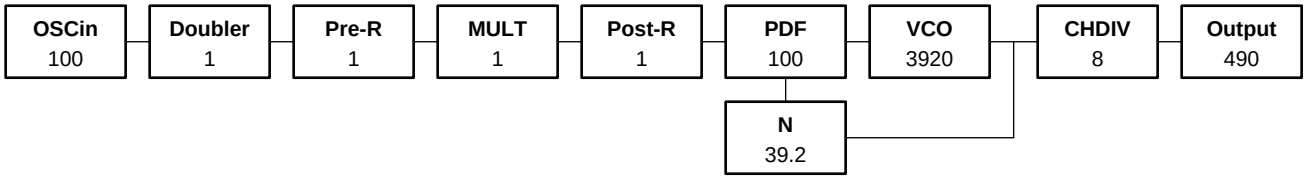


Figure 181. Application Example Frequency Plan

Then, program these registers to make LMX2572 locks to the target output frequency:

- OSC_2X = 0
- PLL_R_PRE = 1
- MULT = 1
- PLL_R = 1
- PLL_N[18:16] = 0; PLL_N[15:0] = 39
- PLL_NUM[31:16] = 24; PLL_NUM[15:0] = 27136
- PLL_DEN[31:16] = 122; PLL_DEN[15:0] = 4680
- CHDIV = 8

Then program these registers to enable FSK SPI FAST mode:

- FSK_MODE_SEL = 3
- FSK_DEV_SCALE = 1
- FSK_EN = 1

A Mathlab script is then developed to generate the necessary codes that will be used to continuously bit-stream the LMX2572. These codes are uploaded to the data generator DG2020, which will generate the SPI data to *modulate* the LMX2572.

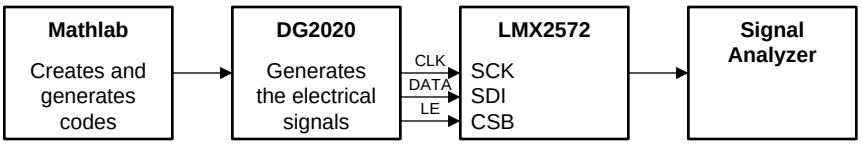


Figure 182. Application Example Test Setup

8.2.3 Application Curves

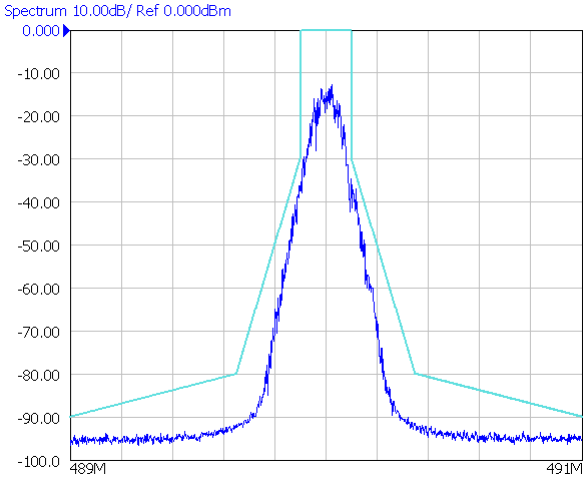


Figure 183. Gaussian 4FSK Modulated Spectrum

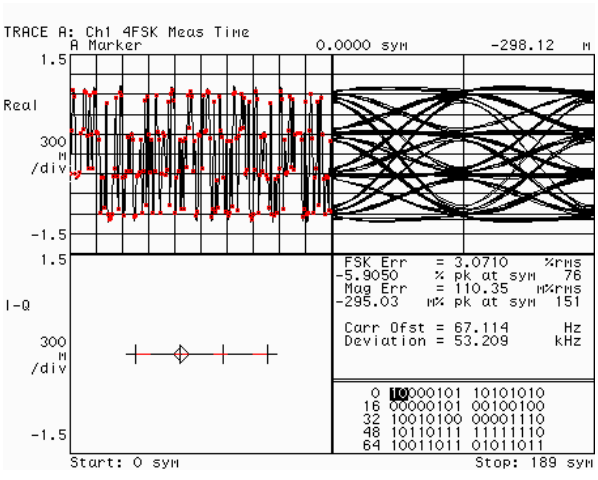


Figure 184. Gaussian 4FSK Modulation Quality

8.3 Do's and Don'ts

- RFout output buffers do not need an external pullup. An AC-couple to the load is good enough.
- The last shunt capacitor of the loop filter should be placed close to the Vtune pin.

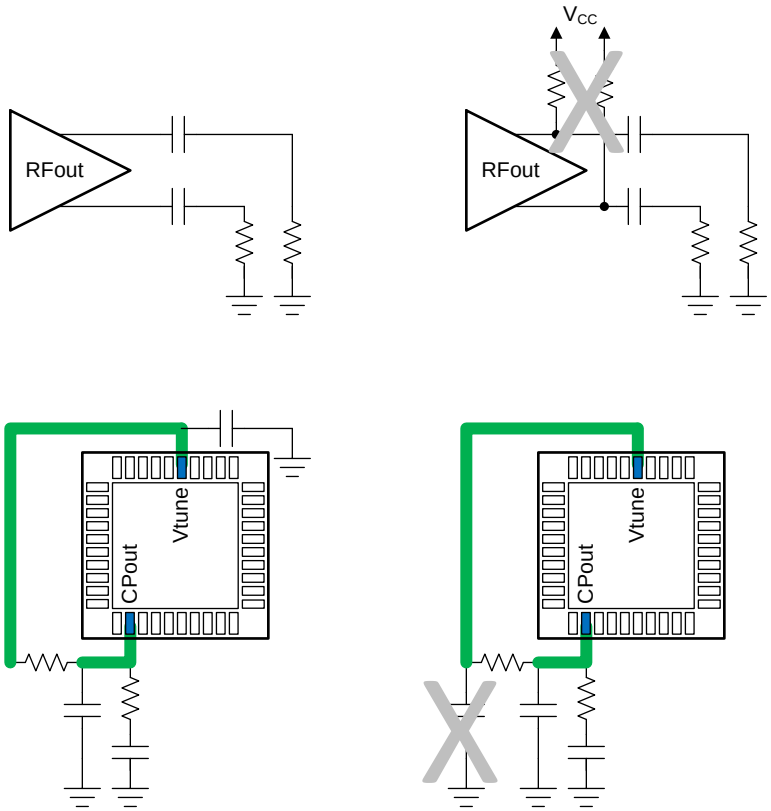


Figure 185. Do's and Don'ts

9 Power Supply Recommendations

TI recommends placing a 100-nF capacitor close to each of the power supply pins. If fractional spurs are a large concern, use a ferrite bead to each of these power supply pins to reduce spurs to a small degree. This device has integrated LDOs, which improves the resistance to power supply noise. Figure 186 is a typical application example.

This device can be powered by an external DC/DC buck converter, such as the TPS62150. Note that although Rtps1 and Rtps2 are 1.5 Ω in the schematic, they could be potentially replaced with a larger resistor value or inductor value for better power supply filtering. Alternatively, the use of a larger capacitance value for C2 and C4 could also result in better power supply filtering.

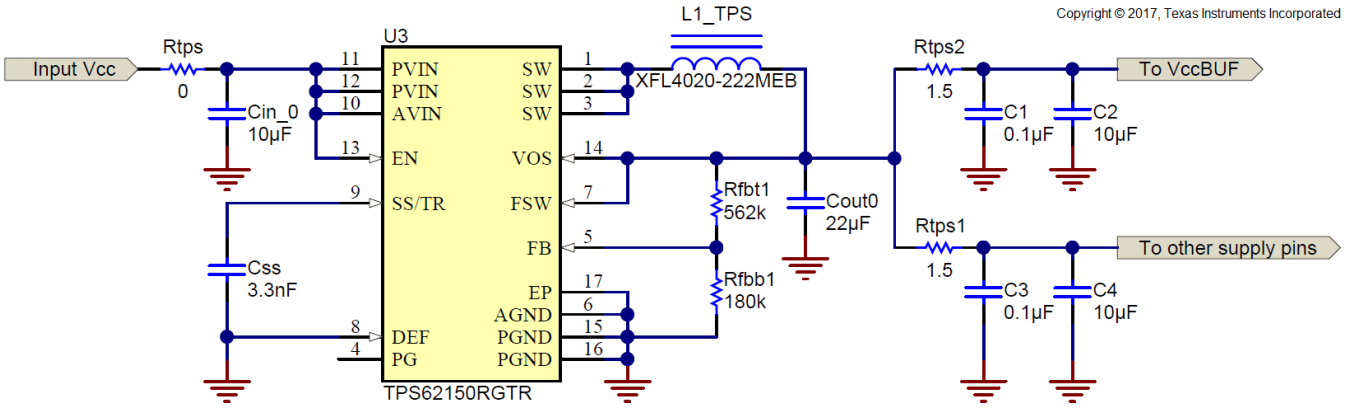
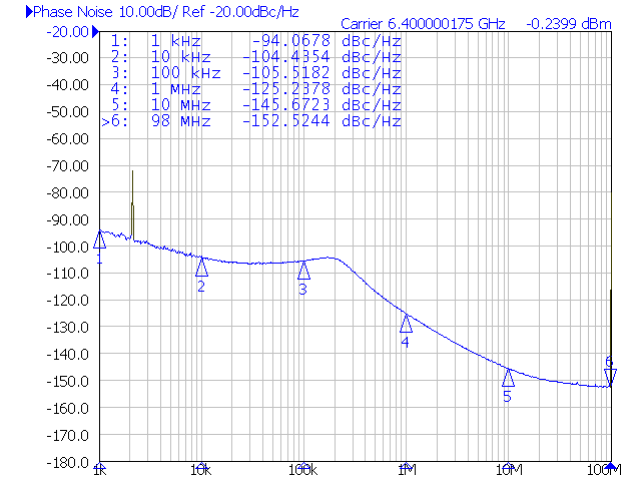
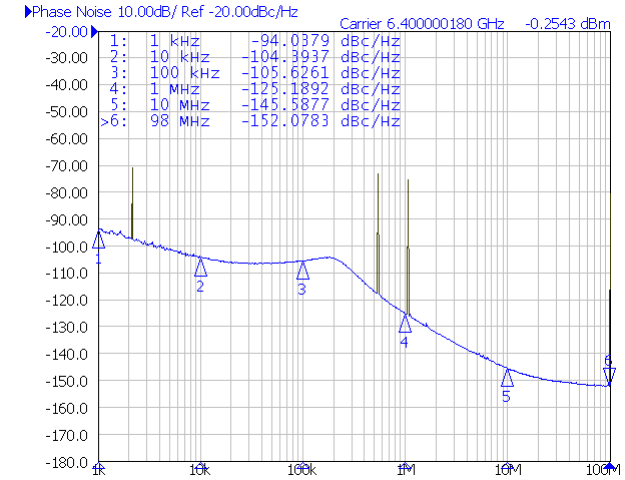


Figure 186. Power Supply With a DC/DC Converter



LDO output = 3.3 V; Current = 80 mA

Figure 187. Phase Noise With LDO Power Supply



DC/DC input = 5 V; DC/DC output = 3.3 V; Current = 56 mA

Figure 188. Phase Noise With DC/DC Power Supply

The power consumption of LMX2572 depends on its configuration. The data as shown in the Electrical Characteristics table represent the current consumption at some specific conditions. It is possible to get a smaller or higher current consumption than what is specified in the data sheet. To get a rough estimation on current consumption at a particular configuration, use TICS Pro.

10 Layout

10.1 Layout Guidelines

In general, the layout guidelines are similar to most other PLL devices. Here are some specific guidelines:

- GND pins may be routed on the package back to the DAP.
- The OSCin pins are internally biased and must be AC-coupled.
- The RampClk, RampDir, and SysRefReq can be grounded to the DAP if not used.
- Get a loop filter capacitor as close to the Vtune pin as possible to this. This may mean separating it from the rest of the loop filter.
- If a single-ended output is necessary, the other side must have the same loading. However, the routing for the used side can be optimized by routing the complementary side through a via to the other side of the board. On this side, make the load look equivalent to the side that is used.
- Ensure the DAP on the device is well-grounded with many vias, preferably copper filled.
- Have a thermal pad that is as large as the exposed pad. Add vias to the thermal pad to maximize thermal performance.
- Use a low loss dielectric material, such as Rogers 4003, for optimal output power.

10.2 Layout Example

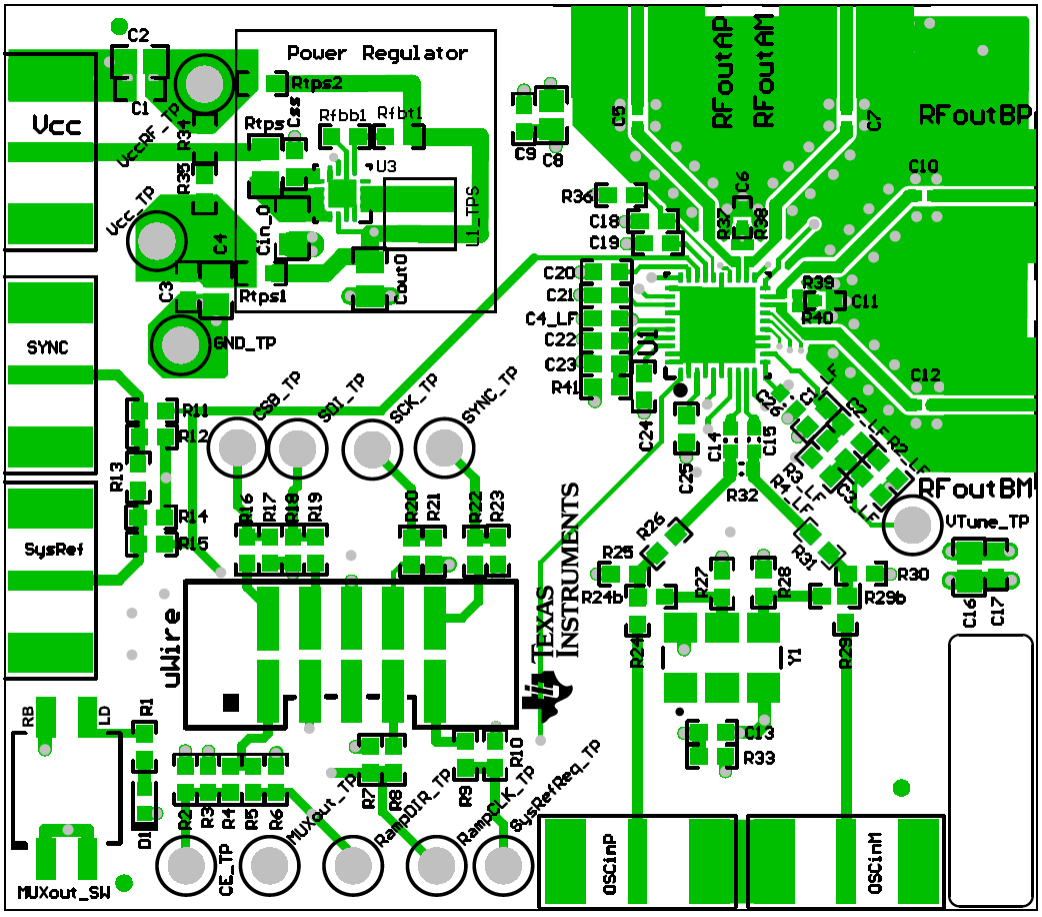


Figure 189. Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

Texas Instruments has several software tools to aid in the development at www.ti.com. Among these tools are:

- PLLatinum Sim program for designing loop filters, simulating phase noise and spurs.
- TICS Pro software to understand how to program the device and for programming the EVM board.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- *TPS62150 3–17V 1A Step-down converter with dcs-control* (SLVSAL5)
- *AN-1879 Fractional N frequency synthesis* (SNAA062)
- *Frequency shift keying with LMX2571* (SNAA309)
- *PLL performance, simulation, and design handbook* (SNAA106)
- *LMX2572EVM User's guide* (SNAU217)

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMX2572RHAR	ACTIVE	VQFN	RHA	40	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 85	LMX2572	Samples
LMX2572RHAT	ACTIVE	VQFN	RHA	40	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 85	LMX2572	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

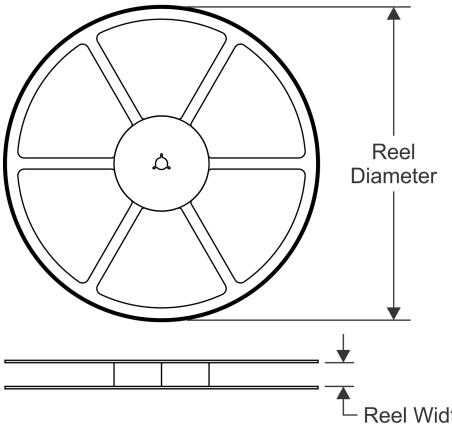
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

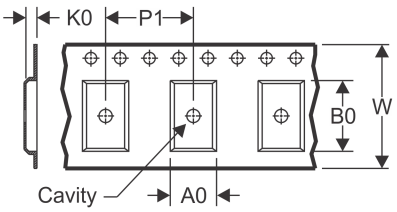
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

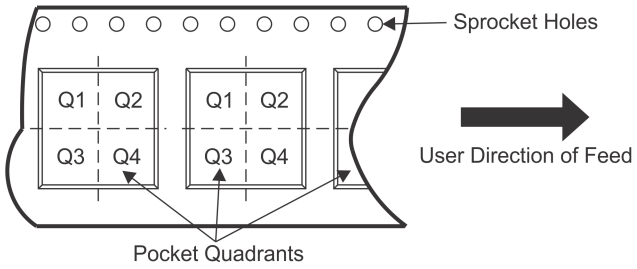


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

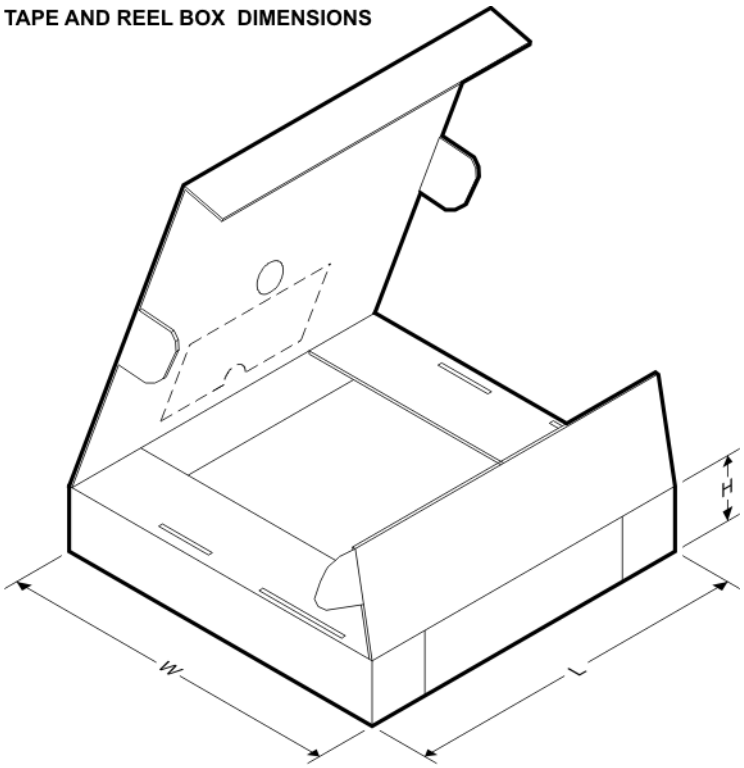
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMX2572RHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q1
LMX2572RHAT	VQFN	RHA	40	250	178.0	16.4	6.3	6.3	1.5	12.0	16.0	Q1

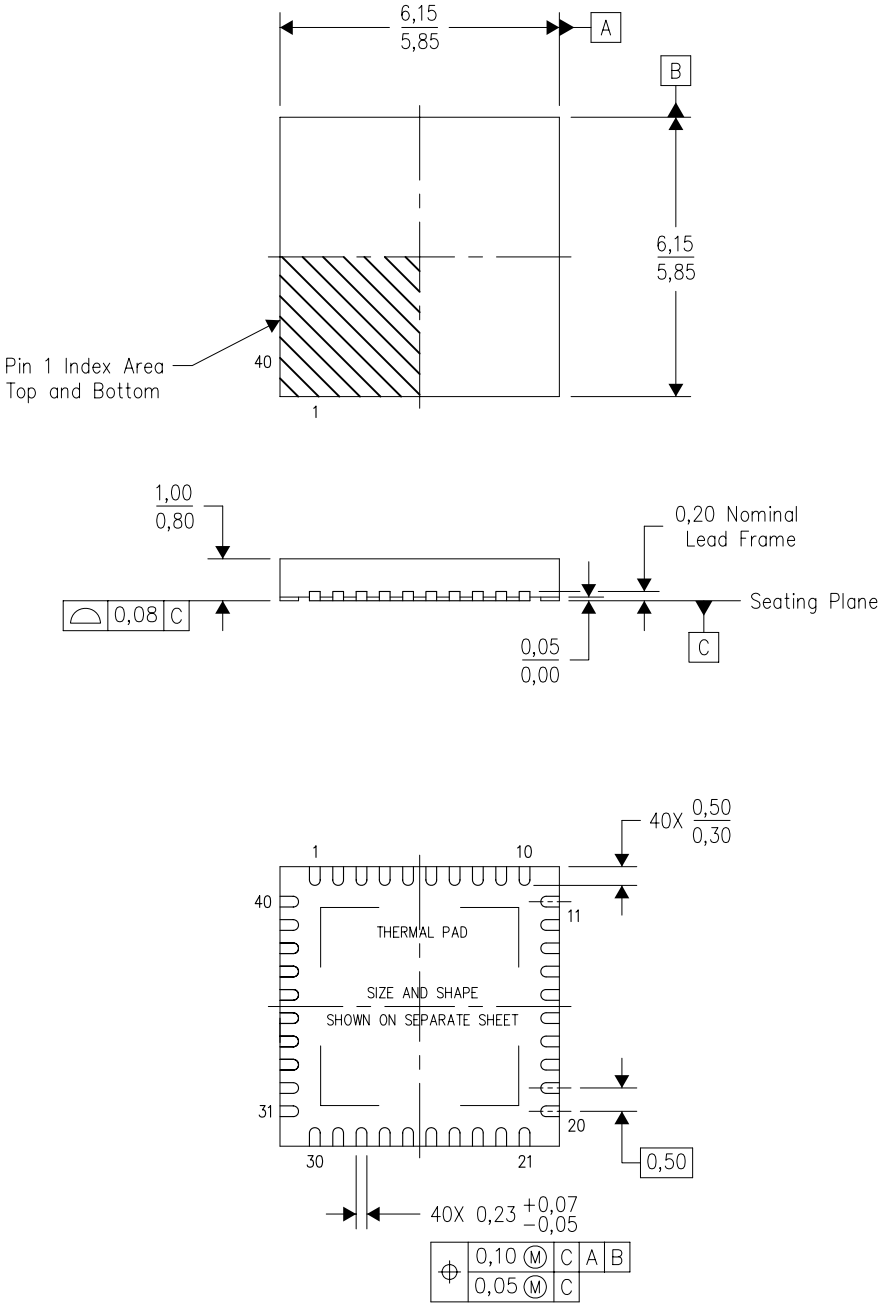
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMX2572RHAR	VQFN	RHA	40	2500	367.0	367.0	38.0
LMX2572RHAT	VQFN	RHA	40	250	210.0	185.0	35.0

RHA (S–PVQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD



Bottom View

4204276/E 06/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Package complies to JEDEC MO–220 variation VJJD–2.

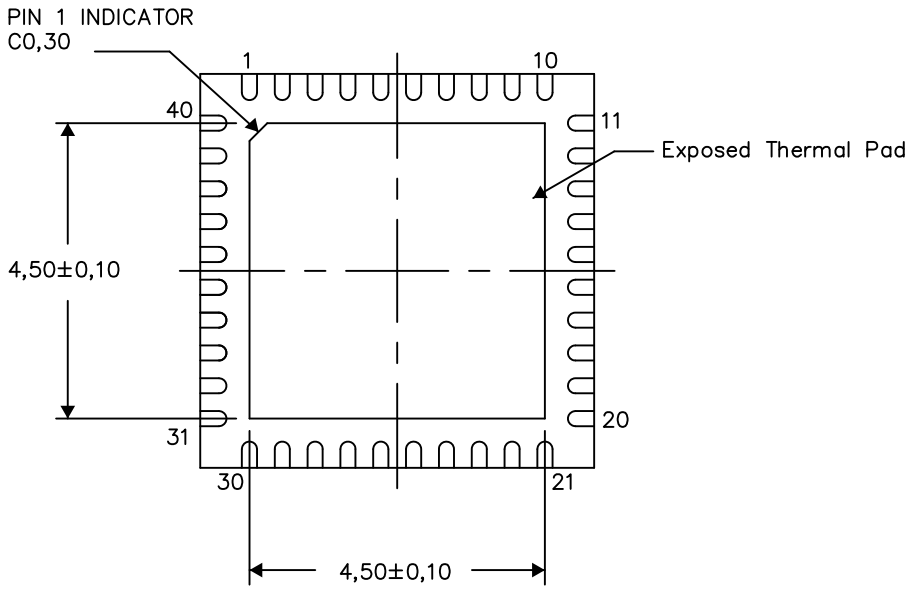
RHA (S–PVQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



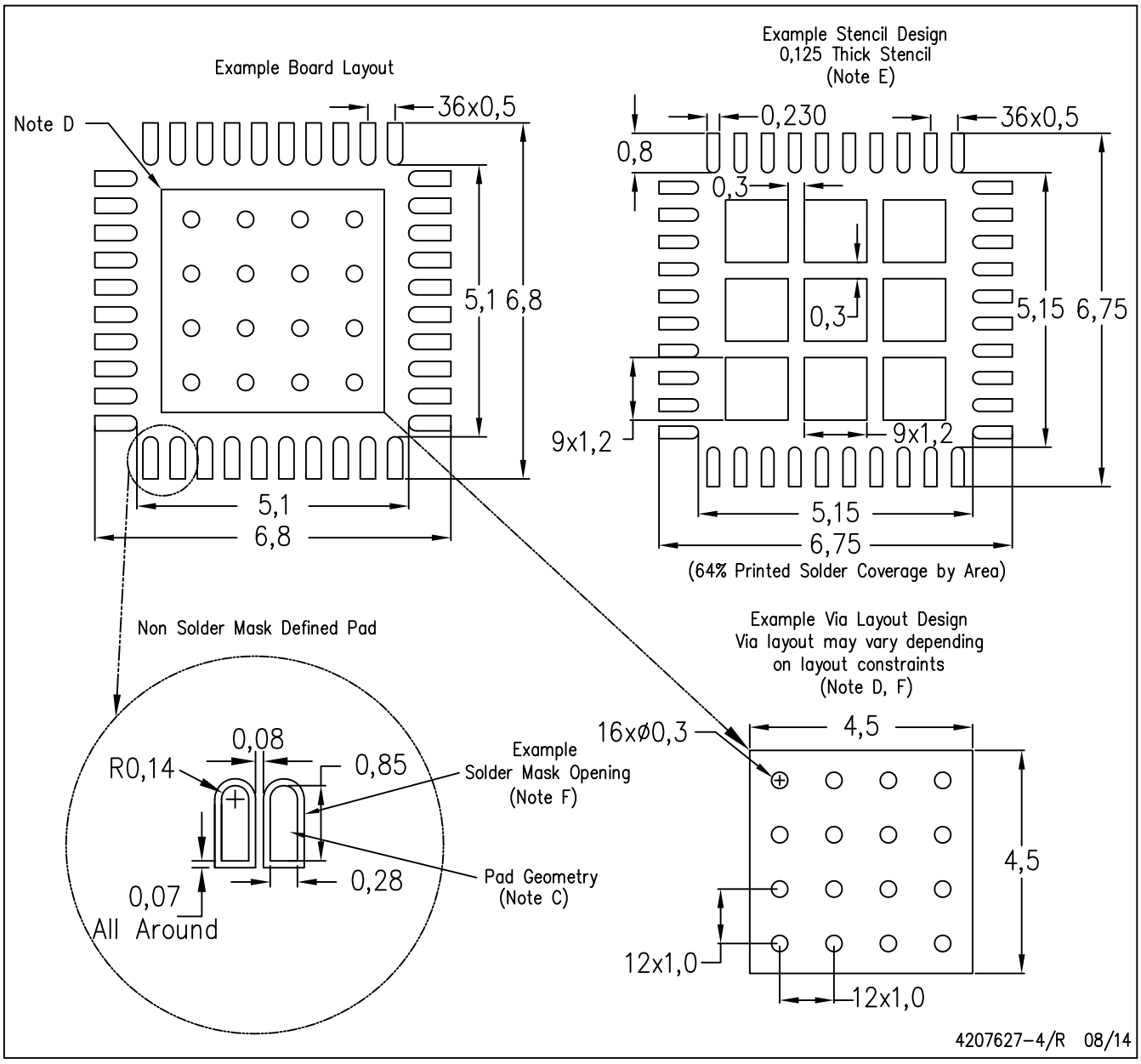
Bottom View

Exposed Thermal Pad Dimensions

4206355–4/X 08/14

NOTES: A. All linear dimensions are in millimeters

RHA (S–PVQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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