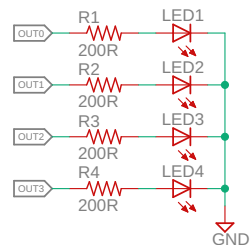
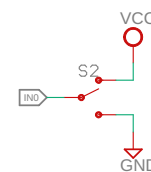


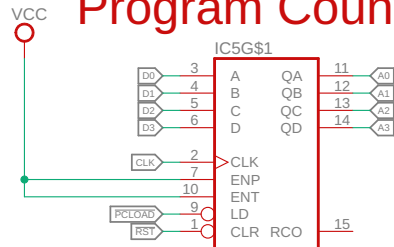
Output



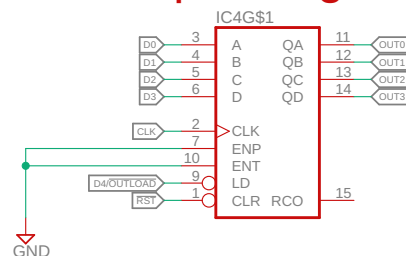
Input



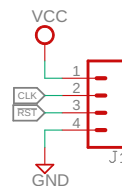
Program Counter



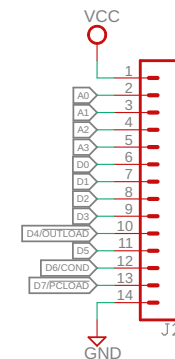
Output Register



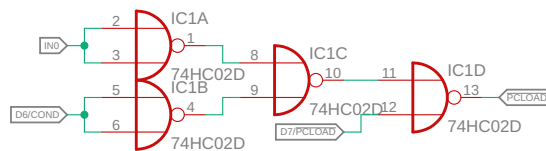
Power Clock/Reset



Address/Data Bus



Instruction Decode



TITLE: CPU-1 3-Chipbit

Document Number:

REV:

Date: 12/28/22 8:15 AM

Sheet: 1/1