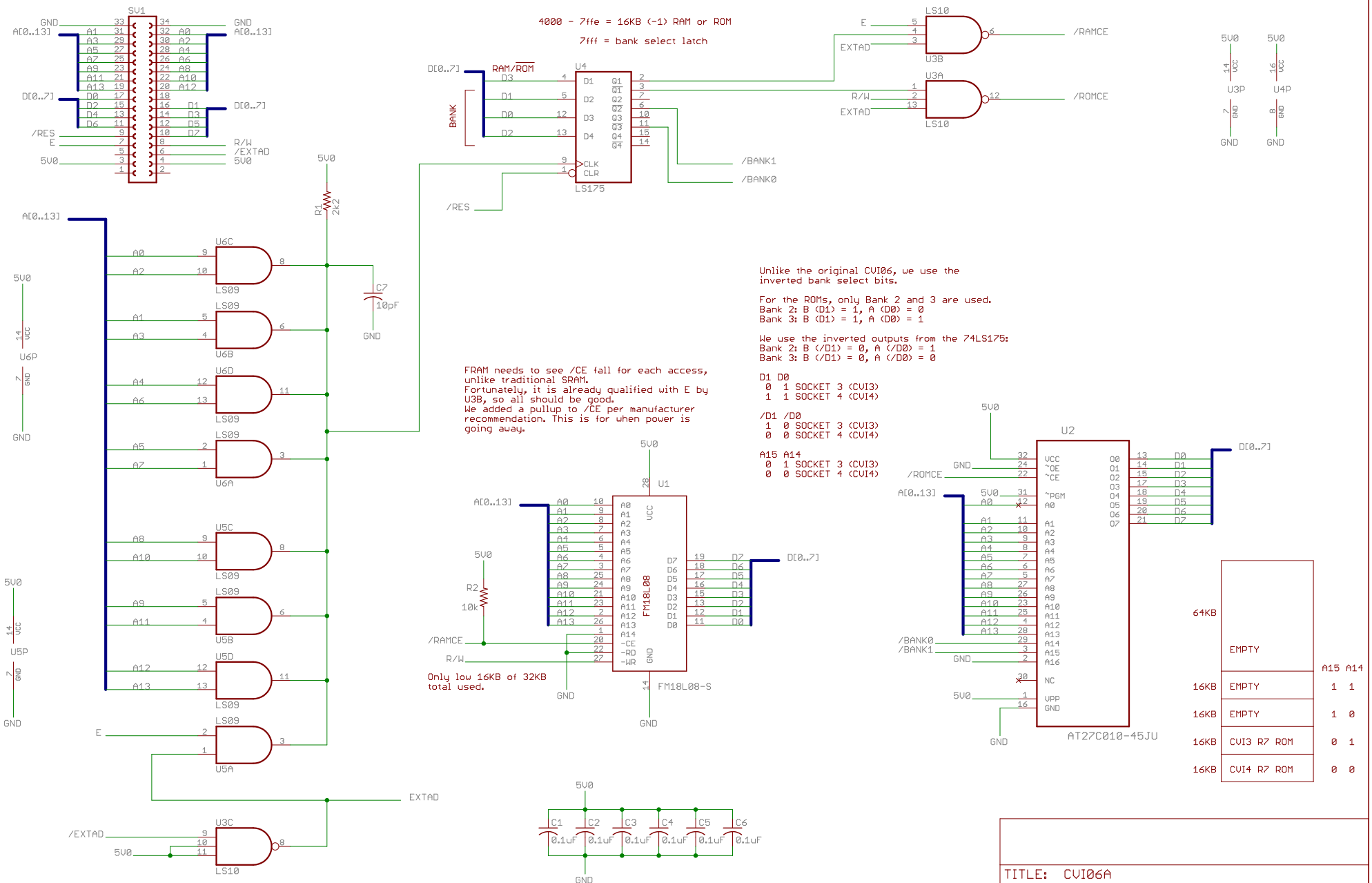
SV1
GND
A[0..13]
DI[0..7]
/RES
E
5V0
R/W
/EXTAD
4000 - 7ffe = 16KB (-1) RAM or ROM
7fff = bank select latch
RAM/ROM
BANK
U4
LS175
/BANK1
/BANK0
LS10
U3B
U3A
/RAMCE
/ROMCE
U3P
U4P
R1
2k2
C7
10pF
U6C
U6B
U6D
U6A
U5C
U5B
U5D
U5A
U6P
U5P
EXTAD
U3C
Unlike the original CVI06, we use the
inverted bank select bits.
For the ROMs, only Bank 2 and 3 are used.
Bank 2: B (D1) = 1, A (D0) = 0
Bank 3: B (D1) = 1, A (D0) = 1
We use the inverted outputs from the 74LS175:
Bank 2: B (/D1) = 0, A (/D0) = 1
Bank 3: B (/D1) = 0, A (/D0) = 0
D1 D0
0 1 SOCKET 3 (CVI3)
1 1 SOCKET 4 (CVI4)
/D1 /D0
1 0 SOCKET 3 (CVI3)
0 0 SOCKET 4 (CVI4)
A15 A14
0 1 SOCKET 3 (CVI3)
0 0 SOCKET 4 (CVI4)
FRAM needs to see /CE fall for each access,
unlike traditional SRAM.
Fortunately, it is already qualified with E by
U3B, so all should be good.
We added a pullup to /CE per manufacturer
recommendation. This is for when power is
going away.
U1
FM18L08
FM18L08-S
R2
10k
Only low 16KB of 32KB
total used.
U2
AT27C010-45JU
64KB
EMPTY
16KB
EMPTY
CVI3 R7 ROM
CVI4 R7 ROM
A15 A14
1 1
1 0
0 1
0 0
C1
C2
C3
C4
C5
C6
0.1uF
TITLE: CVI06A
Document Number:
REV:
Date: 1/27/20 20:09
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