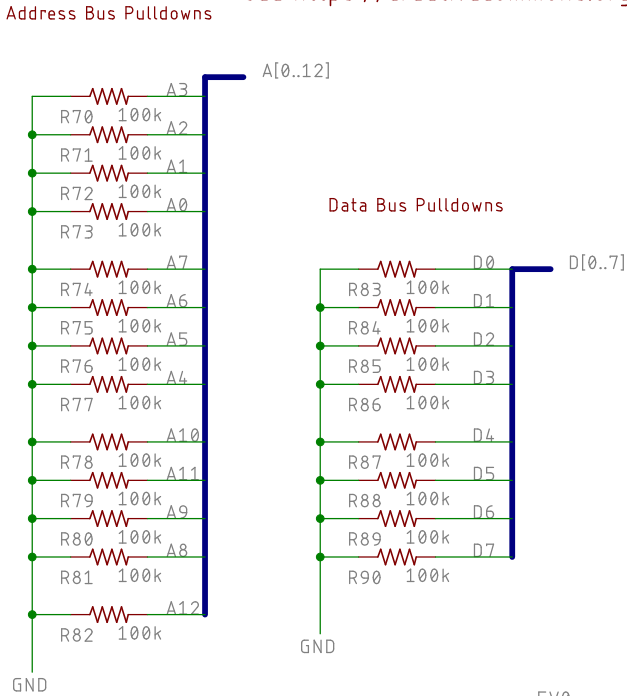
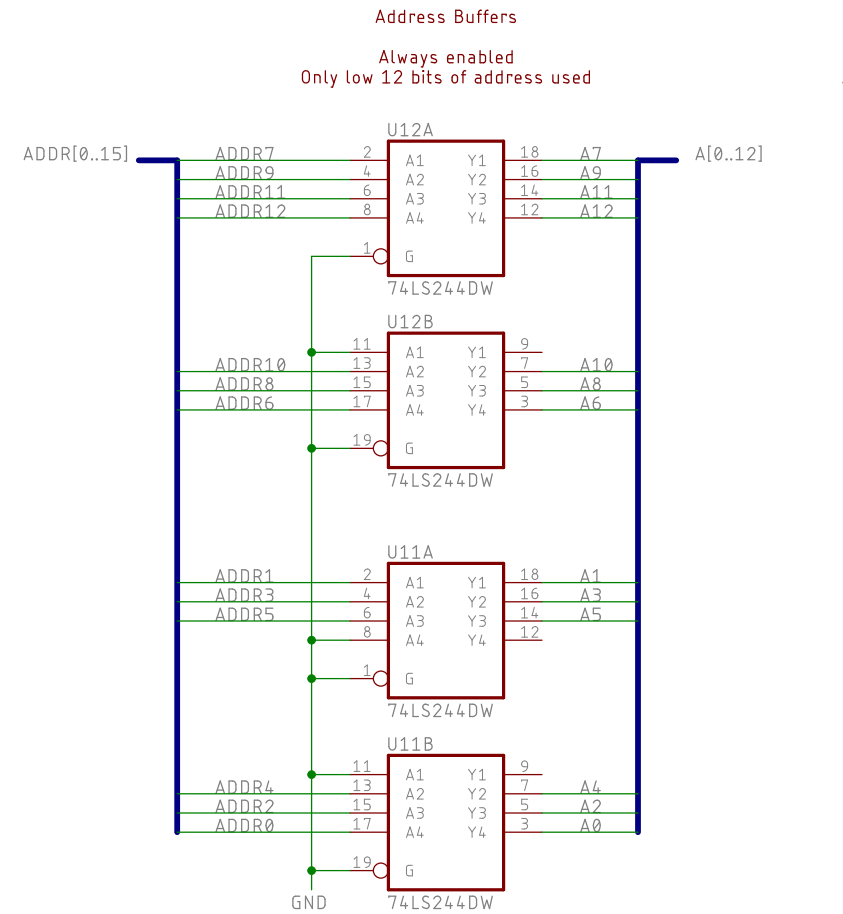
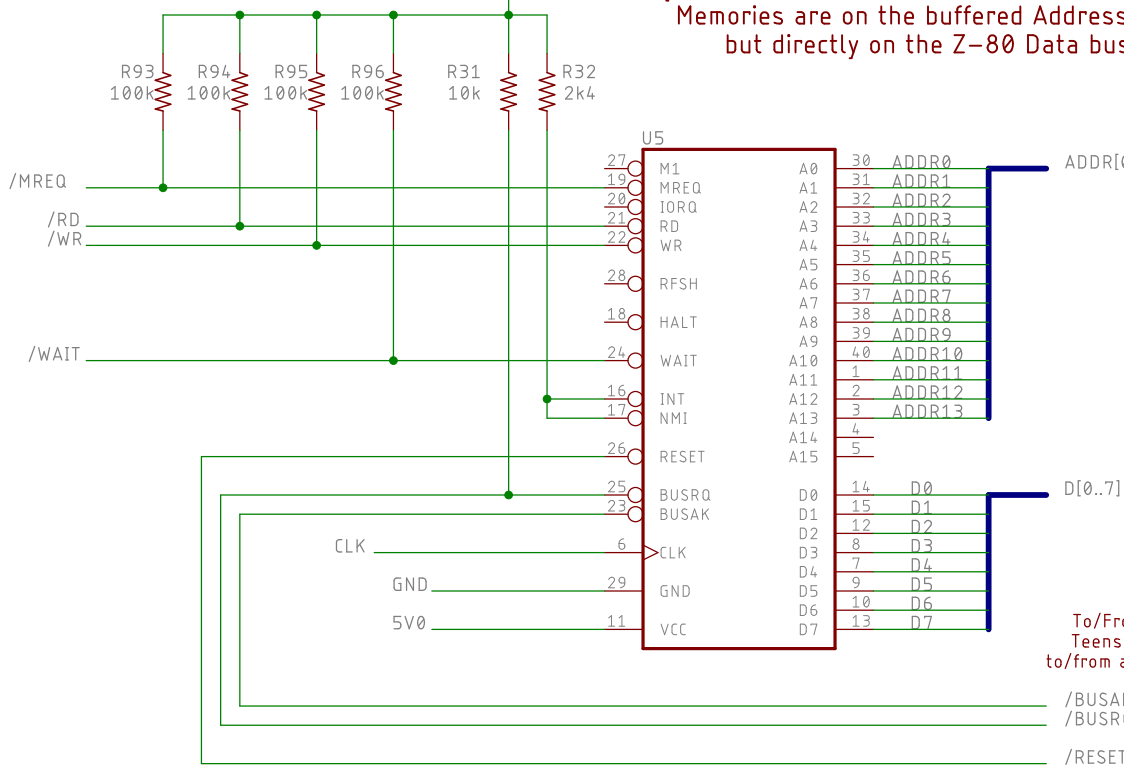


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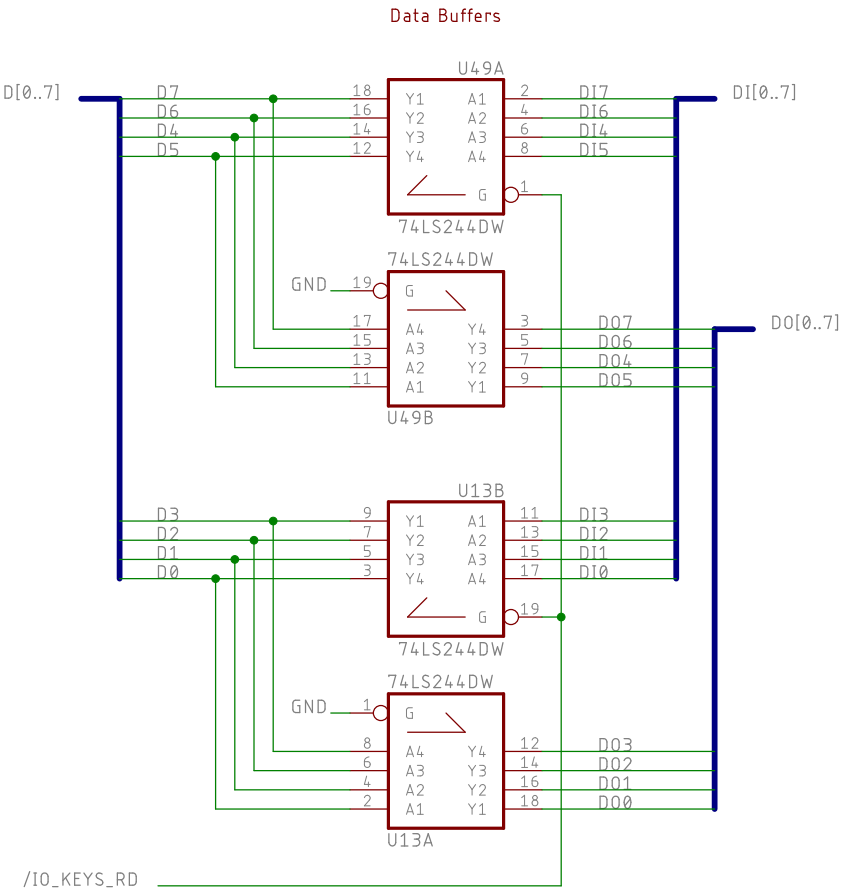
Teensy sits on Z-80 side of Address and Data.
Teensy 4.1 is not 5V-tolerant, LVC buffers to level shift.
Memories are on the buffered Address bus,
but directly on the Z-80 Data bus.



To/From Teensy
Teensy can DMA
to/from all addresses

Teensy controls Z-80 reset

Outputs from Teensy only need to pull DOWN



8000 0000 ROM A (1) x x 0 0 0 0
8800 0800 ROM B (2) 0 0 1 0
9000 1000 ROM C (3) 0 1 0 0
D800 9800 I/O 0 1 1 0
DC00 9C00 KEYS 0 1 1 1

A000 2000 RAM LO 1 0
B000 3000 RAM HI 1 1

All I/O is memory mapped.
Z-80 IO Ports are unused.
Code does not use /INT or /NMI.
/RFSH is not used.
/BUSREQ is not used.
/HALT is not used.

Z-80, BUFFERS, DECODE

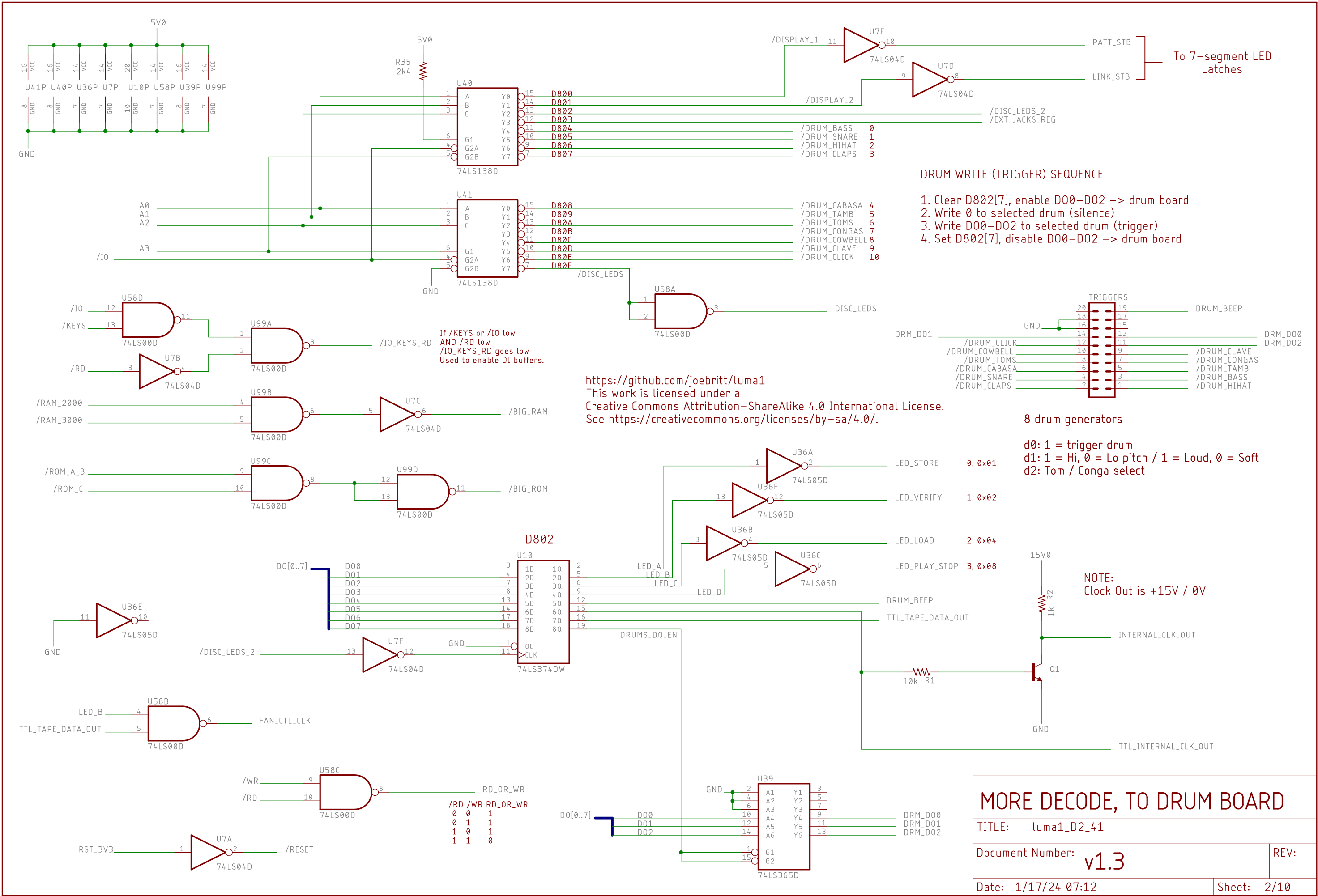
TITLE: luma1_D2_41

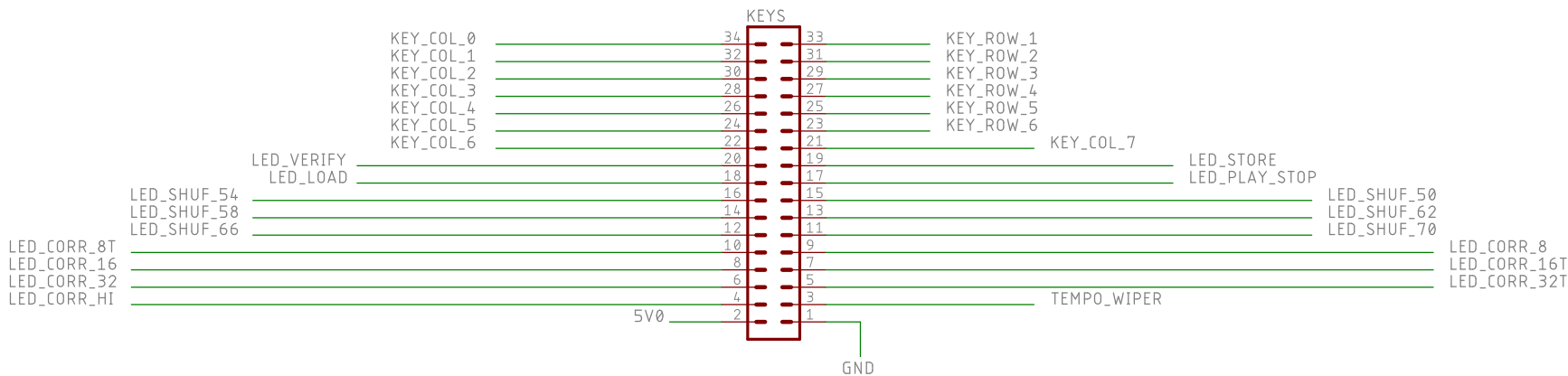
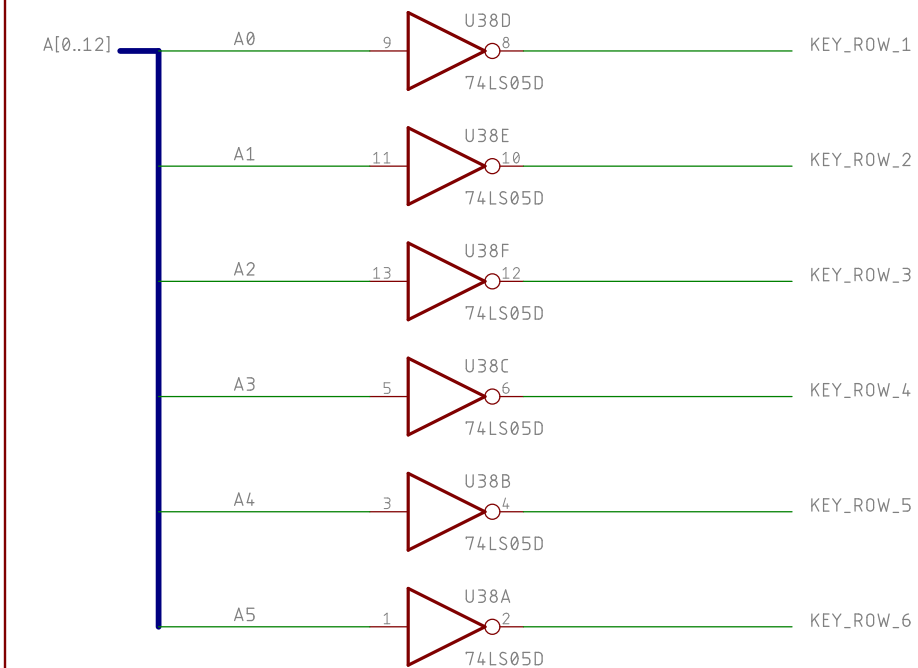
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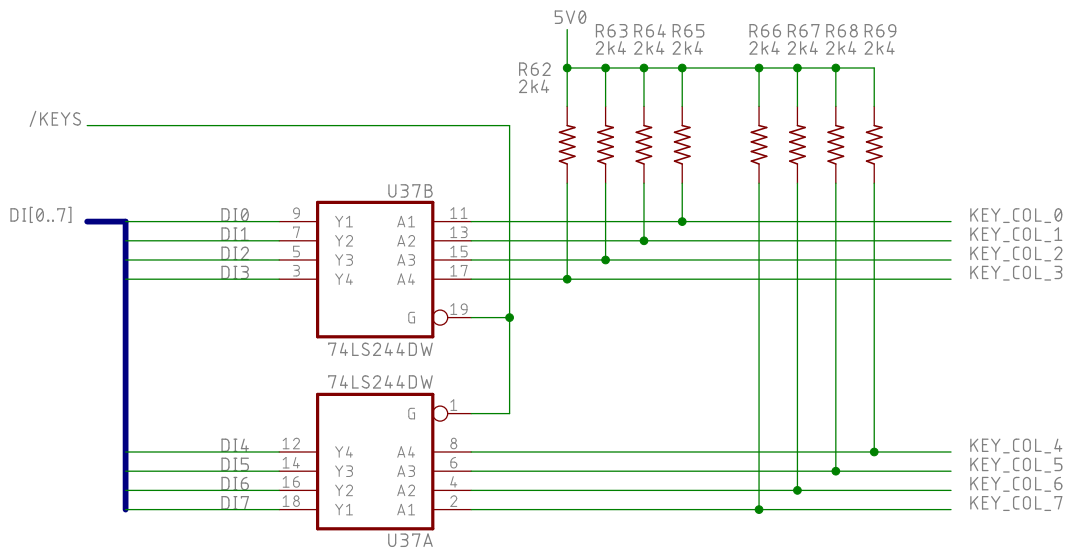
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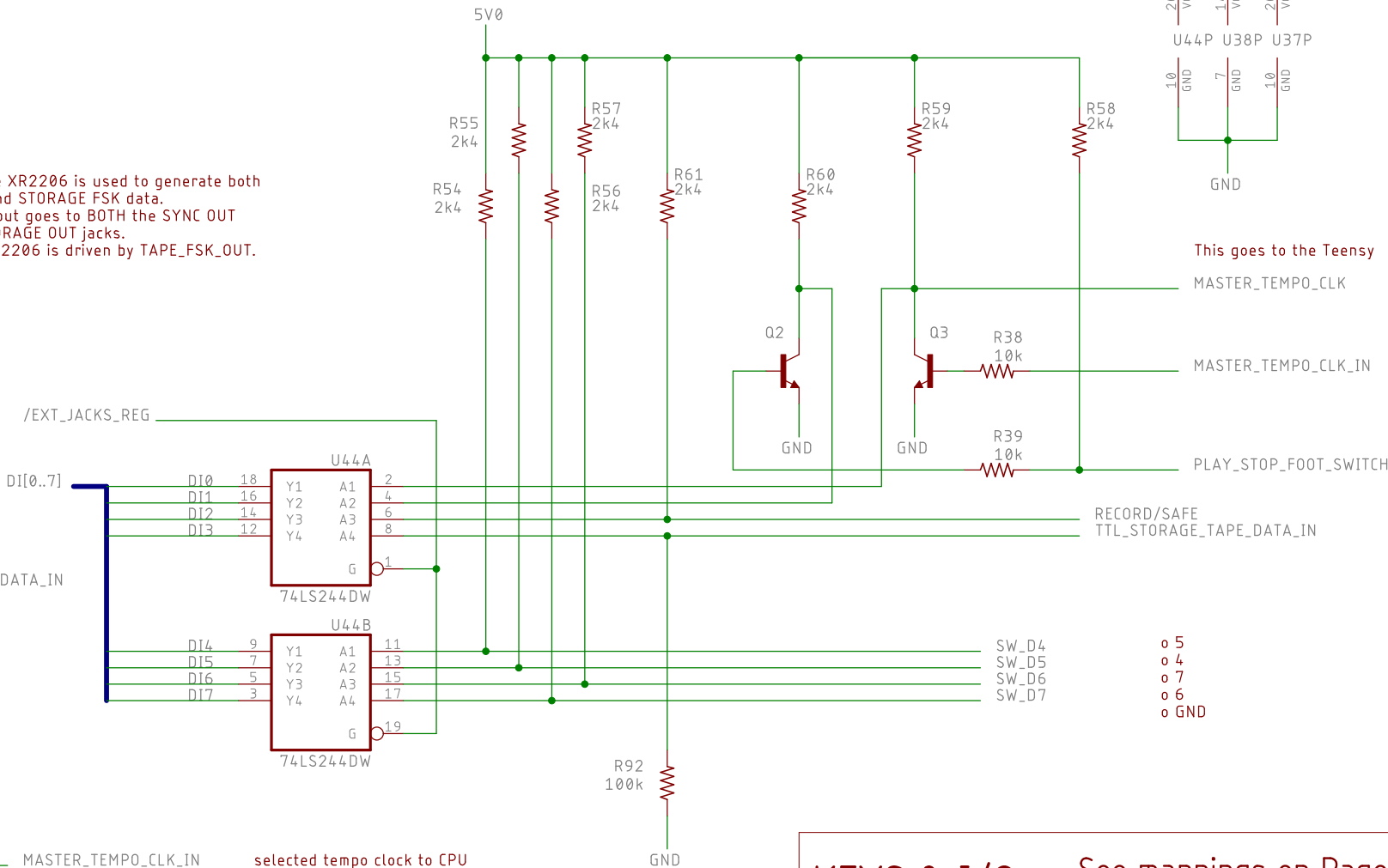




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A single XR2206 is used to generate both
SYNC and STORAGE FSK data.
It's output goes to BOTH the SYNC OUT
and STORAGE OUT jacks.
That XR2206 is driven by TAPE_FSK_OUT.



x x TAPE_STORAGE_IN
x x TTL_STORAGE_TAPE_DATA_IN

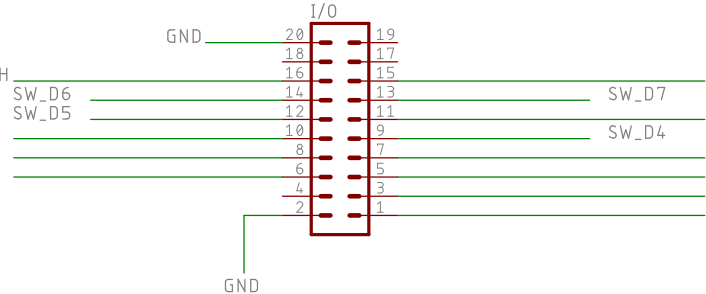
x x TAPE_STORAGE_OUT
x x TAPE_SYNC_OUT
x x TTL_TAPE_DATA_OUT

x x TAPE_SYNC_IN
x x TTL_TAPE_SYNC_CLK

Rev3 omits the EXT CLK IN jack, which accepts a 5V clock

PLAY/STOP footswitch jack
bit 6 (2) of rotary switch
bit 5 (1) of rotary switch
x tip of TAPE STORAGE IN jack
x tip of TAPE SYNC OUTPUT jack
x tip of TAPE SYNC INPUT jack

TAPE_STORAGE_IN
TAPE_SYNC_OUT
TAPE_SYNC_IN



MASTER_TEMPO_CLK_IN
RECORD/SAFE
TAPE_STORAGE_OUT
TTL_TAPE_SYNC_CLK
INTERNAL_CLK_OUT
INTERNAL_TEMPO_CLK

selected tempo clock to CPU
bit 7 (3) of rotary switch
bit 4 (0) of rotary switch

x tip of TAPE STORAGE OUT jack
x from XR2211 tone decoder (tape sync decoder)
tip of INTERNAL CLOCK OUT jack
tempo clock from XR2206 on D (CPU) board

KEYS & I/O See mappings on Page 9

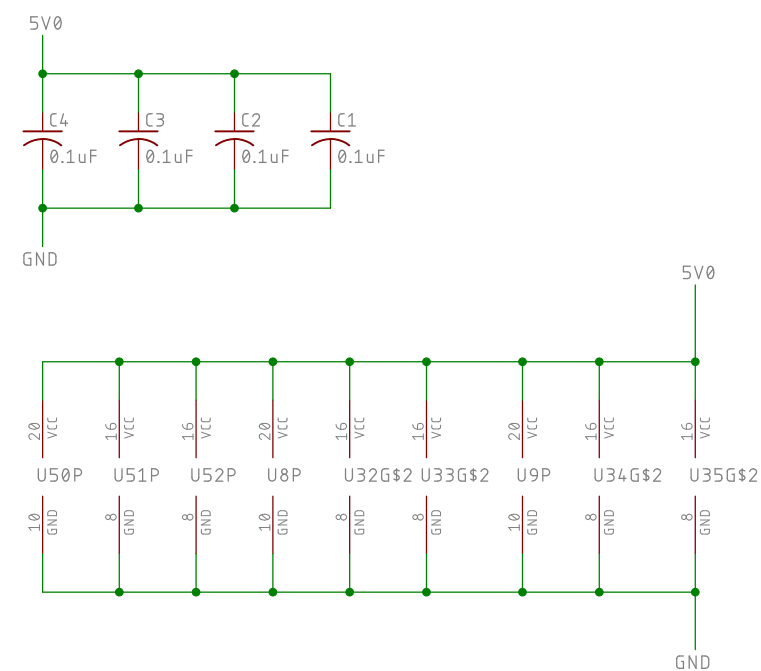
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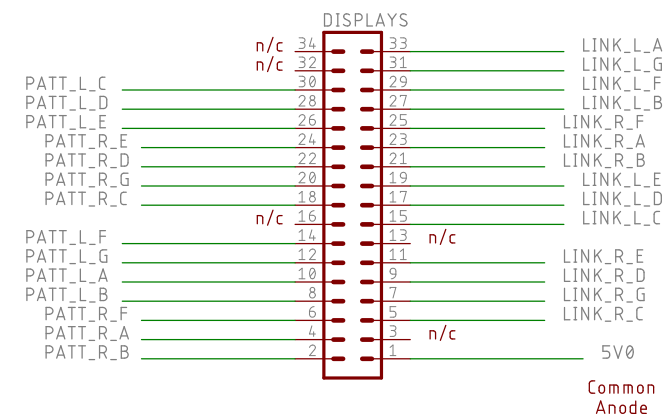
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LINK_R_G

NOTE!
In original design, headers are rotated 180 degrees.
Legacy connector headers are a special footprint,
with signals rotated.



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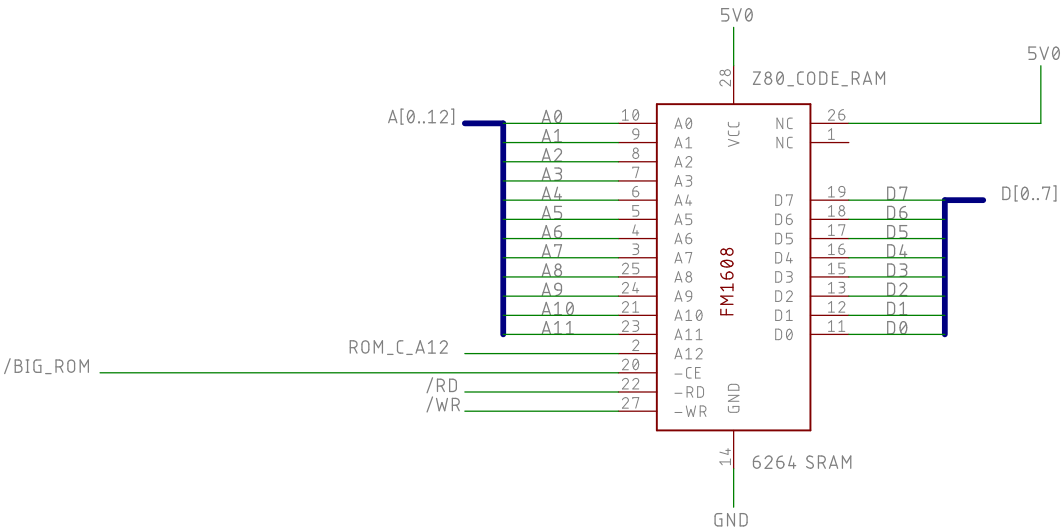
REV:

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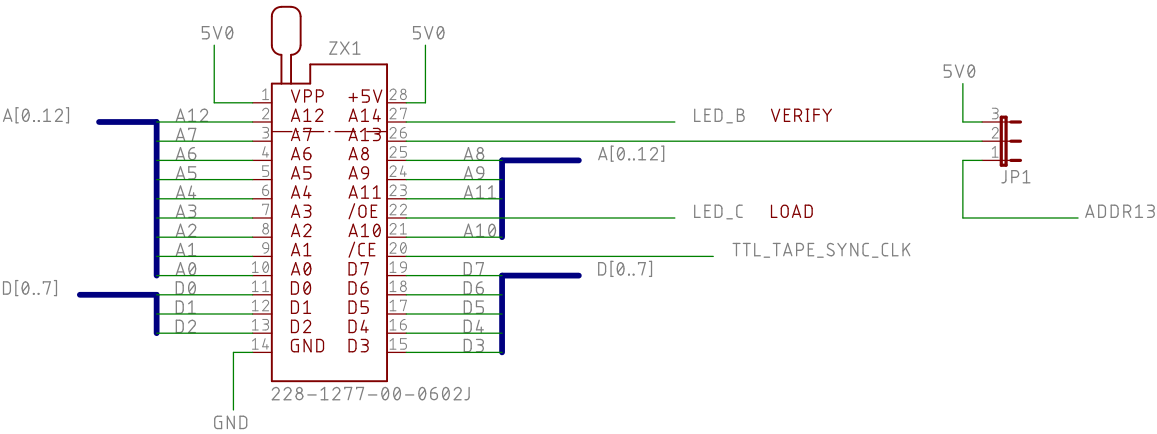
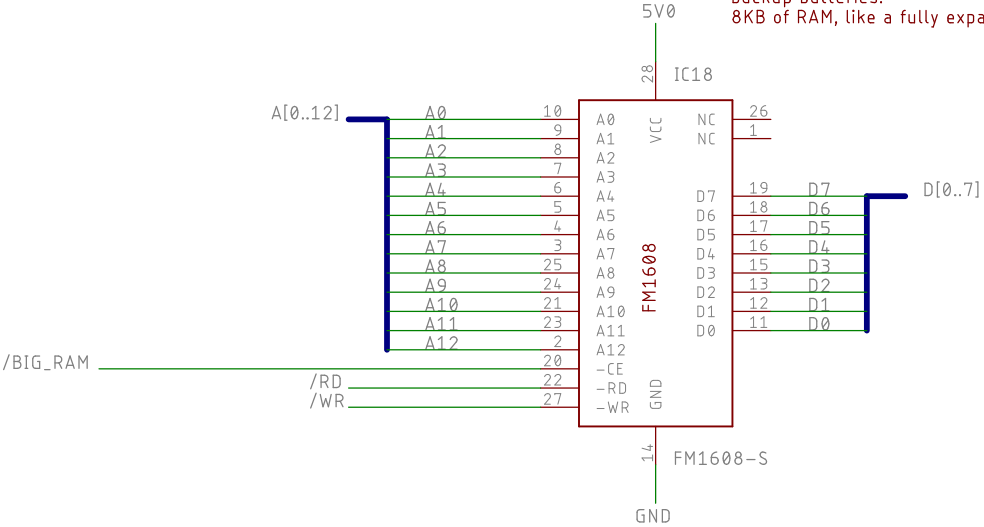
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FRAM
EPROM
Replacement

Need (/ROM_1_2 == 0) || (/ROM_3 == 0) term



FM1608 FRAM eliminates need for backup batteries.
8KB of RAM, like a fully expanded LM-1.



EPROM Reading is a total hack.

1. MENU -> EPROM DUMP, pause Z-80, Teensy takes bus
2. Prompt user for EPROM size
3. Tell user how to set power jumper
4. Data bus Z-80 -> Teensy
5. Addr bus Z-80 <- Teensy
6. Drive A13..A0 Z-80 Addr bus
7. Drive A14 = 0 on LED_B = 0
8. Drive /OE = 0, LED_C = 0
9. Ask user to insert EPROM, hit a key
10. Read EPROM: present Addr[0..13], delay 100uS to settle, read data bus, repeat for all bytes up to 16KB
12. If 27256, ask user to remove EPROM, flip A14 to 1 (LED_B = 1), repeat steps 8-11
13. Drive /OE = 1, LED_C = 1
14. Save buffer someplace on SD, and/or in voice RAM

MEMORY

TITLE: luma1_D2_41

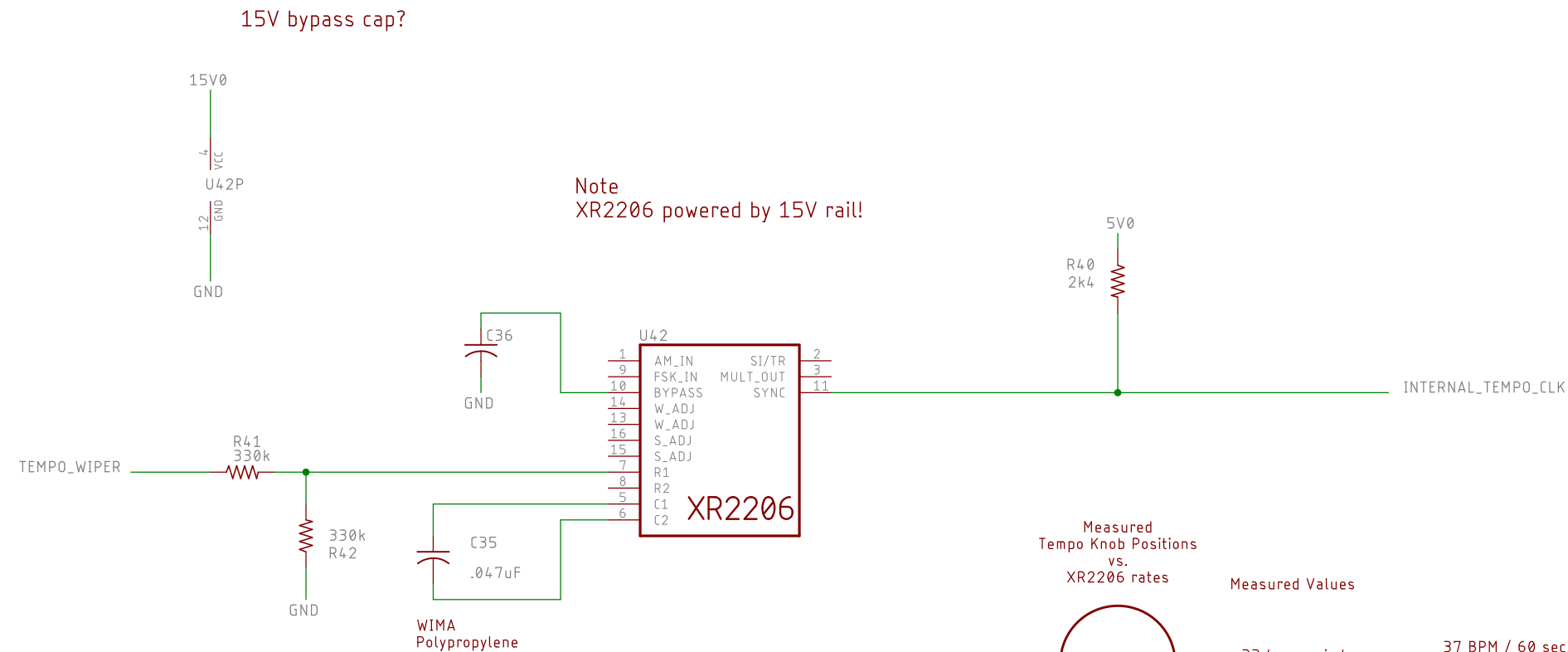
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Measured Tempo Knob Positions vs. XR2206 rates	Measured Values	Ideal Values Internally 48 PPQN
	33.4ms period 37 BPM (LED readout)	37 BPM / 60 sec/min = 0.617 BPS (quarter notes per sec) 0.617 Qnotes/sec * 48 PPQ = 29.6 Pulses Per Sec 1/29.6 PPS = 33.8 ms
	12.4ms period 100 BPM (LED readout)	100 BPM / 60 sec/min = 1.67 BPS (quarter notes per sec) 1.67 Qnotes/sec * 48 PPQ = 80 Pulses Per Sec 1/80 PPS = 12.5 ms
	7.8ms period 161 BPM (LED readout)	161 BPM / 60 sec/min = 2.684 BPS (quarter notes per sec) 2.684 Qnotes/sec * 48 PPQ = 128.8 Pulses Per Sec 1/128.8 PPS = 7.8 ms

MIDI Clock is only 24 PPQ.
So, for each MIDI Clock received, the Teensy generates 2 clock pulses.

This is a little tricky.
The Teensy measures the time from the previous MIDI Clock,
and generates 2 pulses that fit in that time.

For 161 BPM, we need to generate 2x 7.8ms periods, so edges every 3.9ms.

TEMPO OSC & SYNC DECODER

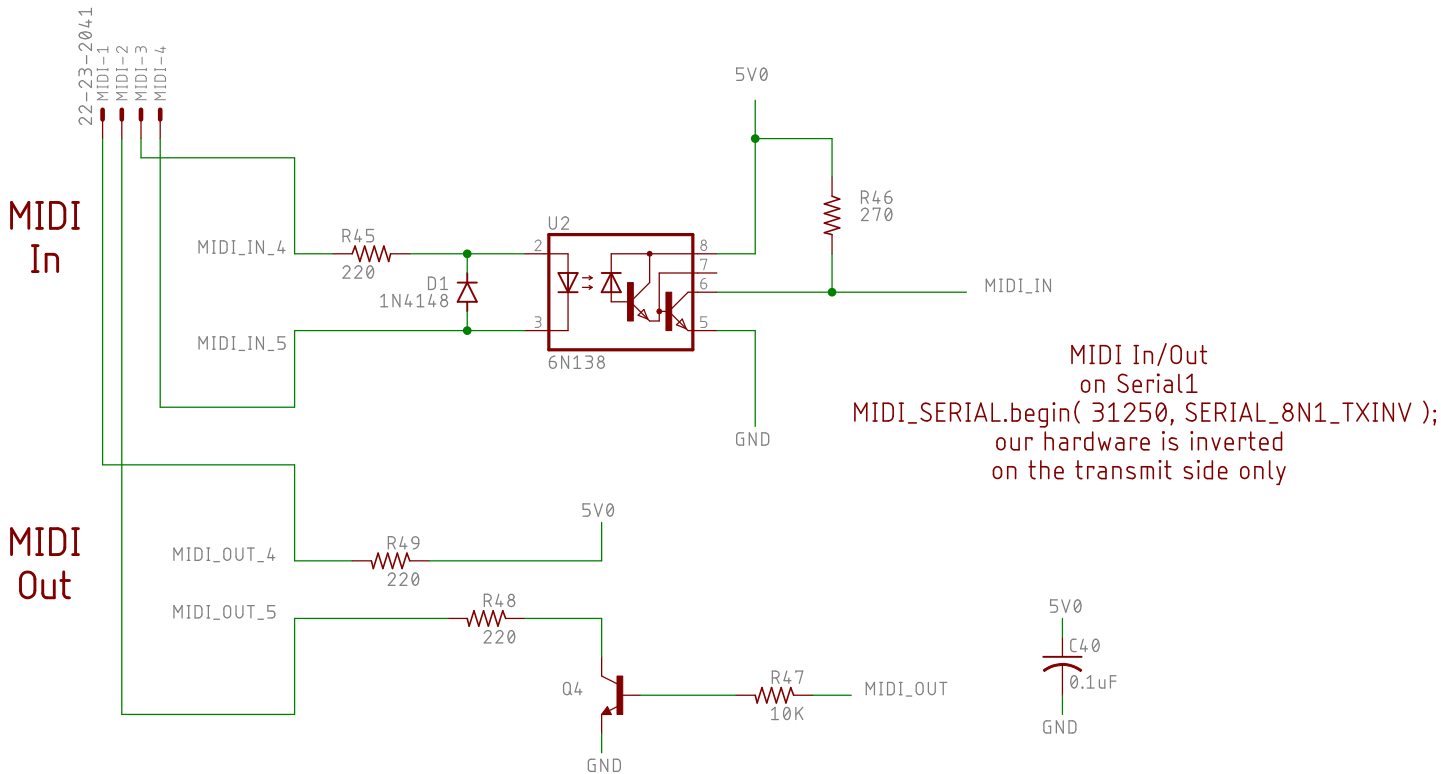
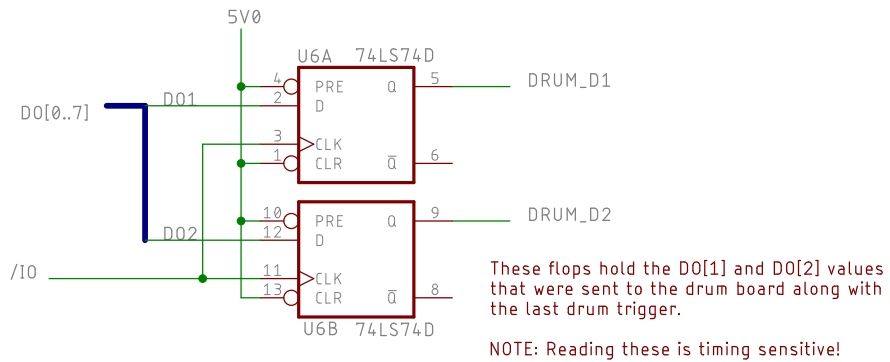
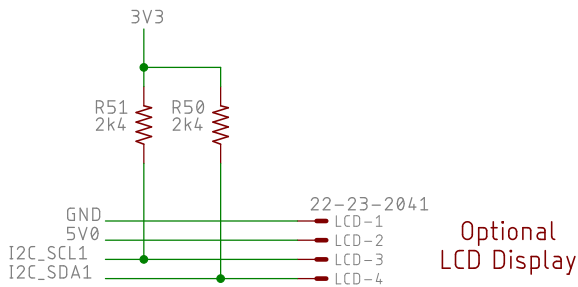
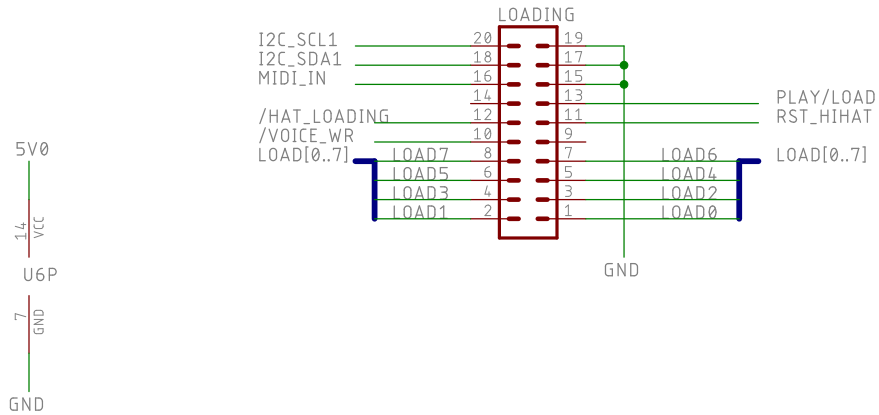
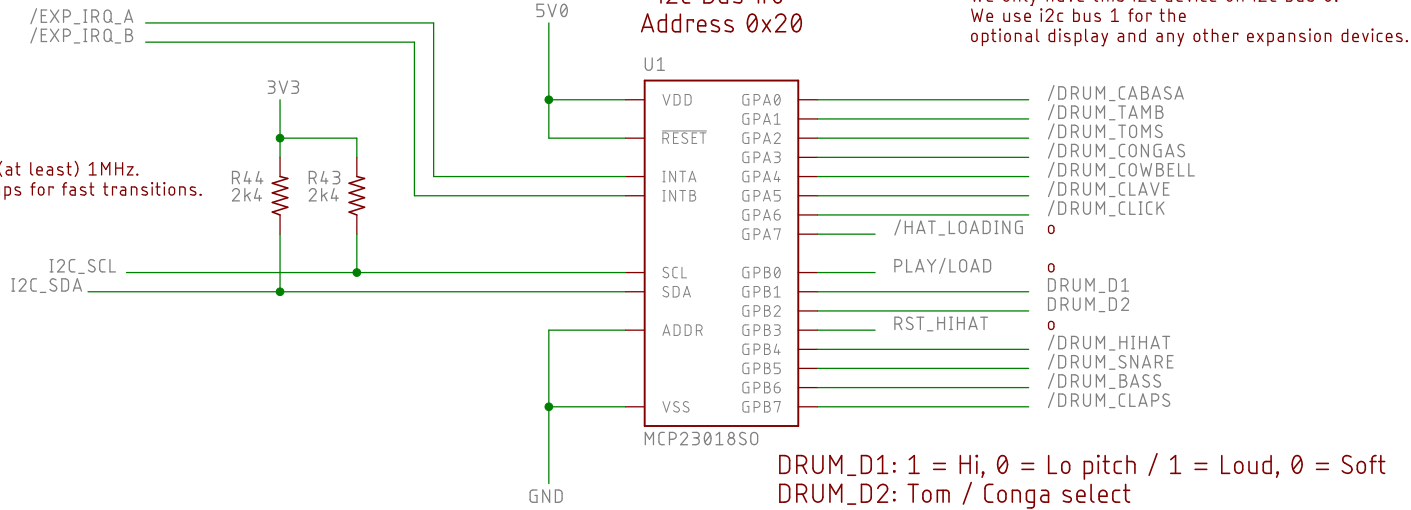
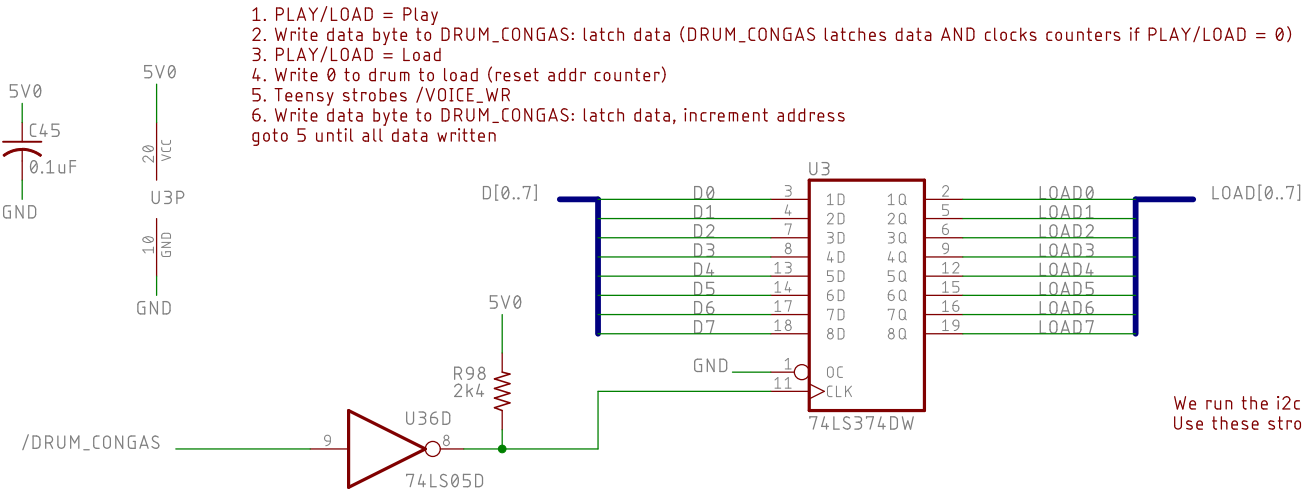
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MISCELLANEOUS

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Key Matrix		DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
ROW 1	DC01	7 07	6 06	5 05	4 04	3 03	2 02	1 01	0 00
ROW 2	DC02	ADJ SHUFL 0F	AUTO CORR 0E	LENGTH 0D	ERASE 0C	COPY 0B	REC 0A	9 09	8 08
ROW 3	DC04	PLAY STOP 17	DELETE 16	INSERT 15	LAST ENTRY 14	--> 13	<-- 12	CHAIN # 11	CHAIN ON/OFF 10
ROW 4	DC08	TOM ^ 1F	TOM V 1E	CONGA ^ 1D	CONGA V 1C	LOAD 1B	VERIFY 1A	SAVE 19	TEMPO 18
ROW 5	DC10	HIHAT / 27	COWBELL 26	HIHAT o 25	HIHAT o 24	BASS o 23	BASS o 22	SNARE o 21	SNARE o 20
ROW 6	DC20	x 2F	x 2E	CABASA o 2D	CABASA o 2C	TAMB o 2B	TAMB o 2A	CLAPS 29	CLAVE 28

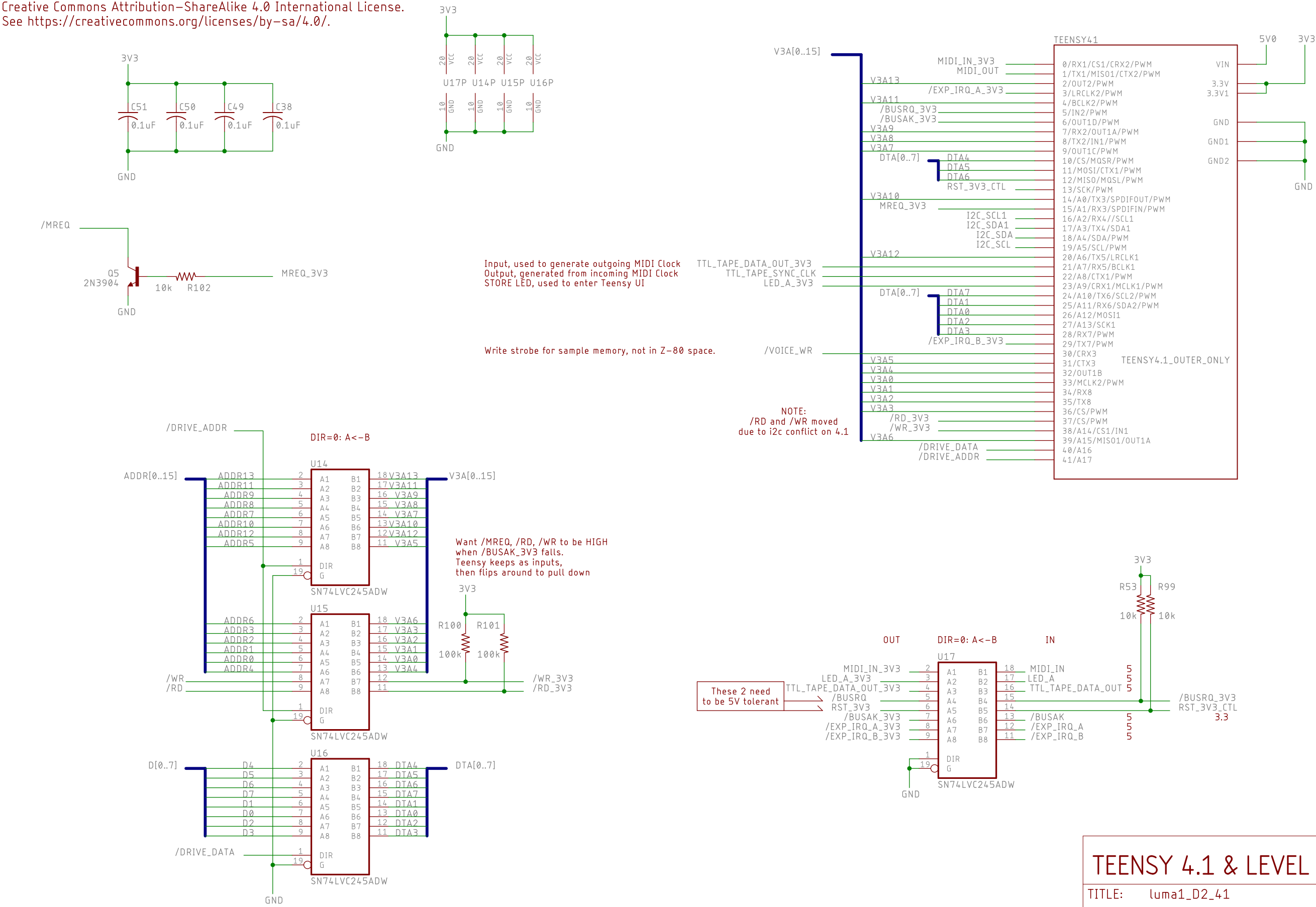
80 = no key

Jacks		DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
	D803	CLK OUT SEL SWITCH	CLK OUT SEL SWITCH	CLK OUT SEL SWITCH	CLK OUT SEL SWITCH	TAPE STORE FROM from XR2211?	REC /SAFE	REMOTE PLAY/STOP FOOT SW	TAPE SYNC FROM TEMPO CLOCK

KEYS & I/O MAPPINGS

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TEENSY 4.1 & LEVEL SHIFTERS

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