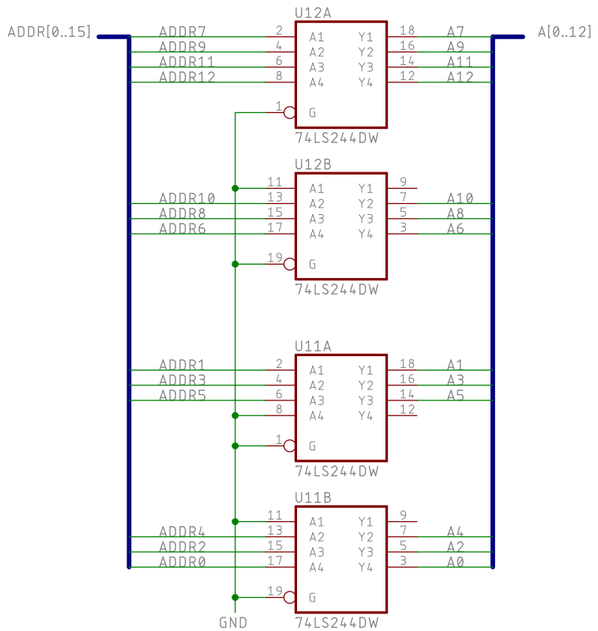
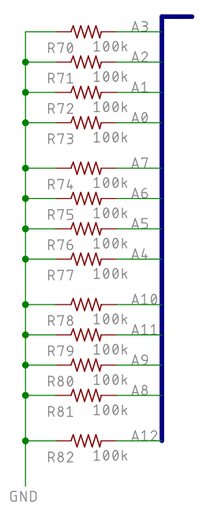
Address Buffers

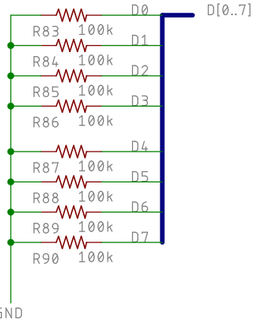
Always enabled
Only low 12 bits of address used



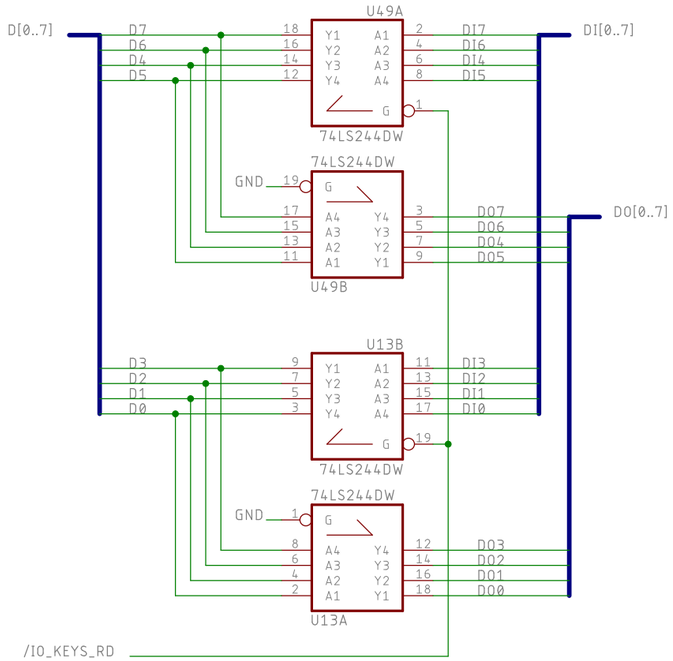
Address Bus Pulldowns

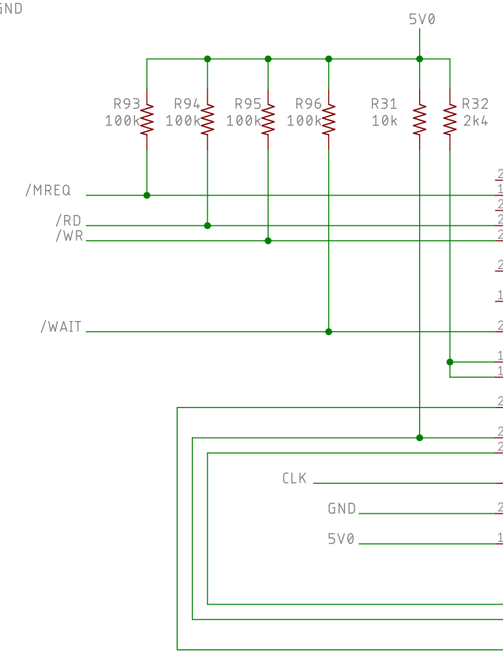


Data Bus Pulldowns



Data Buffers



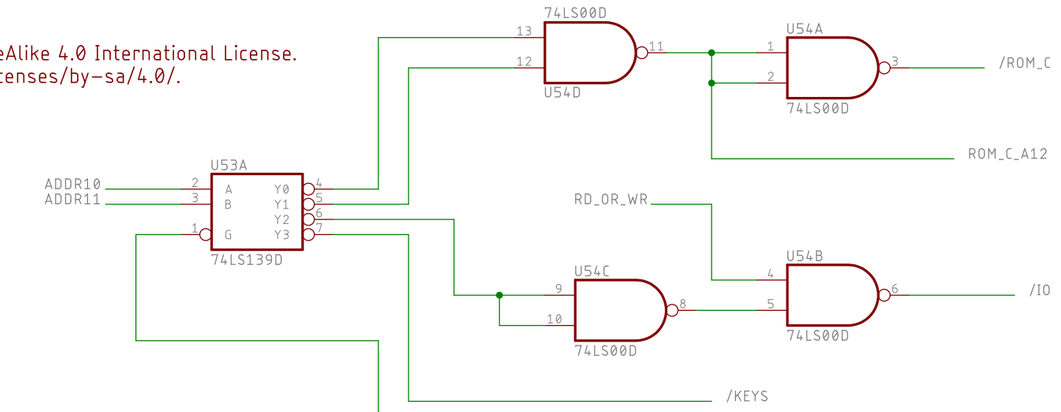


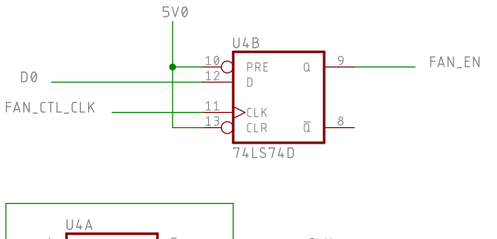
Teensy sits on Z-80 side of Address and Data.
Teensy 3.5 is 3.3V, but 5V-tolerant.
Memories are on the buffered Address bus,
but directly on the Z-80 Data bus.

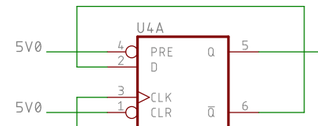
To/From Teensy
Teensy can DMA
to/from all addresses

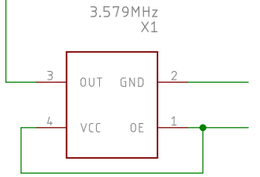
Teensy controls Z-80 reset

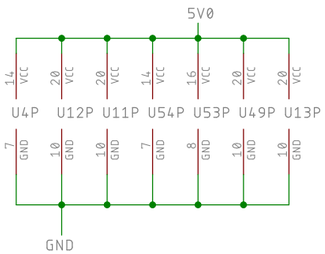
Outputs from Teensy only need to pull DOWN











						A	A	A	A	A	A	A	A	A	A
						1	1	1	1	1	1	0	0	0	0
						5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0
	8000	0000	ROM A (1)			x	x	0	0	0	0				
											1				
	8800	0800	ROM B (2)					0	0	1	0				
										1	1				
	9000	1000	ROM C (3)					0	1	0	0				
										0	1				
D800	9800	1800	I/O					0	1	1	0				
DC00	9C00	1C00	KEYS					0	1	1	1				
	A000	2000	RAM LO					1	0						
	B000	3000	RAM HI					1	1						

All I/O is memory mapped.
Z-80 IO Ports are unused.

Code does not use /INT or /NMI.
/RFRSH is not used.
/BUSREQ is not used.
/HALT is not used.

Z-80, BUFFERS, DECODE

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5V0

U41P U40P U36P U7P U10P U58P U39P U99P

GND

5V0

R35
2k4

U40

74LS138D

/DISPLAY_1

U7E

74LS04D

U7D

74LS04D

PATT_STB

LINK_STB

To 7-segment LED Latches

/DISPLAY_2

/DISC_LEDS_2

/EXT_JACKS_REG

/DRUM_BASS 0
/DRUM_SNARE 1
/DRUM_HIHAT 2
/DRUM_CLAPS 3

U41

74LS138D

A0
A1
A2
A3
/IO

/DRUM_CABASA 4
/DRUM_TAMB 5
/DRUM_TOMS 6
/DRUM_CONGAS 7
/DRUM_COWBELL 8
/DRUM_CLAVE 9
/DRUM_CLICK 10

GND

/DISC_LEDS

U58A

74LS00D

DISC_LEDS

DRUM WRITE (TRIGGER) SEQUENCE

1. Clear D802[7], enable D00–D02 -> drum board
2. Write 0 to selected drum (silence)
3. Write D00–D02 to selected drum (trigger)
4. Set D802[7], disable D00–D02 -> drum board

TRIGGERS

DRUM_BEEP
GND
DRM_D01
DRM_D00
DRM_D02
/DRUM_CLICK
/DRUM_COWBELL
/DRUM_TOMS
/DRUM_CABASA
/DRUM_SNARE
/DRUM_CLAPS
/DRUM_CLAVE
/DRUM_CONGAS
/DRUM_TAMB
/DRUM_BASS
/DRUM_HIHAT

8 drum generators

d0: 1 = trigger drum
d1: 1 = Hi, 0 = Lo pitch / 1 = Loud, 0 = Soft
d2: Tom / Conga select

/IO
/KEYS

U58D

74LS00D

U99A

74LS00D

/IO_KEYS_RD

If /KEYS or /IO low
AND /RD low
/IO_KEYS_RD goes low
Used to enable DI buffers.

/RD

U7B

74LS04D

/RAM_2000
/RAM_3000

U99B

74LS00D

U7C

74LS04D

/BIG_RAM

/ROM_A_B
/ROM_C

U99C

74LS00D

U99D

74LS00D

/BIG_ROM

U36A

74LS05D

LED_STORE 0, 0x01

U36F

74LS05D

LED_VERIFY 1, 0x02

U36B

74LS05D

LED_LOAD 2, 0x04

U36C

74LS05D

LED_PLAY_STOP 3, 0x08

D802

U10

74LS374DW

DO[0..7]
DO0
DO1
DO2
DO3
DO4
DO5
DO6
DO7

LED_A
LED_B
LED_C
LED_D

DRUM_BEEP
TTL_TAPE_DATA_OUT
DRUMS_DO_EN

U36E

74LS05D

GND

/DISC_LEDS_2

U7F

74LS04D

GND

15V0

1k R2

INTERNAL_CLK_OUT

Q1

10k R1

GND

NOTE:
Clock Out is +15V / 0V

TTL_INTERNAL_CLK_OUT

LED_B
TTL_TAPE_DATA_OUT

U58B

74LS00D

FAN_CTL_CLK

/WR
/RD

U58C

74LS00D

RD_OR_WR

/RD	/WR	RD_OR_WR
0	0	1
0	1	1
1	0	1
1	1	0

RST_3V3

U7A

74LS04D

/RESET

GND

DO[0..7]
DO0
DO1
DO2

U39

74LS365D

DRM_D00
DRM_D01
DRM_D02

MORE DECODE, TO DRUM BOARD

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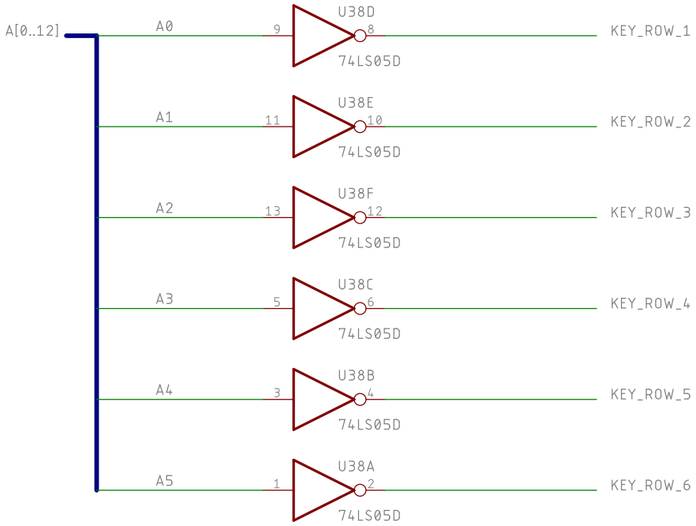
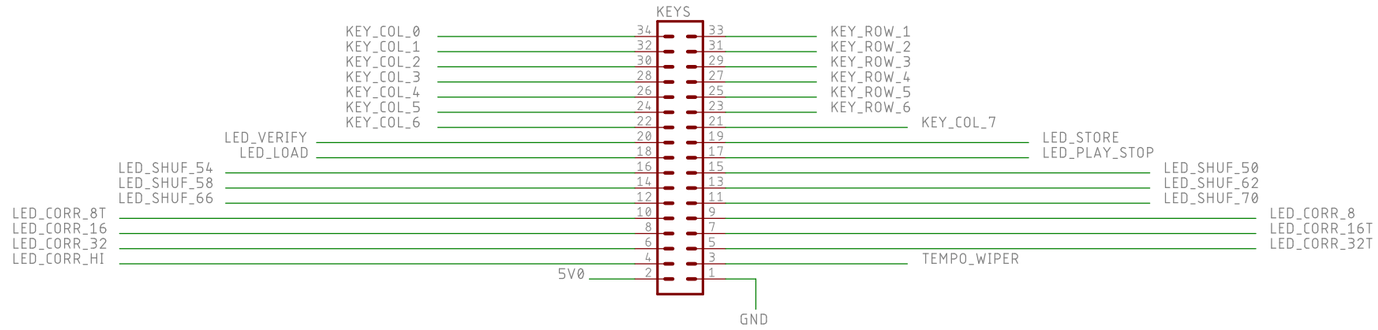
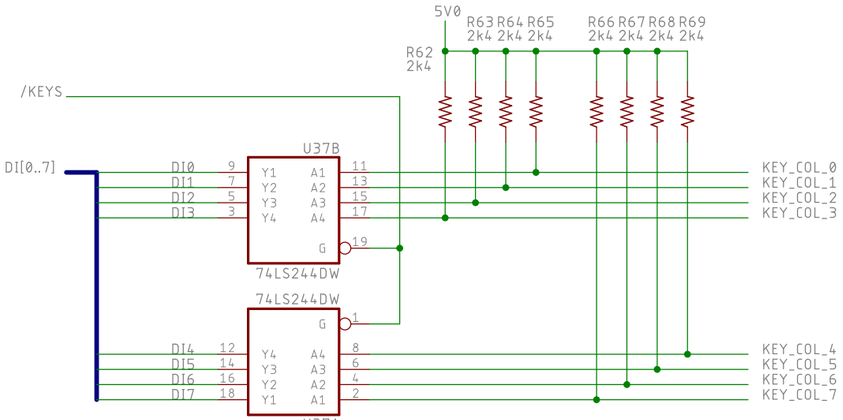
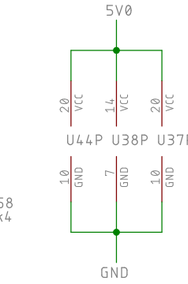
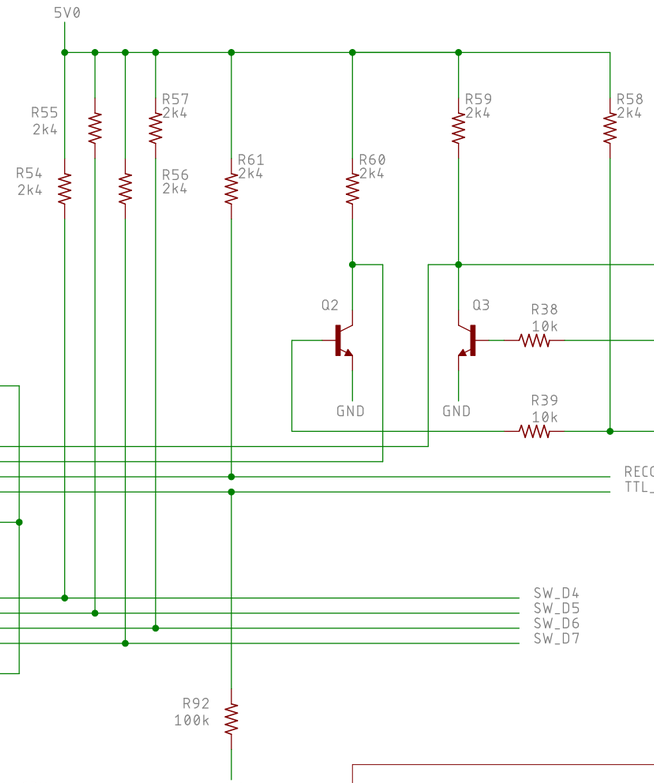


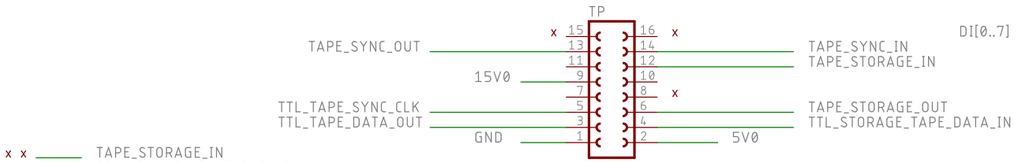




A single XR2206 is used to generate both
SYNC and STORAGE FSK data.
It's output goes to BOTH the SYNC OUT
and STORAGE OUT jacks.
That XR2206 is driven by TAPE_FSK_OUT.





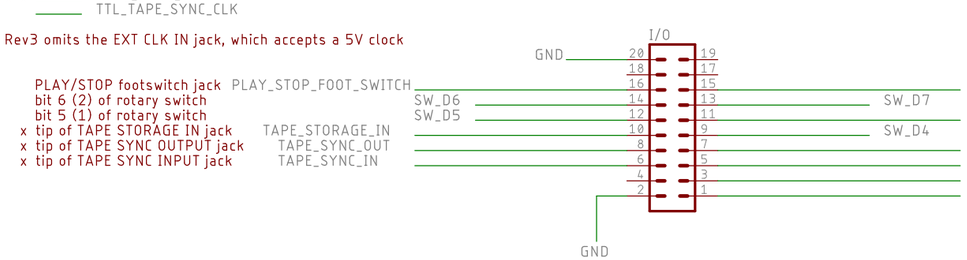


x x TAPE_STORAGE_IN
x TTL_STORAGE_TAPE_DATA_IN

x x TAPE_STORAGE_OUT
x x TAPE_SYNC_OUT
x TTL_TAPE_DATA_OUT

x x TAPE_SYNC_IN
TTL_TAPE_SYNC_CLK

Rev3 omits the EXT CLK IN jack, which accepts a 5V clock



selected tempo clock to CPU
bit 7 (3) of rotary switch
bit 4 (0) of rotary switch

tip of TAPE STORAGE OUT jack x
from XR2211 tone decoder (tape sync decoder) x
tip of INTERNAL CLOCK OUT jack
tempo clock from XR2206 on D (CPU) board

KEYS & I/O

See mappings on Page 9

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D80F

U50

74LS374DW

DISCRETE LEDS

U52

U51

74LS138D

D801

U8

TOP DISPLAY LINK

U32

U33

74LS47D

D800

U9

BOT DISPLAY PATTERN

U34

U35

LINK RIGHT DIG

LINK LEFT DIG

PATT RIGHT DIG

PATT LEFT DIG

U50P U51P U52P U8P U32G$2 U33G$2 U9P U34G$2 U35G$2

NOTE!
When mounting, rotate headers 180 degrees.
This is to match ribbon cables in original design.

DISPLAYS

Common Anode

DISPLAYS		
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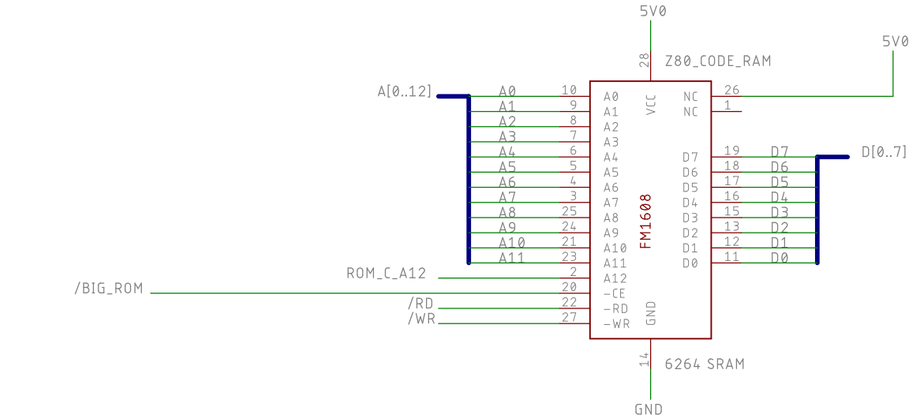
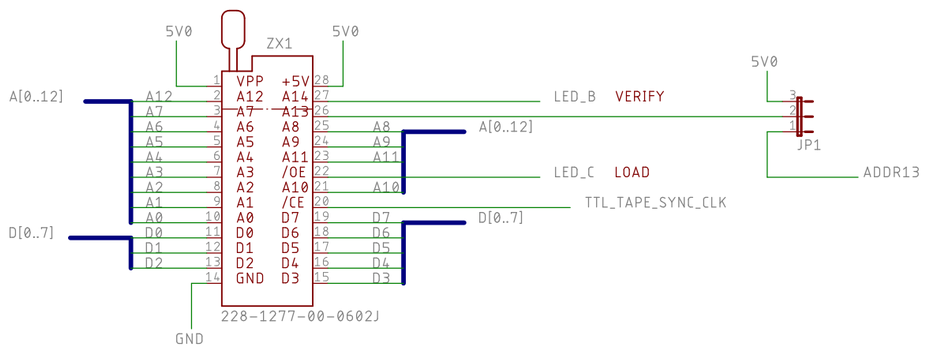
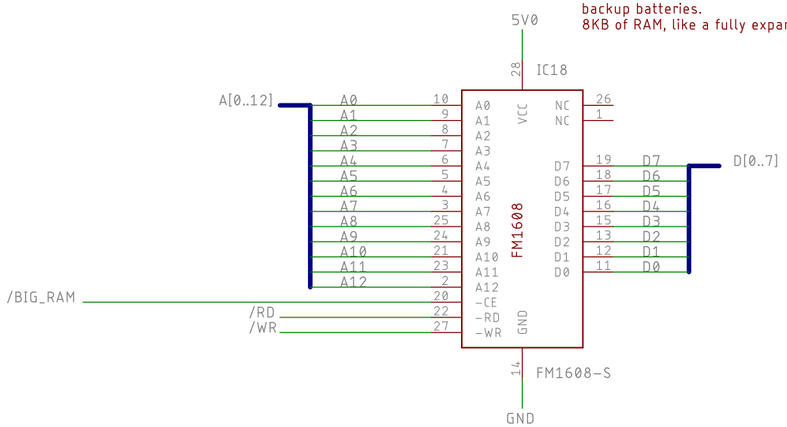
FRAM
EPROM
Replacement



Need (/ROM_1_2 == 0) || (/ROM_3 == 0) term



FM1608 FRAM eliminates need for
backup batteries.
8KB of RAM, like a fully expanded LM-1.



EPROM Reading is a total hack.

1. MENU -> EPROM DUMP, pause Z-80, Teensy takes bus
2. Prompt user for EPROM size
3. Tell user how to set power jumper
4. Data bus Z-80 -> Teensy
5. Addr bus Z-80 <- Teensy
6. Drive A13..A0 Z-80 Addr bus
7. Drive A14 = 0 on LED_B = 0

8. Drive /OE = 0, LED_C = 0
9. Ask user to insert EPROM, hit a key
10. Read EPROM: present Addr[0..13], delay 100uS to settle, read data bus, repeat for all bytes up to 16KB

12. If 27256, ask user to remove EPROM, flip A14 to 1 (LED_B = 1), repeat steps 8-11

13. Drive /OE = 1, LED_C = 1

14. Save buffer someplace on SD, and/or in voice RAM

MEMORY

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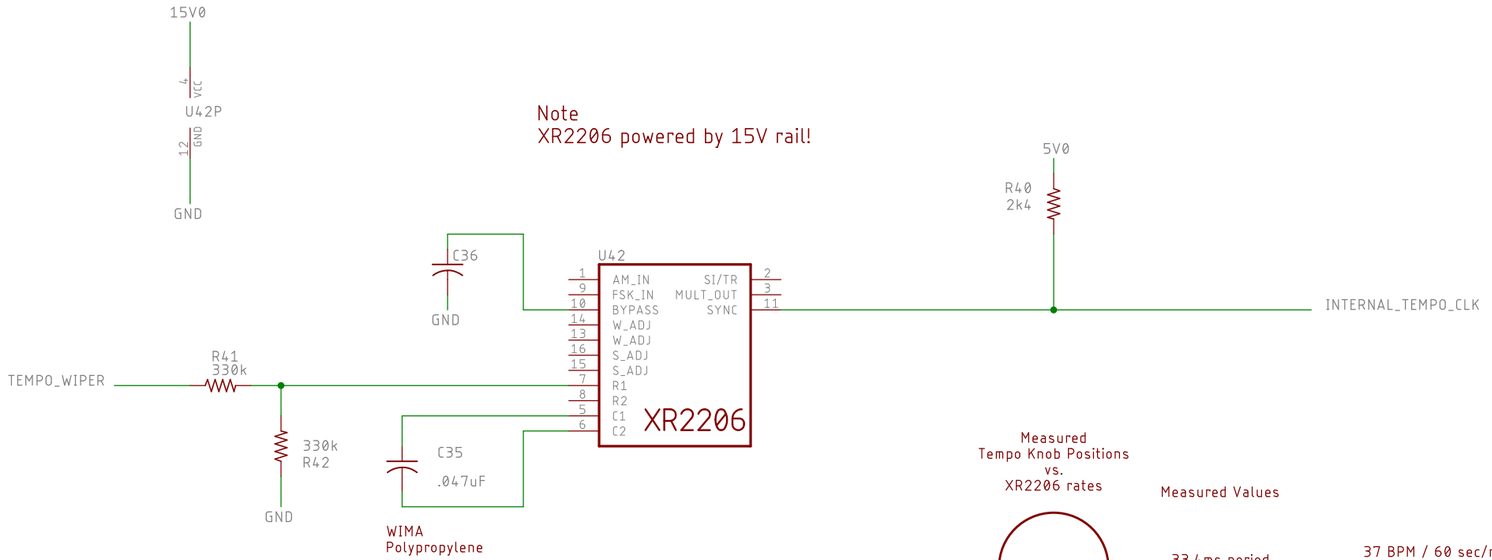
15V bypass cap?



Measured
Tempo Knob Positions
vs.
XR2206 rates

Measured Values

33.4ms period
37 BPM (LED readout)

Ideal Values
Internally 48 PPQN

37 BPM / 60 sec/min = 0.617 BPS (quarter notes per sec)
0.617 Qnotes/sec * 48 PPQ = 29.6 Pulses Per Sec
1/29.6 PPS = 33.8 ms

12.4ms period
100 BPM (LED readout)

100 BPM / 60 sec/min = 1.67 BPS (quarter notes per sec)
1.67 Qnotes/sec * 48 PPQ = 80 Pulses Per Sec
1/80 PPS = 12.5 ms

7.8ms period
161 BPM (LED readout)

161 BPM / 60 sec/min = 2.684 BPS (quarter notes per sec)
2.684 Qnotes/sec * 48 PPQ = 128.8 Pulses Per Sec
1/128.8 PPS = 7.8 ms

MIDI Clock is only 24 PPQ.
So, for each MIDI Clock received, the Teensy generates 2 clock pulses.

This is a little tricky.
The Teensy measures the time from the previous MIDI Clock,
and generates 2 pulses that fit in that time.

For 161 BPM, we need to generate 2x 7.8ms periods, so edges every 3.9ms.

TEMPO OSC & SYNC DECODER

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1. PLAY/LOAD = Play
2. Write data byte to DRUM_CONGAS: latch data (DRUM_CONGAS latches data AND clocks counters if PLAY/LOAD = 0)
3. PLAY/LOAD = Load
4. Write 0 to drum to load (reset addr counter)
5. Teensy strobes /VOICE_WR
6. Write data byte to DRUM_CONGAS: latch data, increment address
goto 5 until all data written

5V0
C45
0.1uF
GND

5V0
U3P
20 VCC
10 GND
GND

D[0..7]
D0 3
D1 4
D2 7
D3 8
D4 13
D5 14
D6 17
D7 18

U3
1D 1Q 2 LOAD0
2D 2Q 5 LOAD1
3D 3Q 6 LOAD2
4D 4Q 9 LOAD3
5D 5Q 12 LOAD4
6D 6Q 15 LOAD5
7D 7Q 16 LOAD6
8D 8Q 19 LOAD7
GND 1 OC
11 CLK
74LS374DW

LOAD[0..7]

5V0
R98
2k4

/DRUM_CONGAS 9
U36D
8
74LS05D

Take interrupt on any drum strobe falling.
This will latch the port values at the edge that
triggered the interrupt.
Each port must be handled independently,
hence the separate interrupts.
This is a very timing sensitive operation.
We only have this i2c device on i2c bus 0.
We use i2c bus 1 for the
optional display and any other expansion devices.

i2c Bus #0
Address 0x20

/EXP_IRQ_A
/EXP_IRQ_B

5V0
3V3
R44 2k4
R43 2k4

We run the i2c bus at (at least) 1MHz.
Use these strong pullups for fast transitions.

I2C_SCL
I2C_SDA

U1
VDD GPA0 /DRUM_CABASA
GPA1 /DRUM_TAMB
RESET GPA2 /DRUM_TOMS
GPA3 /DRUM_CONGAS
INTA GPA4 /DRUM_COWBELL
INTB GPA5 /DRUM_CLAVE
GPA6 /DRUM_CLICK
GPA7 /HAT_LOADING o
SCL GPB0 PLAY/LOAD o
SDA GPB1 DRUM_D1
GPB2 DRUM_D2
ADDR GPB3 RST_HIHAT o
GPB4 /DRUM_HIHAT
GPB5 /DRUM_SNARE
GPB6 /DRUM_BASS
VSS GPB7 /DRUM_CLAPS
MCP23018SO

GND

DRUM_D1: 1 = Hi, 0 = Lo pitch / 1 = Loud, 0 = Soft
DRUM_D2: Tom / Conga select

LOADING
I2C_SCL1 20 19
I2C_SDA1 18 17
MIDI_IN 16 15
14 13 PLAY/LOAD
/HAT_LOADING 12 11 RST_HIHAT
/VOICE_WR 10 9
LOAD[0..7] LOAD7 8 7 LOAD6 LOAD[0..7]
LOAD5 6 5 LOAD4
LOAD3 4 3 LOAD2
LOAD1 2 1 LOAD0
GND

5V0
U6P
14 VCC
7 GND
GND

3V3
R51 2k4
R50 2k4
GND
5V0
I2C_SCL1
I2C_SDA1
22-23-2041
LCD-1
LCD-2
LCD-3
LCD-4

Optional
LCD Display

5V0
U6A 74LS74D
DO[0..7]
DO1 4 PRE Q 5 DRUM_D1
2 D
3 CLK
1 CLR Q 6
DO2 10 PRE Q 9 DRUM_D2
12 D
11 CLK
/IO 13 CLR Q 8
U6B 74LS74D

These flops hold the DO[1] and DO[2] values
that were sent to the drum board along with
the last drum trigger.

NOTE: Reading these is timing sensitive!

22-23-2041
MIDI-1
MIDI-2
MIDI-3
MIDI-4

MIDI
In

5V0
MIDI_IN_4
R45
220
D1
1N4148
MIDI_IN_5
U2
6N138
R46
270
MIDI_IN
GND

MIDI In/Out
on Serial1
MIDI_SERIAL.begin(31250, SERIAL_8N1_TXINV);
our hardware is inverted
on the transmit side only

MIDI
Out

5V0
MIDI_OUT_4
R49
220
MIDI_OUT_5
R48
220
Q4
R47
10K
MIDI_OUT
GND

5V0
C40
0.1uF
GND

MISCELLANEOUS

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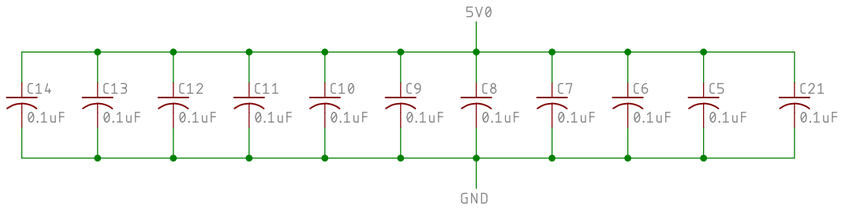
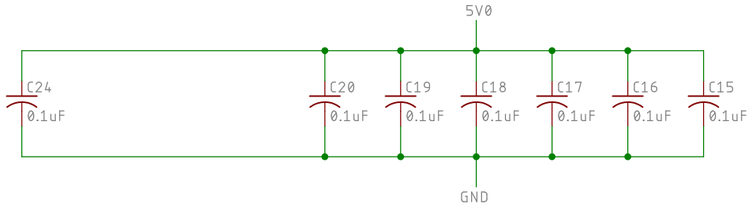
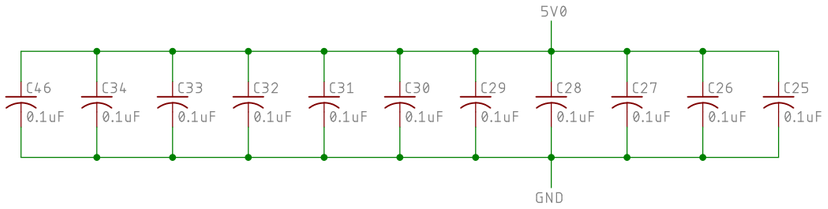
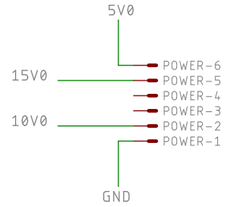


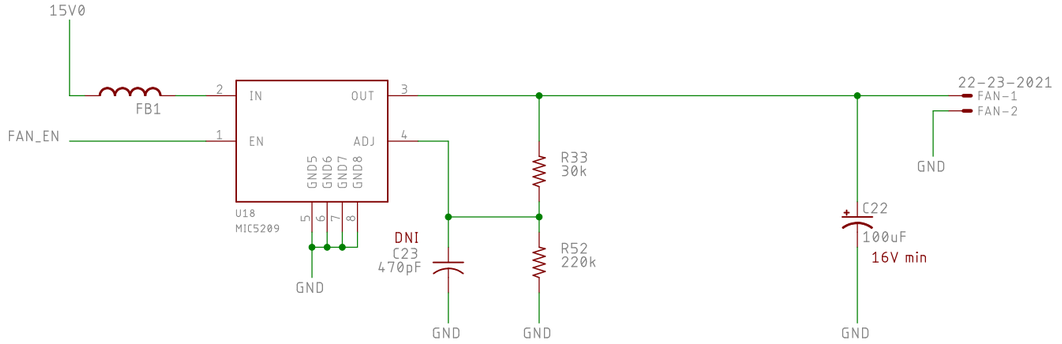




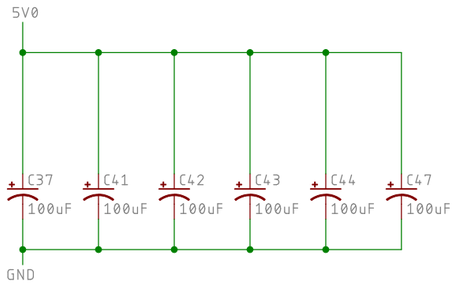
CPU board takes in +10V,
regulates that down to +5V,
uses it locally and passes it
down to the drum board.

+15V used for XR part(s).

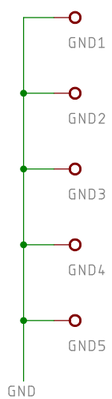




Vout = 1.242V * (1 + R52/R33)
Vout = 1.242V * (1 + (220000 / 30000))
Vout = 1.242V * 8.333 = 10.35V



Keystone 5006 (BLACK)
Loop Test Points



Keystone 5005 (RED)
Loop Test Point

BYPASS & DECOUPLING

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Key Matrix

		DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
ROW 1	DC01	7 07	6 06	5 05	4 04	3 03	2 02	1 01	0 00
ROW 2	DC02	ADJ SHUFL ○ 0F	AUTO CORR ○ 0E	LENGTH ○ 0D	ERASE ○ 0C	COPY 0B	REC 0A	9 09	8 08
ROW 3	DC04	PLAY STOP ○ 17	DELETE ○ 16	INSERT 15	LAST ENTRY ○ 14	-->> ○ 13	<<-- ○ 12	CHAIN # 11	CHAIN ON/OFF 10
ROW 4	DC08	TOM ^ ○ 1F	TOM V ○ 1E	CONGA ^ ○ 1D	CONGA V ○ 1C	LOAD ○ 1B	VERIFY ○ 1A	SAVE ○ 19	TEMPO 18
ROW 5	DC10	HIHAT / ○ 27	COWBELL ○ 26	HIHAT o ○ 25	HIHAT O ○ 24	BASS o ○ 23	BASS O ○ 22	SNARE o ○ 21	SNARE O ○ 20
ROW 6	DC20	x 2F	x 2E	CABASA o ○ 2D	CABASA O ○ 2C	TAMB o ○ 2B	TAMB O ○ 2A	CLAPS ○ 29	CLAVE ○ 28

80 = no key

Jacks

		DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
	D803	CLK OUT SEL SWITCH	CLK OUT SEL SWITCH	CLK OUT SEL SWITCH	CLK OUT SEL SWITCH	TAPE STORE FROM from XR2211?	REC /SAFE	REMOTE PLAY/STOP FOOT SW	TAPE SYNC FROM ↑ TEMPO CLOCK

KEYS & I/O MAPPINGS

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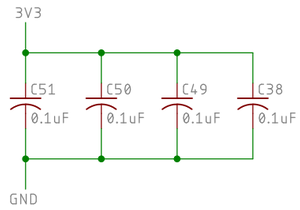
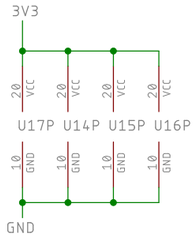
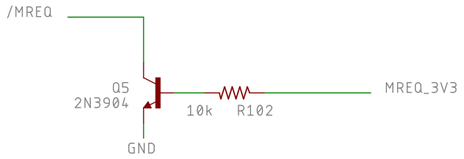
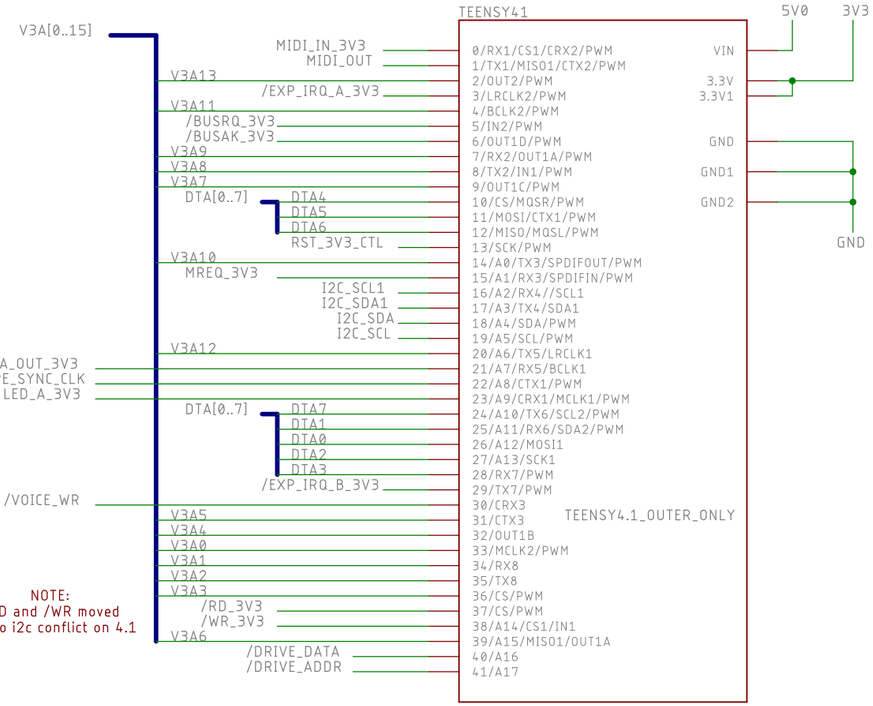




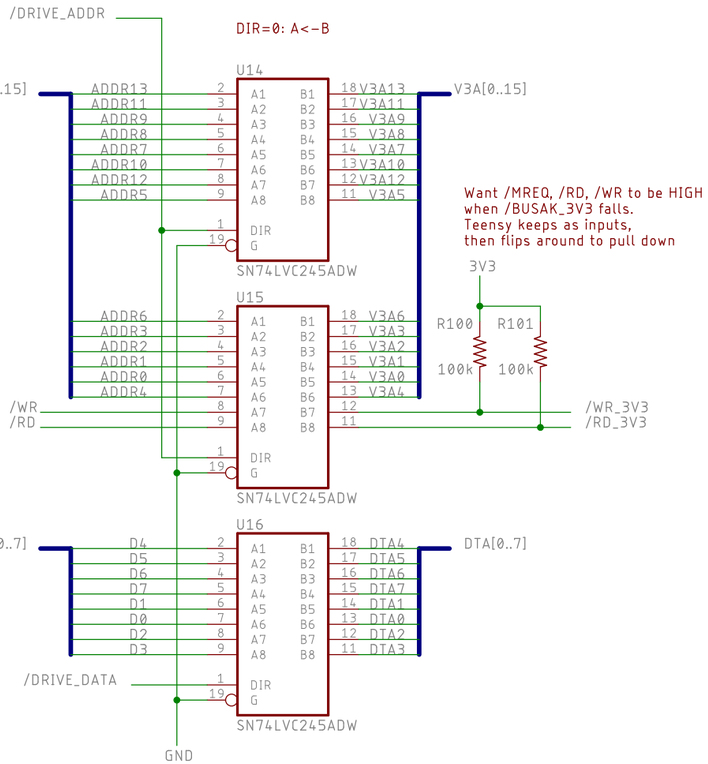


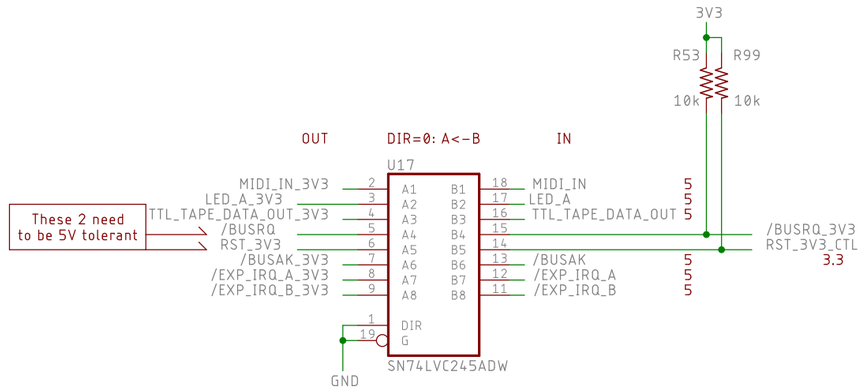


Input, used to generate outgoing MIDI Clock
Output, generated from incoming MIDI Clock
STORE LED, used to enter Teensy UI

Write strobe for sample memory, not in Z-80 space.

NOTE:
/RD and /WR moved
due to i2c conflict on 4.1





TEENSY 4.1 & LEVEL SHIFTERS

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