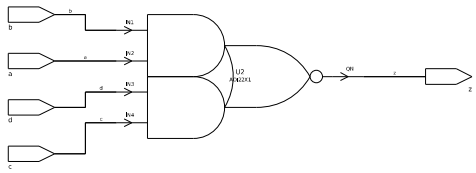
Combo Logic - `if` Statement

- SystemVerilog provides `always_comb` to model combinatorial logic
- A sensitivity list is inferred (any RHS expressions)
- Also sensitive to changes within the contents of functions used
- LHS variables cannot be written from any other processes
- Warnings occur if non-combo logic is detected (latch inference)
- Use blocking assignment inside `always_comb`

```
module simple_combo(
  input        a, b, c, d,
  output reg   z);
  //make a AOI22 gate
  always_comb
    z = ~((a & b) | (c & d));
endmodule
```

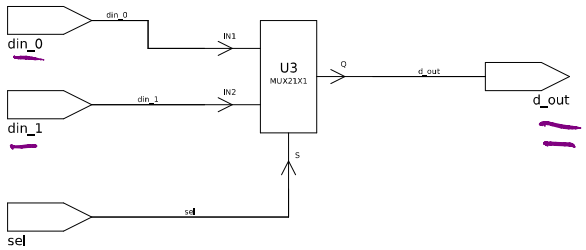


Combo Logic - `if` Statement

Slightly More Interesting Combo Logic

```
module mux2_1 (
   input      sel,
   input      din_0, din_1,
   output reg d_out
   );

  always_comb
    if (sel)
      d_out = din_1;
    else
      d_out = din_0;
endmodule
```

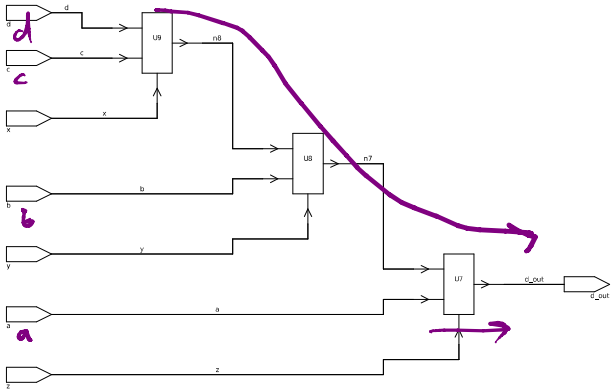


Combo Logic - `if` Statement

Nested IF statements can produce slow logic
Can you see the implied priority?

```
module serial_mux (
   input      a,b,c,d,x,y,z,
   output reg d_out
   );

  always_comb
    if (z)
      d_out = a;
    else if (y)
      d_out = b;
    else if (x)
      d_out = c;
    else
      d_out = d;
endmodule
```

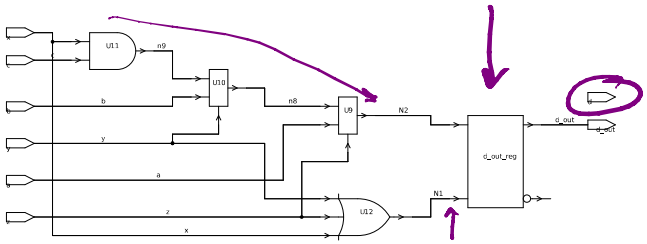


Combo Logic - `if` Statement

IF with no concluding else produces what...

```
module mux_broken (
   input      a,b,c,d,x,y,z,
   output reg d_out
   );

  always_comb
    if (z)
      d_out = a;
    else if (y)
      d_out = b;
    else if (x)
      d_out = c;
//    else
//      d_out = d;
endmodule
```



Combo Logic - `if` Statement

IF without concluding else... did it compile correctly?

```
Model Technology ModelSim SE vlog 6.6a Compiler 2010.03 Mar 19 2010
-- Compiling module serial_mux_broken
Top level modules:
        serial_mux_broken
slana.eecs.oregonstate.edu:
```

What about synthesis?

```
Inferred memory devices in process
in routine serial_mux_broken line 6 in file 'serial_mux_broken.sv'.
=========================================================================
|    Register Name    | Type  | Width | Bus | MB | AR | AS | SR | SS | ST |
=========================================================================
|      d_out_reg      | Latch |   1   |  N  | N  | N  | N  | -  | -  | -  |
=========================================================================
Warning:  serial_mux_broken.sv:6: Netlist for always_comb block contains a latch.
Presto compilation completed successfully.
Information: There are 1 potential problems in your design.
Please run 'check_design' for more information. (LINT-99)
```