Power Saving Techniques in Digital Systems

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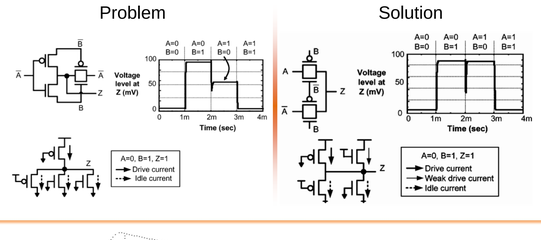
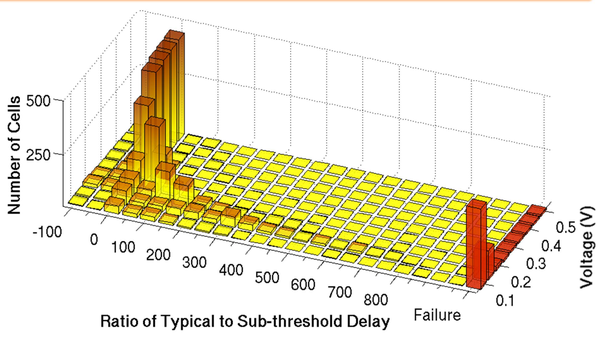
Guaranteed Operation of Any Standard Cell Library in Sub-threshold

Problems With Current Cell Libraries

- Transistor stacking degrades output voltage level often beyond readable level.
- Sequential Logic cells with ratioed feedback fail to change state all together.

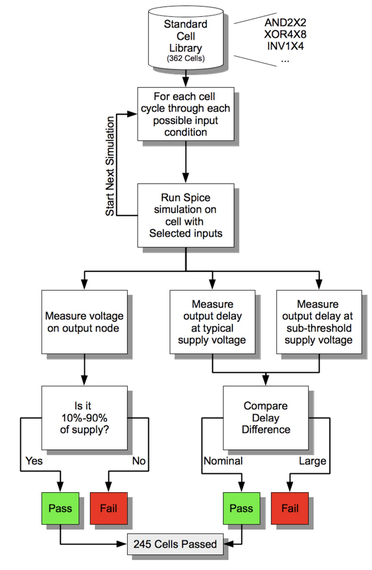




Delay skew due to voltage decrease in cells

Our Method

1.Generate input pairs for each cell and run spice simulation at sub-threshold voltage.
2.Verify expected voltage at each output to by within 1% of supply
3.Compare in-out delay with delay when run at typical voltage

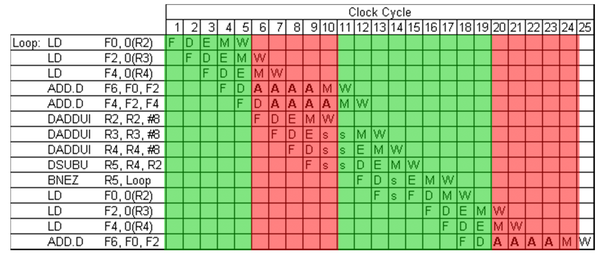


An Architecture Extension to Approach Optimal Power Gating

Power Gating

- $P = \frac{1}{2} C*V^2*f$
- Power saved by turning off unused portions of system.
- Usually done with large PMOS between supply and cell

Motivation for Look-Ahead Power Gating

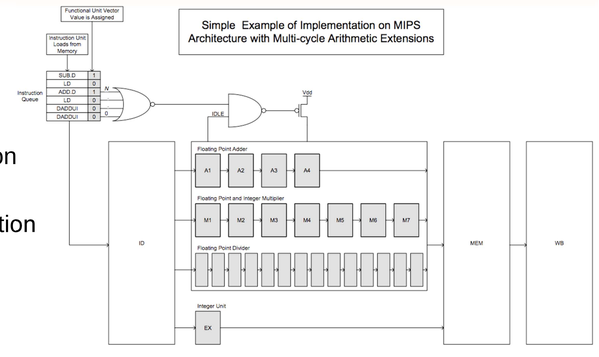


= Cycles to potentially save power

The Technique

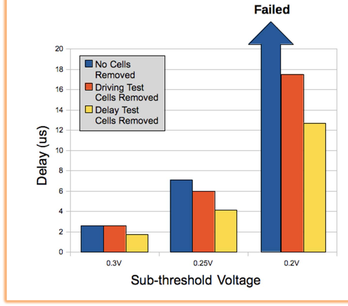
Call $N = MAX[(t_{startup} + t_{shutdown}), t_{breakeven}]$
N represents the number of cycles required to:
* shutdown and then startup a functional unit
* overcome the power overhead of turning off/on

1. Always check next N instructions from instruction queue for FPU use
2. If any do, startup FPU; Otherwise, shut it down

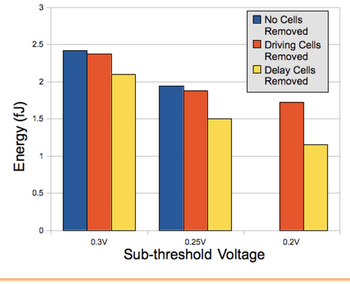


Results

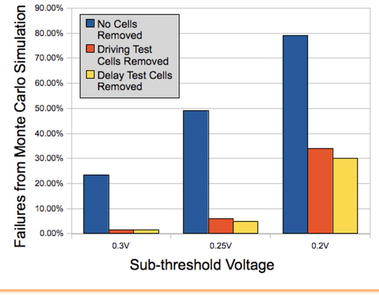
Delay



Power

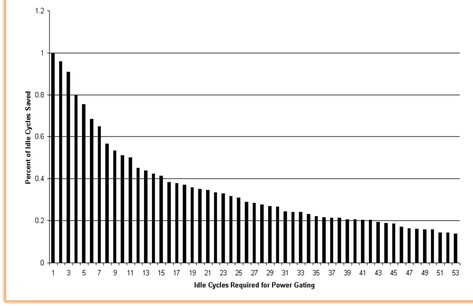


Monte Carlo Failures



Power Savings Simulation Results (SimpleScalar simulator)

Persistence of Vision Floating Point Addition Operations



XAnim Floating Point Multiplication Operations