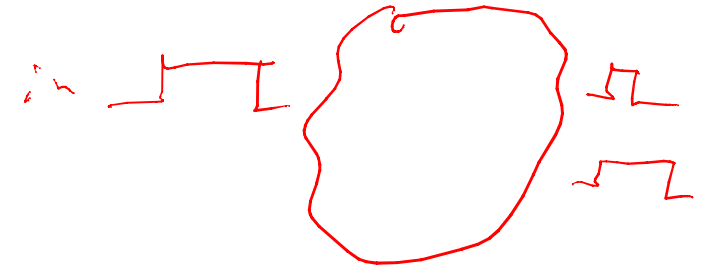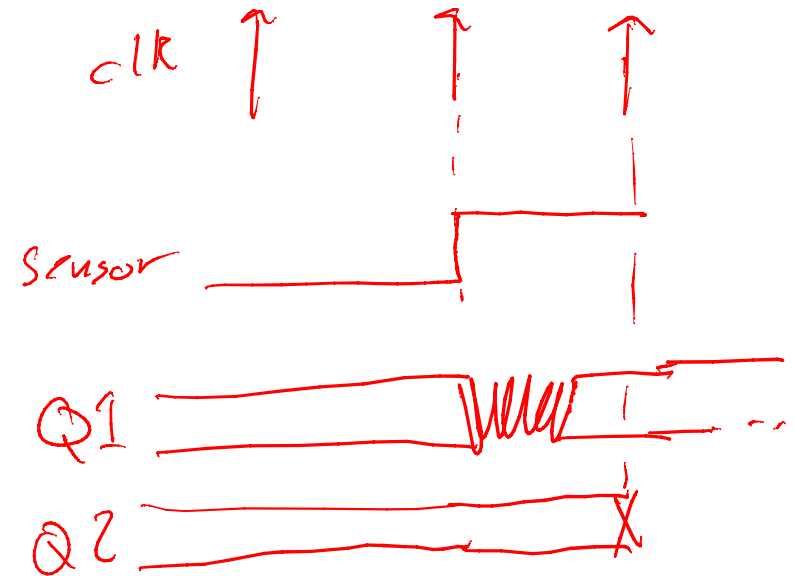# Counter_sm

- Synchronize in with clk

Proper Debug Technique

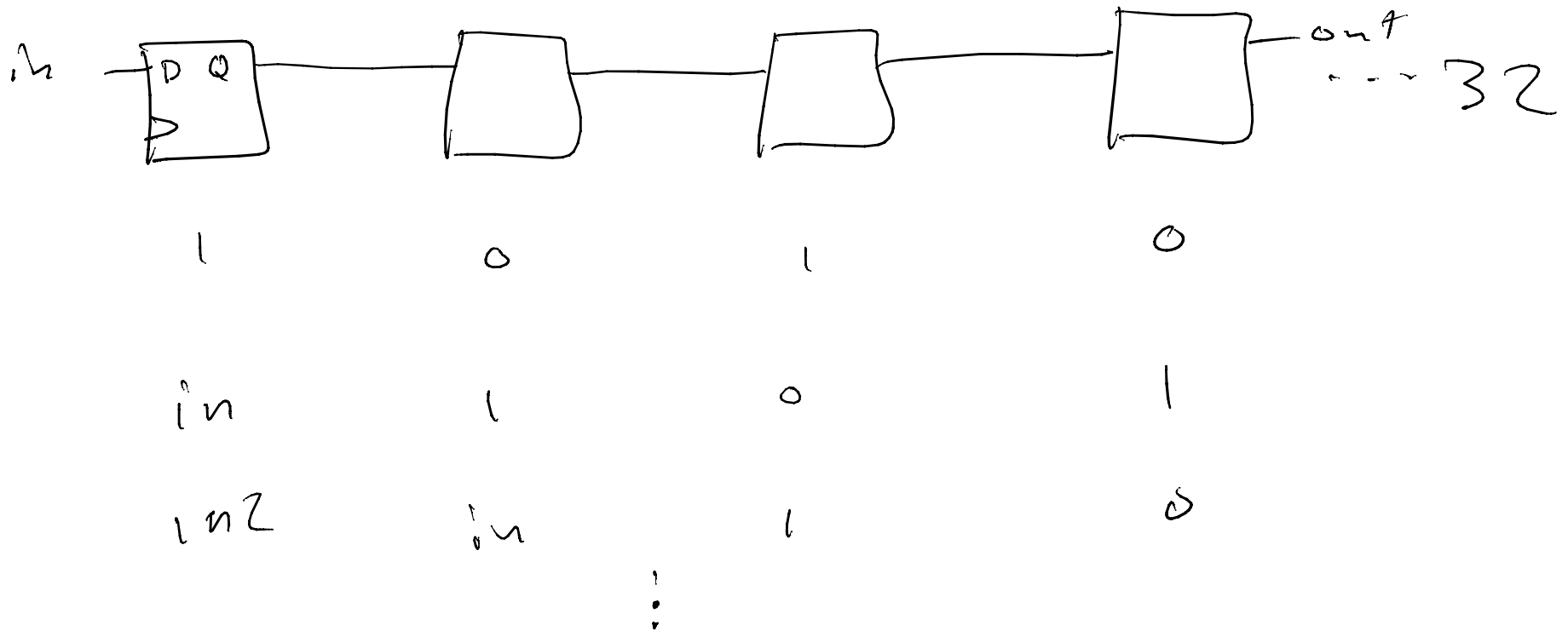DONE

clk

Sensor

Q1

Q2
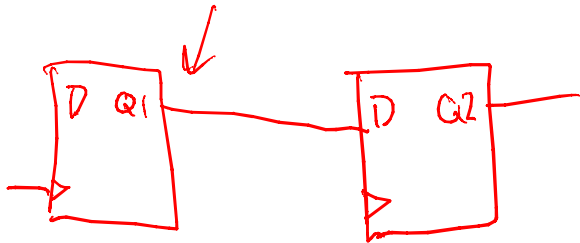
divider_even

$N = 4$

Shift Register

in [31:0]
load
shift
reset_n
> clk

out

LED

in → | D Q | — | | — | | — | | → out
         |>   --- 32

    1   0   1   0

   in   1   0   1

   in2   in   1   0

                     :

Buffer

LED

load

in[0]

load

in[1]

clk

load

shift

not
quite

Q

Fifo

wr

restart_mem

reset_n

clk_mem

rd —

clk <

async. reset_u
sync restart

write_ptr

data_in

BYTE1

8

BYTE2

read_ptr

read_ptr
write_ptr

empty_raw

Q D
clk

empty

wr
reset
clk_mem

D

+

rd
reset
clk

D

+
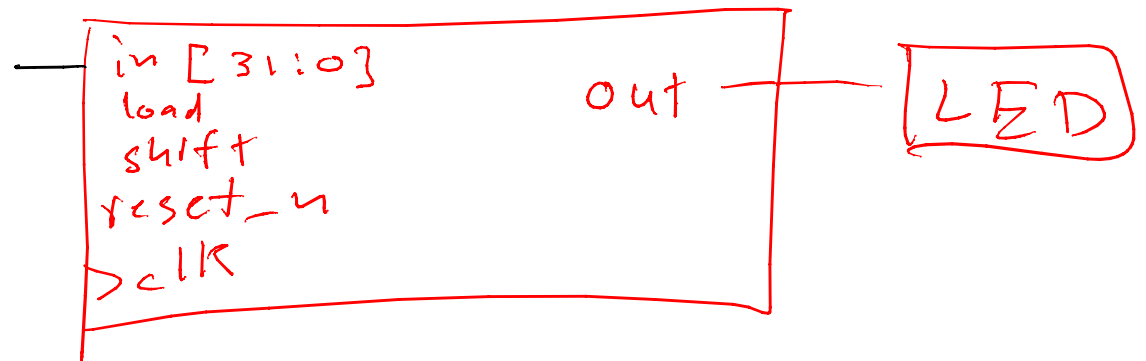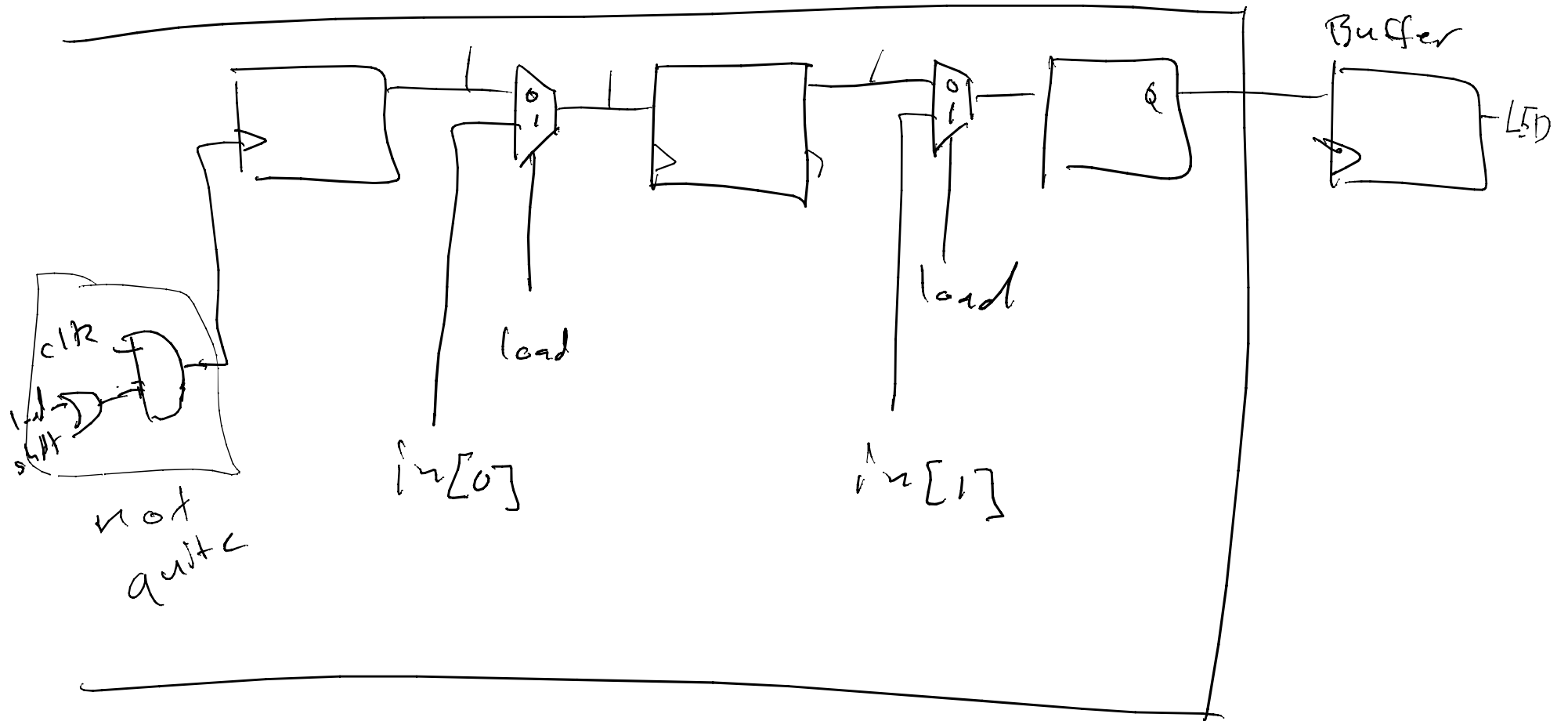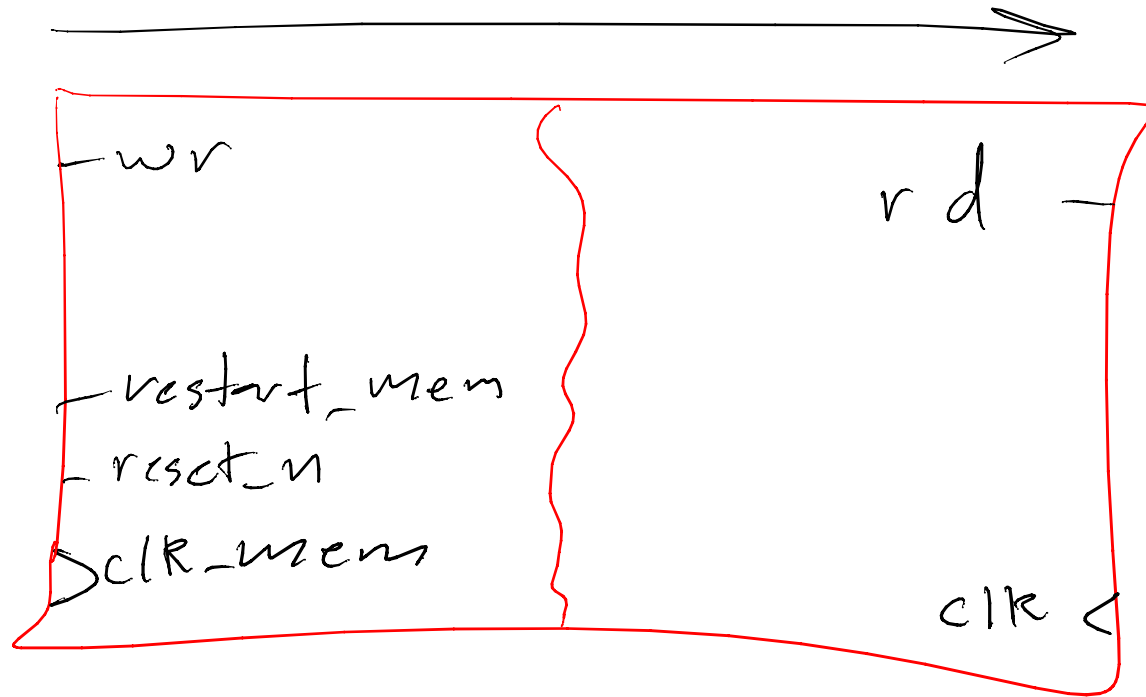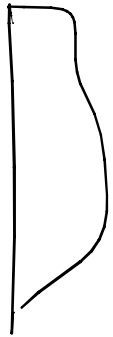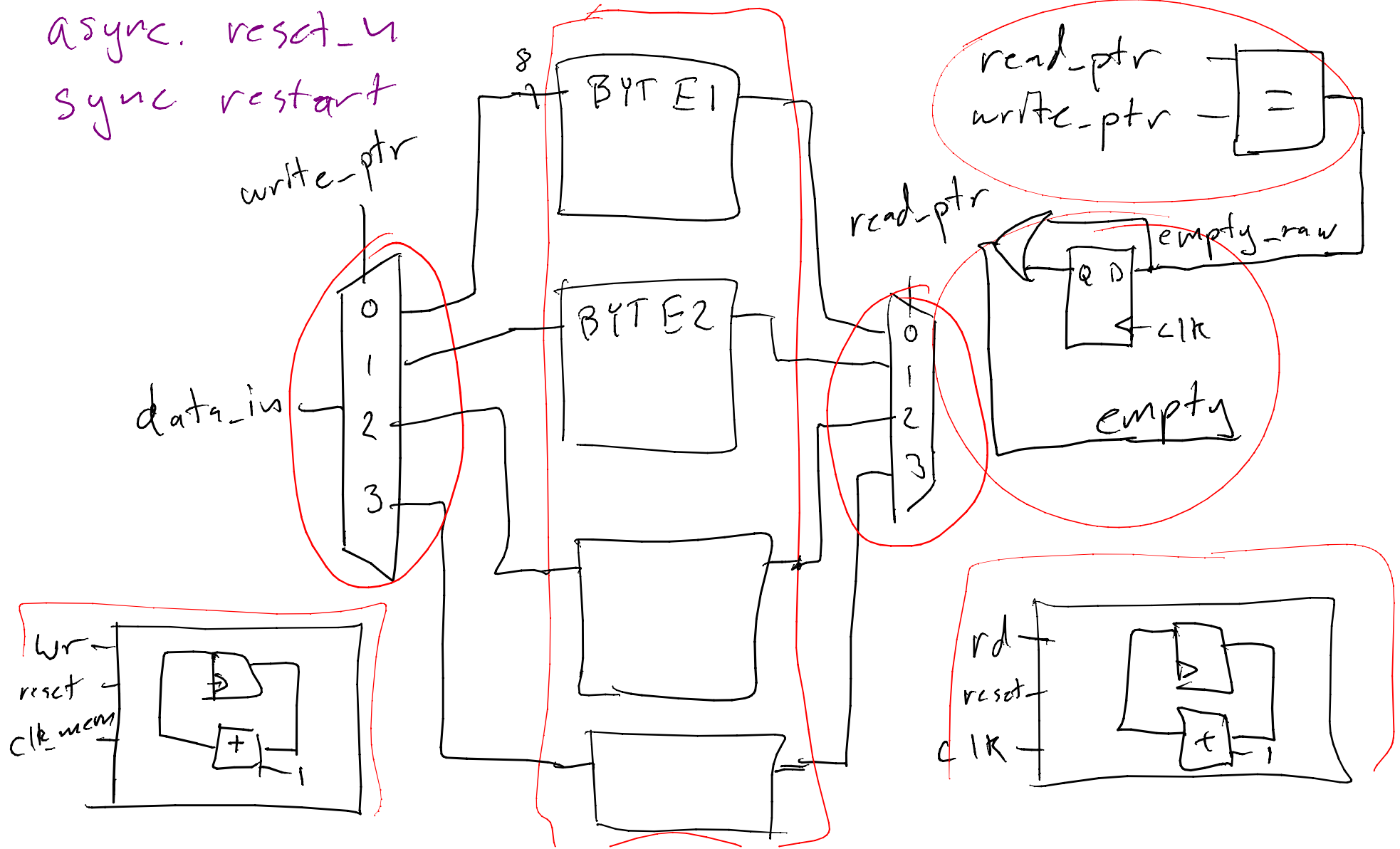
Mem-to-FIFO State Machine

ROM_data[7:0]

ROM_re
ROM_ce
[3:0] ROM_addr

- - - - - - - - - -

restart

fifo_wr

reset_n   [7:0] data_mem_to_fifo

clk_mem

clk_mem

reset/restart

ROM_ce

ROM_re

fifo_wr

ROM_addr   0 X 1 X 2 X 3