Oregon State University College of Engineering

Methods to Improve Reliability in Sub/Near-Threshold Circuits

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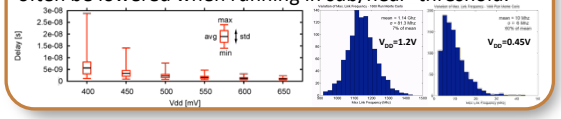
The Problem

Sub/near-threshold operation has been used to realize 10X power improvements over super-threshold circuits. However, as VDD is lowered, timing variations are exacerbated and circuit performance becomes unpredictable beyond tolerance.

Unpredictable Logic

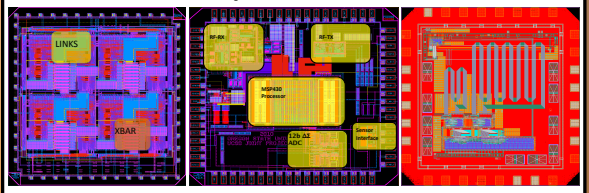
As VDD is lowered, delay variations are exacerbated. Current methods like Razor circuits are not robust enough to detect errors generated by large variations (greater than 1.5X). The maximum operating frequency must often be lowered when running in sub/near- threshold.



Design Automation

Design and integration of reliable custom sub/near-threshold circuits into a traditional digital design flow is challenging and time intensive. Automating the design, optimization and integration process will allow reliable, energy efficient, low-voltage logic and communication circuits to be implemented with the ease and design time advantages of a traditional digital design flow.

Previous/Current Work



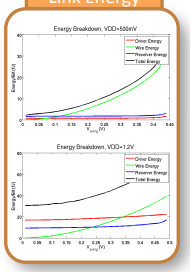
90nm, 1.2V 4-node network-on-chip with low-swing links/crossbar (May 2009)

90nm, 0.5V single-chip, wireless EKG/EEG sensor SoC with near-threshold digital processing (May 2010)

65nm, 0.45V adjustable voltage swing links with 2-bit RX cal, 10-bit RX cal and 3 tap DFE (May 2010)

Energy Efficient Sub/Near-Threshold Links

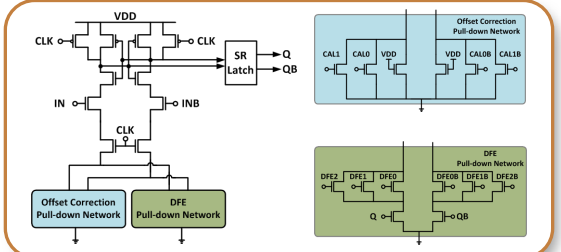
Link Energy



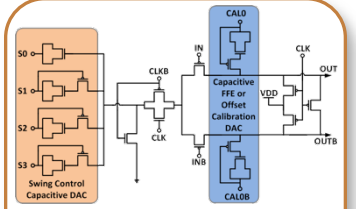
0.4V, 16bit MADD operation: 200fJ
Moving 16bits 300um: 250fJ
Communication is still expensive in sub/near-threshold!

	Conventional Full Swing	Schinkle (JSSCC '09)	Stojanovic (ISSCC '09)	Our TFC Router	New Goal
Wire Length	1mm	2mm	10mm	1mm	1-5mm
Supply	1.2V	1.2V	-	1.2V	0.5V
Transceiver Area	21um^2	TX:~20um	2880um^2	23um^2	20-30um^2
Signal Swing	1.2V	120mV	200mV	250mV	50mV
Energy/Bit	305fJ	105fJ	356fJ	28fJ	1-5fJ/mm

RX Offset Correction & DFE



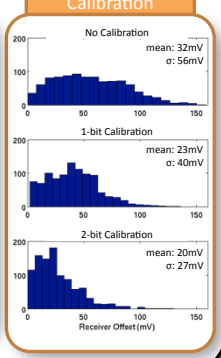
TX Calibration



TX voltage swing is set by a charge sharing capacitor DAC during calibration to match the RX offset, allowing robust operation at the lowest allowable swing for each receiver.

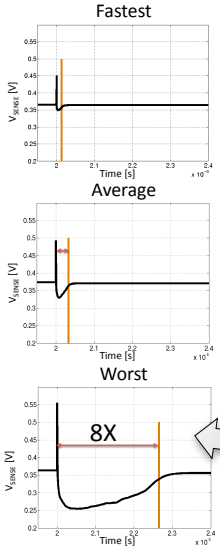
TX calibration taps may be used to fine tune offset calibration or as FFE taps.

RX Offset Calibration



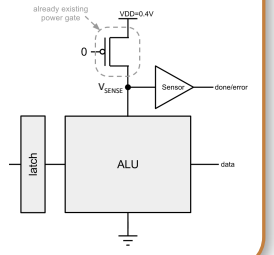
Sub/Near-Threshold Logic Timing Improvement

Current Profiles (16-bit MADD)



Current-Sensing Completion Detection

A simple analog sensor can be designed to detect a change in voltage between a power gate and any logic such as an ALU .



The worst case delay is far too large (8X) to be detected by conventional methods like Razor (which can detect a maximum of 1.5X delay). However, a current-sensor is able to detect the slow computation.

This Current-Sensing Completion Detection method has many advantages:

- ✓Detecting delay-related errors greater than 1.5X.
- ✓Robust operation at the max speed of the circuit.
- ✓Allows digital circuits to operate asynchronously in sub/near-threshold.
- ✓Can improve guarantee reliability of operation across process corners.

Detection Process