The Importance of Low-Power, Variability-Aware CMOS: Methods to Improve Performance

Abstract

Sub-threshold supply voltage operation of digital logic has seen increased popularity due to the importance of energy efficiency in energy-constrained applications such as emerging bio-sensor applications and remote wireless systems. Unfortunately, several problems exist that prevent conventional digital standard-cell designs from functioning efficiently in the sub-threshold region (0.2V-0.4V). The primary problem is that of threshold voltage variation. In sub-threshold these variations can vary circuit delays by more than 2.5 times their nominal value. This presentation will provide insight into how low-power circuits can be modified for better performance under these variations. Two techniques will be explored in detail: an automated sub-threshold digital standard-cell performance improvement technique and a new class of sub-threshold error detection circuitry based on current sensing completion detection. Using these techniques on sub-threshold circuits greatly improves reliability, energy, and speed. Furthermore it will be shown that, if used correctly, these techniques can boost throughput by over 70% over conventional sub-threshold digital designs.

Biography

Joe Crop received a B.S. degree in electrical and computer engineering from Oregon State University in 2009. He is now working towards his Ph.D. degree at Oregon State as a Research Assistant in the VLSI research group. Joe has held several teaching positions across Oregon State over the past five years. Most recently he was the instructor of a summer-term Computer Architecture class. His research focuses on making low-power circuits more reliable in the presence of wide variations of all forms. For more information visit his website at: http://people.oregonstate.edu/~cropj.

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