Design Automation Methodology for Improving the Variability of Synthesized Digital Circuits Operating in the Sub/Near-Threshold Regime

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Outline

- Motivations for Sub-threshold logic design
- Existing techniques and their Limitations
- Proposed Technique
- Results
- Conclusions

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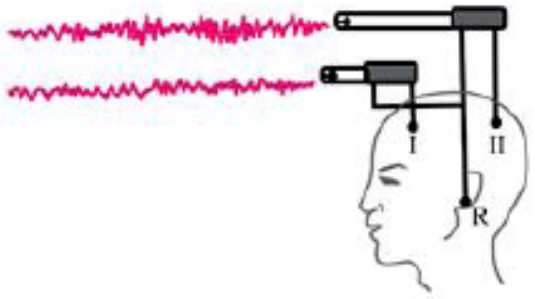
Motivation for Sub-Threshold Operation

- Battery Capacities are not improving as fast as CMOS
- Users expect long battery life
- Sensor networks need to operate remotely for longer

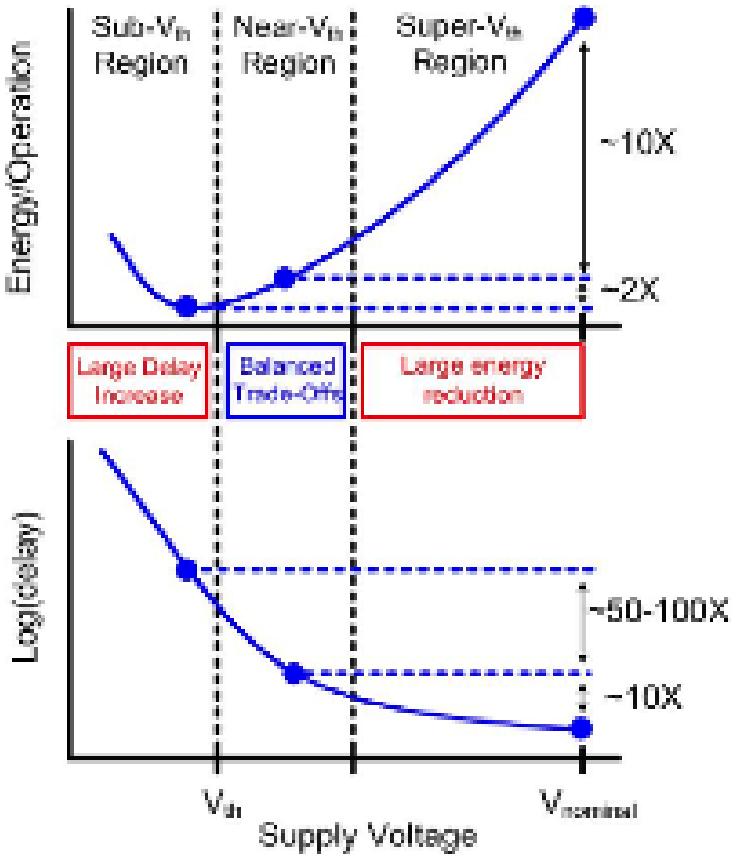


RFID **Mobile Phones** **Wireless Sensor Nodes**

- **We need more energy-efficiency to meet these demands**

Energy Efficiency ⇨ Sub-Threshold

- **Lower Energy = Lower V_{DD}**
  - $E = {}^{1}/_{2}\, CV^2$
  - ✓ 10x-15x energy improvement
  - x 1000x-10000x slower
- **Challenge: Variation**
  - Each die has a different max speed
  - Yield decreases



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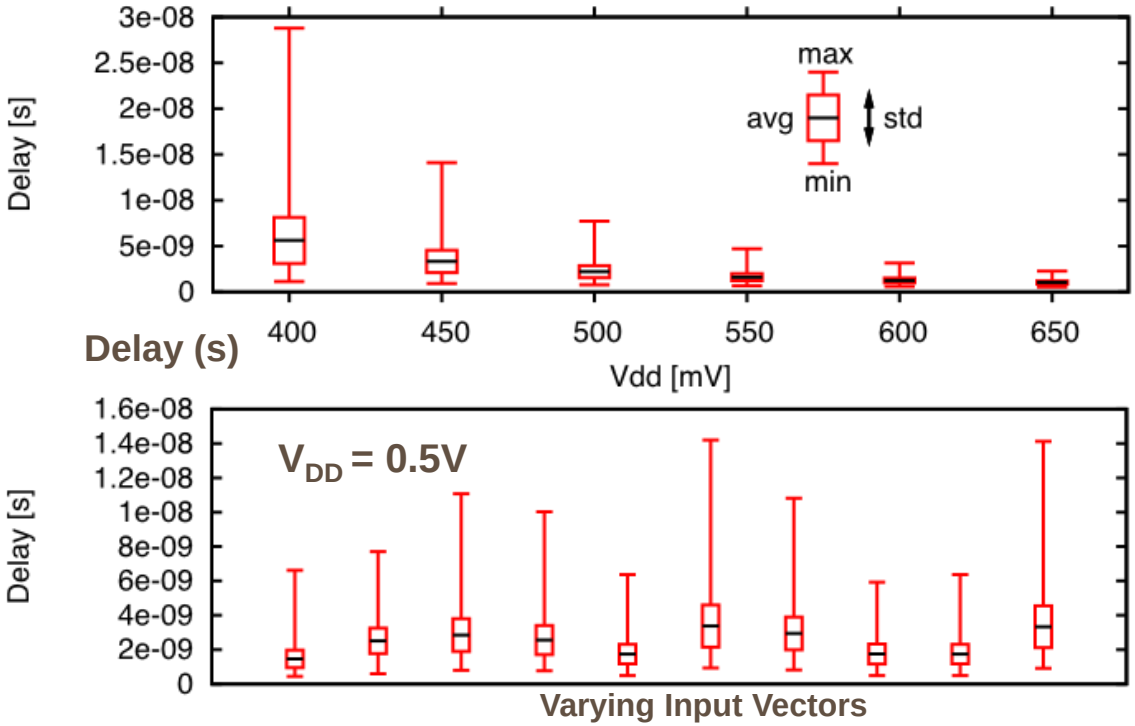
Sub-Threshold Operation ~ 0.4V

- **Sub-threshold current is exponentially dependent on V_{th}**
  - Amplifies effects of process variation and device mismatch on delay

$$I_{SUB} = \frac{W}{L_{eff}} \cdot \mu_{eff} \cdot C_d \cdot V_T^2 \cdot e^{\left(\frac{V_{gs}-V_{th}}{m \cdot V_T}\right)} \cdot \left(1 - e^{-\frac{V_{ds}}{V_T}}\right)$$

Hanson; *DAC ,2007*



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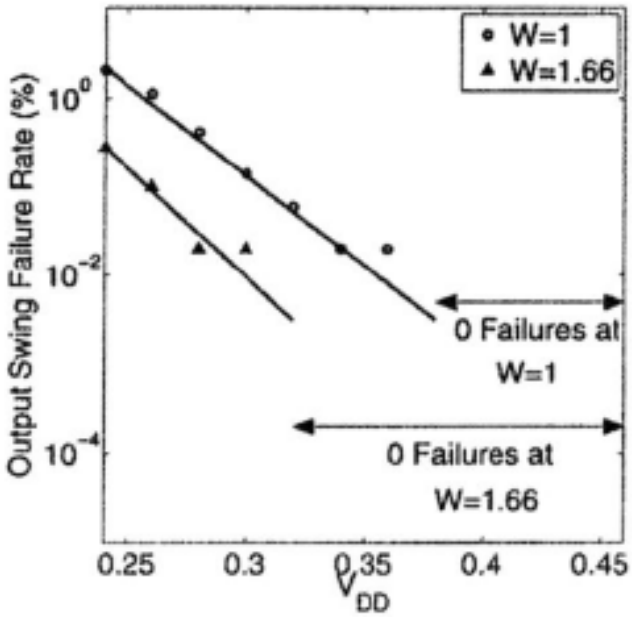
Traditional Sub-Threshold Improvement Techniques

- Variation: $\sigma V_{th} \propto 1/\sqrt{WL}$

- Increasing transistor W
  - lowers variability
  - increases power

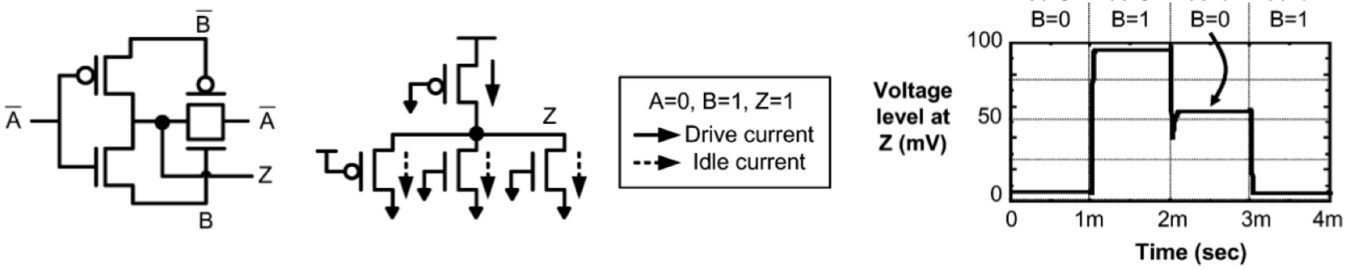
- The same is true for PMOS/NMOS width ratio



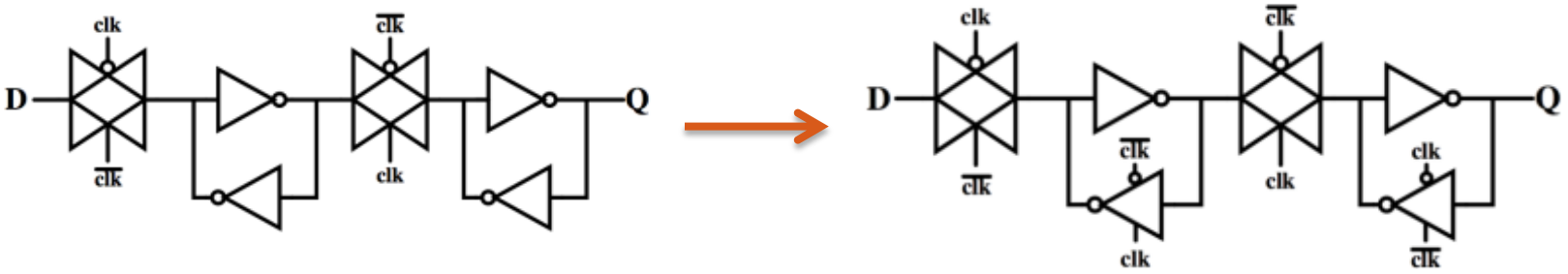
[1] Kwong, J.; Chandrakasan, A.P.; , "Variation-Driven Device Sizing for Minimum Energy Sub-threshold Circuits," *Low Power Electronics and Design, 2006. ISLPED'06. Proceedings of the 2006 International Symposium on* , vol., no., pp.8-13, 4-6 Oct. 2006

Traditional Sub-Threshold Improvement Techniques

- Parallel devices
  - High-Speed XOR2



- Tri-state feedback paths in flip-flops



Optimizing Digital Synthesis for Sub-Threshold

- Problems:
  - Manual inspection of every cell
  - Expensive redesign
  - No portability
- Solution:
  - Automate detection
  - Removal instead of redesign
  - Use existing timing libraries

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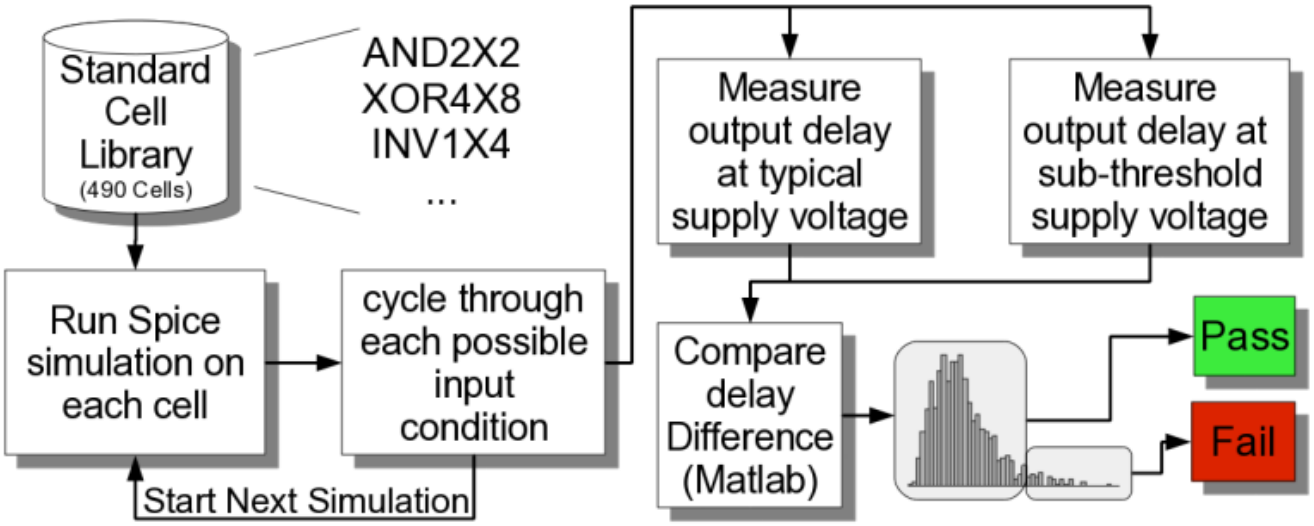
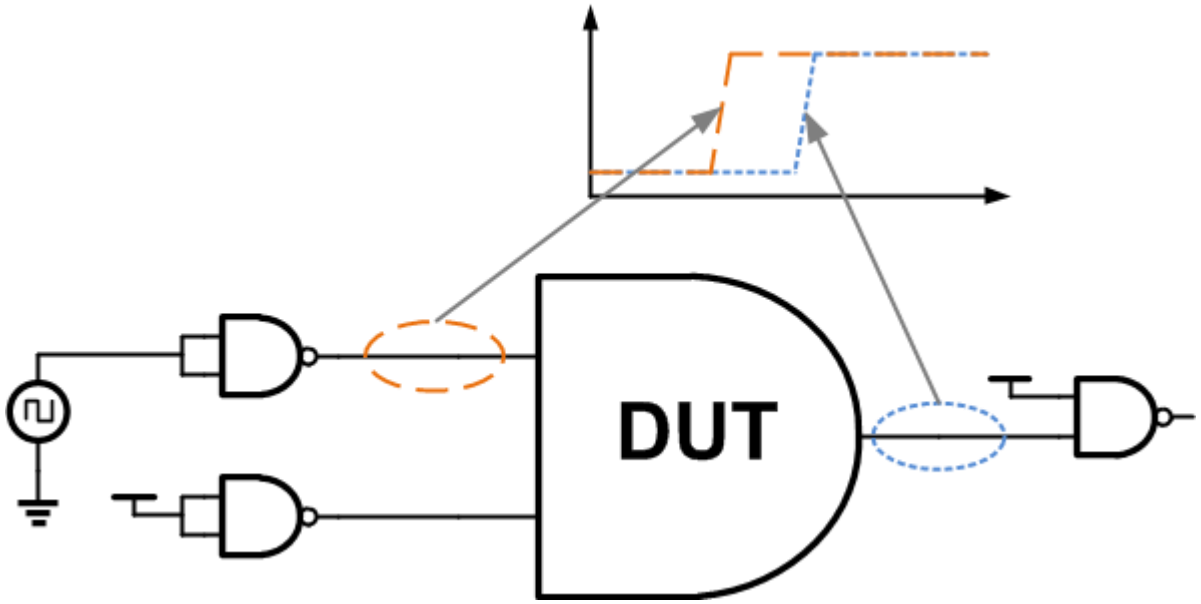


1. Cells are analyzed for timing
   - Compare **delay** of cells in sub-threshold to super-threshold
2. Cells are removed that simply don't work in sub-threshold
3. Cells are statistically removed

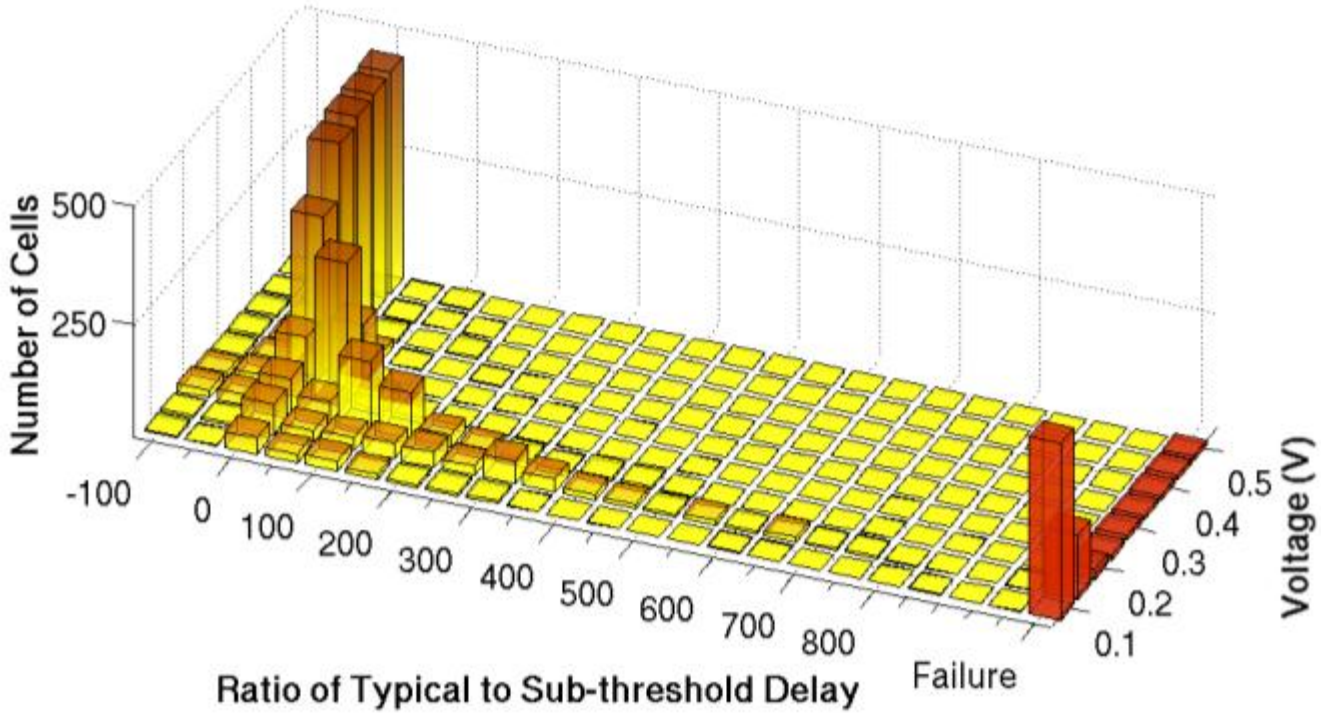
Typical Cell Testing Procedure

- Each cell driven/loaded by NAND2
- Delay is measured from input to output of DUT

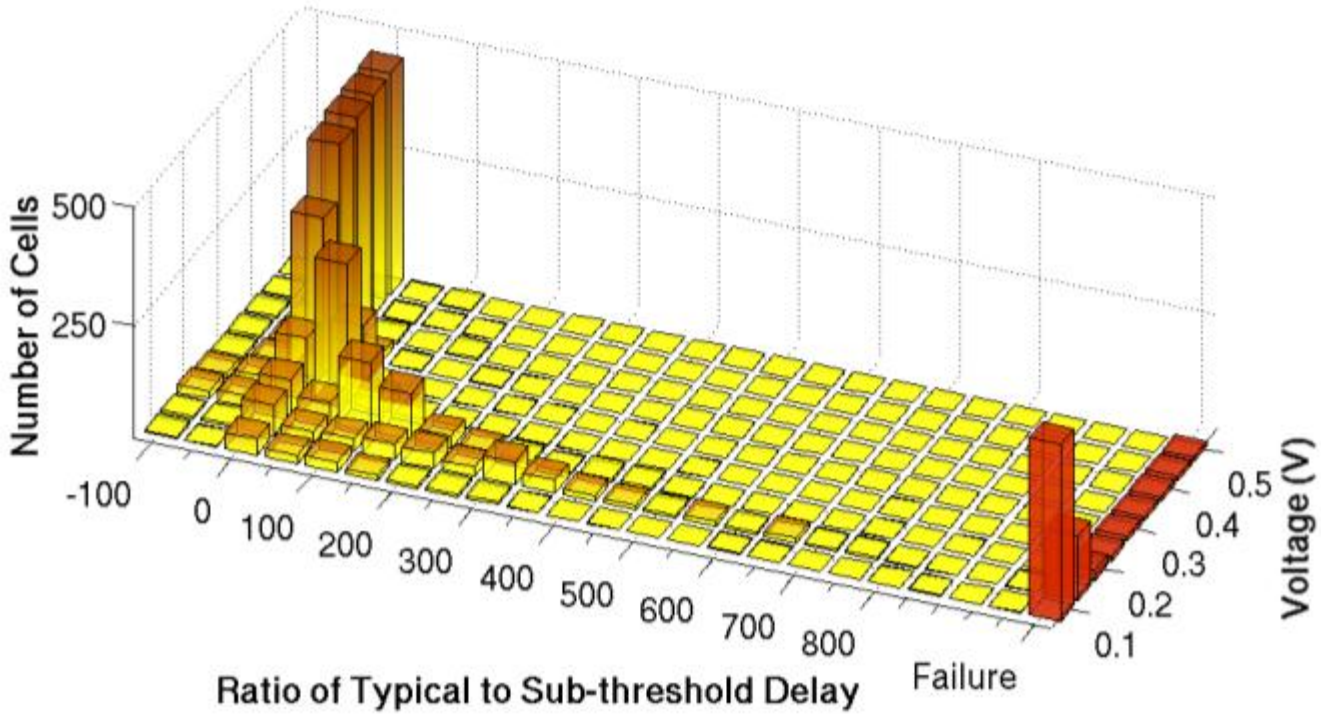


Histogram of Cell Delays

- As V_{DD} is lowered, delay distribution widens
- Failures begin to occur



Cell Removal Decisions



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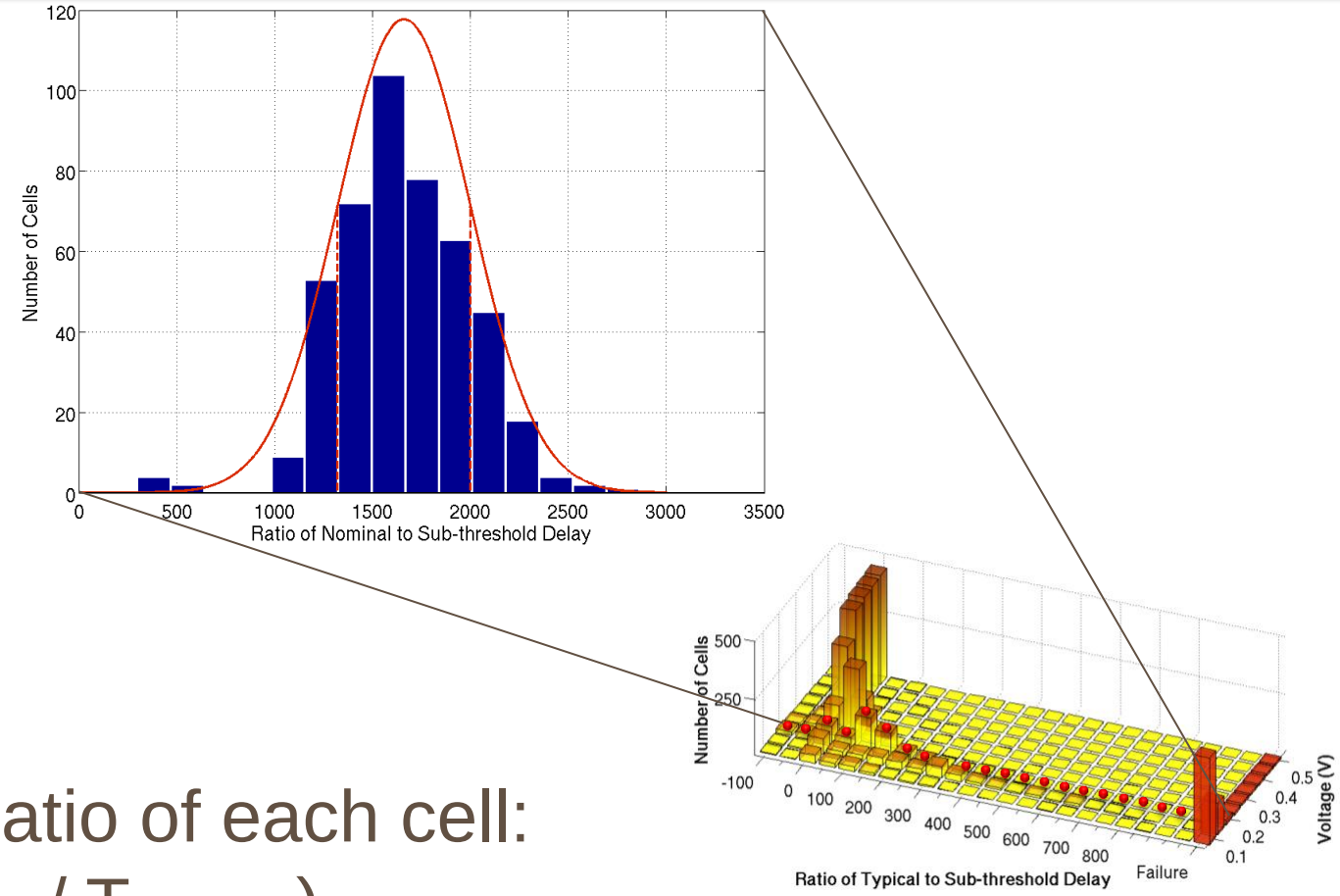
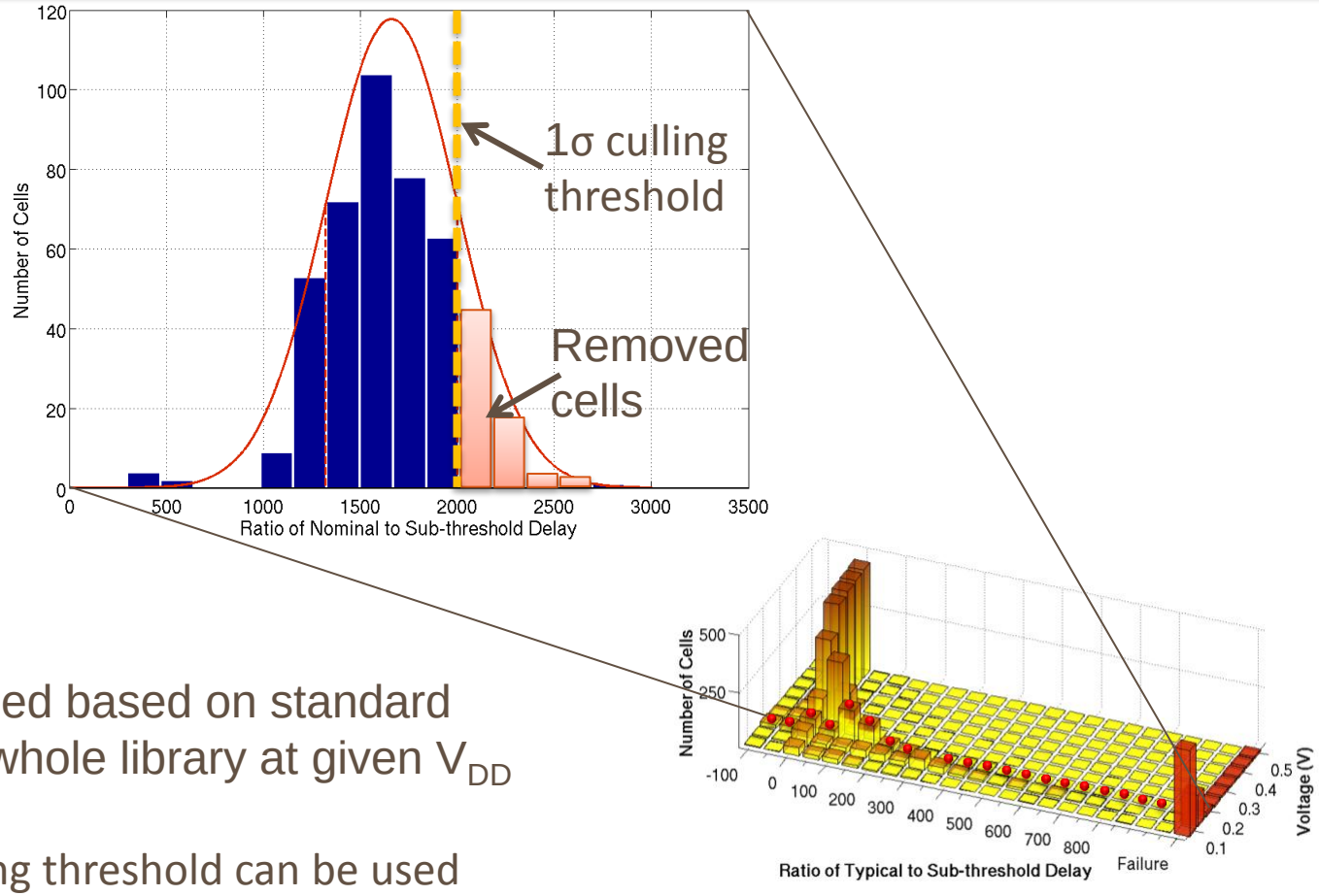
Cell Removal Decisions



- Delay Ratio of each cell:
  - ($T_{d\text{-}sub}$ / $T_{d\text{-}super}$)

Cell Removal Decisions



- Cells are culled based on standard deviation of whole library at given V_{DD}
- 1σ or 2σ culling threshold can be used

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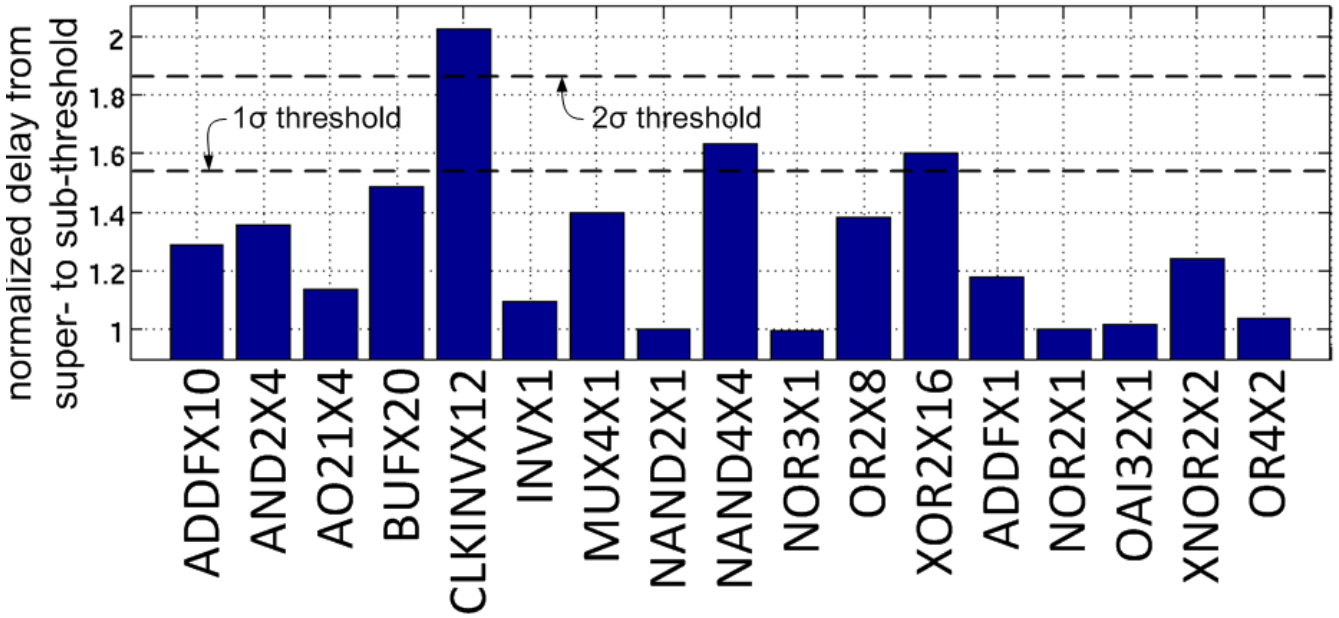
Removed Cells

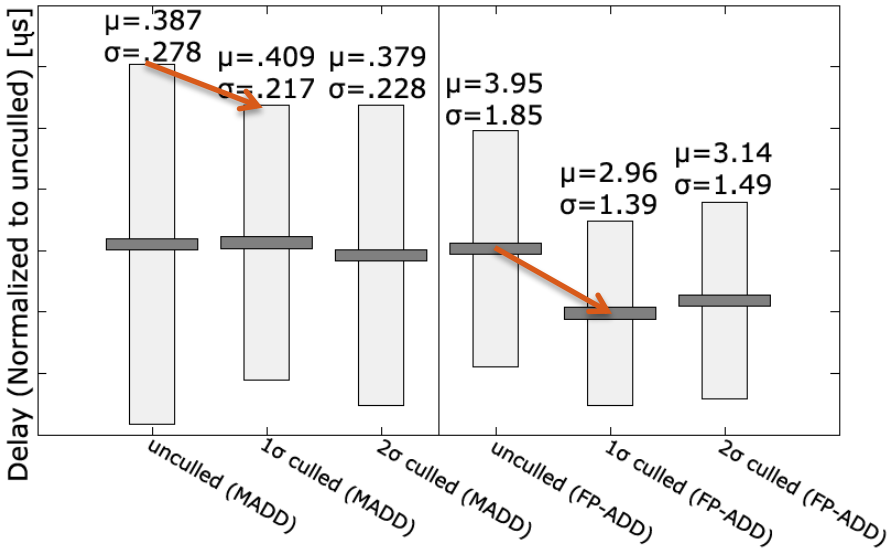
- Example of removed cells:

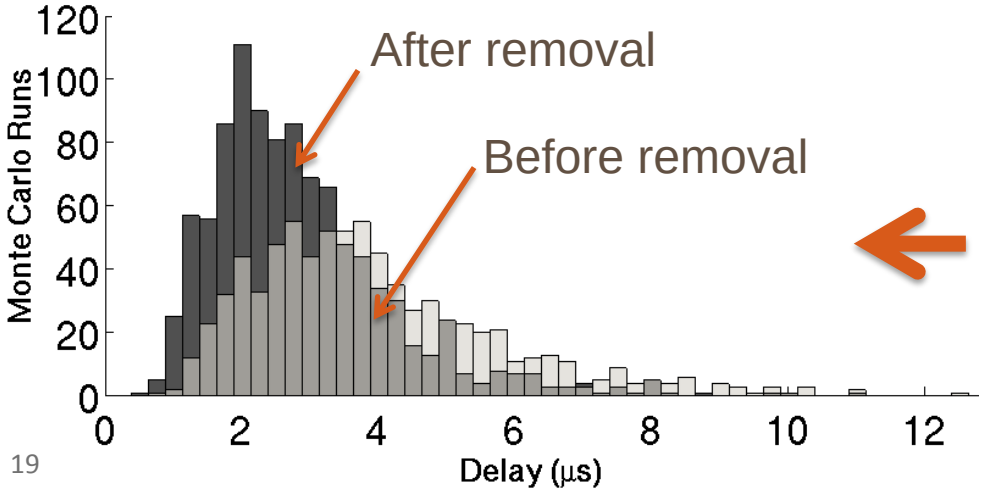


- Most cells that do not scale well:
  - Bad PMOS/NMOS width ratios
  - Cells designed for speed (usually large)
  - Large number of inputs

Delay Improvements

- Two designs were tested
  - Multiply Add (MADD)
  - Floating-Point Add (FP-ADD)
- Faster mean speed
- Reduction of outliers





- FP-ADD

Metric	Improvement
Standard Deviation	25%
Worst Case Delay	28%
Outliers	68%

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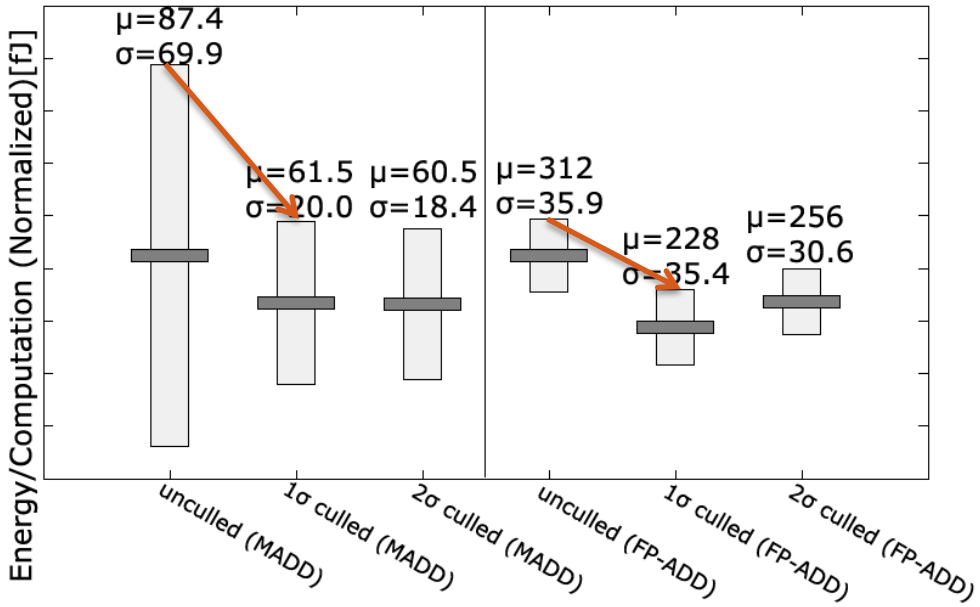
Energy Improvements

- With delays getting faster, naturally energy lowers
- Area is also lowered resulting in smaller leakage energy

Metric	Improvement
Standard Deviation	> 71%
Worst Case Energy	37% less
Average Energy	6-68% reduction



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Comparison of synthesized designs

- FP-ADD @ 1.2V = 3.66pJ/operation
- FP-ADD @ 300mV = 312fJ/operation
- FP-ADD @ 300mV, culled = 228fJ/operation

- Design goes from 10X energy improvement to 15X energy improvement

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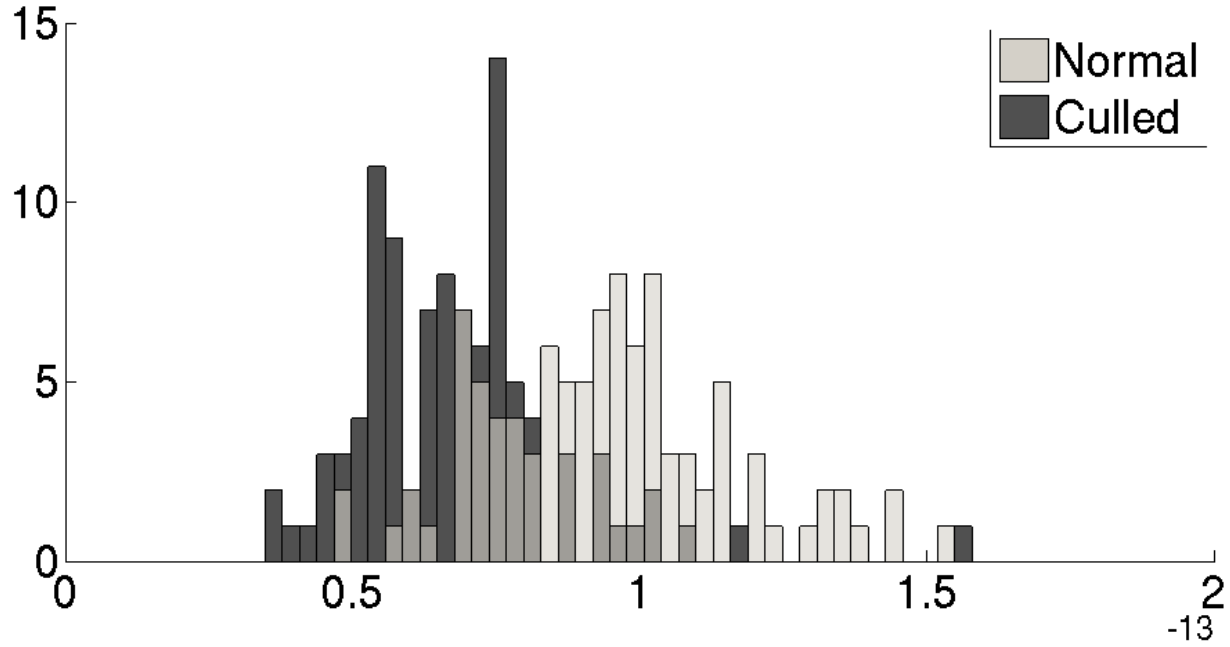
Conclusions

- Benefits of this methodology:
  - Fast
  - Reliable
  - Cost Effective
  - Scalable
- Improvements in:
  - Area
  - Delay
  - Energy
  - **Worst-case performance**

Questions?

BACKUP 1: Leakage energy graph

- Unwanted leakage is removed



BACKUP 2: Energy improvement graph

- Energy is lowered dramatically
- FP-ADD, 1 sigma culled vs. normal