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OBJECTIVE

PhD student researcher looking to continue a career in VLSI circuits and systems.

EDUCATION

Oregon State University (PhD ECE)
Current PhD student at Oregon State University actively participating in research in the VLSI group on ultra low-power integrated circuits.

Oregon State University (BS ECE)
Recent graduate from Oregon State University with a Bachelors of Science in Electrical Computer Engineering and a minor in Computer Science.

EXPERIENCE

Design Intern: Interned at Intel designing I/O circuits for next-generation server processors in 22nm CMOS. (Summer 2012)

Instructor: Taught ECE 473/573 to a mixed class of senior undergrads and graduate students. The class focused on digital design with Verilog, advanced synthesis techniques, and scripting.

Research Intern: Spent the summer as a research intern at Fudan University in Shanghai, China. Research focused on low-power and low-energy encryption engine optimization for integrated RFID systems. (Summer 2011)

Research Assistant: Currently researching resiliant ultra low-power digital circuits and architectures in the VLSI group at OSU (SRC,NSF,DOE,DOD,NSA, and DARPA funded). (Sept. 2010 – Present)

Summer Class Instructor: Taught class of computer science students over summer term. Material included computer architecture concepts, advanced assembly programming, and digital/CMOS logic. (Summer 2010)

Graduate Teaching Assistant: Teaching Computer Architecture / EE classes to undergraduate students. Topics range from digital logic and basic computer architecture to advanced CMOS circuit design.(Sept. 2009 – 2011)

Pre-college Outreach Programs Instructor at OSU: Currently teaches web design and other technology-oriented classes to both middle school and high school students through the university. (2006 – Present)

TECHNICAL SKILLS

Programming Languages: Java, C, C++, PHP, JavaScript, REST, AJAX, JSON, Android SDK, SQL, HTML, Perl, Python, UNIX/Linux Shell Scripting, Verilog, VHDL, Skill, LaTeX, Microsoft Assembly (MASM), AVR Assembly/C/C++/Arduino, TI MSP430 Assembly, SPICE, LabWindows CVI (LabView)

Engineering: Matlab, SPICE/HSIM, Cadence/Spectre, Xilinx FPGA Toolset, Sun Grid Engine, ModelSim, Synopsys Design Vision, SoC Encounter (+ CPF/UPF), Mentor Graphics PADS/Altium PCB Design Software, LabView, Focused Ion Bean (FIB)/Scanning Electron Microscope (SEM), Rad Worker 2

PUBLICATIONS

Krimer, E.; **Crop, J.**; Erez, M.; and Chiang, P.; "Replication-Free Single-Event Transient (SET) Detection for Eliminating Silent Data Corruption in CMOS Logic," Silicon Errors in Logic - System Effects (SELSE-9), Stanford University, March 2013

Crop, J.; Pawlowski, R.; and Chiang, P.; "Regaining Throughput Using Completion Detection for Error-Resilient, Near-Threshold Logic", Design Automation Conference (DAC), 2012

Chen, C-H; **Crop, J**; Chiang, P; Temes, G; , "A 12-Bit 7 W/Channel 1 Khz/Channel Incremental ADC for Biosensor Interface Circuits" ISCAS 2012

Pawlowski, R; Krimer, E.; **Crop, J**; Postman, J; Chiang, P.; Erez, M.; , "Synctium-I: A 530mV, 10-lane SIMD Processor with Variation Resiliency in 45nm-SOI" ISSCC 2012

Xiao, M; Xiang, S; Wang, J; **Crop,J**; , "Design of a UHF RFID Tag Baseband with the Hummingbird Cryptographic Engine" ASICON 2011

Crop, J.; Krimer, E.; Moezzi-Madani, N.; Pawlowski, R.; Ruggeri, T.; Chiang, P.; Erez, M.; , "Error Detection and Recovery Techniques for Variation-Aware CMOS Computing: A Comprehensive Review." J. Low Power Electron. Appl. 2011, 1, 334-356

Crop, J.; Pawlowski, R.; Moezzi-Madani, N.; Jackson, J.; Chaing, P.; , "Design automation methodology for improving the variability of synthesized digital circuits operating in the sub/near-threshold regime," Green Computing Conference and Workshops (IGCC), 2011 International , vol., no., pp.1-6, 25-28 July 2011

Moezzi-Madani, N.; Thorolfsson, T.; **Crop, J**.; Chiang, P.; Davis, W.R.; , "An energy-efficient 64-QAM MIMO detector for emerging wireless standards," Design, Automation & Test in Europe Conference & Exhibition (DATE), 2011 , vol., no., pp.1-6, 14-18 March 2011

Crop, J.; Fairbanks, S.; Pawlowski, R.; Chiang, P.; , "150mV sub-threshold Asynchronous multiplier for low-power sensor applications," VLSI Design Automation and Test (VLSI-DAT), 2010 International Symposium on , vol., no., pp.254-257, 26-29 April 2010