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Sub/Near-Threshold Variation Tolerance and Greater-than-2x Delay Detection

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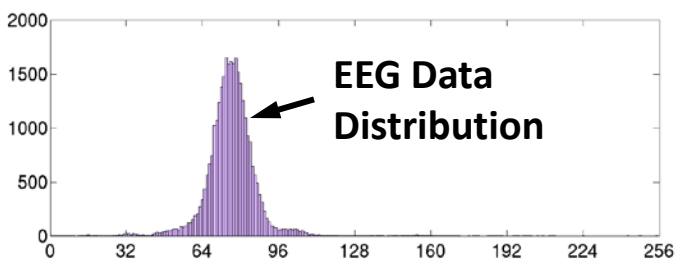
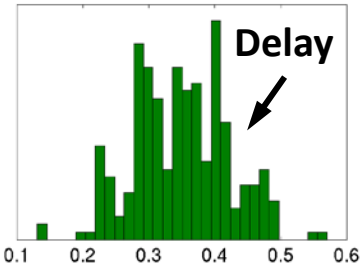
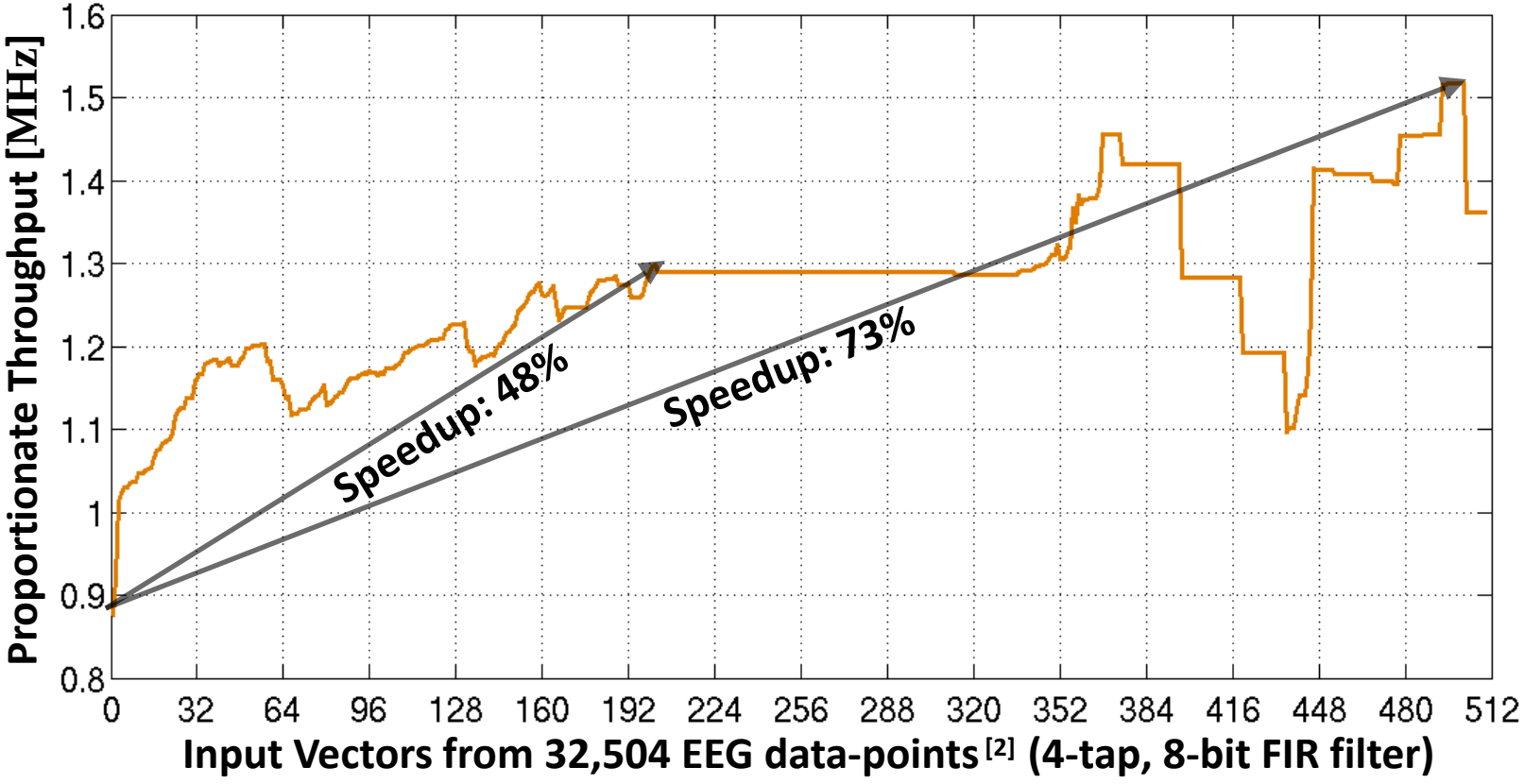
Motivation: Theoretical Throughput

- Slow paths replaced by 2-3 clock delays
- Take advantage of path-activation probabilities



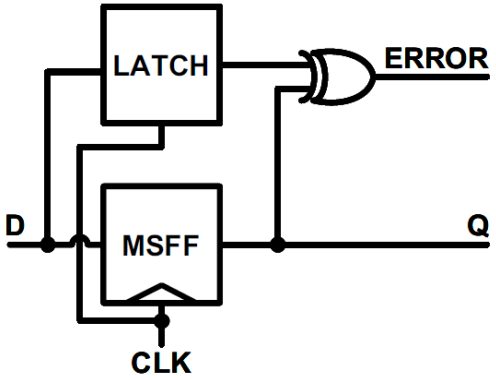




[2] EEG Data: One subject (80 trials) from a visual attention task http://sccn.ucsd.edu/~arno/fam2data/publicly_available_EEG_data.html

Conventional Razor Circuits

- Large Area and Power
  - Razor-FF at every output w/ 64-bit OR tree
- Might not work in sub-threshold
  - Tunable Replica Circuits (TRCs) only good for dynamic variation
  - Max delay can't be greater than 2x



[1] Bowman, K.A.; Tschanz, J.W.; Nam Sung Kim; Lee, J.C.; Wilkerson, C.B.; Lu, S.-L.L.; Karnik, T.; De, V.K.; , "Energy-efficient and metastability-immune timing-error detection and recovery circuits for dynamic variation tolerance," *Integrated Circuit Design and Technology and Tutorial, 2008. ICICDT 2008. IEEE International Conference on* , vol., no., pp.155-158, 2-4 June 2008

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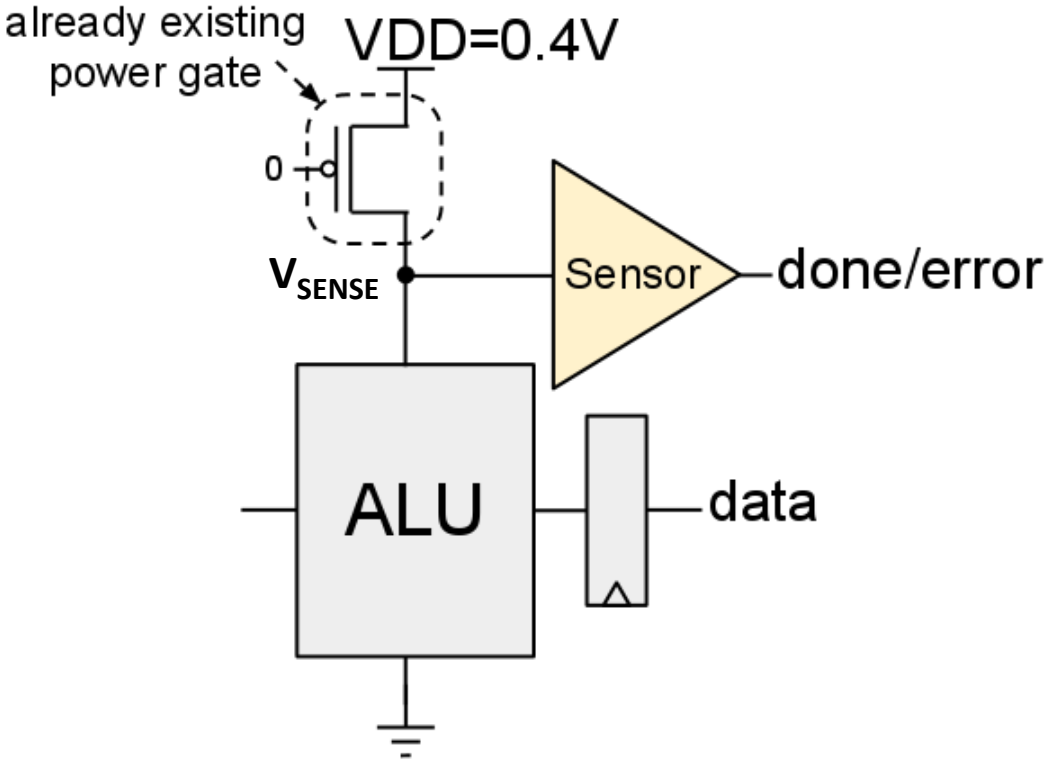
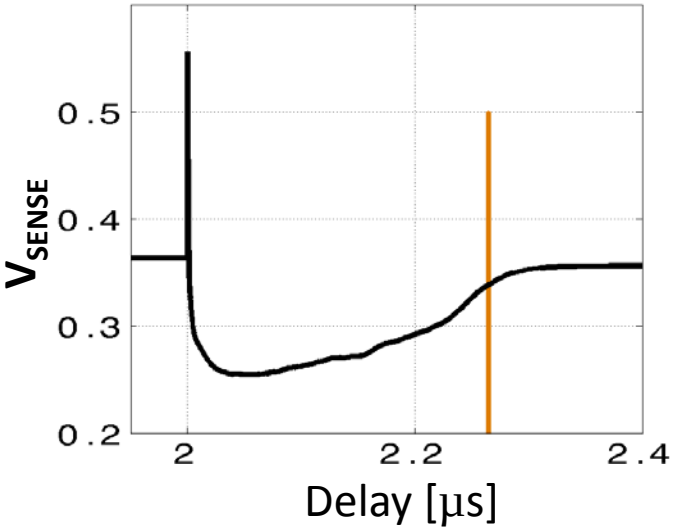
Current Sensing Completion Detection





- Completion can be based on current profile
  - Smaller droop = faster operation
  - Computation *always* finished before current settles

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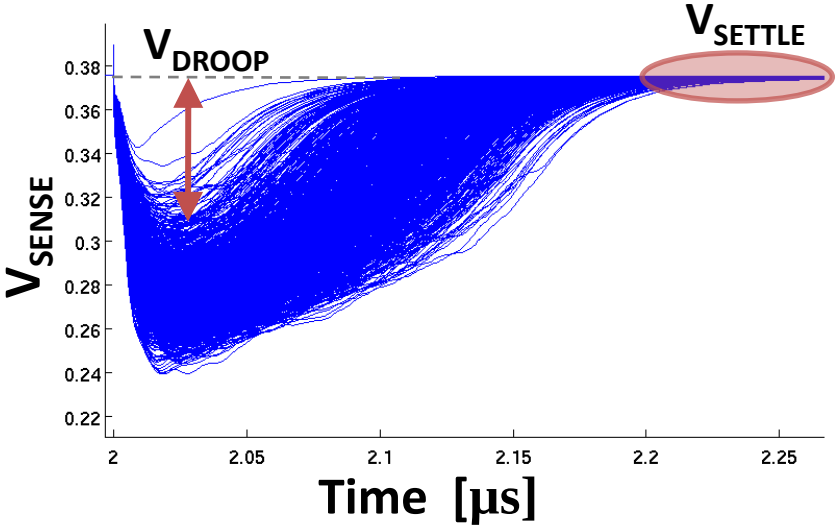
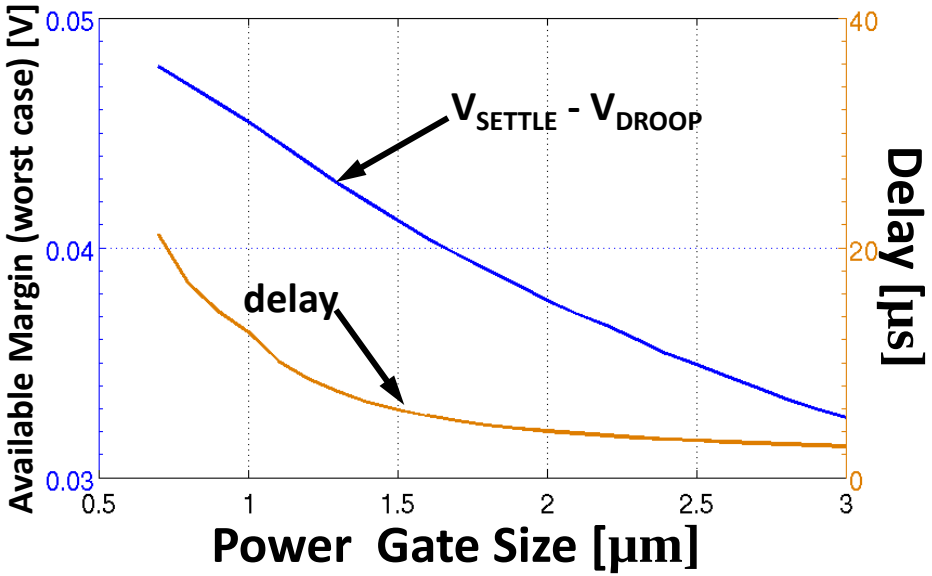
Monte Carlo Characteristics (1µm Power-Gate with 16-bit MADD)





- $V_{SETTLE} - V_{DROOP}$ is always positive at worst case
- Delay begins to converge as droop decreases linearly

Future Work

- Design robust sub-threshold detector
  - Precise quantizer (< 5mV input sensitivity)
  - Power supply noise cancelation/immunity
  - Analog / Digital synthesis integration
- Fabricate Test Chip
  - 40nm CMOS
  - Pipelined