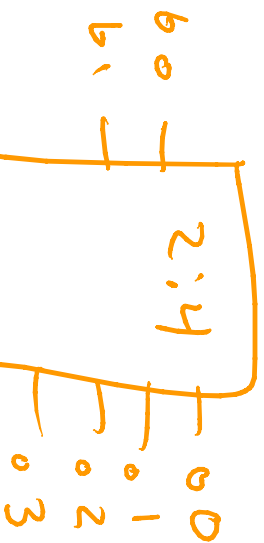


Decoder



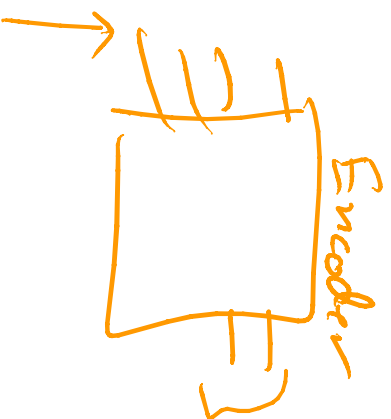
0	1	2	3
00	01	10	11

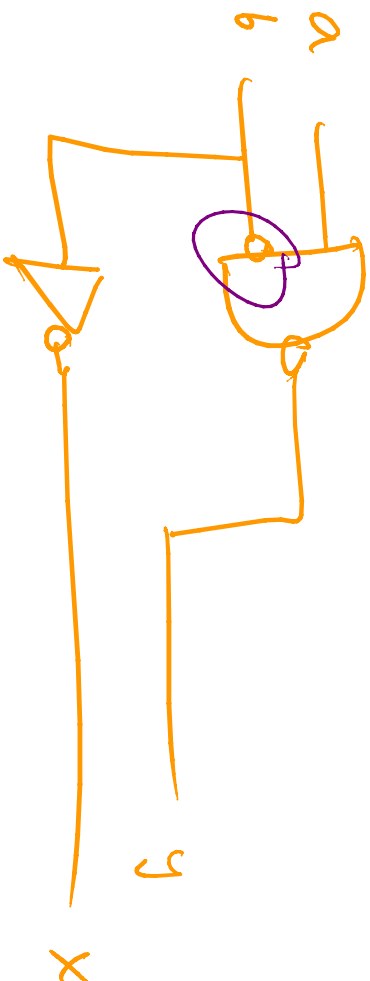
0001	0010	0100	1000
1110	1101	1011	0111



Inputs

0001 { 0011 { 0111 { 1111



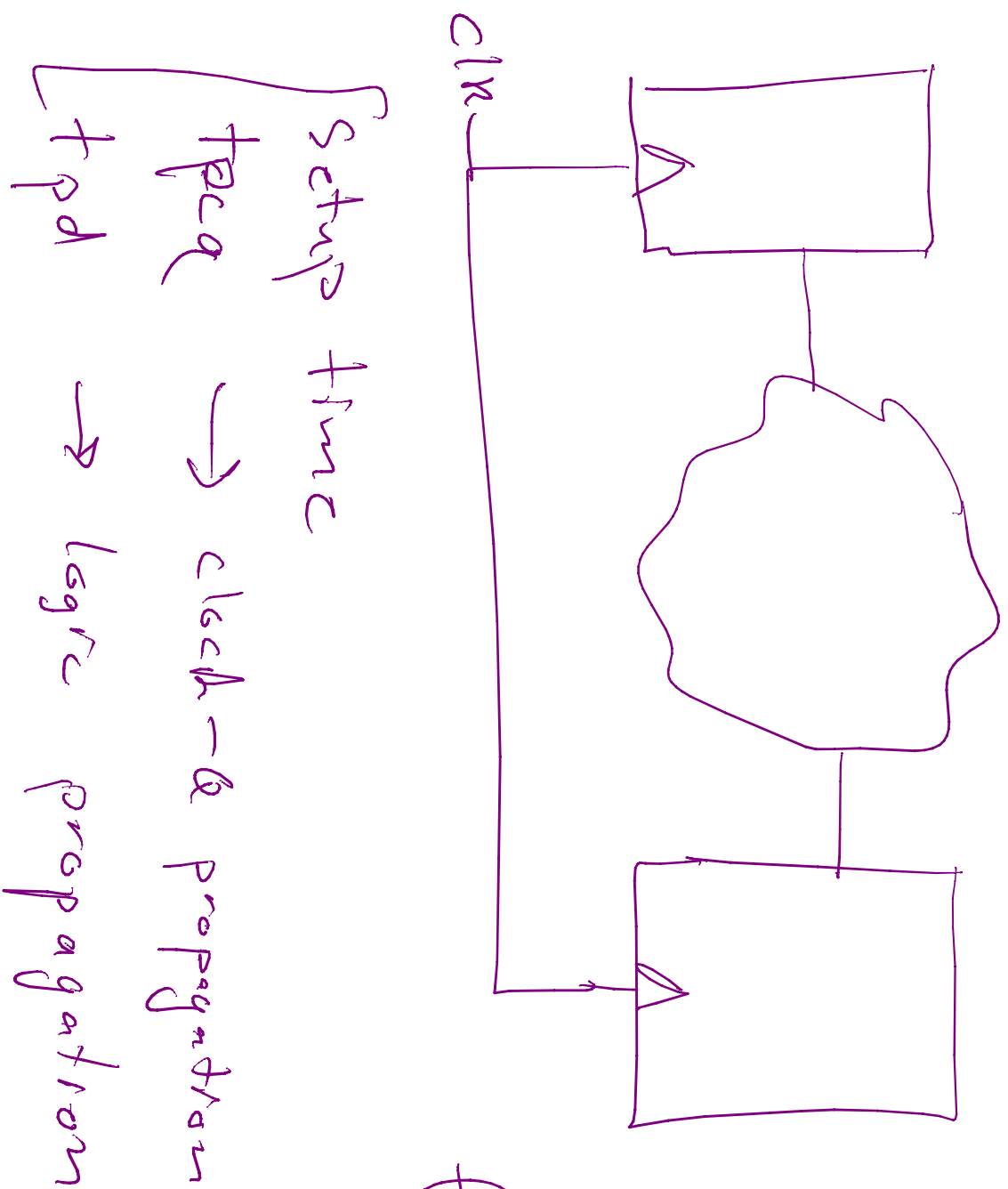


NAND		cd	Pd
Inv	10	20	
	2		6

Pd in out

b y

cd x



$$f = 1/t$$

Hold Time Violation

$$t_{cca} + t_{cd} > t_{hold}$$

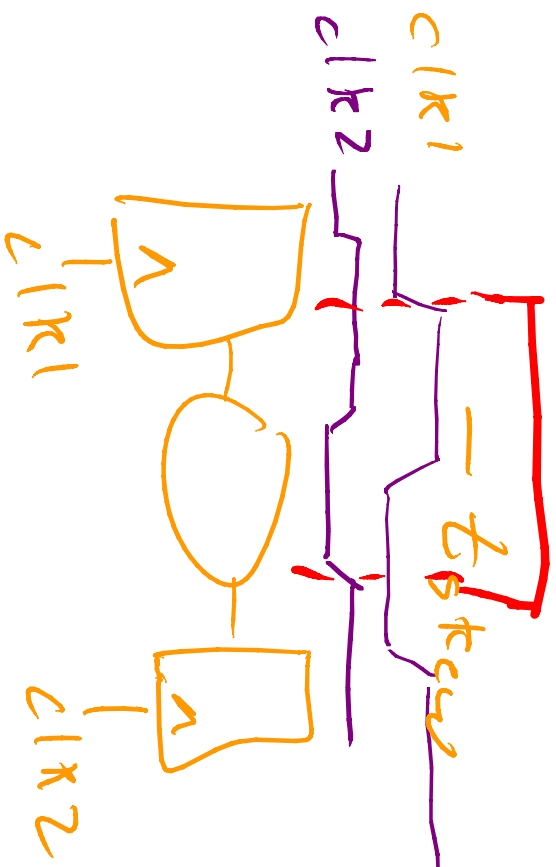
clock- &
contamination

logic
contamination

2 must be
> 1 for no
hold violation

Setup time + skew

$$(t_{pd} + t_{skew}) < (t_{setup})$$



$\left[\begin{array}{l} \text{clk } \underline{2} \\ \text{before} \end{array} \right.$

$\left. \begin{array}{l} \text{happens} \\ \text{clk } \underline{1} \end{array} \right\}$

2 must be
 < 1 for
 no violation

hold time + skew

$$t_{cq} + t_{cd} > t_{hold}$$

