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Regaining Throughput Using Completion Detection for Error-Resilient Near-Threshold Logic

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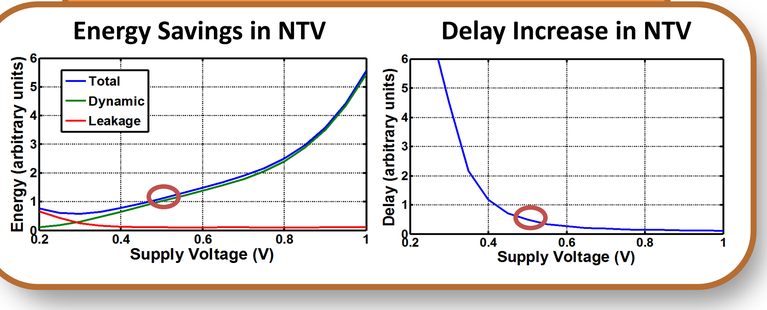
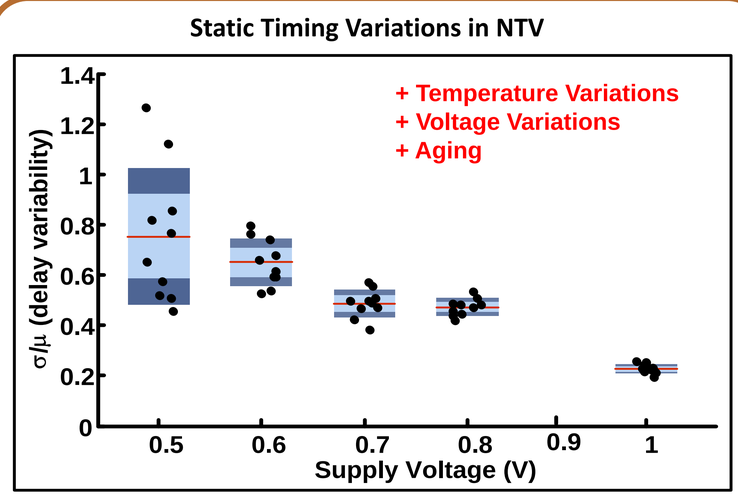
The Problem

Near-threshold operation can provide a substantial reduction in energy. However, as VDD is lowered, timing variations are exacerbated and circuit performance becomes unpredictable beyond tolerances.

Near-Threshold (NTV) = Low Energy + Longer Delays



Lower VDD → Delay Uncertainty



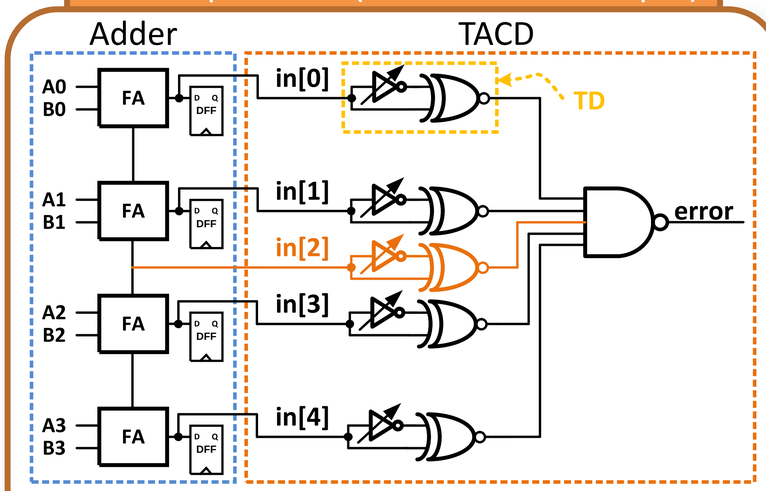
Our Goal

Error detectors that significantly improve throughput at NTV

→ Detector must be robust and resilient to variation at NTV

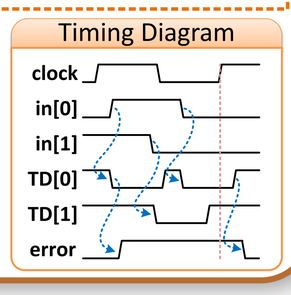
Detector 1: Transition Detecting Completion Detection (TACD)

TACD Operation (4-bit adder example)



- Throughput increase limited by added transition detector delays in error signal

Timing Diagram



Timing Requirements

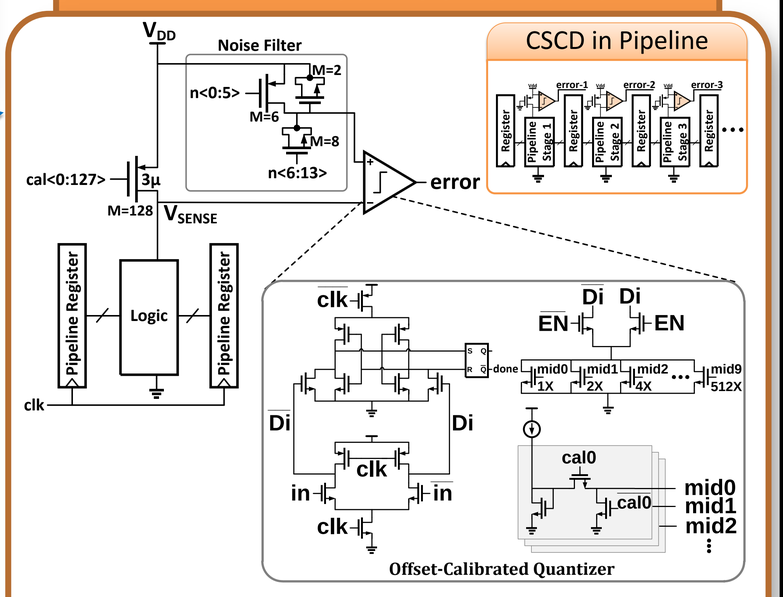
$$d_{inv} = d_{NAND\ tree} + \Delta_{toggle\ max} + d_{margin}$$

- d_{inv}: delay of tunable TDs
- $d_{NAND\ tree}$: delay of global NAND
- d_{margin}: PVT margins from EDA
- $\Delta_{toggle\ max}$: worst case time between any two output transitions

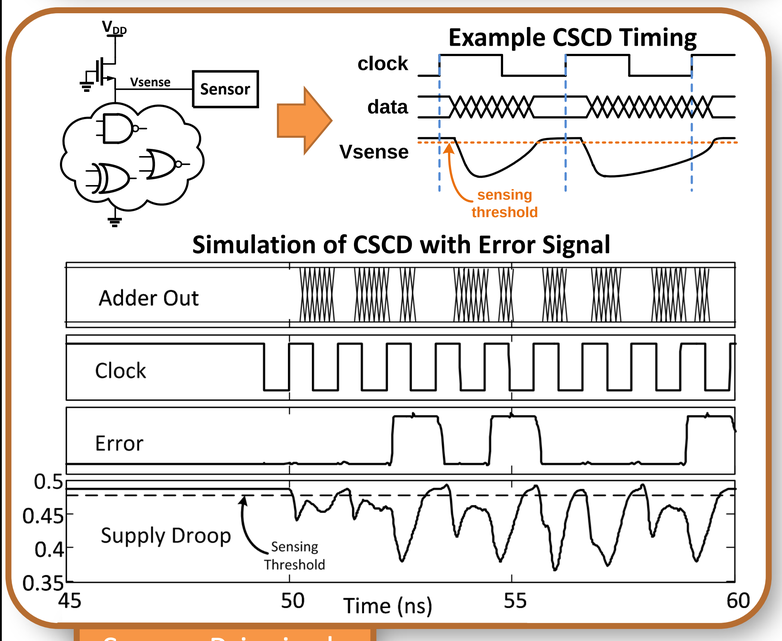
- **Output Glitch Tolerance**: $\Delta_{toggle\ max}$ must be less than the time between two consecutive output transitions or unwanted glitches.

Detector 2: Current Sensing Completion Detection (CSCD)

CSCD Circuit Schematic

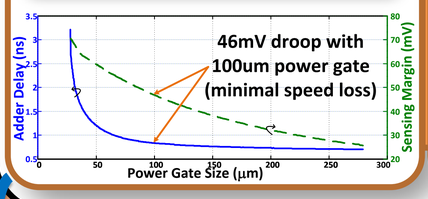


- **Digitally controlled sensing threshold**
- **Supply noise rejection filter**
- **Tunable across PVT variations**



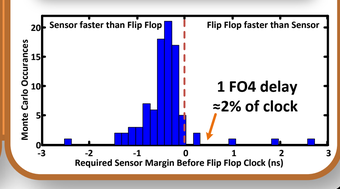
Sensor Principals

- Large sensing droops can be achieved with minimal speed loss



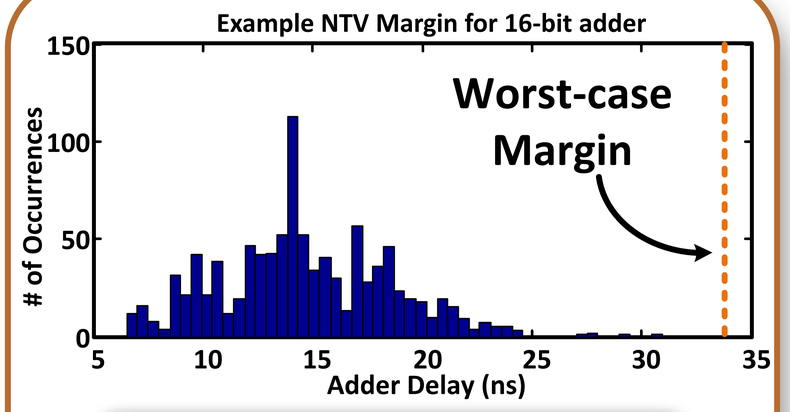
Sensor Resiliency

- Sensor conversion speed is faster than pipeline clock-Q delay across Monte Carlo



Conventional Methods

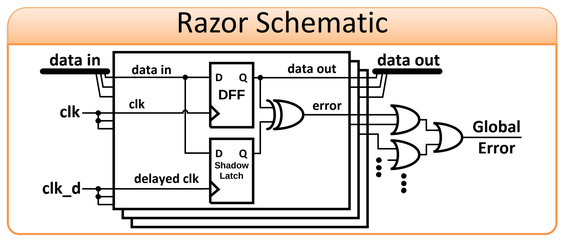
Delay Margining



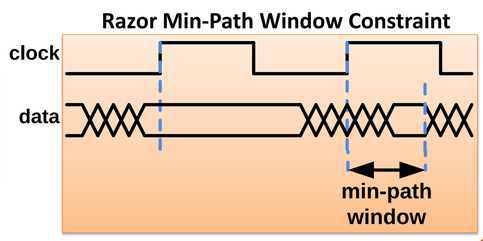
- Can result in over 200% speed decrease across Monte Carlo [6]

Timing Error Detection (Razor)

Razor Schematic



- Detection window limited by buffer insertion which is difficult to control



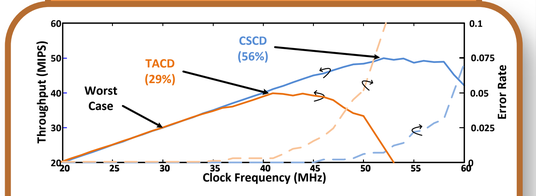
Performance Comparison

	No Detection (16-bit Adder)	Razor	TACD	CSCD
Detection Window	none	~20% after clock	> 70% before clock	~95% before clock
Throughput Potential	none	< 20%	Dependent on TDs (> 20%)	Limited by Sensing Margin (> 50%)
NYV Adaptability	none	none	Tunable Transition Detectors	Sensor Calibration

	No Detection (16-bit Adder)	Razor	TACD	CSCD
Average Energy (fJ/cycle)	192.5	976.5	910.3	195.9
Simulated Throughput (MIPS)	32	38.4 (20%)	41 (28%)	49.9 (56%)
Area Overhead (μm^2)	15495	24080 (155%)	15796 (102%)	16005 (103%)

INSIGHT: Larger Detection Window → Larger Throughput Potential

Throughput Comparison



- TACD Throughput saturates due to finite TD and NAND tree delay
- CSCD throughput saturates due to settling time of virtual supply