Vectors in Verilog

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Vectors

- AKA
  - Busses
  - Multi-bit wires
  - Arrays (busses of busses)

Examples

```
wire a;                  //scalar net, default
wire [7:0] bus;          //8-bit bus
wire [31:0] busA, busB;  //2 32-bit busses
reg [127:0] my_reg; //registers can be busses
reg [0:3] big_endian; //usually not a good idea
```

- Tips
  - The MSB is always on the LEFT!
    - “Always” put the largest number on the left (Little endian)
  - Avoid multiple declarations per wire

Vector Part Selections

- Standard Notation

```
assign y = busA[7];
assign x = busA[4:2];

assign x = busA[2:4];
    //illegal based on how busA was
    originally defined as little endian
```

- Cool Shortcuts (to avoid)

```
assign z = busA[31-:8] //busA[31:24]
assign z = busA[24+:8] //busA[31:24]
assign z = busA[31-:8] //busA[24:31] BAD!
Assign z = busA[24+:8] //busA[24:31] BAD!
```

Arrays

- Arrays can only be defined as:
  - *reg, integer, time, real, realtime, vector*
  - *Generally used for modeling (not synthesis)*

```
reg [4:0] x[7:0];
```

  - Array of 8 x's, each being 5 bits wide

```
integer m[4:0] [255:0];
```

  - 2-dimensional array or integers

```
reg [2:0] 4d [15:0] [3:0] [11:0] [1:0];
```

  - 4-dimensional array