

Dr. Patrick Chiang

Methods to Improve Reliability in Sub/Near-Threshold Circuits

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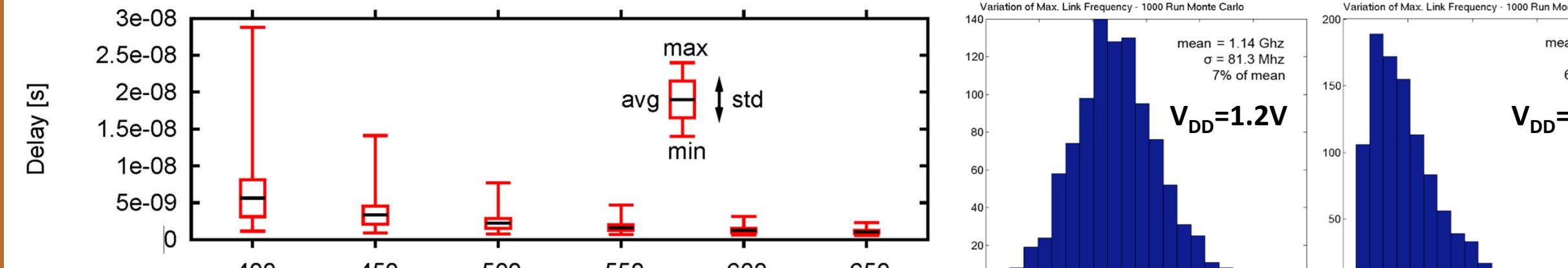
Jacob Postman
Joe Crop

The Problem

Sub/near-threshold operation can provide a 10X reduction in energy. However, as VDD is lowered, timing variations are exacerbated and circuit performance becomes unpredictable beyond tolerances.

Unpredictable Logic

Current methods of error detection within digital logic like Razor circuits are not robust enough to detect errors generated by large variations (greater than 1.2X). The maximum operating frequency must often be lowered when running in sub/near-threshold to tolerate process variation.



Expensive Communication

Technology scaling enables increased parallelism which can offset the performance loss of energy-optimal, low-voltage operation. However, the energy required to move data remains a critical bottleneck. Energy-efficient signaling techniques can be scaled with supply voltage, but require extreme attention to area constraints and the amplified effects of process variation.

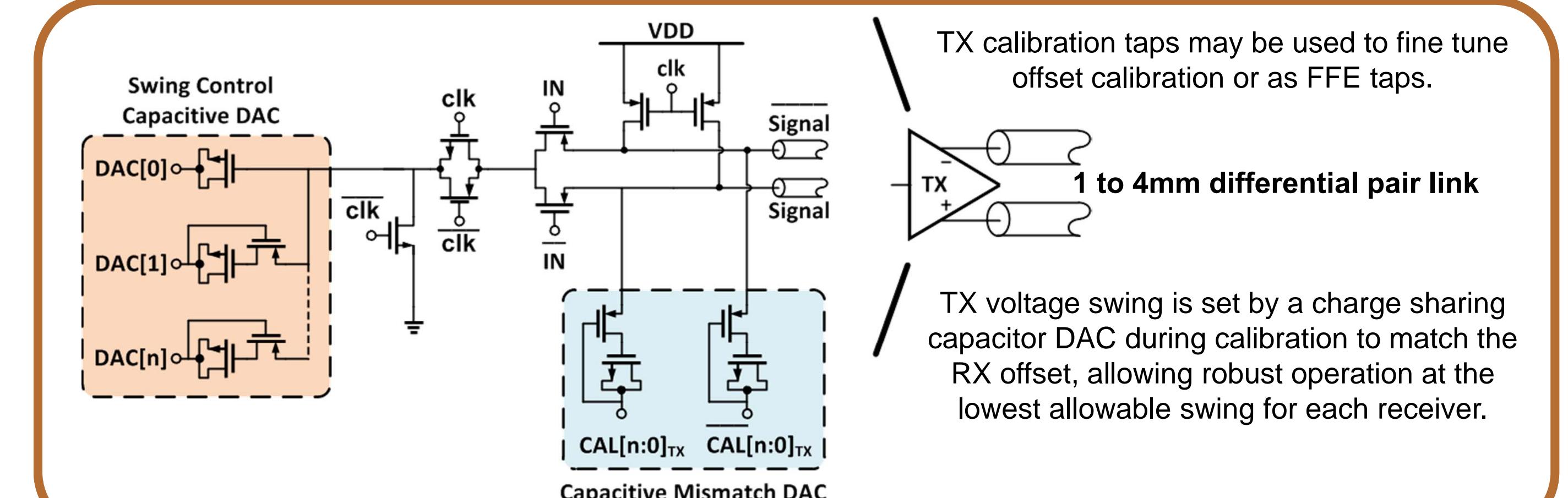
Energy Efficient Links

0.4V, 16bit MADD operation: 200fJ

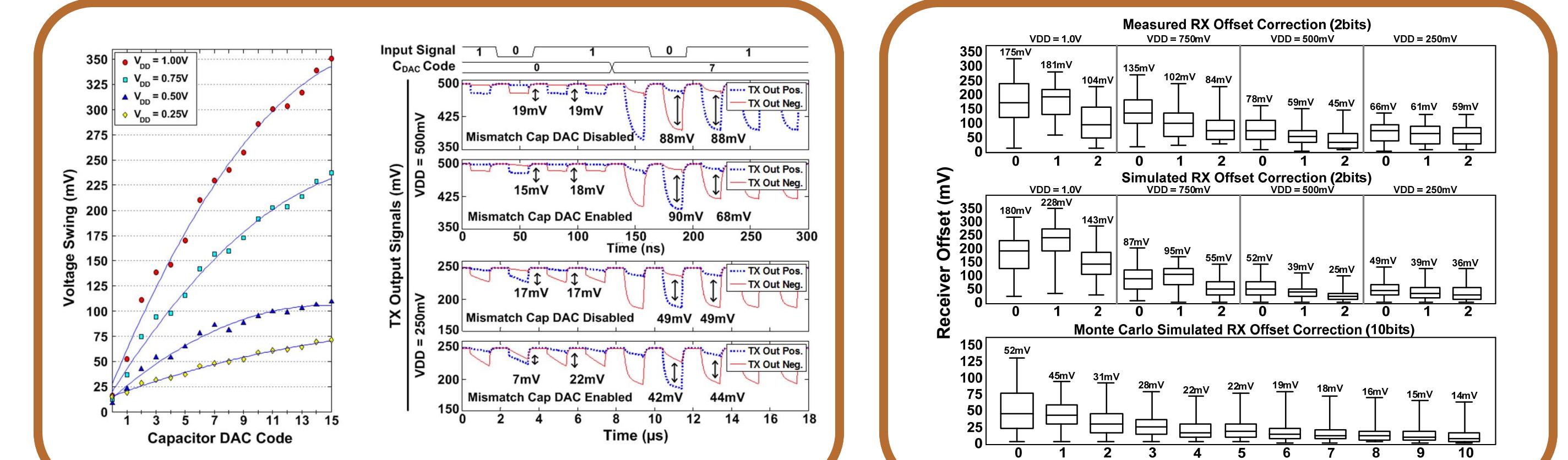
Moving 16bits 300um: 250fJ

Communication is still expensive in sub/near-threshold!

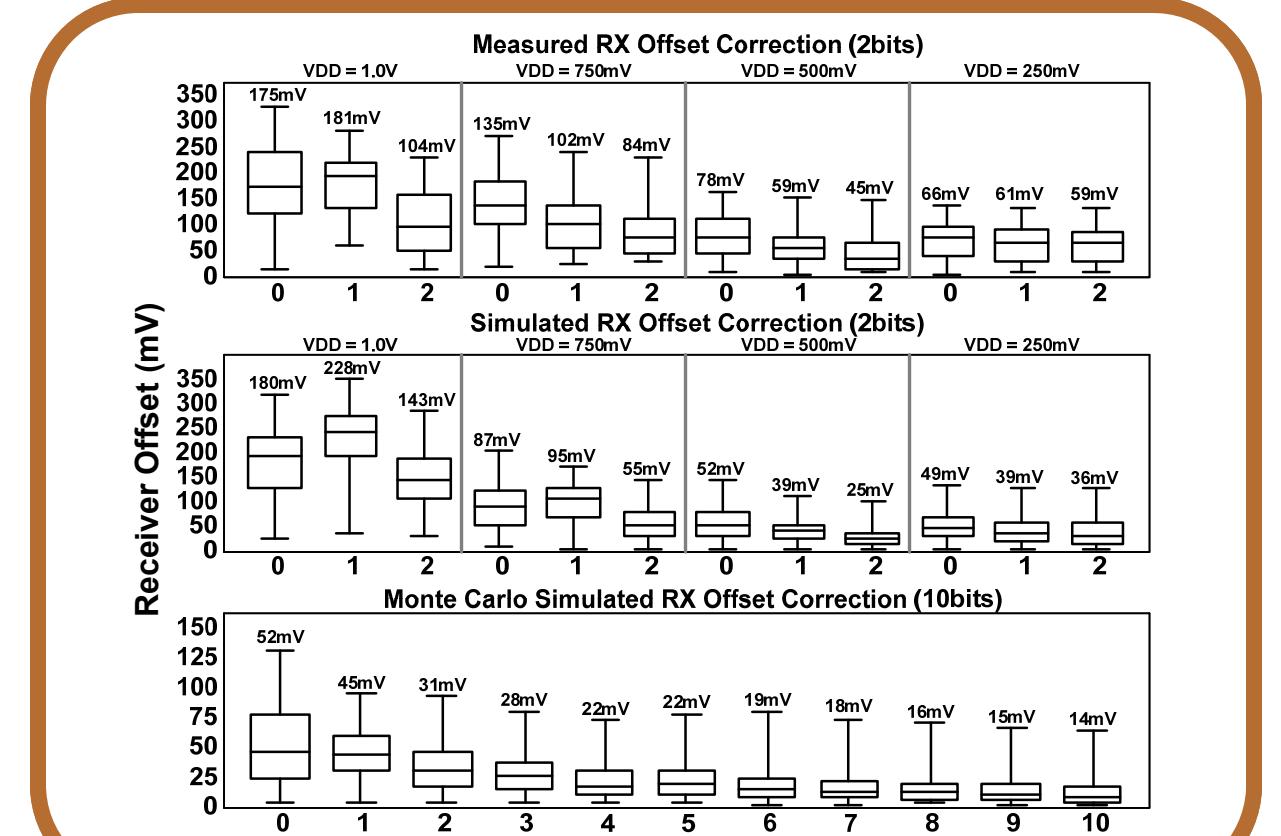
TX Swing Control & Calibration



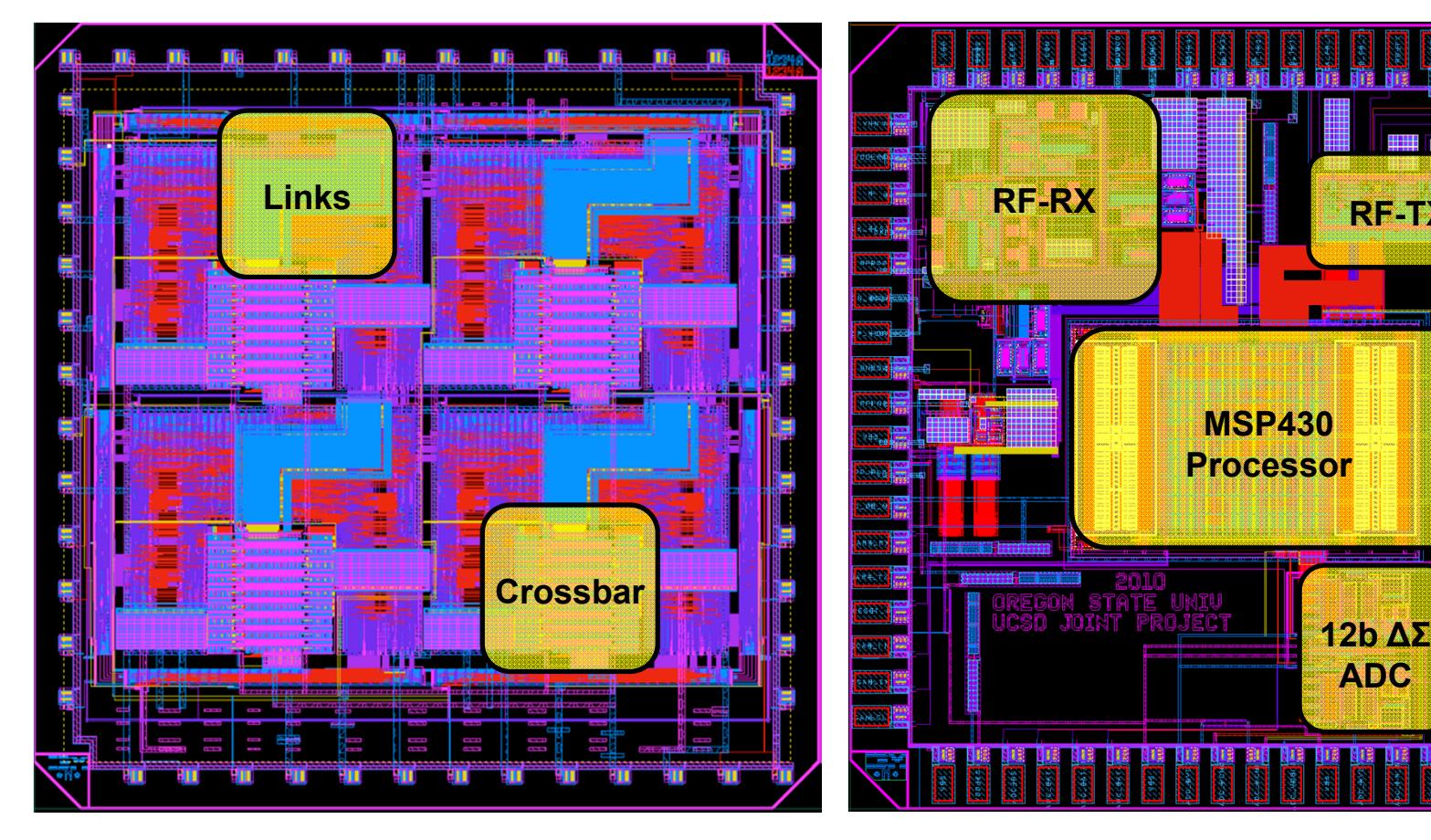
TX Swing Control



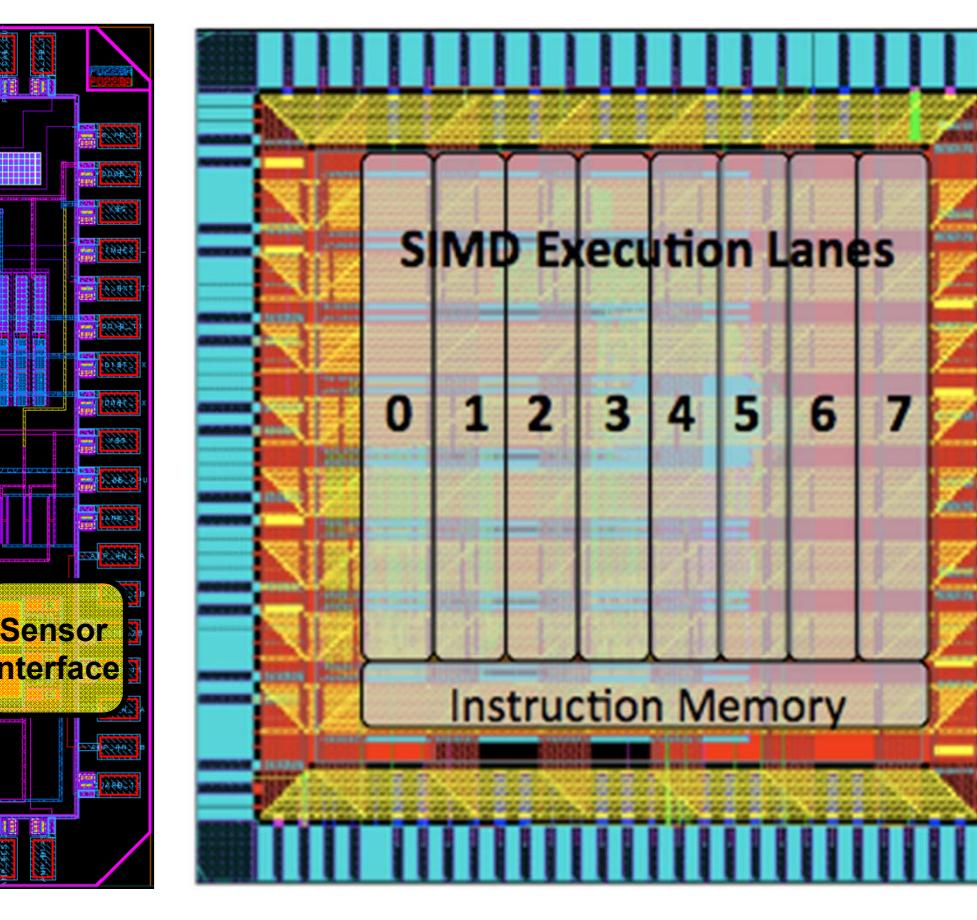
RX Offset Correction



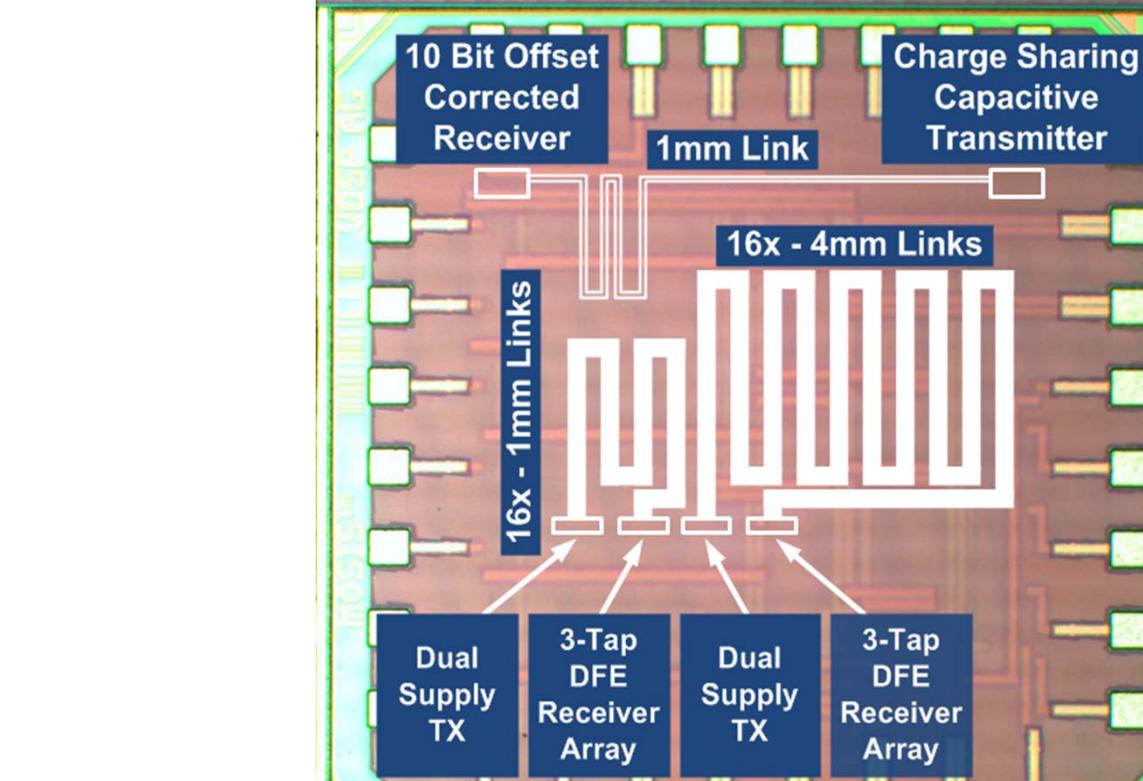
Previous & Current Work



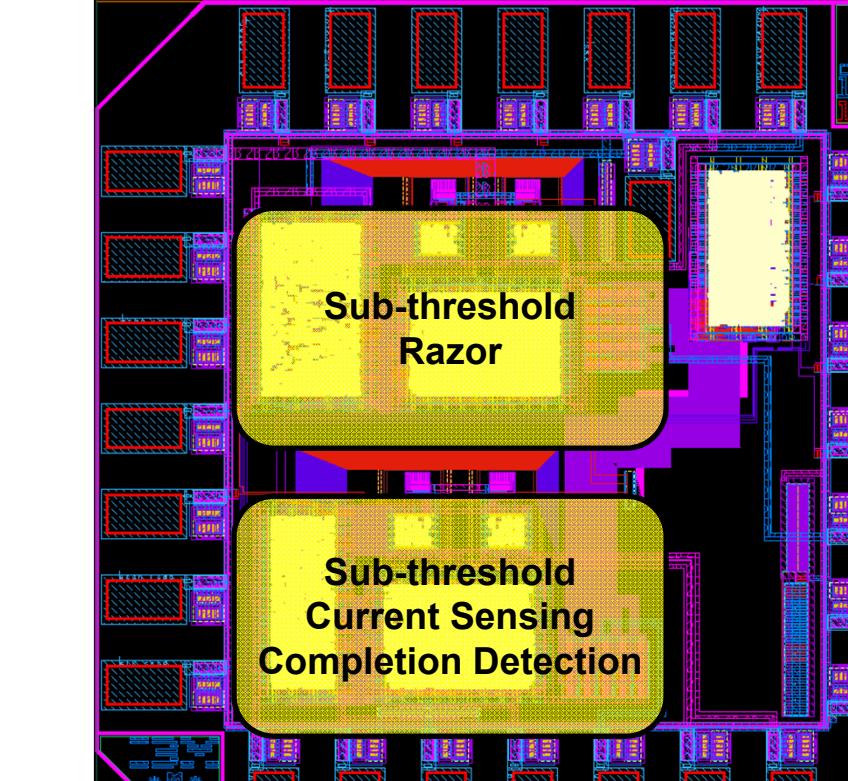
90nm, 1.2V, 4-node network-on-chip with low-swing links/crossbar
(Tapeout: May 2009)



90nm, 0.5V single-chip, wireless EKG/EEG sensor SoC with near-threshold digital processing
(Tapeout: May 2010)

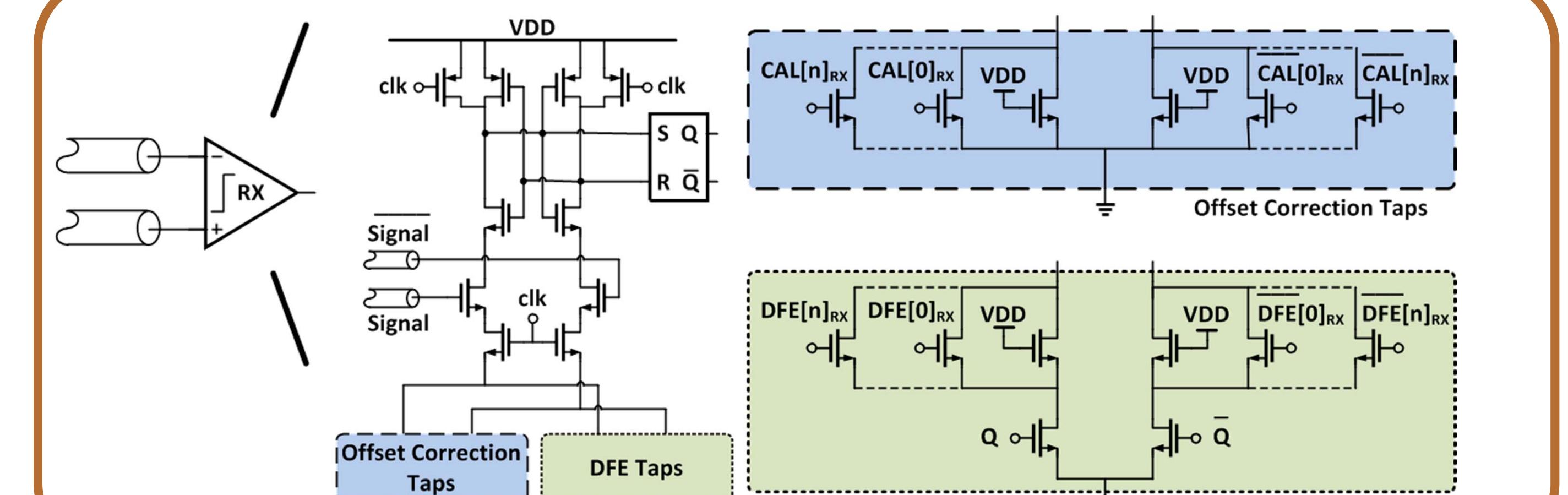


45nm, 0.5V, 10-lane SIMD processor with error detection and correction
(Tapeout: June 2010)



65nm, 0.4V low voltage swing links with 2-bit RX cal,
10-bit RX cal and 3 tap DFE
(Tapeout: May 2010)

RX Offset Correction & DFE



Type	This Work				
	Conventional Full-Swing Router (ISSCC '09)(JSSCC '09)	Capacitive-TX 10b RX Cal, No DFE			Dual Supply-TX 2b RX Cal, 3b DFE
Technology	22nm	90nm	90nm	90nm	65nm
Supply Voltage	0.7V	1.2V	1.2V	1.2V	0.25V
Wire Length (mm)	1.2	2	1	10	1
Data Rate (bps)	7G	9G	300M	9G	5M
Signal Swing (mV)	700	1200	250	~200	~40
E/bit/mm	250fJ	405fJ	64fJ	35.6fJ	8.4fJ
Transceiver Area	N/A	23um ²	2880um ²	N/A	TX 122um ² RX 112um ² Total 234um ²
					TX 5.5um ² RX 35.1um ² Total 40.6um ²

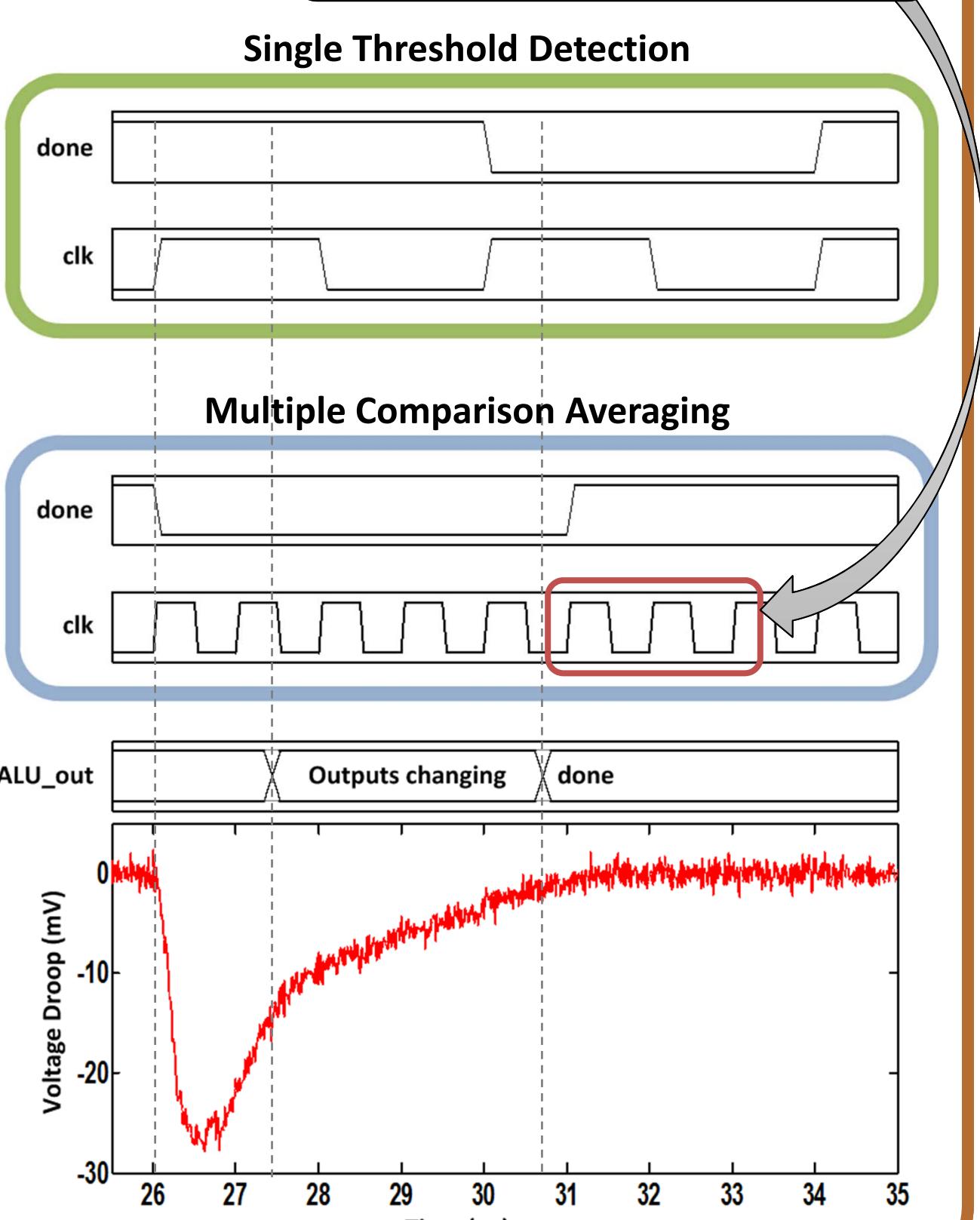
¹Design is optimized for $V_{DD}=0.25\text{-}0.5\text{V}$ with a large dynamic range of signal swings. At 1V and 622Mbps (lowest frequency limit of the BER), a BER of 5e-8 was observed. E/b, BER, and data rate can be improved significantly at higher supply by device resizing. Area can be reduced with less TX-cap tunability.

Error Detection in Logic

Current Profile Detection Techniques

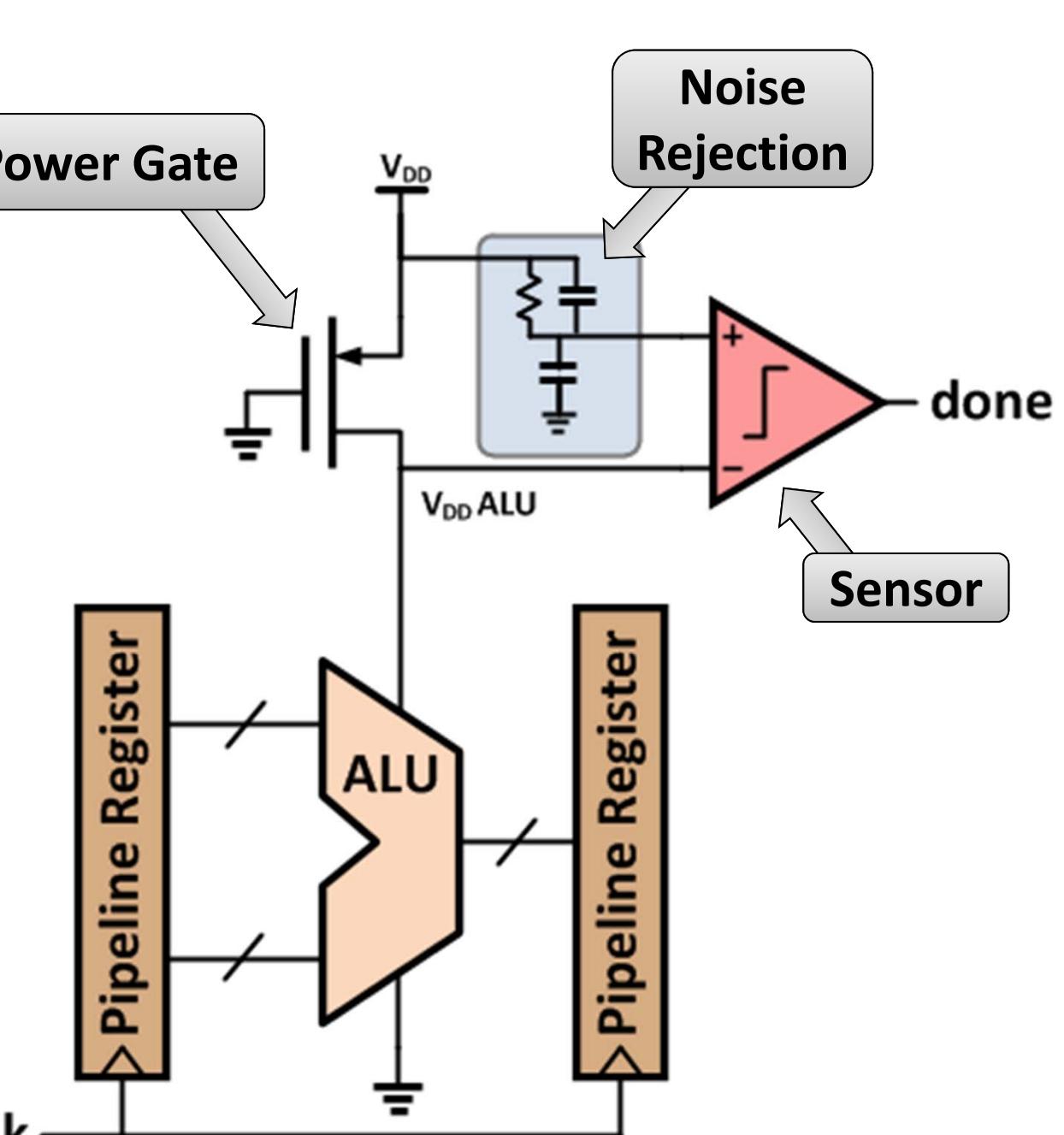
Many different detection techniques can be used to detect completion.

Multiple samples can be averaged after a done signal in order to filter noise-related error

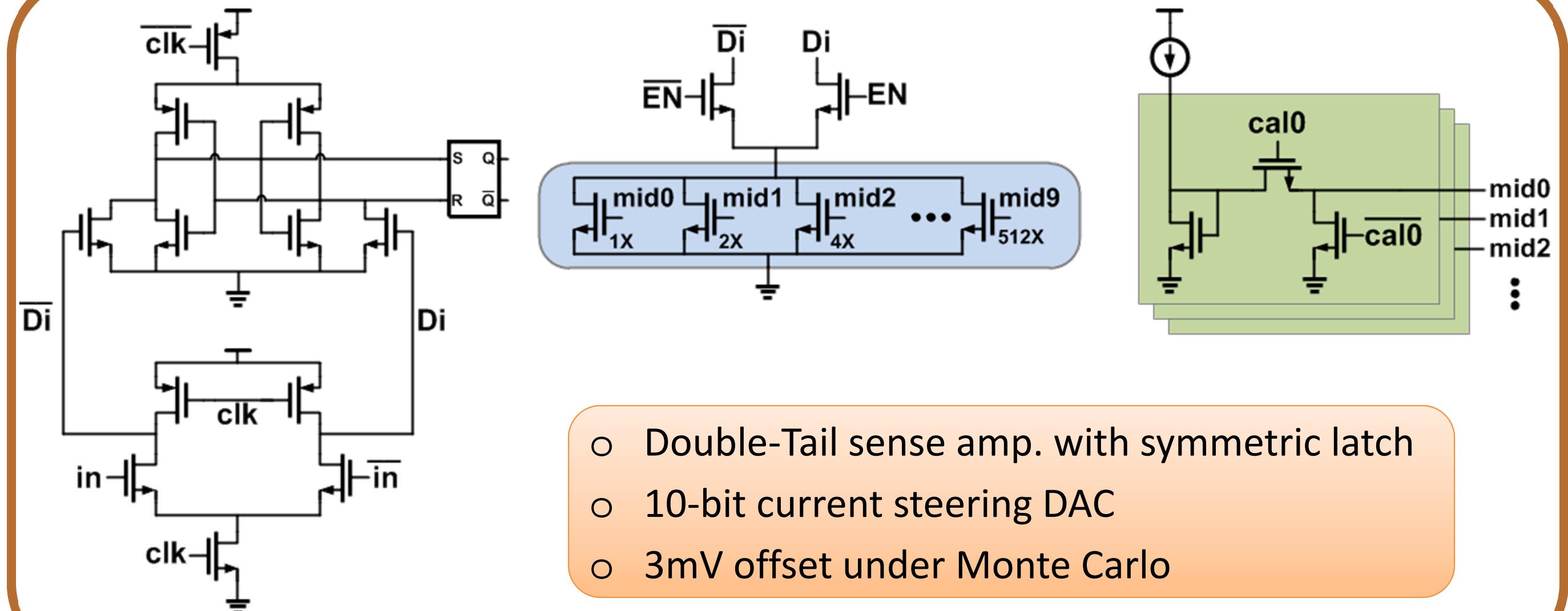


Error Detection Test Chip Design

A simple analog sensor has been designed to detect a change in voltage across a power gate, relative to current consumption.



Current Sensor

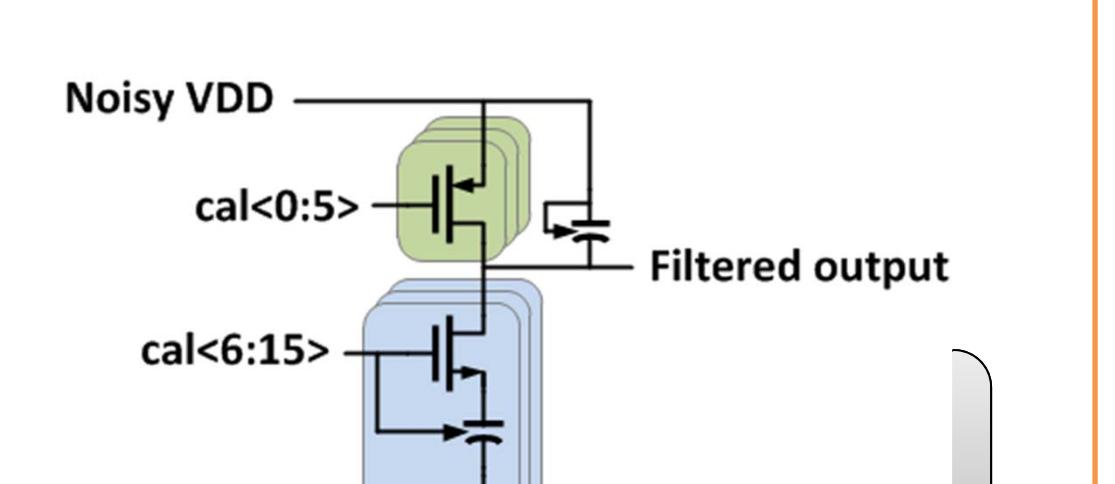


- Double-Tail sense amp. with symmetric latch
- 10-bit current steering DAC
- 3mV offset under Monte Carlo

Noise Rejection Calibration

Noise Matching Circuit

A simple tunable RC network has been designed to match the noise shaping characteristics of the power gate and ALU. If it is matched, the differential inputs to the comparator will have no noise.



Calibration

20mVpp supply noise reduced to less than 300μVpp with proper calibration

