Joseph A. Crop

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OBJECTIVE A successful digital mixed-signal engineer looking to make a big impact

EDUCATION

PhD, Electrical Computer Engineering, Oregon State University (2014)
Concentration: Reliability of ultra low-power digital mixed-signal integrated circuits

BS, Electrical Computer Engineering, Oregon State University (2009)
Minor: Computer Science

EXPERIENCE

Senior Principal Member of Technical Staff: Currently works at *Maxim Integrated* (Now ADI) designing mixed-signal IP for a broad range of applications.

- *Mixed-Signal IP Projects:* Digital calibration of Pipeline and SAR ADCs, Hybrid PLLs, power converters, memory controllers, and process qualification test chips.
- *Product Contributions:* RF-to-bits Hybrid-Radio Receivers, Audio DACs, Next Generation Ultrasound Frontends, Power Converters, ADCs
- *Digital Expertise:* Lead team that architected an automated UVM simulation flow and UVM regmap generation, I2C, SPI, OTP, and other digital IPs that are used in the vast majority new designs across Maxim.

Design Intern: Interned at Intel designing I/O circuits for next-generation server processors in 22nm CMOS. (Summer 2012)

Instructor: Taught ECE 473/573 to a mixed class of senior undergrads and graduate students. The class focused on digital design with SystemVerilog, advanced synthesis techniques, and scripting. (Spring 2013)

Research Intern: Spent the summer as a research intern at Fudan University in Shanghai, China. Research focused on low-power and low-energy encryption engine optimization for integrated RFID systems. (Summer 2011)

Research Assistant: Researched resilient ultra low-power digital circuits and architectures in the VLSI group at OSU (SRC,NSF,DOE,DOD,NSA, and DARPA funded) as well as bio-medical sensor SOCs. (2010 — 2014)

Summer Class Instructor: Taught class of computer science students over summer term. Material included computer architecture concepts, advanced assembly programming, and digital/CMOS logic. (Summer 2010)

Graduate Teaching Assistant: Taught Computer Architecture / EE classes to undergraduate students. Topics range from digital logic and basic computer architecture to advanced CMOS circuit design. (2009 — 2011)

Pre-college Outreach Programs Instructor: Taught web design and other technology-oriented classes to both middle school and high school students through OSU. (2006 — 2014)

TECHNICAL SKILLS

Programming Languages: Java, C, C++, PHP, JavaScript, REST, AJAX, JSON, Android SDK, SQL, HTML, Perl, Python, UNIX/Linux Shell Scripting, Verilog, SystemVerilog, Verilog AMS, UVM, VHDL, Skill, LaTeX, Microsoft Assembly (MASM), AVR Assembly/C/C++/Arduino, TI MSP430 Assembly, SPICE, LabWindows CVI (LabView)

Engineering: Matlab, SPICE/HSIM/NCSIM, Virtuoso/Spectre, Xilinx FPGA Toolset, Sun Grid Engine, ModelSim, Synopsys Design Vision, SoC Encounter (+ CPF/UPF), Altium PCB Design Software, LabView, Focused Ion Bean (FIB)/Scanning Electron Microscope (SEM)

PUBLICATIONS

B. Querbach, R.Khanna, S.Puligundla, D. Blankenbeckler, **J.Crop**, P.Y. Chiang. "Architecture of a Reusable BIST Engine for Detection and Autocorrection of Memory Failures and for IO Debug, Validation, Link Training, and Power Optimization on 14-nm SoC", IEEE Design & Test, 2016

R. Pawlowski, **J. Crop**, M. Cho, J. Tschanz, V. De, T. Fairbanks, H. Quinn, S. Borkar, and P.Y. Chiang, "Characterization of Radiation-Induced SRAM and Logic Soft Errors from 0.33V to 1.0V in 65nm CMOS", CICC, 2014

R. Pawlowski, **J. Crop**, M. Cho, J. Tschanz, V. De, S. Borkar, T. Fairbanks, H. Quinn, P. Chiang "A Reference Design for Effective Characterization of Soft Error Vulnerability of Ultra-low Voltage Logic and Memory Circuits", SELSE Workshop, 2014

Krimer, E.; **Crop, J.**; Erez, M.; and Chiang, P.; "Replication-Free Single-Event Transient (SET) Detection for Eliminating Silent Data Corruption in CMOS Logic," Silicon Errors in Logic - System Effects (SELSE-9), Stanford University, March 2013

Crop, J.; Pawlowski, R.; and Chiang, P.; "Regaining Throughput Using Completion Detection for Error-Resilient, Near-Threshold Logic", DAC, 2012

Chen, C-H; **Crop, J**; Chiang, P; Temes, G; , "A 12-Bit 7 W/Channel 1 Khz/Channel Incremental ADC for Biosensor Interface Circuits" ISCAS 2012

Pawlowski, R; Krimer, E.; **Crop, J**; Postman, J; Chiang, P.; Erez, M.; , "Synctium-I: A 530mV, 10-lane SIMD Processor with Variation Resiliency in 45nm-SOI" ISSCC 2012

Xiao, M; Xiang, S; Wang, J; **Crop,J**; , "Design of a UHF RFID Tag Baseband with the Hummingbird Cryptographic Engine" ASICON 2011

Crop, J.; Krimer, E.; Moezzi-Madani, N.; Pawlowski, R.; Ruggeri, T.; Chiang, P.; Erez, M.; , "Error Detection and Recovery Techniques for Variation-Aware CMOS Computing: A Comprehensive Review." J. Low Power Electron. Appl. 2011, 1, 334-356

Crop, J.; Pawlowski, R.; Moezzi-Madani, N.; Jackson, J.; Chaing, P.; , "Design automation methodology for improving the variability of synthesized digital circuits operating in the sub/near-threshold regime," IGCC, 2011

Moezzi-Madani, N.; Thorolfsson, T.; **Crop, J.**; Chiang, P.; Davis, W.R.; , "An energy efficient 64-QAM MIMO detector for emerging wireless standards," Design, Automation & Test in Europe Conference & Exhibition (DATE) , 2011

Crop, J.; Fairbanks, S.; Pawlowski, R.; Chiang, P.; , "150mV sub-threshold Asynchronous multiplier for low-power sensor applications," VLSI Design Automation and Test (VLSI-DAT), 2010