Test #	Test	ALUCtrl (4 bits)	A (32 bits)	B (32 bits)	W (32 bits)	Zero
1	ADD 0, 0	2	0x00000000	0x00000000	0x00000000	1
2	ADD 0, −1	2	0x00000000	0xFFFFFFFF	0xFFFFFFFF	0
3	ADD −1, 1	2	0xFFFFFFFF	0x00000001	0x00000000	1
4	ADD *FF*, 1	2	0x000000FF	Øx1	Øx100	Ø
5	SUB 0, 0	6	0x00000000	0x00000000	0x00000000	1
6	SUB 1, −1	6	Øx1	ØFFFFFFF	0x2	0
7	SUB 1, 1	6	Øx1	Øx1	0x00000000	1
8	SLT 0, 0	7	0x00000000	0x00000000	0x00000000	1
9	SLT 0, 1	7	ØxØ	Øx1	0x00000001	0
10	SLT 0, −1	7	ØxO	ØxFFFFFFFF	0x00000000	1
11	SLT 1, 0	7	1	0	0x00000000	1
12	SLT −1, 0	7	0xFFFFFFFF	ØxØ	Øx1	0
13	AND 0xFFFFFFFF, 0xFFFFFFFF	Ø	0xFFFFFFFF	0xFFFFFFFF	0xFFFFFFFF	0
14	AND 0xFFFFFFFF, 0xCAFEBABE	Ø	0xFFFFFFFF	0xCAFEBABE	0xCAFEBABE	0
15	AND 0x00000000, 0xFFFFFFFF	Ø	0x00000000	0xFFFFFFFF	0x00000000	1
16	AND 0x12345678, 0x87654321	Ø	0x12345678	0x87654321	2200220	0
17	OR 0xF0F0F0F0, 0x0000FFFF	1	0xF0F0F0F0	0x0000FFFF	F0F0FFFF	0
18	OR 0x12345678, 0x87654321	1	0x12345678	0x87654321	7FFFFFFF	0
19	SLL 0x12345678,0x2	3	0x12345678	0x00000002	48D15E0	Ø
20	SLL 0x80000000,0x3	3	0x80000000	Øx3	20000000	Ø
21	SRL 0x00000001,0x3	4	0x00000001	0x00000003	Øx0	1
22	SRL 0x00001234,0x6	4	0x00001234	0x00000006	Øx48	Ø

Tab. 1: ALU Test Vectors

11. During the in-lab, you will be implementing the ALU block. As part of the design process, you need to develop an appropriate set of test vectors to verify basic functionality. Complete Table 1 (submit hardcopy or via email) to verify that all 7 ALU operations work as designed. Note that all values are expressed in **hexadecimal**. You will use this table to test the ALU Verilog code that you will implement during the in-lab (**make sure to keep a copy of your submitted answers**) .