# Lab 10

Hazard Unit Design

# What is hazard unit?

- No structural hazard.
- Only data and control hazards.
- FSM (Finite State Machine) that generates 3 signals (PCWrite, IFWriet, Bubble)

# Data Hazards

- Need to keep destination register of past 3 instruction.
- Compare with current register $R_A$ and $R_B$.
- Never have a hazard from $0.
- If $R_A$ or $R_B$ are not being used set them to 0.
- Immediate type of instruction RB is valid?

# Data Hazards (Bubble)

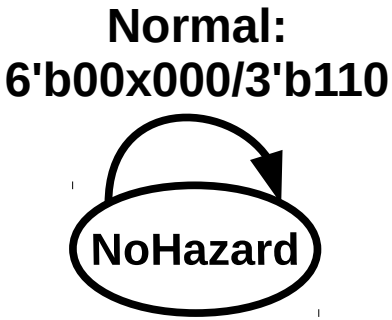
- Bubble should be 1 if current instruction is reading one of the registers that was destination by previous any of the previous three instructions.
- Hold Bubble high for appropriate amount of time.
- If cmp1=1 then generate 3 cycles of bubble.
- If cmp2=1 then generate 2 cycles of bubble.
- If cmp3=1 then generate 1 cycle of bubble.
- If Bubble is one the current instruction is not to be executed until Bubble is set to 0. (PCWrite=IFWrite=0)

```
cmp1 = (((rs==rw1)||(rt==rw1))&&(rw1!= 0)) ? 1:0
cmp2 = (((rs==rw2)||(rt==rw2))&&(rw2!= 0)) ? 1:0
cmp3 = (((rs==rw3)||(rt==rw3))&&(rw3!= 0)) ? 1:0
```

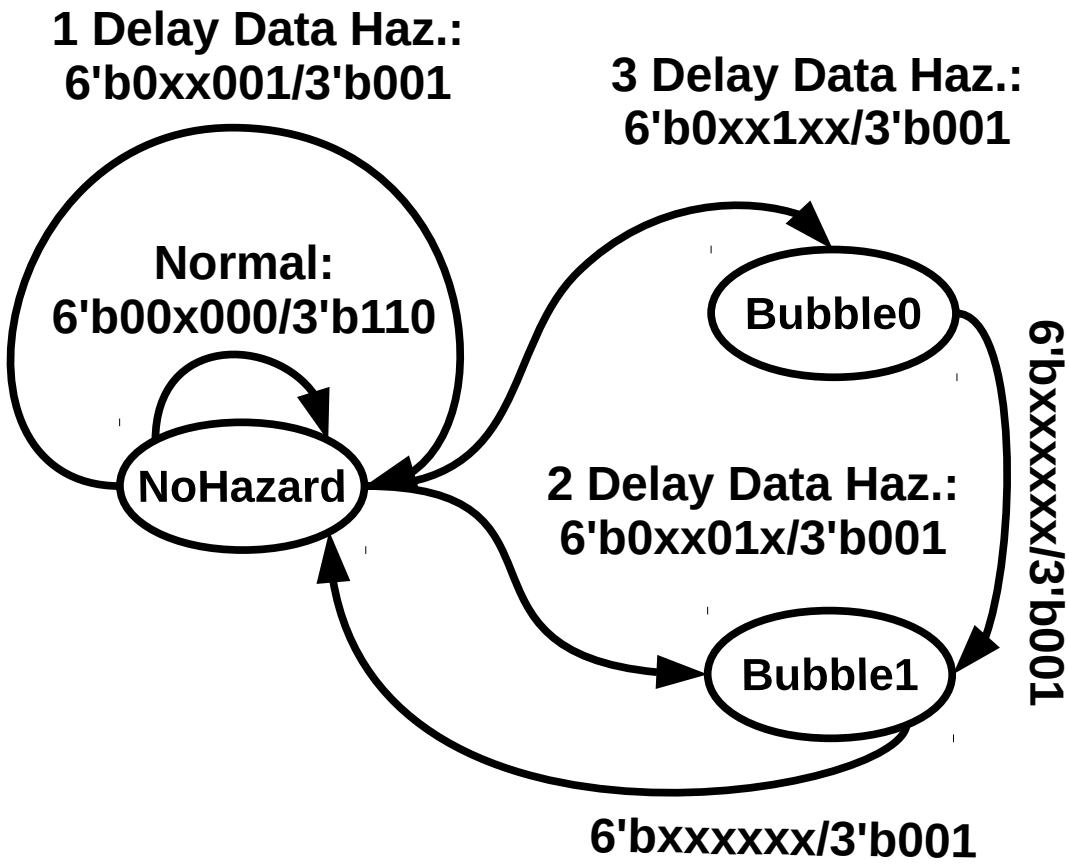
# Control Hazards

- Use PCWrite and IFWrite to handle the hazard.
- If Jump=1 then PCWrite=0 for 1 cycles.
- If Branch=1 then PCWrite=0 for 2 cycles.
- IFWrite must be 0 for one additional cycle than PCWrite unless the instruction is a branch, and branch is **Not taken**.
- Pay attention to signal priorities.

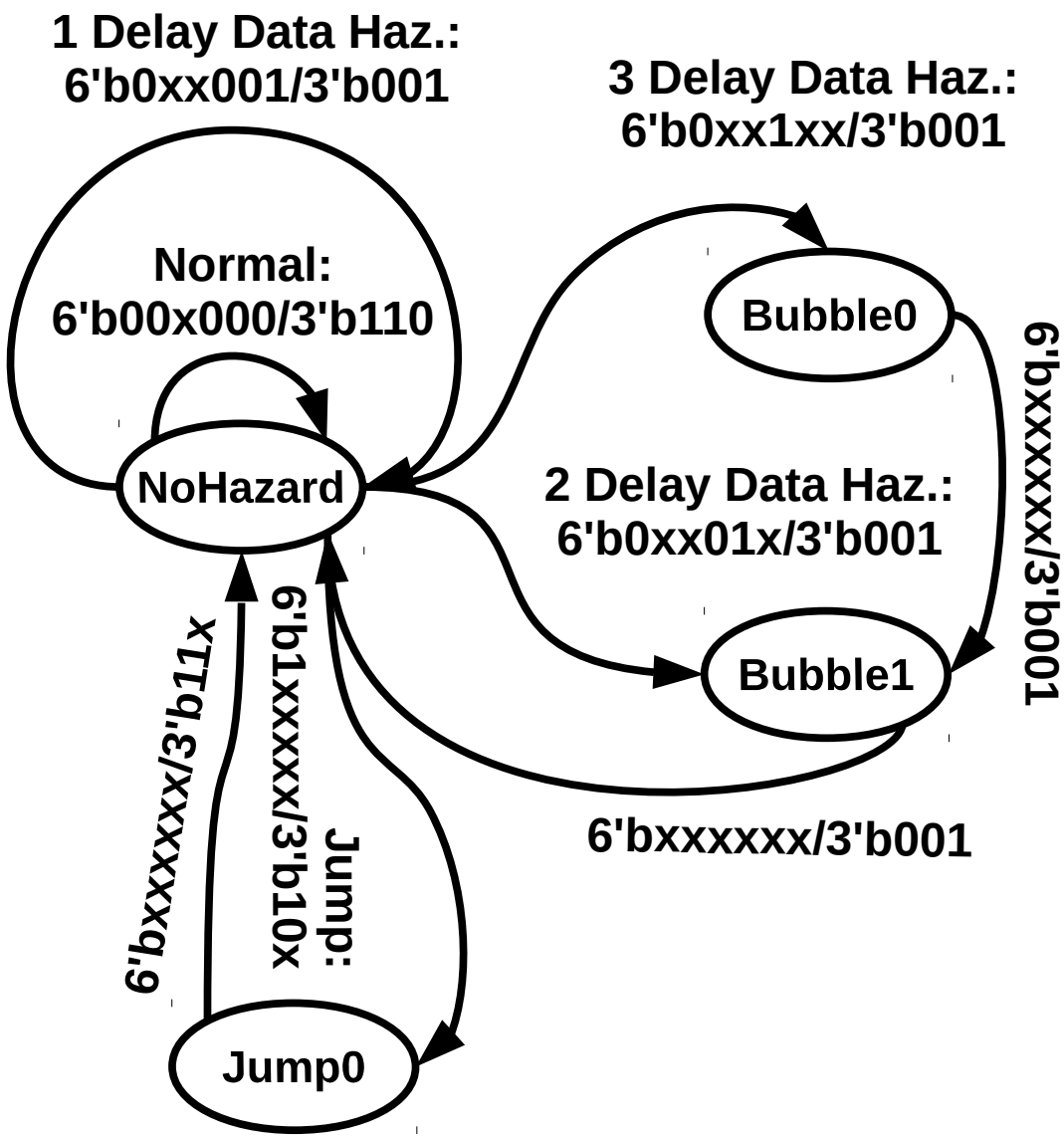
**{Jump,Branch,ALUZero4,Comp1,Comp2,Comp3}/{PCWrite,IFWrite,Bubble}**

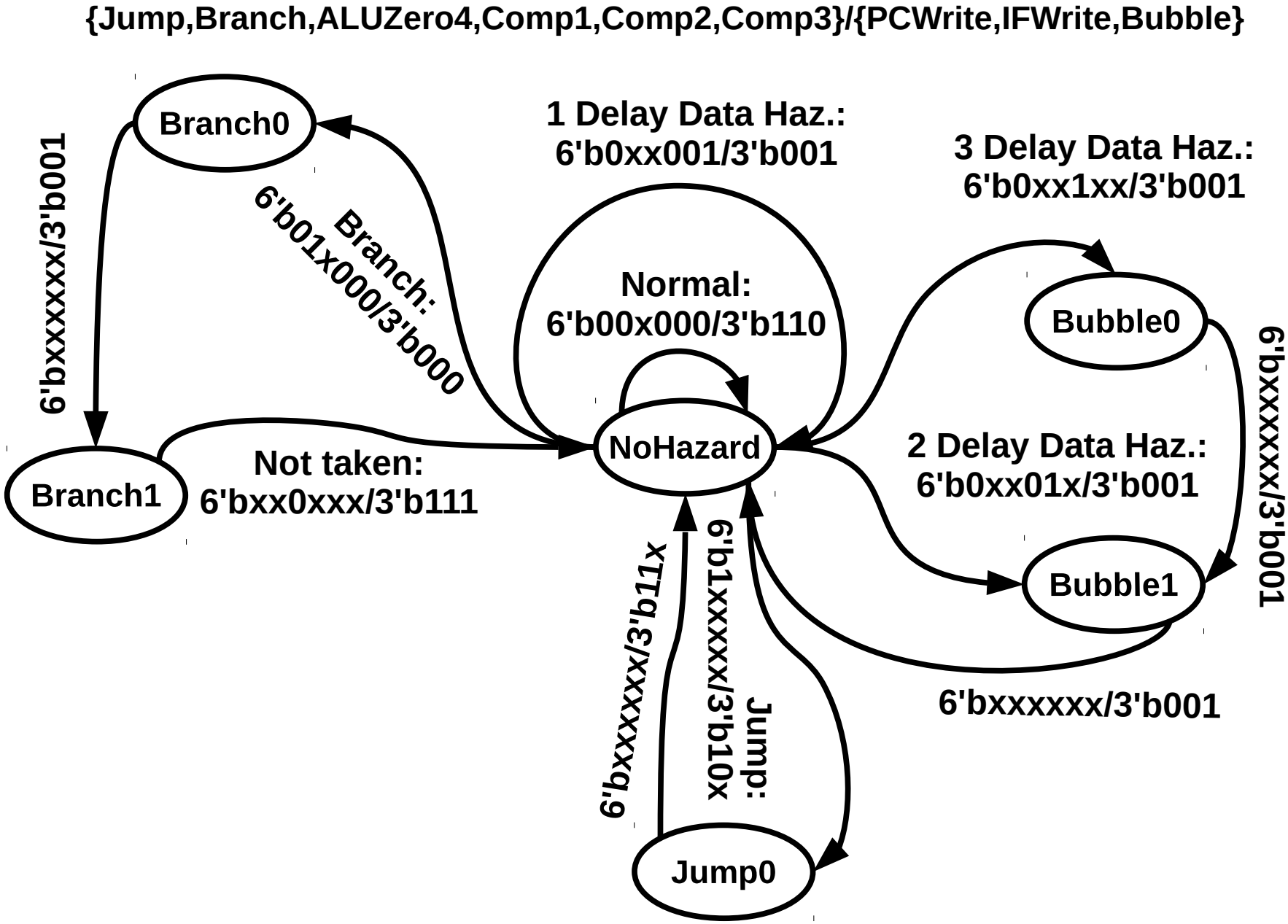


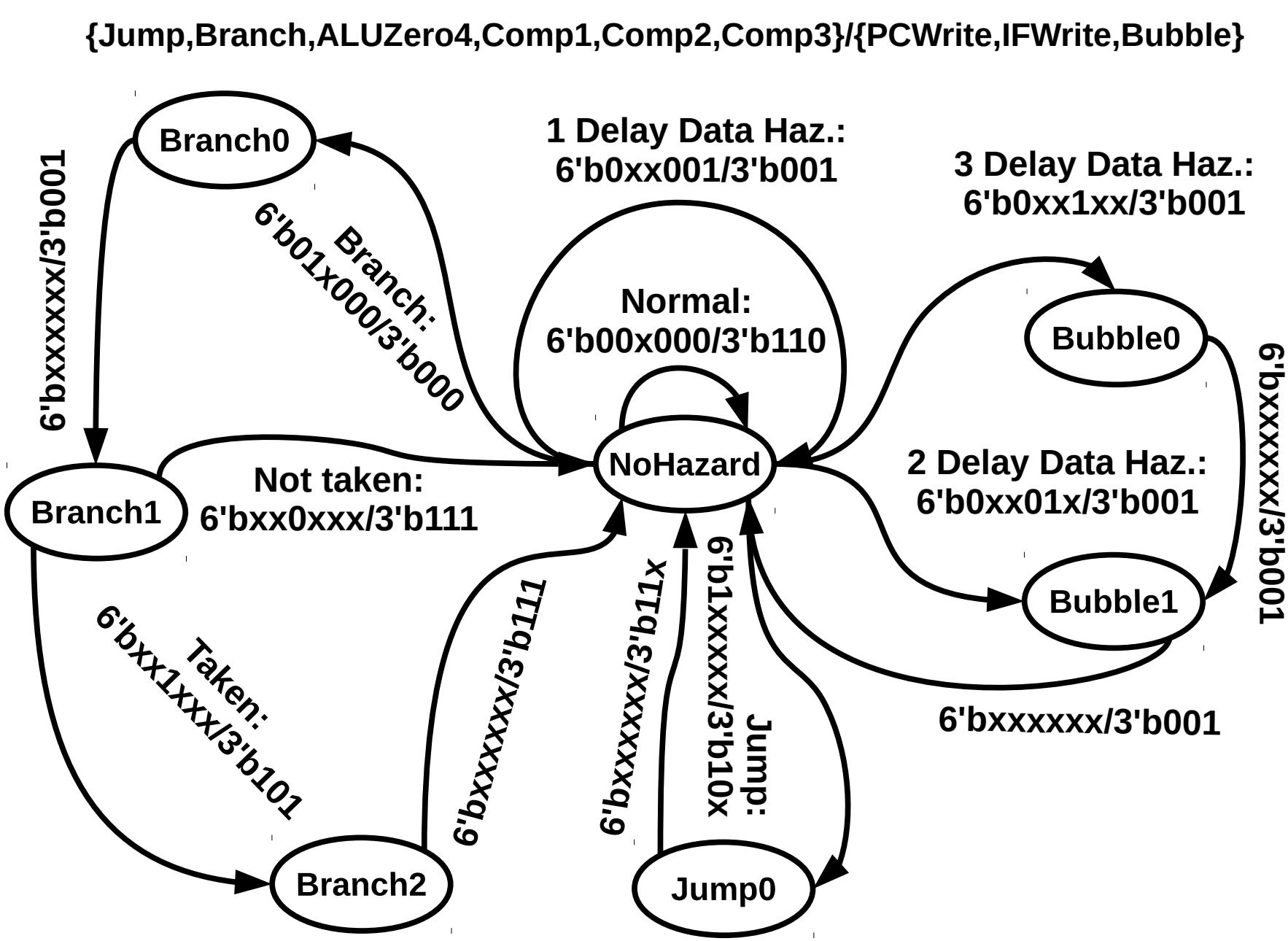
**{Jump,Branch,ALUZero4,Comp1,Comp2,Comp3}/{PCWrite,IFWrite,Bubble}**



**{Jump,Branch,ALUZero4,Comp1,Comp2,Comp3}/{PCWrite,IFWrite,Bubble}**




{Jump,Branch,ALUZero4,Comp1,Comp2,Comp3}/{PCWrite,IFWrite,Bubble}
Branch0
Branch1
NoHazard
Bubble0
Bubble1
Jump0
6'bxxxxxx/3'b001
Branch:
6'b01x000/3'b000
1 Delay Data Haz.:
6'b0xx001/3'b001
Normal:
6'b00x000/3'b110
3 Delay Data Haz.:
6'b0xx1xx/3'b001
2 Delay Data Haz.:
6'b0xx01x/3'b001
6'bxxxxxx/3'b001
Not taken:
6'bxx0xxx/3'b111
6'bxxxxxx/3'b11x
6'b1xxxxx/3'b10x
Jump:
6'bxxxxxx/3'b001


{Jump,Branch,ALUZero4,Comp1,Comp2,Comp3}/{PCWrite,IFWrite,Bubble}
Branch0
1 Delay Data Haz.:
6'b0xx001/3'b001
3 Delay Data Haz.:
6'b0xx1xx/3'b001
6'bxxxxxx/3'b001
Branch:
6'b01x000/3'b000
Normal:
6'b00x000/3'b110
Bubble0
NoHazard
2 Delay Data Haz.:
6'b0xx01x/3'b001
Branch1
Not taken:
6'bxx0xxx/3'b111
Bubble1
Taken:
6'bxx1xxx/3'b101
6'bxxxxxx/3'b111
6'bxxxxxx/3'b11x
6'b1xxxxx/3'b10x
Jump:
6'bxxxxxx/3'b001
Branch2
Jump0