Experiment 10: The RISC-Y Processor

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ECE 526/Lab

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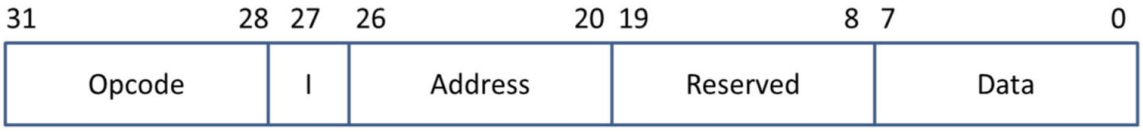
I. Purpose

In this experiment, a simplified, reduced instruction set computer (RISC) is designed utilizing the modules created in previous experiments. This is not a pipelined design and as such, the RISC machine requires 4 clock periods to perform each instruction due to the 4 cycle design; FETCH, DECODE, EXECUTE, and UPDATE. There is a single instruction format that is represented in the following figure:



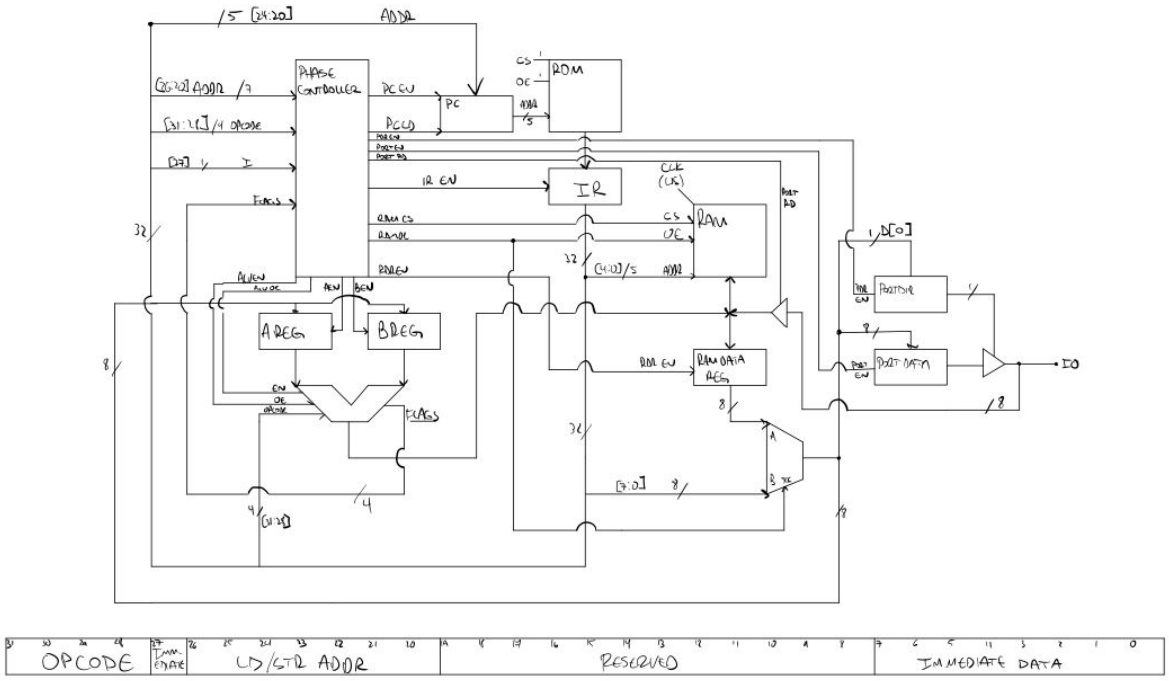
This design is capable of performing the following operations; load, store, add, subtract, and, or, exclusive-or, not, branch unconditionally, branch if zero, branch if negative, branch if overflow, and branch if carry. These are mapped to the following binary codes:

MNEMONIC	INSTRUCTION	OPCODE
LOAD	Load a register	4'b0000
STORE	Store ALU Output	4'b0001
ADD	Add A and B	4'b0010
SUB	Subtract B from A	4'b0011
AND	Bitwise AND of A and B	4'b0100
OR	Bitwise OR of A and B	4'b0101
XOR	Bitwise XOR of A and B	4'b0110
NOT	Bitwise inversion of A	4'b0111
B	Unconditional Branch	4'b1000
BZ	Branch if Z flag is set	4'b1001
BN	Branch if N flag is set	4'b1010
BV	Branch if OVF flag is set	4'b1011
BC	Branch if C flag is set	4'b1100

The instructions in this design are stored on read-only memory, which drives the operations on 8-bit numbers from either direct addressing, or immediate values. ROM is sized at 32-bits x 32-bits and the RAM is 8-bits x 32-bits. The memories are mapped to the following addresses:

Decimal Address	Device
0-31	ROM
32-63	RAM
64	ALU A Register
65	ALU B Register
66	Port Direction Register
67	I/O Port

II. Methodology



To better understand the complete system, a schematic was constructed which provided a full overview of the datapath, control path, and components required, as seen in the figure above. With this schematic, a top level was created, and each component was instantiated, beginning with an asynchronous assert, synchronous deassert reset. A scalable, resettable register and non-resettable register were created, along with a simple tristate buffer for the IO components. The control unit was then placed in the top level and the control signals were created.

With the control unit in place, I instantiated each subsequent component in a clockwise manner in relation to the schematic, with the IO logic being the final component set added. It was determined that the following registers needed a reset; A, B, PC, and the port direction register. And the remaining were coded without.

As the specification stated that the bidirectional bus should never be allowed to float, the PORT_RD signal was used as the default “on” for the bus, and was subsequently turned off when other components needed to interface. Upon completing the wiring in the top level, there

were a few minor changes made to the existing ALU, ROM, and RAM modules. These changes included changing from a clocked output of each, to a combinational output.

To test the machine, a program was written in hexadecimal and was read into the ROM using the verilog directive $readmemh(). A simple test bench was then constructed to generate a clock and the 2 initial IO values. To determine the clock runtime, the number of instructions in the program were multiplied by 4 times the clock pulse, which was set at 100ns. The program was then run till completion and the output logged in a log file. The program, as loaded in the ROM can be seen in the following table:

ROM Hex Address	Mnemonic Instruction	Hex Instruction
00	STORE IO, RAM[0]	1430 0000
01	STORE IO, RAM[1]	1430 0001
02	LOAD A, RAM[0]	0400 0000
03	LOAD B, RAM[1]	0410 0001
04	ADD A, B	2000 0000
05	STORE (A+B), RAM[2]	1000 0002
06	BN PC, 0x08	A080 0000
07	-	-
08	LOAD IMMEDIATE B, 1	0C10 0001
09	SUB A, B	3000 0000
0A	STR (A-B), RAM[3]	1000 0003
0B	BZ PC, 0x0F	90F0 0000
0C	-	-
0D	-	-
0E	-	-
0F	LOAD A, RAM[2]	0400 0002
10	AND A, B	4000 0000
11	OR A, B	5000 0000
12	XOR A, B	6000 0000

13	NOT A	7000 0000
14	B PC, 0x16	8160 0000
15	-	-
16	LOAD IMMEDIATE PDR, 1	0C20 0001
17	LOAD IMMEDIATE A, 255	0C00 00FF
18	LOAD IMMEDIATE B, 127	0C10 007F
19	ADD A, B	2000 0000
1A	BC PC, 0x1B	C1B0 0000
1B	LOAD IMMEDIATE A, 127	0C00 007F
1C	ADD A, B	2000 0000
1D	BV PC, 0x1E	B1E0 0000
1E	LOAD IMMEDIATE IO, 42	0C30 002A
1F	-	

III. Results / Analysis

Each instruction is given in its mnemonic, hexadecimal, and binary forms as a header to the 4 cycle output of each instruction in the test suit.

Note: This section contains only the posedge CLK output of each phase per instruction, for brevity.

STR IO, RAM[0]
0x1430 0000

0	0	0	1	x	1	0	0	0	0	1	1	x	x	x	x	x	x	x	x	x	x	x	0	0	0	0	0	0	0	0

```
TIME = 150
CONTROL:   CLK=1    RST_=1
OPERATION: INSTRUCTION=[0001][0][1000011][000000000000][00000000]
           PHASE=FETCH  OPCODE=0001 ADDR=[00]00000  I_DATA=[0]00000000
```

```
STORAGE:    MEM[0]=x MEM[1]=x     MEM[2]=x
REGISTERS: A_REG=0   B_REG=0      RDR_REG=x    DIR_REG=0    PORT_REG=x
SIGNALS:    RAMDATA=1     ALUOUT=z     BUS=00000001
FLAGS:      CF=x ZF=x     SF=x     OF=x     IF=0
CONTROLS:   IR_EN=1   A_EN=0   B_EN=0   PDR_EN=0     PORT_EN=0    PORT_RD=1
            PC_EN=0   PC_LOAD=0    ALU_EN=0     ALU_OE=0     RAM_OE=0     RDR_EN=0
RAM_CS=1
I/O:        IO=[1]00000001
```

```
TIME = 250
CONTROL:    CLK=1     RST_=1
OPERATION: INSTRUCTION=[0001][0][1000011][000000000000][00000000]
           PHASE=DECODE OPCODE=0001 ADDR=[00]00000   I_DATA=[0]00000000
STORAGE:    MEM[0]=x MEM[1]=x     MEM[2]=x
REGISTERS: A_REG=0   B_REG=0      RDR_REG=x    DIR_REG=0    PORT_REG=x
SIGNALS:    RAMDATA=1     ALUOUT=z     BUS=00000001
FLAGS:      CF=x ZF=x     SF=x     OF=x     IF=0
CONTROLS:   IR_EN=0   A_EN=0   B_EN=0   PDR_EN=0     PORT_EN=0    PORT_RD=1
           PC_EN=0   PC_LOAD=0    ALU_EN=0     ALU_OE=0     RAM_OE=0     RDR_EN=0
RAM_CS=0
I/O:        IO=[1]00000001
```

```
TIME = 350
CONTROL:    CLK=1     RST_=1
OPERATION: INSTRUCTION=[0001][0][1000011][000000000000][00000000]
           PHASE=EXECUTE     OPCODE=0001 ADDR=[00]00000   I_DATA=[0]00000000
STORAGE:    MEM[0]=1 MEM[1]=x     MEM[2]=x
REGISTERS: A_REG=0   B_REG=0      RDR_REG=x    DIR_REG=0    PORT_REG=x
SIGNALS:    RAMDATA=1     ALUOUT=z     BUS=00000001
FLAGS:      CF=x ZF=x     SF=x     OF=x     IF=0
CONTROLS:   IR_EN=0   A_EN=0   B_EN=0   PDR_EN=0     PORT_EN=0    PORT_RD=1
           PC_EN=0   PC_LOAD=0    ALU_EN=0     ALU_OE=0     RAM_OE=0     RDR_EN=0
RAM_CS=0
I/O:        IO=[1]00000001
```

```
TIME = 450
CONTROL:    CLK=1     RST_=1
OPERATION: INSTRUCTION=[0001][0][1000011][000000000000][00000000]
           PHASE=UPDATE OPCODE=0001 ADDR=[00]00000   I_DATA=[0]00000000
```

```
STORAGE:    MEM[0]=1 MEM[1]=x     MEM[2]=x
REGISTERS: A_REG=0   B_REG=0      RDR_REG=x    DIR_REG=0    PORT_REG=x
SIGNALS:    RAMDATA=1     ALUOUT=z     BUS=00000001
FLAGS:      CF=x ZF=x     SF=x     OF=x     IF=0
CONTROLS:   IR_EN=0   A_EN=0   B_EN=0   PDR_EN=0     PORT_EN=0    PORT_RD=1
           PC_EN=1   PC_LOAD=0    ALU_EN=0     ALU_OE=0     RAM_OE=0     RDR_EN=0
RAM_CS=1
I/O:        IO=[1]00000001
```

STR IO, RAM[1]
0x1430 0001

0	0	0	1	x	1	0	0	0	0	1	1	x	x	x	x	x	x	x	x	x	x	x	0	0	0	0	0	0	0	1

```
TIME = 550
CONTROL:    CLK=1     RST_=1
OPERATION: INSTRUCTION=[0001][0][1000011][000000000000][00000000]
           PHASE=FETCH   OPCODE=0001 ADDR=[01]00001   I_DATA=[0]00000000
STORAGE:    MEM[0]=1 MEM[1]=x     MEM[2]=x
REGISTERS: A_REG=0   B_REG=0      RDR_REG=x    DIR_REG=0    PORT_REG=x
SIGNALS:    RAMDATA=128   ALUOUT=z     BUS=10000000
FLAGS:      CF=x ZF=x     SF=x     OF=x     IF=0
CONTROLS:   IR_EN=1   A_EN=0   B_EN=0   PDR_EN=0     PORT_EN=0    PORT_RD=1
           PC_EN=0   PC_LOAD=0    ALU_EN=0     ALU_OE=0     RAM_OE=0     RDR_EN=0
RAM_CS=1
I/O:        IO=[128]10000000
```

```
TIME = 650
CONTROL:    CLK=1     RST_=1
OPERATION: INSTRUCTION=[0001][0][1000011][000000000000][00000001]
           PHASE=DECODE OPCODE=0001 ADDR=[01]00001   I_DATA=[1]00000001
STORAGE:    MEM[0]=1 MEM[1]=x     MEM[2]=x
REGISTERS: A_REG=0   B_REG=0      RDR_REG=x    DIR_REG=0    PORT_REG=x
SIGNALS:    RAMDATA=128   ALUOUT=z     BUS=10000000
FLAGS:      CF=x ZF=x     SF=x     OF=x     IF=0
CONTROLS:   IR_EN=0   A_EN=0   B_EN=0   PDR_EN=0     PORT_EN=0    PORT_RD=1
```

```
          PC_EN=0   PC_LOAD=0    ALU_EN=0     ALU_OE=0     RAM_OE=0     RDR_EN=0
RAM_CS=0
I/O:        IO=[128]10000000
```

```
TIME = 750
CONTROL:    CLK=1     RST_=1
OPERATION: INSTRUCTION=[0001][0][1000011][000000000000][00000001]
           PHASE=EXECUTE     OPCODE=0001 ADDR=[01]00001   I_DATA=[1]00000001
STORAGE:    MEM[0]=1 MEM[1]=128   MEM[2]=x
REGISTERS: A_REG=0   B_REG=0      RDR_REG=x    DIR_REG=0    PORT_REG=x
SIGNALS:    RAMDATA=128   ALUOUT=z     BUS=10000000
FLAGS:      CF=x ZF=x     SF=x     OF=x     IF=0
CONTROLS:   IR_EN=0   A_EN=0   B_EN=0   PDR_EN=0     PORT_EN=0    PORT_RD=1
           PC_EN=0   PC_LOAD=0    ALU_EN=0     ALU_OE=0     RAM_OE=0     RDR_EN=0
RAM_CS=0
I/O:        IO=[128]10000000
```

```
TIME = 850
CONTROL:    CLK=1     RST_=1
OPERATION: INSTRUCTION=[0001][0][1000011][000000000000][00000001]
           PHASE=UPDATE OPCODE=0001 ADDR=[01]00001   I_DATA=[1]00000001
STORAGE:    MEM[0]=1 MEM[1]=128   MEM[2]=x
REGISTERS: A_REG=0   B_REG=0      RDR_REG=x    DIR_REG=0    PORT_REG=x
SIGNALS:    RAMDATA=128   ALUOUT=z     BUS=10000000
FLAGS:      CF=x ZF=x     SF=x     OF=x     IF=0
CONTROLS:   IR_EN=0   A_EN=0   B_EN=0   PDR_EN=0     PORT_EN=0    PORT_RD=1
           PC_EN=1   PC_LOAD=0    ALU_EN=0     ALU_OE=0     RAM_OE=0     RDR_EN=0
RAM_CS=1
I/O:        IO=[128]10000000
```

LD A, RAM[0]
0x0400 0000

0	0	0	0	0	1	0	0	0	0	0	0	x	x	x	x	x	x	x	x	x	x	x	0	0	0	0	0	0	0	0

```
TIME = 950
CONTROL:   CLK=1    RST_=1
OPERATION: INSTRUCTION=[0001][0][1000011][000000000000][00000001]
           PHASE=FETCH  OPCODE=0001 ADDR=[02]00010  I_DATA=[1]00000001
STORAGE:   MEM[0]=1 MEM[1]=128  MEM[2]=x
REGISTERS: A_REG=0  B_REG=0     RDR_REG=x   DIR_REG=0   PORT_REG=x
SIGNALS:   RAMDATA=128  ALUOUT=z    BUS=10000000
FLAGS:     CF=x ZF=x    SF=x    OF=x    IF=0
CONTROLS:  IR_EN=1  A_EN=0  B_EN=0  PDR_EN=0    PORT_EN=0   PORT_RD=1
           PC_EN=0  PC_LOAD=0   ALU_EN=0    ALU_OE=0    RAM_OE=0    RDR_EN=0
RAM_CS=1
I/O:       IO=[128]10000000
```

```
TIME = 1050
CONTROL:   CLK=1    RST_=1
OPERATION: INSTRUCTION=[0000][0][1000000][000000000000][00000000]
           PHASE=DECODE OPCODE=0000 ADDR=[02]00010  I_DATA=[x]xxxxxxxx
STORAGE:   MEM[0]=1 MEM[1]=128  MEM[2]=x
REGISTERS: A_REG=0  B_REG=0     RDR_REG=x   DIR_REG=0   PORT_REG=x
SIGNALS:   RAMDATA=1    ALUOUT=z    BUS=00000001
FLAGS:     CF=x ZF=x    SF=x    OF=x    IF=0
CONTROLS:  IR_EN=0  A_EN=1  B_EN=0  PDR_EN=0    PORT_EN=0   PORT_RD=0
           PC_EN=0  PC_LOAD=0   ALU_EN=0    ALU_OE=0    RAM_OE=1    RDR_EN=1
RAM_CS=0
I/O:       IO=[128]10000000
```

```
TIME = 1150
CONTROL:   CLK=1    RST_=1
OPERATION: INSTRUCTION=[0000][0][1000000][000000000000][00000000]
           PHASE=EXECUTE    OPCODE=0000 ADDR=[02]00010  I_DATA=[1]00000001
STORAGE:   MEM[0]=1 MEM[1]=128  MEM[2]=x
REGISTERS: A_REG=x  B_REG=0     RDR_REG=1   DIR_REG=0   PORT_REG=x
SIGNALS:   RAMDATA=1    ALUOUT=z    BUS=00000001
FLAGS:     CF=x ZF=x    SF=x    OF=x    IF=0
CONTROLS:  IR_EN=0  A_EN=1  B_EN=0  PDR_EN=0    PORT_EN=0   PORT_RD=0
           PC_EN=0  PC_LOAD=0   ALU_EN=0    ALU_OE=0    RAM_OE=1    RDR_EN=1
RAM_CS=0
```

```
I/O:        IO=[128]10000000
```

```
TIME = 1250
CONTROL:    CLK=1     RST_=1
OPERATION:  INSTRUCTION=[0000][0][1000000][000000000000][00000000]
            PHASE=UPDATE OPCODE=0000 ADDR=[02]00010   I_DATA=[0]00000000
STORAGE:    MEM[0]=1 MEM[1]=128   MEM[2]=x
REGISTERS:  A_REG=1   B_REG=0      RDR_REG=1    DIR_REG=0    PORT_REG=x
SIGNALS:    RAMDATA=128   ALUOUT=z     BUS=10000000
FLAGS:      CF=x ZF=x     SF=x     OF=x     IF=0
CONTROLS:   IR_EN=0   A_EN=0   B_EN=0   PDR_EN=0     PORT_EN=0    PORT_RD=1
            PC_EN=1   PC_LOAD=0    ALU_EN=0     ALU_OE=0     RAM_OE=0     RDR_EN=0
RAM_CS=1
I/O:        IO=[128]10000000
```

LD B, RAM[1]
0x0410 0001

0	0	0	0	0	1	0	0	0	0	0	1	x	x	x	x	x	x	x	x	x	x	x	0	0	0	0	0	0	0	1

```
TIME = 1350
CONTROL:    CLK=1     RST_=1
OPERATION:  INSTRUCTION=[0000][0][1000000][000000000000][00000000]
            PHASE=FETCH   OPCODE=0000 ADDR=[03]00011   I_DATA=[0]00000000
STORAGE:    MEM[0]=1 MEM[1]=128   MEM[2]=x
REGISTERS:  A_REG=1   B_REG=0      RDR_REG=1    DIR_REG=0    PORT_REG=x
SIGNALS:    RAMDATA=128   ALUOUT=z     BUS=10000000
FLAGS:      CF=x ZF=x     SF=x     OF=x     IF=0
CONTROLS:   IR_EN=1   A_EN=0   B_EN=0   PDR_EN=0     PORT_EN=0    PORT_RD=1
            PC_EN=0   PC_LOAD=0    ALU_EN=0     ALU_OE=0     RAM_OE=0     RDR_EN=0
RAM_CS=1
I/O:        IO=[128]10000000
```

```
TIME = 1450
CONTROL:    CLK=1     RST_=1
```

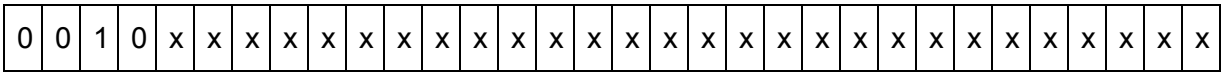
```
OPERATION: INSTRUCTION=[0000][0][1000001][000000000000][00000001]
           PHASE=DECODE OPCODE=0000 ADDR=[03]00011  I_DATA=[1]00000001
STORAGE:   MEM[0]=1 MEM[1]=128  MEM[2]=x
REGISTERS: A_REG=1  B_REG=0     RDR_REG=1   DIR_REG=0   PORT_REG=x
SIGNALS:   RAMDATA=128  ALUOUT=z    BUS=10000000
FLAGS:     CF=x ZF=x    SF=x    OF=x    IF=0
CONTROLS:  IR_EN=0  A_EN=0  B_EN=1  PDR_EN=0    PORT_EN=0   PORT_RD=0
           PC_EN=0  PC_LOAD=0   ALU_EN=0    ALU_OE=0    RAM_OE=1    RDR_EN=1
RAM_CS=0
I/O:       IO=[128]10000000
```

```
TIME = 1550
CONTROL:   CLK=1    RST_=1
OPERATION: INSTRUCTION=[0000][0][1000001][000000000000][00000001]
           PHASE=EXECUTE    OPCODE=0000 ADDR=[03]00011  I_DATA=[128]10000000
STORAGE:   MEM[0]=1 MEM[1]=128  MEM[2]=x
REGISTERS: A_REG=1  B_REG=1     RDR_REG=128 DIR_REG=0   PORT_REG=x
SIGNALS:   RAMDATA=128  ALUOUT=z    BUS=10000000
FLAGS:     CF=x ZF=x    SF=x    OF=x    IF=0
CONTROLS:  IR_EN=0  A_EN=0  B_EN=1  PDR_EN=0    PORT_EN=0   PORT_RD=0
           PC_EN=0  PC_LOAD=0   ALU_EN=0    ALU_OE=0    RAM_OE=1    RDR_EN=1
RAM_CS=0
I/O:       IO=[128]10000000
```

```
TIME = 1650
CONTROL:   CLK=1    RST_=1
OPERATION: INSTRUCTION=[0000][0][1000001][000000000000][00000001]
           PHASE=UPDATE OPCODE=0000 ADDR=[03]00011  I_DATA=[1]00000001
STORAGE:   MEM[0]=1 MEM[1]=128  MEM[2]=x
REGISTERS: A_REG=1  B_REG=128   RDR_REG=128 DIR_REG=0   PORT_REG=x
SIGNALS:   RAMDATA=128  ALUOUT=z    BUS=10000000
FLAGS:     CF=x ZF=x    SF=x    OF=x    IF=0
CONTROLS:  IR_EN=0  A_EN=0  B_EN=0  PDR_EN=0    PORT_EN=0   PORT_RD=1
           PC_EN=1  PC_LOAD=0   ALU_EN=0    ALU_OE=0    RAM_OE=0    RDR_EN=0
RAM_CS=1
I/O:       IO=[128]10000000
```

ADD A, B

0x2000 0000




```
TIME = 1750
CONTROL:    CLK=1     RST_=1
OPERATION: INSTRUCTION=[0000][0][1000001][000000000000][00000001]
           PHASE=FETCH   OPCODE=0000 ADDR=[04]00100   I_DATA=[1]00000001
STORAGE:    MEM[0]=1 MEM[1]=128   MEM[2]=x
REGISTERS: A_REG=1   B_REG=128    RDR_REG=128 DIR_REG=0    PORT_REG=x
SIGNALS:    RAMDATA=128   ALUOUT=z     BUS=10000000
FLAGS:      CF=x ZF=x     SF=x     OF=x     IF=0
CONTROLS:   IR_EN=1   A_EN=0   B_EN=0   PDR_EN=0     PORT_EN=0    PORT_RD=1
           PC_EN=0   PC_LOAD=0    ALU_EN=0     ALU_OE=0     RAM_OE=0     RDR_EN=0
RAM_CS=1
I/O:        IO=[128]10000000
```

```
TIME = 1850
CONTROL:    CLK=1     RST_=1
OPERATION: INSTRUCTION=[0010][0][0000000][000000000000][00000000]
           PHASE=DECODE OPCODE=0010 ADDR=[04]00100   I_DATA=[0]00000000
STORAGE:    MEM[0]=1 MEM[1]=128   MEM[2]=x
REGISTERS: A_REG=1   B_REG=128    RDR_REG=128 DIR_REG=0    PORT_REG=x
SIGNALS:    RAMDATA=128   ALUOUT=z     BUS=10000000
FLAGS:      CF=x ZF=x     SF=x     OF=x     IF=0
CONTROLS:   IR_EN=0   A_EN=0   B_EN=0   PDR_EN=0     PORT_EN=0    PORT_RD=1
           PC_EN=0   PC_LOAD=0    ALU_EN=1     ALU_OE=0     RAM_OE=0     RDR_EN=0
RAM_CS=1
I/O:        IO=[128]10000000
```

```
TIME = 1950
CONTROL:    CLK=1     RST_=1
OPERATION: INSTRUCTION=[0010][0][0000000][000000000000][00000000]
           PHASE=EXECUTE     OPCODE=0010 ADDR=[04]00100   I_DATA=[0]00000000
STORAGE:    MEM[0]=1 MEM[1]=128   MEM[2]=x
REGISTERS: A_REG=1   B_REG=128    RDR_REG=128 DIR_REG=0    PORT_REG=x
```

```
SIGNALS:    RAMDATA=128  ALUOUT=z     BUS=10000000
FLAGS:      CF=0 ZF=0     SF=1     OF=0     IF=0
CONTROLS:   IR_EN=0   A_EN=0   B_EN=0   PDR_EN=0     PORT_EN=0    PORT_RD=1
           PC_EN=0   PC_LOAD=0    ALU_EN=1     ALU_OE=0     RAM_OE=0     RDR_EN=0
RAM_CS=1
I/O:        IO=[128]10000000
```

```
TIME = 2050
CONTROL:    CLK=1     RST_=1
OPERATION: INSTRUCTION=[0010][0][0000000][000000000000][00000000]
PHASE=UPDATE OPCODE=0010 ADDR=[04]00100   I_DATA=[0]00000000
STORAGE:    MEM[0]=1 MEM[1]=128   MEM[2]=x
REGISTERS: A_REG=1   B_REG=128    RDR_REG=128 DIR_REG=0    PORT_REG=x
SIGNALS:    RAMDATA=128  ALUOUT=z     BUS=10000000
FLAGS:      CF=0 ZF=0     SF=1     OF=0     IF=0
CONTROLS:   IR_EN=0   A_EN=0   B_EN=0   PDR_EN=0     PORT_EN=0    PORT_RD=1
           PC_EN=1   PC_LOAD=0    ALU_EN=0     ALU_OE=0     RAM_OE=0     RDR_EN=0
RAM_CS=1
I/O:        IO=[128]10000000
```

STR A+B, RAM[2]
0x1000 0002

0	0	0	1	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	x	x	x	x	0	0	0	0	0	0	1	0

```
TIME = 2150
CONTROL:    CLK=1     RST_=1
OPERATION: INSTRUCTION=[0010][0][0000000][000000000000][00000000]
           PHASE=FETCH   OPCODE=0010 ADDR=[05]00101   I_DATA=[0]00000000
STORAGE:    MEM[0]=1 MEM[1]=128   MEM[2]=x
REGISTERS: A_REG=1   B_REG=128    RDR_REG=128 DIR_REG=0    PORT_REG=x
SIGNALS:    RAMDATA=128  ALUOUT=z     BUS=10000000
FLAGS:      CF=0 ZF=0     SF=1     OF=0     IF=0
CONTROLS:   IR_EN=1   A_EN=0   B_EN=0   PDR_EN=0     PORT_EN=0    PORT_RD=1
           PC_EN=0   PC_LOAD=0    ALU_EN=0     ALU_OE=0     RAM_OE=0     RDR_EN=0
```

```
RAM_CS=1
I/O:        IO=[128]10000000
```

```
TIME = 2250
CONTROL:    CLK=1     RST_=1
OPERATION: INSTRUCTION=[0001][0][0000000][000000000000][00000010]
           PHASE=DECODE OPCODE=0001 ADDR=[05]00101   I_DATA=[2]00000010
STORAGE:    MEM[0]=1 MEM[1]=128   MEM[2]=x
REGISTERS: A_REG=1   B_REG=128    RDR_REG=128 DIR_REG=0    PORT_REG=x
SIGNALS:    RAMDATA=129   ALUOUT=129   BUS=10000001
FLAGS:      CF=0 ZF=0     SF=1     OF=0     IF=0
CONTROLS:   IR_EN=0   A_EN=0   B_EN=0   PDR_EN=0     PORT_EN=0    PORT_RD=0
           PC_EN=0   PC_LOAD=0    ALU_EN=0     ALU_OE=1     RAM_OE=0     RDR_EN=0
RAM_CS=0
I/O:        IO=[128]10000000
```

```
TIME = 2350
CONTROL:    CLK=1     RST_=1
OPERATION: INSTRUCTION=[0001][0][0000000][000000000000][00000010]
           PHASE=EXECUTE     OPCODE=0001 ADDR=[05]00101   I_DATA=[2]00000010
STORAGE:    MEM[0]=1 MEM[1]=128   MEM[2]=129
REGISTERS: A_REG=1   B_REG=128    RDR_REG=128 DIR_REG=0    PORT_REG=x
SIGNALS:    RAMDATA=129   ALUOUT=129   BUS=10000001
FLAGS:      CF=0 ZF=0     SF=1     OF=0     IF=0
CONTROLS:   IR_EN=0   A_EN=0   B_EN=0   PDR_EN=0     PORT_EN=0    PORT_RD=0
           PC_EN=0   PC_LOAD=0    ALU_EN=0     ALU_OE=1     RAM_OE=0     RDR_EN=0
RAM_CS=0
I/O:        IO=[128]10000000
```

```
TIME = 2450
CONTROL:    CLK=1     RST_=1
OPERATION: INSTRUCTION=[0001][0][0000000][000000000000][00000010]
           PHASE=UPDATE OPCODE=0001 ADDR=[05]00101   I_DATA=[2]00000010
STORAGE:    MEM[0]=1 MEM[1]=128   MEM[2]=129
REGISTERS: A_REG=1   B_REG=128    RDR_REG=128 DIR_REG=0    PORT_REG=x
SIGNALS:    RAMDATA=128   ALUOUT=z     BUS=10000000
FLAGS:      CF=0 ZF=0     SF=1     OF=0     IF=0
```

```
CONTROLS:  IR_EN=0  A_EN=0  B_EN=0  PDR_EN=0    PORT_EN=0   PORT_RD=1
          PC_EN=1  PC_LOAD=0   ALU_EN=0    ALU_OE=0    RAM_OE=0    RDR_EN=0
RAM_CS=1
I/O:       IO=[128]10000000
```

BN PC, 0x08
0xA080 0000

1	0	1	0	x	x	x	0	1	0	0	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

```
TIME = 2550
CONTROL:   CLK=1    RST_=1
OPERATION: INSTRUCTION=[0001][0][0000000][000000000000][00000010]
          PHASE=FETCH  OPCODE=0001 ADDR=[06]00110  I_DATA=[2]00000010
STORAGE:   MEM[0]=1 MEM[1]=128  MEM[2]=129
REGISTERS: A_REG=1  B_REG=128   RDR_REG=128 DIR_REG=0   PORT_REG=x
SIGNALS:   RAMDATA=128  ALUOUT=z    BUS=10000000
FLAGS:     CF=0 ZF=0    SF=1    OF=0    IF=0
CONTROLS:  IR_EN=1  A_EN=0  B_EN=0  PDR_EN=0    PORT_EN=0   PORT_RD=1
          PC_EN=0  PC_LOAD=0   ALU_EN=0    ALU_OE=0    RAM_OE=0    RDR_EN=0
RAM_CS=1
I/O:       IO=[128]10000000
```

```
TIME = 2650
CONTROL:   CLK=1    RST_=1
OPERATION: INSTRUCTION=[1010][0][0001000][000000000000][00000000]
          PHASE=DECODE OPCODE=1010 ADDR=[06]00110  I_DATA=[0]00000000
STORAGE:   MEM[0]=1 MEM[1]=128  MEM[2]=129
REGISTERS: A_REG=1  B_REG=128   RDR_REG=128 DIR_REG=0   PORT_REG=x
SIGNALS:   RAMDATA=128  ALUOUT=z    BUS=10000000
FLAGS:     CF=0 ZF=0    SF=1    OF=0    IF=0
CONTROLS:  IR_EN=0  A_EN=0  B_EN=0  PDR_EN=0    PORT_EN=0   PORT_RD=1
          PC_EN=0  PC_LOAD=0   ALU_EN=0    ALU_OE=0    RAM_OE=0    RDR_EN=0
RAM_CS=1
I/O:       IO=[128]10000000
```

```
TIME = 2750
CONTROL:   CLK=1    RST_=1
OPERATION: INSTRUCTION=[1010][0][0001000][000000000000][00000000]
           PHASE=EXECUTE    OPCODE=1010 ADDR=[06]00110  I_DATA=[0]00000000
STORAGE:   MEM[0]=1 MEM[1]=128  MEM[2]=129
REGISTERS: A_REG=1  B_REG=128   RDR_REG=128 DIR_REG=0   PORT_REG=x
SIGNALS:   RAMDATA=128  ALUOUT=z    BUS=10000000
FLAGS:     CF=0 ZF=0    SF=1    OF=0    IF=0
CONTROLS:  IR_EN=0  A_EN=0  B_EN=0  PDR_EN=0    PORT_EN=0   PORT_RD=1
           PC_EN=0  PC_LOAD=0   ALU_EN=0    ALU_OE=0    RAM_OE=0    RDR_EN=0
RAM_CS=1
I/O:       IO=[128]10000000
```

```
TIME = 2850
CONTROL:   CLK=1    RST_=1
OPERATION: INSTRUCTION=[1010][0][0001000][000000000000][00000000]
           PHASE=UPDATE OPCODE=1010 ADDR=[06]00110  I_DATA=[0]00000000
STORAGE:   MEM[0]=1 MEM[1]=128  MEM[2]=129
REGISTERS: A_REG=1  B_REG=128   RDR_REG=128 DIR_REG=0   PORT_REG=x
SIGNALS:   RAMDATA=128  ALUOUT=z    BUS=10000000
FLAGS:     CF=0 ZF=0    SF=1    OF=0    IF=0
CONTROLS:  IR_EN=0  A_EN=0  B_EN=0  PDR_EN=0    PORT_EN=0   PORT_RD=1
           PC_EN=1  PC_LOAD=1   ALU_EN=0    ALU_OE=0    RAM_OE=0    RDR_EN=0
RAM_CS=1
I/O:       IO=[128]10000000
```

LDI B, 1
0x0C10 0001

0	0	0	0	1	1	0	0	0	0	0	1	x	x	x	x	x	x	x	x	x	x	x	0	0	0	0	0	0	0	1

```
TIME = 2950
CONTROL:   CLK=1    RST_=1
```

```
OPERATION: INSTRUCTION=[1010][0][0001000][000000000000][00000000]
           PHASE=FETCH  OPCODE=1010 ADDR=[08]01000  I_DATA=[0]00000000
STORAGE:   MEM[0]=1 MEM[1]=128  MEM[2]=129
REGISTERS: A_REG=1  B_REG=128   RDR_REG=128 DIR_REG=0   PORT_REG=x
SIGNALS:   RAMDATA=128  ALUOUT=z    BUS=10000000
FLAGS:     CF=0 ZF=0    SF=1    OF=0    IF=0
CONTROLS:  IR_EN=1  A_EN=0  B_EN=0  PDR_EN=0    PORT_EN=0   PORT_RD=1
           PC_EN=0  PC_LOAD=0   ALU_EN=0    ALU_OE=0    RAM_OE=0    RDR_EN=0
RAM_CS=1
I/O:       IO=[128]10000000
```

```
TIME = 3050
CONTROL:   CLK=1    RST_=1
OPERATION: INSTRUCTION=[0000][1][1000001][000000000000][00000001]
           PHASE=DECODE OPCODE=0000 ADDR=[08]01000  I_DATA=[1]00000001
STORAGE:   MEM[0]=1 MEM[1]=128  MEM[2]=129
REGISTERS: A_REG=1  B_REG=128   RDR_REG=128 DIR_REG=0   PORT_REG=x
SIGNALS:   RAMDATA=128  ALUOUT=z    BUS=10000000
FLAGS:     CF=0 ZF=0    SF=1    OF=0    IF=1
CONTROLS:  IR_EN=0  A_EN=0  B_EN=1  PDR_EN=0    PORT_EN=0   PORT_RD=1
           PC_EN=0  PC_LOAD=0   ALU_EN=0    ALU_OE=0    RAM_OE=0    RDR_EN=0
RAM_CS=1
I/O:       IO=[128]10000000
```

```
TIME = 3150
CONTROL:   CLK=1    RST_=1
OPERATION: INSTRUCTION=[0000][1][1000001][000000000000][00000001]
           PHASE=EXECUTE    OPCODE=0000 ADDR=[08]01000  I_DATA=[1]00000001
STORAGE:   MEM[0]=1 MEM[1]=128  MEM[2]=129
REGISTERS: A_REG=1  B_REG=1     RDR_REG=128 DIR_REG=0   PORT_REG=x
SIGNALS:   RAMDATA=128  ALUOUT=z    BUS=10000000
FLAGS:     CF=0 ZF=0    SF=1    OF=0    IF=1
CONTROLS:  IR_EN=0  A_EN=0  B_EN=1  PDR_EN=0    PORT_EN=0   PORT_RD=1
           PC_EN=0  PC_LOAD=0   ALU_EN=0    ALU_OE=0    RAM_OE=0    RDR_EN=0
RAM_CS=1
I/O:       IO=[128]10000000
```

```
TIME = 3250
CONTROL:    CLK=1     RST_=1
OPERATION: INSTRUCTION=[0000][1][1000001][000000000000][00000001]
           PHASE=UPDATE OPCODE=0000 ADDR=[08]01000   I_DATA=[1]00000001
STORAGE:    MEM[0]=1 MEM[1]=128   MEM[2]=129
REGISTERS: A_REG=1   B_REG=1      RDR_REG=128 DIR_REG=0    PORT_REG=x
SIGNALS:    RAMDATA=128   ALUOUT=z     BUS=10000000
FLAGS:      CF=0 ZF=0     SF=1     OF=0     IF=1
CONTROLS:   IR_EN=0   A_EN=0   B_EN=0   PDR_EN=0     PORT_EN=0    PORT_RD=1
           PC_EN=1   PC_LOAD=0    ALU_EN=0     ALU_OE=0     RAM_OE=0     RDR_EN=0
RAM_CS=1
I/O:        IO=[128]10000000
```

SUB A, B

0x3000 0000

0	0	1	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

```
TIME = 3350
CONTROL:    CLK=1     RST_=1
OPERATION: INSTRUCTION=[0000][1][1000001][000000000000][00000001]
           PHASE=FETCH   OPCODE=0000 ADDR=[09]01001   I_DATA=[1]00000001
STORAGE:    MEM[0]=1 MEM[1]=128   MEM[2]=129
REGISTERS: A_REG=1   B_REG=1      RDR_REG=128 DIR_REG=0    PORT_REG=x
SIGNALS:    RAMDATA=128   ALUOUT=z     BUS=10000000
FLAGS:      CF=0 ZF=0     SF=1     OF=0     IF=1
CONTROLS:   IR_EN=1   A_EN=0   B_EN=0   PDR_EN=0     PORT_EN=0    PORT_RD=1
           PC_EN=0   PC_LOAD=0    ALU_EN=0     ALU_OE=0     RAM_OE=0     RDR_EN=0
RAM_CS=1
I/O:        IO=[128]10000000
```

```
TIME = 3450
CONTROL:    CLK=1     RST_=1
OPERATION: INSTRUCTION=[0011][0][0000000][000000000000][00000000]
           PHASE=DECODE OPCODE=0011 ADDR=[09]01001   I_DATA=[0]00000000
STORAGE:    MEM[0]=1 MEM[1]=128   MEM[2]=129
REGISTERS: A_REG=1   B_REG=1      RDR_REG=128 DIR_REG=0    PORT_REG=x
SIGNALS:    RAMDATA=128   ALUOUT=z     BUS=10000000
```

```
FLAGS:      CF=0 ZF=0     SF=1     OF=0     IF=0
CONTROLS:   IR_EN=0   A_EN=0   B_EN=0   PDR_EN=0     PORT_EN=0    PORT_RD=1
           PC_EN=0   PC_LOAD=0    ALU_EN=1     ALU_OE=0     RAM_OE=0     RDR_EN=0
RAM_CS=1
I/O:        IO=[128]10000000
```

```
TIME = 3550
CONTROL:    CLK=1     RST_=1
OPERATION: INSTRUCTION=[0011][0][0000000][000000000000][00000000]
           PHASE=EXECUTE     OPCODE=0011 ADDR=[09]01001   I_DATA=[0]00000000
STORAGE:    MEM[0]=1 MEM[1]=128   MEM[2]=129
REGISTERS: A_REG=1   B_REG=1      RDR_REG=128 DIR_REG=0    PORT_REG=x
SIGNALS:    RAMDATA=128   ALUOUT=z     BUS=10000000
FLAGS:      CF=0 ZF=1     SF=0     OF=0     IF=0
CONTROLS:   IR_EN=0   A_EN=0   B_EN=0   PDR_EN=0     PORT_EN=0    PORT_RD=1
           PC_EN=0   PC_LOAD=0    ALU_EN=1     ALU_OE=0     RAM_OE=0     RDR_EN=0
RAM_CS=1
I/O:        IO=[128]10000000
```

```
TIME = 3650
CONTROL:    CLK=1     RST_=1
OPERATION: INSTRUCTION=[0011][0][0000000][000000000000][00000000]
           PHASE=UPDATE OPCODE=0011 ADDR=[09]01001   I_DATA=[0]00000000
STORAGE:    MEM[0]=1 MEM[1]=128   MEM[2]=129
REGISTERS: A_REG=1   B_REG=1      RDR_REG=128 DIR_REG=0    PORT_REG=x
SIGNALS:    RAMDATA=128   ALUOUT=z     BUS=10000000
FLAGS:      CF=0 ZF=1     SF=0     OF=0     IF=0
CONTROLS:   IR_EN=0   A_EN=0   B_EN=0   PDR_EN=0     PORT_EN=0    PORT_RD=1
           PC_EN=1   PC_LOAD=0    ALU_EN=0     ALU_OE=0     RAM_OE=0     RDR_EN=0
RAM_CS=1
I/O:        IO=[128]10000000
```

STR A-B, RAM[3]
0x1000 0003

0	0	0	1	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	x	x	x	x	0	0	0	0	0	0	1	1

```
TIME = 3750
CONTROL:    CLK=1     RST_=1
OPERATION: INSTRUCTION=[0011][0][0000000][000000000000][00000000]
           PHASE=FETCH   OPCODE=0011 ADDR=[0a]01010   I_DATA=[0]00000000
STORAGE:    MEM[0]=1 MEM[1]=128   MEM[2]=129
REGISTERS: A_REG=1   B_REG=1      RDR_REG=128 DIR_REG=0    PORT_REG=x
SIGNALS:    RAMDATA=128   ALUOUT=z     BUS=10000000
FLAGS:      CF=0 ZF=1     SF=0     OF=0     IF=0
CONTROLS:   IR_EN=1   A_EN=0   B_EN=0   PDR_EN=0     PORT_EN=0    PORT_RD=1
           PC_EN=0   PC_LOAD=0    ALU_EN=0     ALU_OE=0     RAM_OE=0     RDR_EN=0
RAM_CS=1
I/O:        IO=[128]10000000
```

```
TIME = 3850
CONTROL:    CLK=1     RST_=1
OPERATION: INSTRUCTION=[0001][0][0000000][000000000000][00000011]
           PHASE=DECODE OPCODE=0001 ADDR=[0a]01010   I_DATA=[3]00000011
STORAGE:    MEM[0]=1 MEM[1]=128   MEM[2]=129
REGISTERS: A_REG=1   B_REG=1      RDR_REG=128 DIR_REG=0    PORT_REG=x
SIGNALS:    RAMDATA=0     ALUOUT=0     BUS=00000000
FLAGS:      CF=0 ZF=1     SF=0     OF=0     IF=0
CONTROLS:   IR_EN=0   A_EN=0   B_EN=0   PDR_EN=0     PORT_EN=0    PORT_RD=0
           PC_EN=0   PC_LOAD=0    ALU_EN=0     ALU_OE=1     RAM_OE=0     RDR_EN=0
RAM_CS=0
I/O:        IO=[128]10000000
```

```
TIME = 3950
CONTROL:    CLK=1     RST_=1
OPERATION: INSTRUCTION=[0001][0][0000000][000000000000][00000011]
           PHASE=EXECUTE     OPCODE=0001 ADDR=[0a]01010   I_DATA=[3]00000011
STORAGE:    MEM[0]=1 MEM[1]=128   MEM[2]=129
REGISTERS: A_REG=1   B_REG=1      RDR_REG=128 DIR_REG=0    PORT_REG=x
SIGNALS:    RAMDATA=0     ALUOUT=0     BUS=00000000
FLAGS:      CF=0 ZF=1     SF=0     OF=0     IF=0
CONTROLS:   IR_EN=0   A_EN=0   B_EN=0   PDR_EN=0     PORT_EN=0    PORT_RD=0
           PC_EN=0   PC_LOAD=0    ALU_EN=0     ALU_OE=1     RAM_OE=0     RDR_EN=0
```

```
RAM_CS=0
I/O:        IO=[128]10000000
```

```
TIME = 4050
CONTROL:    CLK=1     RST_=1
OPERATION: INSTRUCTION=[0001][0][0000000][000000000000][00000011]
           PHASE=UPDATE OPCODE=0001 ADDR=[0a]01010  I_DATA=[3]00000011
STORAGE:    MEM[0]=1 MEM[1]=128  MEM[2]=129
REGISTERS: A_REG=1  B_REG=1      RDR_REG=128 DIR_REG=0    PORT_REG=x
SIGNALS:    RAMDATA=128  ALUOUT=z     BUS=10000000
FLAGS:      CF=0 ZF=1     SF=0     OF=0     IF=0
CONTROLS:   IR_EN=0  A_EN=0  B_EN=0  PDR_EN=0     PORT_EN=0    PORT_RD=1
           PC_EN=1  PC_LOAD=0    ALU_EN=0     ALU_OE=0     RAM_OE=0     RDR_EN=0
RAM_CS=1
I/O:        IO=[128]10000000
```

BZ PC, 0x0F

0x90F0 0000

1	0	0	1	x	x	x	0	1	1	1	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

```
TIME = 4150
CONTROL:    CLK=1     RST_=1
OPERATION: INSTRUCTION=[0001][0][0000000][000000000000][00000011]
           PHASE=FETCH  OPCODE=0001 ADDR=[0b]01011  I_DATA=[3]00000011
STORAGE:    MEM[0]=1 MEM[1]=128  MEM[2]=129
REGISTERS: A_REG=1  B_REG=1      RDR_REG=128 DIR_REG=0    PORT_REG=x
SIGNALS:    RAMDATA=128  ALUOUT=z     BUS=10000000
FLAGS:      CF=0 ZF=1     SF=0     OF=0     IF=0
CONTROLS:   IR_EN=1  A_EN=0  B_EN=0  PDR_EN=0     PORT_EN=0    PORT_RD=1
           PC_EN=0  PC_LOAD=0    ALU_EN=0     ALU_OE=0     RAM_OE=0     RDR_EN=0
RAM_CS=1
I/O:        IO=[128]10000000
```

```
TIME = 4250
CONTROL:    CLK=1     RST_=1
```

```
OPERATION: INSTRUCTION=[1001][0][0001111][000000000000][00000000]
           PHASE=DECODE OPCODE=1001 ADDR=[0b]01011  I_DATA=[0]00000000
STORAGE:   MEM[0]=1 MEM[1]=128  MEM[2]=129
REGISTERS: A_REG=1  B_REG=1     RDR_REG=128 DIR_REG=0   PORT_REG=x
SIGNALS:   RAMDATA=128  ALUOUT=z    BUS=10000000
FLAGS:     CF=0 ZF=1    SF=0    OF=0    IF=0
CONTROLS:  IR_EN=0  A_EN=0  B_EN=0  PDR_EN=0    PORT_EN=0   PORT_RD=1
           PC_EN=0  PC_LOAD=0   ALU_EN=0    ALU_OE=0    RAM_OE=0    RDR_EN=0
RAM_CS=1
I/O:       IO=[128]10000000
```

```
TIME = 4350
CONTROL:   CLK=1    RST_=1
OPERATION: INSTRUCTION=[1001][0][0001111][000000000000][00000000]
           PHASE=EXECUTE    OPCODE=1001 ADDR=[0b]01011  I_DATA=[0]00000000
STORAGE:   MEM[0]=1 MEM[1]=128  MEM[2]=129
REGISTERS: A_REG=1  B_REG=1     RDR_REG=128 DIR_REG=0   PORT_REG=x
SIGNALS:   RAMDATA=128  ALUOUT=z    BUS=10000000
FLAGS:     CF=0 ZF=1    SF=0    OF=0    IF=0
CONTROLS:  IR_EN=0  A_EN=0  B_EN=0  PDR_EN=0    PORT_EN=0   PORT_RD=1
           PC_EN=0  PC_LOAD=0   ALU_EN=0    ALU_OE=0    RAM_OE=0    RDR_EN=0
RAM_CS=1
I/O:       IO=[128]10000000
TIME = 4450
CONTROL:   CLK=1    RST_=1
OPERATION: INSTRUCTION=[1001][0][0001111][000000000000][00000000]
           PHASE=UPDATE OPCODE=1001 ADDR=[0b]01011  I_DATA=[0]00000000
STORAGE:   MEM[0]=1 MEM[1]=128  MEM[2]=129
REGISTERS: A_REG=1  B_REG=1     RDR_REG=128 DIR_REG=0   PORT_REG=x
SIGNALS:   RAMDATA=128  ALUOUT=z    BUS=10000000
FLAGS:     CF=0 ZF=1    SF=0    OF=0    IF=0
CONTROLS:  IR_EN=0  A_EN=0  B_EN=0  PDR_EN=0    PORT_EN=0   PORT_RD=1
           PC_EN=1  PC_LOAD=1   ALU_EN=0    ALU_OE=0    RAM_OE=0    RDR_EN=0
RAM_CS=1
I/O:       IO=[128]10000000
```

LD A, RAM[2]

0x0400 0002

0	0	0	0	0	1	0	0	0	0	0	0	x	x	x	x	x	x	x	x	x	x	x	0	0	0	0	0	0	1	0

```
TIME = 4550
CONTROL:    CLK=1     RST_=1
OPERATION: INSTRUCTION=[1001][0][0001111][000000000000][00000000]
           PHASE=FETCH   OPCODE=1001 ADDR=[0f]01111   I_DATA=[0]00000000
STORAGE:    MEM[0]=1 MEM[1]=128   MEM[2]=129
REGISTERS: A_REG=1   B_REG=1      RDR_REG=128 DIR_REG=0    PORT_REG=x
SIGNALS:    RAMDATA=128   ALUOUT=z     BUS=10000000
FLAGS:      CF=0 ZF=1     SF=0     OF=0     IF=0
CONTROLS:   IR_EN=1   A_EN=0   B_EN=0   PDR_EN=0     PORT_EN=0    PORT_RD=1
           PC_EN=0   PC_LOAD=0    ALU_EN=0     ALU_OE=0     RAM_OE=0     RDR_EN=0
RAM_CS=1
I/O:        IO=[128]10000000
```

```
TIME = 4650
CONTROL:    CLK=1     RST_=1
OPERATION: INSTRUCTION=[0000][0][1000000][000000000000][00000010]
           PHASE=DECODE OPCODE=0000 ADDR=[0f]01111   I_DATA=[128]10000000
STORAGE:    MEM[0]=1 MEM[1]=128   MEM[2]=129
REGISTERS: A_REG=1   B_REG=1      RDR_REG=128 DIR_REG=0    PORT_REG=x
SIGNALS:    RAMDATA=129   ALUOUT=z     BUS=10000001
FLAGS:      CF=0 ZF=1     SF=0     OF=0     IF=0
CONTROLS:   IR_EN=0   A_EN=1   B_EN=0   PDR_EN=0     PORT_EN=0    PORT_RD=0
           PC_EN=0   PC_LOAD=0    ALU_EN=0     ALU_OE=0     RAM_OE=1     RDR_EN=1
RAM_CS=0
I/O:        IO=[128]10000000
```

```
TIME = 4750
CONTROL:    CLK=1     RST_=1
OPERATION: INSTRUCTION=[0000][0][1000000][000000000000][00000010]
           PHASE=EXECUTE     OPCODE=0000 ADDR=[0f]01111   I_DATA=[129]10000001
STORAGE:    MEM[0]=1 MEM[1]=128   MEM[2]=129
REGISTERS: A_REG=128     B_REG=1      RDR_REG=129 DIR_REG=0    PORT_REG=x
SIGNALS:    RAMDATA=129   ALUOUT=z     BUS=10000001
FLAGS:      CF=0 ZF=1     SF=0     OF=0     IF=0
```

```
CONTROLS:  IR_EN=0  A_EN=1  B_EN=0  PDR_EN=0    PORT_EN=0   PORT_RD=0
          PC_EN=0  PC_LOAD=0   ALU_EN=0    ALU_OE=0    RAM_OE=1    RDR_EN=1
RAM_CS=0
I/O:       IO=[128]10000000
```

```
TIME = 4850
CONTROL:   CLK=1    RST_=1
OPERATION: INSTRUCTION=[0000][0][1000000][000000000000][00000010]
          PHASE=UPDATE OPCODE=0000 ADDR=[0f]01111  I_DATA=[2]00000010
STORAGE:   MEM[0]=1 MEM[1]=128  MEM[2]=129
REGISTERS: A_REG=129    B_REG=1     RDR_REG=129 DIR_REG=0   PORT_REG=x
SIGNALS:   RAMDATA=128  ALUOUT=z    BUS=10000000
FLAGS:     CF=0 ZF=1    SF=0    OF=0    IF=0
CONTROLS:  IR_EN=0  A_EN=0  B_EN=0  PDR_EN=0    PORT_EN=0   PORT_RD=1
          PC_EN=1  PC_LOAD=0   ALU_EN=0    ALU_OE=0    RAM_OE=0    RDR_EN=0
RAM_CS=1
I/O:       IO=[128]10000000
```

AND A, B

0x4000 0000

0	1	0	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

```
TIME = 4950
CONTROL:   CLK=1    RST_=1
OPERATION: INSTRUCTION=[0000][0][1000000][000000000000][00000010]
          PHASE=FETCH  OPCODE=0000 ADDR=[10]10000  I_DATA=[2]00000010
STORAGE:   MEM[0]=1 MEM[1]=128  MEM[2]=129
REGISTERS: A_REG=129    B_REG=1     RDR_REG=129 DIR_REG=0   PORT_REG=x
SIGNALS:   RAMDATA=128  ALUOUT=z    BUS=10000000
FLAGS:     CF=0 ZF=1    SF=0    OF=0    IF=0
CONTROLS:  IR_EN=1  A_EN=0  B_EN=0  PDR_EN=0    PORT_EN=0   PORT_RD=1
          PC_EN=0  PC_LOAD=0   ALU_EN=0    ALU_OE=0    RAM_OE=0    RDR_EN=0
RAM_CS=1
I/O:       IO=[128]10000000
```

```
TIME = 5050
CONTROL:   CLK=1    RST_=1
OPERATION: INSTRUCTION=[0100][0][0000000][000000000000][00000000]
           PHASE=DECODE OPCODE=0100 ADDR=[10]10000  I_DATA=[0]00000000
STORAGE:   MEM[0]=1 MEM[1]=128  MEM[2]=129
REGISTERS: A_REG=129    B_REG=1     RDR_REG=129 DIR_REG=0   PORT_REG=x
SIGNALS:   RAMDATA=128  ALUOUT=[1]00000001    BUS=10000000
FLAGS:     CF=0 ZF=1    SF=0    OF=0    IF=0
CONTROLS:  IR_EN=0  A_EN=0  B_EN=0  PDR_EN=0    PORT_EN=0   PORT_RD=1
           PC_EN=0  PC_LOAD=0   ALU_EN=1    ALU_OE=0    RAM_OE=0    RDR_EN=0
RAM_CS=1
I/O:       IO=[128]10000000
```

```
TIME = 5150
CONTROL:   CLK=1    RST_=1
OPERATION: INSTRUCTION=[0100][0][0000000][000000000000][00000000]
           PHASE=EXECUTE    OPCODE=0100 ADDR=[10]10000  I_DATA=[0]00000000
STORAGE:   MEM[0]=1 MEM[1]=128  MEM[2]=129
REGISTERS: A_REG=129    B_REG=1     RDR_REG=129 DIR_REG=0   PORT_REG=x
SIGNALS:   RAMDATA=128  ALUOUT=[1]00000001    BUS=10000000
FLAGS:     CF=0 ZF=0    SF=0    OF=0    IF=0
CONTROLS:  IR_EN=0  A_EN=0  B_EN=0  PDR_EN=0    PORT_EN=0   PORT_RD=1
           PC_EN=0  PC_LOAD=0   ALU_EN=1    ALU_OE=0    RAM_OE=0    RDR_EN=0
RAM_CS=1
I/O:       IO=[128]10000000
```

```
TIME = 5250
CONTROL:   CLK=1    RST_=1
OPERATION: INSTRUCTION=[0100][0][0000000][000000000000][00000000]
           PHASE=UPDATE OPCODE=0100 ADDR=[10]10000  I_DATA=[0]00000000
STORAGE:   MEM[0]=1 MEM[1]=128  MEM[2]=129
REGISTERS: A_REG=129    B_REG=1     RDR_REG=129 DIR_REG=0   PORT_REG=x
SIGNALS:   RAMDATA=128  ALUOUT=[1]00000001    BUS=10000000
FLAGS:     CF=0 ZF=0    SF=0    OF=0    IF=0
CONTROLS:  IR_EN=0  A_EN=0  B_EN=0  PDR_EN=0    PORT_EN=0   PORT_RD=1
           PC_EN=1  PC_LOAD=0   ALU_EN=0    ALU_OE=0    RAM_OE=0    RDR_EN=0
RAM_CS=1
```

```
I/O:        IO=[128]10000000
```

OR A, B

0x5000 0000

0	1	0	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

```
TIME = 5350
CONTROL:    CLK=1     RST_=1
OPERATION: INSTRUCTION=[0100][0][0000000][000000000000][00000000]
           PHASE=FETCH   OPCODE=0100 ADDR=[11]10001   I_DATA=[0]00000000
STORAGE:    MEM[0]=1 MEM[1]=128   MEM[2]=129
REGISTERS: A_REG=129     B_REG=1      RDR_REG=129 DIR_REG=0    PORT_REG=x
SIGNALS:    RAMDATA=128   ALUOUT=[1]00000001     BUS=10000000
FLAGS:      CF=0 ZF=0     SF=0     OF=0     IF=0
CONTROLS:   IR_EN=1   A_EN=0   B_EN=0   PDR_EN=0     PORT_EN=0    PORT_RD=1
           PC_EN=0   PC_LOAD=0    ALU_EN=0     ALU_OE=0     RAM_OE=0     RDR_EN=0
RAM_CS=1
I/O:        IO=[128]10000000
```

```
TIME = 5450
CONTROL:    CLK=1     RST_=1
OPERATION: INSTRUCTION=[0101][0][0000000][000000000000][00000000]
           PHASE=DECODE OPCODE=0101 ADDR=[11]10001   I_DATA=[0]00000000
STORAGE:    MEM[0]=1 MEM[1]=128   MEM[2]=129
REGISTERS: A_REG=129     B_REG=1      RDR_REG=129 DIR_REG=0    PORT_REG=x
SIGNALS:    RAMDATA=128   ALUOUT=[1]00000001     BUS=10000000
FLAGS:      CF=0 ZF=0     SF=0     OF=0     IF=0
CONTROLS:   IR_EN=0   A_EN=0   B_EN=0   PDR_EN=0     PORT_EN=0    PORT_RD=1
           PC_EN=0   PC_LOAD=0    ALU_EN=1     ALU_OE=0     RAM_OE=0     RDR_EN=0
RAM_CS=1
I/O:        IO=[128]10000000
```

```
TIME = 5550
CONTROL:    CLK=1     RST_=1
OPERATION: INSTRUCTION=[0101][0][0000000][000000000000][00000000]
```

```
          PHASE=EXECUTE    OPCODE=0101 ADDR=[11]10001  I_DATA=[0]00000000
STORAGE:   MEM[0]=1 MEM[1]=128  MEM[2]=129
REGISTERS: A_REG=129    B_REG=1     RDR_REG=129 DIR_REG=0   PORT_REG=x
SIGNALS:   RAMDATA=128  ALUOUT=[129]10000001    BUS=10000000
FLAGS:     CF=0 ZF=0    SF=1    OF=0    IF=0
CONTROLS:  IR_EN=0  A_EN=0  B_EN=0  PDR_EN=0    PORT_EN=0   PORT_RD=1
          PC_EN=0  PC_LOAD=0   ALU_EN=1    ALU_OE=0    RAM_OE=0    RDR_EN=0
RAM_CS=1
I/O:       IO=[128]10000000
```

```
TIME = 5650
CONTROL:   CLK=1    RST_=1
OPERATION: INSTRUCTION=[0101][0][0000000][000000000000][00000000]
          PHASE=UPDATE OPCODE=0101 ADDR=[11]10001  I_DATA=[0]00000000
STORAGE:   MEM[0]=1 MEM[1]=128  MEM[2]=129
REGISTERS: A_REG=129    B_REG=1     RDR_REG=129 DIR_REG=0   PORT_REG=x
SIGNALS:   RAMDATA=128  ALUOUT=[129]10000001    BUS=10000000
FLAGS:     CF=0 ZF=0    SF=1    OF=0    IF=0
CONTROLS:  IR_EN=0  A_EN=0  B_EN=0  PDR_EN=0    PORT_EN=0   PORT_RD=1
          PC_EN=1  PC_LOAD=0   ALU_EN=0    ALU_OE=0    RAM_OE=0    RDR_EN=0
RAM_CS=1
I/O:       IO=[128]10000000
```

XOR A, B

0x6000 0000

0	1	1	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

```
TIME = 5750
CONTROL:   CLK=1    RST_=1
OPERATION: INSTRUCTION=[0101][0][0000000][000000000000][00000000]
          PHASE=FETCH  OPCODE=0101 ADDR=[12]10010  I_DATA=[0]00000000
STORAGE:   MEM[0]=1 MEM[1]=128  MEM[2]=129
REGISTERS: A_REG=129    B_REG=1     RDR_REG=129 DIR_REG=0   PORT_REG=x
SIGNALS:   RAMDATA=128  ALUOUT=[129]10000001   BUS=10000000
FLAGS:     CF=0 ZF=0    SF=1    OF=0    IF=0
CONTROLS:  IR_EN=1  A_EN=0  B_EN=0  PDR_EN=0    PORT_EN=0   PORT_RD=1
          PC_EN=0  PC_LOAD=0   ALU_EN=0    ALU_OE=0    RAM_OE=0    RDR_EN=0
```

```
RAM_CS=1
I/O:        IO=[128]10000000
```

```
TIME = 5850
CONTROL:    CLK=1    RST_=1
OPERATION: INSTRUCTION=[0110][0][0000000][000000000000][00000000]
           PHASE=DECODE OPCODE=0110 ADDR=[12]10010  I_DATA=[0]00000000
STORAGE:    MEM[0]=1 MEM[1]=128  MEM[2]=129
REGISTERS: A_REG=129    B_REG=1     RDR_REG=129 DIR_REG=0   PORT_REG=x
SIGNALS:    RAMDATA=128  ALUOUT=[129]10000001    BUS=10000000
FLAGS:      CF=0 ZF=0    SF=1    OF=0    IF=0
CONTROLS:   IR_EN=0  A_EN=0  B_EN=0  PDR_EN=0    PORT_EN=0   PORT_RD=1
           PC_EN=0  PC_LOAD=0   ALU_EN=1    ALU_OE=0    RAM_OE=0    RDR_EN=0
RAM_CS=1
I/O:        IO=[128]10000000
```

```
TIME = 5950
CONTROL:    CLK=1    RST_=1
OPERATION: INSTRUCTION=[0110][0][0000000][000000000000][00000000]
           PHASE=EXECUTE    OPCODE=0110 ADDR=[12]10010  I_DATA=[0]00000000
STORAGE:    MEM[0]=1 MEM[1]=128  MEM[2]=129
REGISTERS: A_REG=129    B_REG=1     RDR_REG=129 DIR_REG=0   PORT_REG=x
SIGNALS:    RAMDATA=128  ALUOUT=[128]10000000    BUS=10000000
FLAGS:      CF=0 ZF=0    SF=1    OF=0    IF=0
CONTROLS:   IR_EN=0  A_EN=0  B_EN=0  PDR_EN=0    PORT_EN=0   PORT_RD=1
           PC_EN=0  PC_LOAD=0   ALU_EN=1    ALU_OE=0    RAM_OE=0    RDR_EN=0
RAM_CS=1
I/O:        IO=[128]10000000
```

```
TIME = 6050
CONTROL:    CLK=1    RST_=1
OPERATION: INSTRUCTION=[0110][0][0000000][000000000000][00000000]
           PHASE=UPDATE OPCODE=0110 ADDR=[12]10010  I_DATA=[0]00000000
STORAGE:    MEM[0]=1 MEM[1]=128  MEM[2]=129
REGISTERS: A_REG=129    B_REG=1     RDR_REG=129 DIR_REG=0   PORT_REG=x
SIGNALS:    RAMDATA=128  ALUOUT=[128]10000000   BUS=10000000
FLAGS:      CF=0 ZF=0    SF=1    OF=0    IF=0
```

```
CONTROLS:  IR_EN=0  A_EN=0  B_EN=0  PDR_EN=0    PORT_EN=0   PORT_RD=1
          PC_EN=1  PC_LOAD=0   ALU_EN=0    ALU_OE=0    RAM_OE=0    RDR_EN=0
RAM_CS=1
I/O:       IO=[128]10000000
```

NOT A
0x7000 0000

0	1	1	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

```
TIME = 6150
CONTROL:   CLK=1    RST_=1
OPERATION: INSTRUCTION=[0110][0][0000000][000000000000][00000000]
          PHASE=FETCH  OPCODE=0110 ADDR=[13]10011  I_DATA=[0]00000000
STORAGE:   MEM[0]=1 MEM[1]=128  MEM[2]=129
REGISTERS: A_REG=129    B_REG=1     RDR_REG=129 DIR_REG=0   PORT_REG=x
SIGNALS:   RAMDATA=128  ALUOUT=[128]10000000    BUS=10000000
FLAGS:     CF=0 ZF=0    SF=1    OF=0    IF=0
CONTROLS:  IR_EN=1  A_EN=0  B_EN=0  PDR_EN=0    PORT_EN=0   PORT_RD=1
          PC_EN=0  PC_LOAD=0   ALU_EN=0    ALU_OE=0    RAM_OE=0    RDR_EN=0
RAM_CS=1
I/O:       IO=[128]10000000
```

```
TIME = 6250
CONTROL:   CLK=1    RST_=1
OPERATION: INSTRUCTION=[0111][0][0000000][000000000000][00000000]
          PHASE=DECODE OPCODE=0111 ADDR=[13]10011  I_DATA=[0]00000000
STORAGE:   MEM[0]=1 MEM[1]=128  MEM[2]=129
REGISTERS: A_REG=129    B_REG=1     RDR_REG=129 DIR_REG=0   PORT_REG=x
SIGNALS:   RAMDATA=128  ALUOUT=[128]10000000    BUS=10000000
FLAGS:     CF=0 ZF=0    SF=1    OF=0    IF=0
CONTROLS:  IR_EN=0  A_EN=0  B_EN=0  PDR_EN=0    PORT_EN=0   PORT_RD=1
          PC_EN=0  PC_LOAD=0   ALU_EN=1    ALU_OE=0    RAM_OE=0    RDR_EN=0
RAM_CS=1
I/O:       IO=[128]10000000
```

```
TIME = 6350
CONTROL:   CLK=1    RST_=1
OPERATION: INSTRUCTION=[0111][0][0000000][000000000000][00000000]
           PHASE=EXECUTE    OPCODE=0111 ADDR=[13]10011  I_DATA=[0]00000000
STORAGE:   MEM[0]=1 MEM[1]=128  MEM[2]=129
REGISTERS: A_REG=129    B_REG=1     RDR_REG=129 DIR_REG=0   PORT_REG=x
SIGNALS:   RAMDATA=128  ALUOUT=[126]01111110    BUS=10000000
FLAGS:     CF=0 ZF=0    SF=0    OF=0    IF=0
CONTROLS:  IR_EN=0  A_EN=0  B_EN=0  PDR_EN=0    PORT_EN=0   PORT_RD=1
           PC_EN=0  PC_LOAD=0   ALU_EN=1    ALU_OE=0    RAM_OE=0    RDR_EN=0
RAM_CS=1
I/O:       IO=[128]10000000
```

```
TIME = 6450
CONTROL:   CLK=1    RST_=1
OPERATION: INSTRUCTION=[0111][0][0000000][000000000000][00000000]
           PHASE=UPDATE OPCODE=0111 ADDR=[13]10011  I_DATA=[0]00000000
STORAGE:   MEM[0]=1 MEM[1]=128  MEM[2]=129
REGISTERS: A_REG=129    B_REG=1     RDR_REG=129 DIR_REG=0   PORT_REG=x
SIGNALS:   RAMDATA=128  ALUOUT=[126]01111110    BUS=10000000
FLAGS:     CF=0 ZF=0    SF=0    OF=0    IF=0
CONTROLS:  IR_EN=0  A_EN=0  B_EN=0  PDR_EN=0    PORT_EN=0   PORT_RD=1
           PC_EN=1  PC_LOAD=0   ALU_EN=0    ALU_OE=0    RAM_OE=0    RDR_EN=0
RAM_CS=1
I/O:       IO=[128]10000000
```

B PC, 0x16

0x8160 0000

1	0	0	0	x	x	x	1	0	1	1	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

```
TIME = 6550
CONTROL:   CLK=1    RST_=1
OPERATION: INSTRUCTION=[0111][0][0000000][000000000000][00000000]
           PHASE=FETCH  OPCODE=0111 ADDR=[14]10100  I_DATA=[0]00000000
STORAGE:   MEM[0]=1 MEM[1]=128  MEM[2]=129
```

```
REGISTERS: A_REG=129    B_REG=1     RDR_REG=129 DIR_REG=0   PORT_REG=x
SIGNALS:   RAMDATA=128  ALUOUT=z    BUS=10000000
FLAGS:     CF=0 ZF=0    SF=0    OF=0    IF=0
CONTROLS:  IR_EN=1  A_EN=0  B_EN=0  PDR_EN=0    PORT_EN=0   PORT_RD=1
          PC_EN=0  PC_LOAD=0   ALU_EN=0    ALU_OE=0    RAM_OE=0    RDR_EN=0
RAM_CS=1
I/O:       IO=[128]10000000
```

```
TIME = 6650
CONTROL:   CLK=1    RST_=1
OPERATION: INSTRUCTION=[1000][0][0010110][000000000000][00000000]
          PHASE=DECODE OPCODE=1000 ADDR=[14]10100  I_DATA=[0]00000000
STORAGE:   MEM[0]=1 MEM[1]=128  MEM[2]=129
REGISTERS: A_REG=129    B_REG=1     RDR_REG=129 DIR_REG=0   PORT_REG=x
SIGNALS:   RAMDATA=128  ALUOUT=z    BUS=10000000
FLAGS:     CF=0 ZF=0    SF=0    OF=0    IF=0
CONTROLS:  IR_EN=0  A_EN=0  B_EN=0  PDR_EN=0    PORT_EN=0   PORT_RD=1
          PC_EN=0  PC_LOAD=0   ALU_EN=0    ALU_OE=0    RAM_OE=0    RDR_EN=0
RAM_CS=1
I/O:       IO=[128]10000000
```

```
TIME = 6750
CONTROL:   CLK=1    RST_=1
OPERATION: INSTRUCTION=[1000][0][0010110][000000000000][00000000]
          PHASE=EXECUTE    OPCODE=1000 ADDR=[14]10100  I_DATA=[0]00000000
STORAGE:   MEM[0]=1 MEM[1]=128  MEM[2]=129
REGISTERS: A_REG=129    B_REG=1     RDR_REG=129 DIR_REG=0   PORT_REG=x
SIGNALS:   RAMDATA=128  ALUOUT=z    BUS=10000000
FLAGS:     CF=0 ZF=0    SF=0    OF=0    IF=0
CONTROLS:  IR_EN=0  A_EN=0  B_EN=0  PDR_EN=0    PORT_EN=0   PORT_RD=1
          PC_EN=0  PC_LOAD=0   ALU_EN=0    ALU_OE=0    RAM_OE=0    RDR_EN=0
RAM_CS=1
I/O:       IO=[128]10000000
```

```
TIME = 6850
CONTROL:   CLK=1    RST_=1
OPERATION: INSTRUCTION=[1000][0][0010110][000000000000][00000000]
```

```
          PHASE=UPDATE OPCODE=1000 ADDR=[14]10100  I_DATA=[0]00000000
STORAGE:   MEM[0]=1 MEM[1]=128  MEM[2]=129
REGISTERS: A_REG=129    B_REG=1     RDR_REG=129 DIR_REG=0   PORT_REG=x
SIGNALS:   RAMDATA=128  ALUOUT=z    BUS=10000000
FLAGS:     CF=0 ZF=0    SF=0    OF=0    IF=0
CONTROLS:  IR_EN=0  A_EN=0  B_EN=0  PDR_EN=0    PORT_EN=0   PORT_RD=1
          PC_EN=1  PC_LOAD=1   ALU_EN=0    ALU_OE=0    RAM_OE=0    RDR_EN=0
RAM_CS=1
I/O:       IO=[128]10000000
```

LDI PDR, 1
0x0C20 0001

0	0	0	0	1	1	0	0	0	0	1	0	x	x	x	x	x	x	x	x	x	x	x	0	0	0	0	0	0	0	1

```
TIME = 6950
CONTROL:   CLK=1    RST_=1
OPERATION: INSTRUCTION=[1000][0][0010110][000000000000][00000000]
          PHASE=FETCH  OPCODE=1000 ADDR=[16]10110  I_DATA=[0]00000000
STORAGE:   MEM[0]=1 MEM[1]=128  MEM[2]=129
REGISTERS: A_REG=129    B_REG=1     RDR_REG=129 DIR_REG=0   PORT_REG=x
SIGNALS:   RAMDATA=128  ALUOUT=z    BUS=10000000
FLAGS:     CF=0 ZF=0    SF=0    OF=0    IF=0
CONTROLS:  IR_EN=1  A_EN=0  B_EN=0  PDR_EN=0    PORT_EN=0   PORT_RD=1
          PC_EN=0  PC_LOAD=0   ALU_EN=0    ALU_OE=0    RAM_OE=0    RDR_EN=0
RAM_CS=1
I/O:       IO=[128]10000000
```

```
TIME = 7050
CONTROL:   CLK=1    RST_=1
OPERATION: INSTRUCTION=[0000][1][1000010][000000000000][00000001]
          PHASE=DECODE OPCODE=0000 ADDR=[16]10110  I_DATA=[1]00000001
STORAGE:   MEM[0]=1 MEM[1]=128  MEM[2]=129
REGISTERS: A_REG=129    B_REG=1     RDR_REG=129 DIR_REG=0   PORT_REG=x
SIGNALS:   RAMDATA=128  ALUOUT=z    BUS=10000000
FLAGS:     CF=0 ZF=0    SF=0    OF=0    IF=1
```

```
CONTROLS:  IR_EN=0  A_EN=0  B_EN=0  PDR_EN=1    PORT_EN=0   PORT_RD=1
          PC_EN=0  PC_LOAD=0   ALU_EN=0    ALU_OE=0    RAM_OE=0    RDR_EN=0
RAM_CS=1
I/O:       IO=[128]10000000
```

```
TIME = 7150
CONTROL:   CLK=1    RST_=1
OPERATION: INSTRUCTION=[0000][1][1000010][000000000000][00000001]
          PHASE=EXECUTE    OPCODE=0000 ADDR=[16]10110  I_DATA=[1]00000001
STORAGE:   MEM[0]=1 MEM[1]=128  MEM[2]=129
REGISTERS: A_REG=129    B_REG=1     RDR_REG=129 DIR_REG=1   PORT_REG=x
SIGNALS:   RAMDATA=x    ALUOUT=z    BUS=xxxxxxxx
FLAGS:     CF=0 ZF=0    SF=0    OF=0    IF=1
CONTROLS:  IR_EN=0  A_EN=0  B_EN=0  PDR_EN=1    PORT_EN=0   PORT_RD=1
          PC_EN=0  PC_LOAD=0   ALU_EN=0    ALU_OE=0    RAM_OE=0    RDR_EN=0
RAM_CS=1
I/O:       IO=[x]xxxxxxxx
```

```
TIME = 7250
CONTROL:   CLK=1    RST_=1
OPERATION: INSTRUCTION=[0000][1][1000010][000000000000][00000001]
          PHASE=UPDATE OPCODE=0000 ADDR=[16]10110  I_DATA=[1]00000001
STORAGE:   MEM[0]=1 MEM[1]=128  MEM[2]=129
REGISTERS: A_REG=129    B_REG=1     RDR_REG=129 DIR_REG=1   PORT_REG=x
SIGNALS:   RAMDATA=x    ALUOUT=z    BUS=xxxxxxxx
FLAGS:     CF=0 ZF=0    SF=0    OF=0    IF=1
CONTROLS:  IR_EN=0  A_EN=0  B_EN=0  PDR_EN=0    PORT_EN=0   PORT_RD=1
          PC_EN=1  PC_LOAD=0   ALU_EN=0    ALU_OE=0    RAM_OE=0    RDR_EN=0
RAM_CS=1
I/O:       IO=[x]xxxxxxxx
```

LDI A, 255
0x0C00 00FF

0	0	0	0	1	1	0	0	0	0	0	0	x	x	x	x	x	x	x	x	x	x	x	1	1	1	1	1	1	1	1

```
TIME = 7350
```

```
CONTROL:    CLK=1     RST_=1
OPERATION: INSTRUCTION=[0000][1][1000010][000000000000][00000001]
           PHASE=FETCH   OPCODE=0000 ADDR=[17]10111   I_DATA=[1]00000001
STORAGE:    MEM[0]=1 MEM[1]=128   MEM[2]=129
REGISTERS: A_REG=129     B_REG=1      RDR_REG=129 DIR_REG=1    PORT_REG=x
SIGNALS:    RAMDATA=x     ALUOUT=z     BUS=xxxxxxxx
FLAGS:      CF=0 ZF=0     SF=0     OF=0     IF=1
CONTROLS:   IR_EN=1   A_EN=0   B_EN=0   PDR_EN=0     PORT_EN=0    PORT_RD=1
           PC_EN=0   PC_LOAD=0    ALU_EN=0     ALU_OE=0     RAM_OE=0     RDR_EN=0
RAM_CS=1
I/O:        IO=[x]xxxxxxxx
```

```
TIME = 7450
CONTROL:    CLK=1     RST_=1
OPERATION: INSTRUCTION=[0000][1][1000000][000000000000][11111111]
           PHASE=DECODE OPCODE=0000 ADDR=[17]10111   I_DATA=[255]11111111
STORAGE:    MEM[0]=1 MEM[1]=128   MEM[2]=129
REGISTERS: A_REG=129     B_REG=1      RDR_REG=129 DIR_REG=1    PORT_REG=x
SIGNALS:    RAMDATA=x     ALUOUT=z     BUS=xxxxxxxx
FLAGS:      CF=0 ZF=0     SF=0     OF=0     IF=1
CONTROLS:   IR_EN=0   A_EN=1   B_EN=0   PDR_EN=0     PORT_EN=0    PORT_RD=1
           PC_EN=0   PC_LOAD=0    ALU_EN=0     ALU_OE=0     RAM_OE=0     RDR_EN=0
RAM_CS=1
I/O:        IO=[x]xxxxxxxx
```

```
TIME = 7550
CONTROL:    CLK=1     RST_=1
OPERATION: INSTRUCTION=[0000][1][1000000][000000000000][11111111]
           PHASE=EXECUTE     OPCODE=0000 ADDR=[17]10111   I_DATA=[255]11111111
STORAGE:    MEM[0]=1 MEM[1]=128   MEM[2]=129
REGISTERS: A_REG=255     B_REG=1      RDR_REG=129 DIR_REG=1    PORT_REG=x
SIGNALS:    RAMDATA=x     ALUOUT=z     BUS=xxxxxxxx
FLAGS:      CF=0 ZF=0     SF=0     OF=0     IF=1
CONTROLS:   IR_EN=0   A_EN=1   B_EN=0   PDR_EN=0     PORT_EN=0    PORT_RD=1
           PC_EN=0   PC_LOAD=0    ALU_EN=0     ALU_OE=0     RAM_OE=0     RDR_EN=0
RAM_CS=1
I/O:        IO=[x]xxxxxxxx
```

```
TIME = 7650
CONTROL:    CLK=1     RST_=1
OPERATION: INSTRUCTION=[0000][1][1000000][000000000000][11111111]
           PHASE=UPDATE OPCODE=0000 ADDR=[17]10111   I_DATA=[255]11111111
STORAGE:    MEM[0]=1 MEM[1]=128   MEM[2]=129
REGISTERS: A_REG=255     B_REG=1      RDR_REG=129 DIR_REG=1    PORT_REG=x
SIGNALS:    RAMDATA=x     ALUOUT=z     BUS=xxxxxxxx
FLAGS:      CF=0 ZF=0     SF=0     OF=0     IF=1
CONTROLS:   IR_EN=0   A_EN=0   B_EN=0   PDR_EN=0     PORT_EN=0    PORT_RD=1
           PC_EN=1   PC_LOAD=0    ALU_EN=0     ALU_OE=0     RAM_OE=0     RDR_EN=0
RAM_CS=1
I/O:        IO=[x]xxxxxxxx
```

LDI B, 127

0x0C10 007F

0	0	0	0	1	1	0	0	0	0	0	1	x	x	x	x	x	x	x	x	x	x	x	0	1	1	1	1	1	1	1

```
TIME = 7750
CONTROL:    CLK=1     RST_=1
OPERATION: INSTRUCTION=[0000][1][1000000][000000000000][11111111]
           PHASE=FETCH   OPCODE=0000 ADDR=[18]11000   I_DATA=[255]11111111
STORAGE:    MEM[0]=1 MEM[1]=128   MEM[2]=129
REGISTERS: A_REG=255     B_REG=1      RDR_REG=129 DIR_REG=1    PORT_REG=x
SIGNALS:    RAMDATA=x     ALUOUT=z     BUS=xxxxxxxx
FLAGS:      CF=0 ZF=0     SF=0     OF=0     IF=1
CONTROLS:   IR_EN=1   A_EN=0   B_EN=0   PDR_EN=0     PORT_EN=0    PORT_RD=1
           PC_EN=0   PC_LOAD=0    ALU_EN=0     ALU_OE=0     RAM_OE=0     RDR_EN=0
RAM_CS=1
I/O:        IO=[x]xxxxxxxx
```

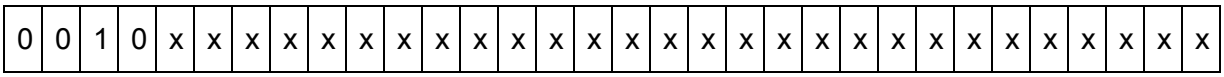
```
TIME = 7850
CONTROL:    CLK=1     RST_=1
OPERATION: INSTRUCTION=[0000][1][1000001][000000000000][01111111]
           PHASE=DECODE OPCODE=0000 ADDR=[18]11000   I_DATA=[127]01111111
STORAGE:    MEM[0]=1 MEM[1]=128   MEM[2]=129
```

```
REGISTERS: A_REG=255    B_REG=1     RDR_REG=129 DIR_REG=1   PORT_REG=x
SIGNALS:   RAMDATA=x    ALUOUT=z    BUS=xxxxxxxx
FLAGS:     CF=0 ZF=0    SF=0    OF=0    IF=1
CONTROLS:  IR_EN=0  A_EN=0  B_EN=1  PDR_EN=0    PORT_EN=0   PORT_RD=1
          PC_EN=0  PC_LOAD=0   ALU_EN=0    ALU_OE=0    RAM_OE=0    RDR_EN=0
RAM_CS=1
I/O:       IO=[x]xxxxxxxx
```

```
TIME = 7950
CONTROL:   CLK=1    RST_=1
OPERATION: INSTRUCTION=[0000][1][1000001][000000000000][01111111]
          PHASE=EXECUTE    OPCODE=0000 ADDR=[18]11000  I_DATA=[127]01111111
STORAGE:   MEM[0]=1 MEM[1]=128  MEM[2]=129
REGISTERS: A_REG=255    B_REG=127   RDR_REG=129 DIR_REG=1   PORT_REG=x
SIGNALS:   RAMDATA=x    ALUOUT=z    BUS=xxxxxxxx
FLAGS:     CF=0 ZF=0    SF=0    OF=0    IF=1
CONTROLS:  IR_EN=0  A_EN=0  B_EN=1  PDR_EN=0    PORT_EN=0   PORT_RD=1
          PC_EN=0  PC_LOAD=0   ALU_EN=0    ALU_OE=0    RAM_OE=0    RDR_EN=0
RAM_CS=1
I/O:       IO=[x]xxxxxxxx
```

```
TIME = 8050
CONTROL:   CLK=1    RST_=1
OPERATION: INSTRUCTION=[0000][1][1000001][000000000000][01111111]
          PHASE=UPDATE OPCODE=0000 ADDR=[18]11000  I_DATA=[127]01111111
STORAGE:   MEM[0]=1 MEM[1]=128  MEM[2]=129
REGISTERS: A_REG=255    B_REG=127   RDR_REG=129 DIR_REG=1   PORT_REG=x
SIGNALS:   RAMDATA=x    ALUOUT=z    BUS=xxxxxxxx
FLAGS:     CF=0 ZF=0    SF=0    OF=0    IF=1
CONTROLS:  IR_EN=0  A_EN=0  B_EN=0  PDR_EN=0    PORT_EN=0   PORT_RD=1
          PC_EN=1  PC_LOAD=0   ALU_EN=0    ALU_OE=0    RAM_OE=0    RDR_EN=0
RAM_CS=1
I/O:       IO=[x]xxxxxxxx
```

ADD A, B
0x2000 0000




```
TIME = 8150
CONTROL:   CLK=1    RST_=1
OPERATION: INSTRUCTION=[0000][1][1000001][000000000000][01111111]
           PHASE=FETCH  OPCODE=0000 ADDR=[19]11001  I_DATA=[127]01111111
STORAGE:   MEM[0]=1 MEM[1]=128  MEM[2]=129
REGISTERS: A_REG=255    B_REG=127   RDR_REG=129 DIR_REG=1   PORT_REG=x
SIGNALS:   RAMDATA=x    ALUOUT=z    BUS=xxxxxxxx
FLAGS:     CF=0 ZF=0    SF=0    OF=0    IF=1
CONTROLS:  IR_EN=1  A_EN=0  B_EN=0  PDR_EN=0    PORT_EN=0   PORT_RD=1
           PC_EN=0  PC_LOAD=0   ALU_EN=0    ALU_OE=0    RAM_OE=0    RDR_EN=0
RAM_CS=1
I/O:       IO=[x]xxxxxxxx
```

```
TIME = 8250
CONTROL:   CLK=1    RST_=1
OPERATION: INSTRUCTION=[0010][0][0000000][000000000000][00000000]
           PHASE=DECODE OPCODE=0010 ADDR=[19]11001  I_DATA=[0]00000000
STORAGE:   MEM[0]=1 MEM[1]=128  MEM[2]=129
REGISTERS: A_REG=255    B_REG=127   RDR_REG=129 DIR_REG=1   PORT_REG=x
SIGNALS:   RAMDATA=x    ALUOUT=z    BUS=xxxxxxxx
FLAGS:     CF=0 ZF=0    SF=0    OF=0    IF=0
CONTROLS:  IR_EN=0  A_EN=0  B_EN=0  PDR_EN=0    PORT_EN=0   PORT_RD=1
           PC_EN=0  PC_LOAD=0   ALU_EN=1    ALU_OE=0    RAM_OE=0    RDR_EN=0
RAM_CS=1
I/O:       IO=[x]xxxxxxxx
```

```
TIME = 8350
CONTROL:   CLK=1    RST_=1
OPERATION: INSTRUCTION=[0010][0][0000000][000000000000][00000000]
           PHASE=EXECUTE    OPCODE=0010 ADDR=[19]11001  I_DATA=[0]00000000
STORAGE:   MEM[0]=1 MEM[1]=128  MEM[2]=129
REGISTERS: A_REG=255    B_REG=127   RDR_REG=129 DIR_REG=1   PORT_REG=x
SIGNALS:   RAMDATA=x    ALUOUT=z    BUS=xxxxxxxx
FLAGS:     CF=1 ZF=0    SF=0    OF=0    IF=0
CONTROLS:  IR_EN=0  A_EN=0  B_EN=0  PDR_EN=0    PORT_EN=0   PORT_RD=1
```

```
          PC_EN=0   PC_LOAD=0    ALU_EN=1     ALU_OE=0     RAM_OE=0     RDR_EN=0
RAM_CS=1
I/O:        IO=[x]xxxxxxxx
```

```
TIME = 8450
CONTROL:    CLK=1     RST_=1
OPERATION: INSTRUCTION=[0010][0][0000000][000000000000][00000000]
          PHASE=UPDATE OPCODE=0010 ADDR=[19]11001   I_DATA=[0]00000000
STORAGE:    MEM[0]=1 MEM[1]=128   MEM[2]=129
REGISTERS: A_REG=255     B_REG=127    RDR_REG=129 DIR_REG=1    PORT_REG=x
SIGNALS:    RAMDATA=x     ALUOUT=z     BUS=xxxxxxxx
FLAGS:      CF=1 ZF=0     SF=0     OF=0     IF=0
CONTROLS:   IR_EN=0   A_EN=0   B_EN=0   PDR_EN=0     PORT_EN=0    PORT_RD=1
          PC_EN=1   PC_LOAD=0    ALU_EN=0     ALU_OE=0     RAM_OE=0     RDR_EN=0
RAM_CS=1
I/O:        IO=[x]xxxxxxxx
```

BC PC, 0x1B
0xC1B0 0000

1	1	0	0	x	x	x	1	1	0	1	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

```
TIME = 8550
CONTROL:    CLK=1     RST_=1
OPERATION: INSTRUCTION=[0010][0][0000000][000000000000][00000000]
          PHASE=FETCH   OPCODE=0010 ADDR=[1a]11010   I_DATA=[0]00000000
STORAGE:    MEM[0]=1 MEM[1]=128   MEM[2]=129
REGISTERS: A_REG=255     B_REG=127    RDR_REG=129 DIR_REG=1    PORT_REG=x
SIGNALS:    RAMDATA=x     ALUOUT=z     BUS=xxxxxxxx
FLAGS:      CF=1 ZF=0     SF=0     OF=0     IF=0
CONTROLS:   IR_EN=1   A_EN=0   B_EN=0   PDR_EN=0     PORT_EN=0    PORT_RD=1
          PC_EN=0   PC_LOAD=0    ALU_EN=0     ALU_OE=0     RAM_OE=0     RDR_EN=0
RAM_CS=1
I/O:        IO=[x]xxxxxxxx
```

```
TIME = 8650
```

```
CONTROL:   CLK=1    RST_=1
OPERATION: INSTRUCTION=[1100][0][0011011][000000000000][00000000]
           PHASE=DECODE OPCODE=1100 ADDR=[1a]11010  I_DATA=[0]00000000
STORAGE:   MEM[0]=1 MEM[1]=128  MEM[2]=129
REGISTERS: A_REG=255    B_REG=127   RDR_REG=129 DIR_REG=1   PORT_REG=x
SIGNALS:   RAMDATA=x    ALUOUT=z    BUS=xxxxxxxx
FLAGS:     CF=1 ZF=0    SF=0    OF=0    IF=0
CONTROLS:  IR_EN=0  A_EN=0  B_EN=0  PDR_EN=0    PORT_EN=0   PORT_RD=1
           PC_EN=0  PC_LOAD=0   ALU_EN=0    ALU_OE=0    RAM_OE=0    RDR_EN=0
RAM_CS=1
I/O:       IO=[x]xxxxxxxx
```

```
TIME = 8750
CONTROL:   CLK=1    RST_=1
OPERATION: INSTRUCTION=[1100][0][0011011][000000000000][00000000]
           PHASE=EXECUTE    OPCODE=1100 ADDR=[1a]11010  I_DATA=[0]00000000
STORAGE:   MEM[0]=1 MEM[1]=128  MEM[2]=129
REGISTERS: A_REG=255    B_REG=127   RDR_REG=129 DIR_REG=1   PORT_REG=x
SIGNALS:   RAMDATA=x    ALUOUT=z    BUS=xxxxxxxx
FLAGS:     CF=1 ZF=0    SF=0    OF=0    IF=0
CONTROLS:  IR_EN=0  A_EN=0  B_EN=0  PDR_EN=0    PORT_EN=0   PORT_RD=1
           PC_EN=0  PC_LOAD=0   ALU_EN=0    ALU_OE=0    RAM_OE=0    RDR_EN=0
RAM_CS=1
I/O:       IO=[x]xxxxxxxx
```

```
TIME = 8850
CONTROL:   CLK=1    RST_=1
OPERATION: INSTRUCTION=[1100][0][0011011][000000000000][00000000]
           PHASE=UPDATE OPCODE=1100 ADDR=[1a]11010  I_DATA=[0]00000000
STORAGE:   MEM[0]=1 MEM[1]=128  MEM[2]=129
REGISTERS: A_REG=255    B_REG=127   RDR_REG=129 DIR_REG=1   PORT_REG=x
SIGNALS:   RAMDATA=x    ALUOUT=z    BUS=xxxxxxxx
FLAGS:     CF=1 ZF=0    SF=0    OF=0    IF=0
CONTROLS:  IR_EN=0  A_EN=0  B_EN=0  PDR_EN=0    PORT_EN=0   PORT_RD=1
           PC_EN=1  PC_LOAD=1   ALU_EN=0    ALU_OE=0    RAM_OE=0    RDR_EN=0
RAM_CS=1
I/O:       IO=[x]xxxxxxxx
```

LDI A, 127

0x0C00 007F

0	0	0	0	1	1	0	0	0	0	0	0	x	x	x	x	x	x	x	x	x	x	x	0	1	1	1	1	1	1	1

```
TIME = 8950
CONTROL:   CLK=1    RST_=1
OPERATION: INSTRUCTION=[1100][0][0011011][000000000000][00000000]
           PHASE=FETCH  OPCODE=1100 ADDR=[1b]11011  I_DATA=[0]00000000
STORAGE:   MEM[0]=1 MEM[1]=128  MEM[2]=129
REGISTERS: A_REG=255    B_REG=127   RDR_REG=129 DIR_REG=1   PORT_REG=x
SIGNALS:   RAMDATA=x    ALUOUT=z    BUS=xxxxxxxx
FLAGS:     CF=1 ZF=0    SF=0    OF=0    IF=0
CONTROLS:  IR_EN=1  A_EN=0  B_EN=0  PDR_EN=0    PORT_EN=0   PORT_RD=1
           PC_EN=0  PC_LOAD=0   ALU_EN=0    ALU_OE=0    RAM_OE=0    RDR_EN=0
RAM_CS=1
I/O:       IO=[x]xxxxxxxx
TIME = 9050
CONTROL:   CLK=1    RST_=1
OPERATION: INSTRUCTION=[0000][1][1000000][000000000000][01111111]
           PHASE=DECODE OPCODE=0000 ADDR=[1b]11011  I_DATA=[127]01111111
STORAGE:   MEM[0]=1 MEM[1]=128  MEM[2]=129
REGISTERS: A_REG=255    B_REG=127   RDR_REG=129 DIR_REG=1   PORT_REG=x
SIGNALS:   RAMDATA=x    ALUOUT=z    BUS=xxxxxxxx
FLAGS:     CF=1 ZF=0    SF=0    OF=0    IF=1
CONTROLS:  IR_EN=0  A_EN=1  B_EN=0  PDR_EN=0    PORT_EN=0   PORT_RD=1
           PC_EN=0  PC_LOAD=0   ALU_EN=0    ALU_OE=0    RAM_OE=0    RDR_EN=0
RAM_CS=1
I/O:       IO=[x]xxxxxxxx
```

```
TIME = 9150
CONTROL:   CLK=1    RST_=1
OPERATION: INSTRUCTION=[0000][1][1000000][000000000000][01111111]
           PHASE=EXECUTE    OPCODE=0000 ADDR=[1b]11011  I_DATA=[127]01111111
STORAGE:   MEM[0]=1 MEM[1]=128  MEM[2]=129
```

```
REGISTERS: A_REG=127    B_REG=127   RDR_REG=129 DIR_REG=1   PORT_REG=x
SIGNALS:   RAMDATA=x    ALUOUT=z    BUS=xxxxxxxx
FLAGS:     CF=1 ZF=0    SF=0    OF=0    IF=1
CONTROLS:  IR_EN=0  A_EN=1  B_EN=0  PDR_EN=0    PORT_EN=0   PORT_RD=1
          PC_EN=0  PC_LOAD=0   ALU_EN=0    ALU_OE=0    RAM_OE=0    RDR_EN=0
RAM_CS=1
I/O:       IO=[x]xxxxxxxx
```

```
TIME = 9250
CONTROL:   CLK=1    RST_=1
OPERATION: INSTRUCTION=[0000][1][1000000][000000000000][01111111]
          PHASE=UPDATE OPCODE=0000 ADDR=[1b]11011  I_DATA=[127]01111111
STORAGE:   MEM[0]=1 MEM[1]=128  MEM[2]=129
REGISTERS: A_REG=127    B_REG=127   RDR_REG=129 DIR_REG=1   PORT_REG=x
SIGNALS:   RAMDATA=x    ALUOUT=z    BUS=xxxxxxxx
FLAGS:     CF=1 ZF=0    SF=0    OF=0    IF=1
CONTROLS:  IR_EN=0  A_EN=0  B_EN=0  PDR_EN=0    PORT_EN=0   PORT_RD=1
          PC_EN=1  PC_LOAD=0   ALU_EN=0    ALU_OE=0    RAM_OE=0    RDR_EN=0
RAM_CS=1
I/O:       IO=[x]xxxxxxxx
```

ADD A, B

0x2000 0000

0	0	1	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

```
TIME = 9350
CONTROL:   CLK=1    RST_=1
OPERATION: INSTRUCTION=[0000][1][1000000][000000000000][01111111]
          PHASE=FETCH  OPCODE=0000 ADDR=[1c]11100  I_DATA=[127]01111111
STORAGE:   MEM[0]=1 MEM[1]=128  MEM[2]=129
REGISTERS: A_REG=127    B_REG=127   RDR_REG=129 DIR_REG=1   PORT_REG=x
SIGNALS:   RAMDATA=x    ALUOUT=z    BUS=xxxxxxxx
FLAGS:     CF=1 ZF=0    SF=0    OF=0    IF=1
CONTROLS:  IR_EN=1  A_EN=0  B_EN=0  PDR_EN=0    PORT_EN=0   PORT_RD=1
          PC_EN=0  PC_LOAD=0   ALU_EN=0    ALU_OE=0    RAM_OE=0    RDR_EN=0
```

```
RAM_CS=1
I/O:        IO=[x]xxxxxxxx
```

```
TIME = 9450
CONTROL:    CLK=1     RST_=1
OPERATION: INSTRUCTION=[0010][0][0000000][000000000000][00000000]
           PHASE=DECODE OPCODE=0010 ADDR=[1c]11100   I_DATA=[0]00000000
STORAGE:    MEM[0]=1 MEM[1]=128   MEM[2]=129
REGISTERS: A_REG=127     B_REG=127    RDR_REG=129 DIR_REG=1    PORT_REG=x
SIGNALS:    RAMDATA=x     ALUOUT=z     BUS=xxxxxxxx
FLAGS:      CF=1 ZF=0     SF=0     OF=0     IF=0
CONTROLS:   IR_EN=0   A_EN=0   B_EN=0   PDR_EN=0     PORT_EN=0    PORT_RD=1
           PC_EN=0   PC_LOAD=0    ALU_EN=1     ALU_OE=0     RAM_OE=0     RDR_EN=0
RAM_CS=1
I/O:        IO=[x]xxxxxxxx
```

```
TIME = 9550
CONTROL:    CLK=1     RST_=1
OPERATION: INSTRUCTION=[0010][0][0000000][000000000000][00000000]
           PHASE=EXECUTE     OPCODE=0010 ADDR=[1c]11100   I_DATA=[0]00000000
STORAGE:    MEM[0]=1 MEM[1]=128   MEM[2]=129
REGISTERS: A_REG=127     B_REG=127    RDR_REG=129 DIR_REG=1    PORT_REG=x
SIGNALS:    RAMDATA=x     ALUOUT=z     BUS=xxxxxxxx
FLAGS:      CF=0 ZF=0     SF=1     OF=1     IF=0
CONTROLS:   IR_EN=0   A_EN=0   B_EN=0   PDR_EN=0     PORT_EN=0    PORT_RD=1
           PC_EN=0   PC_LOAD=0    ALU_EN=1     ALU_OE=0     RAM_OE=0     RDR_EN=0
RAM_CS=1
I/O:        IO=[x]xxxxxxxx
```

```
TIME = 9650
CONTROL:    CLK=1     RST_=1
OPERATION: INSTRUCTION=[0010][0][0000000][000000000000][00000000]
           PHASE=UPDATE OPCODE=0010 ADDR=[1c]11100   I_DATA=[0]00000000
STORAGE:    MEM[0]=1 MEM[1]=128   MEM[2]=129
REGISTERS: A_REG=127     B_REG=127    RDR_REG=129 DIR_REG=1    PORT_REG=x
SIGNALS:    RAMDATA=x     ALUOUT=z     BUS=xxxxxxxx
FLAGS:      CF=0 ZF=0     SF=1     OF=1     IF=0
```

```
CONTROLS:  IR_EN=0  A_EN=0  B_EN=0  PDR_EN=0    PORT_EN=0   PORT_RD=1
          PC_EN=1  PC_LOAD=0   ALU_EN=0    ALU_OE=0    RAM_OE=0    RDR_EN=0
RAM_CS=1
I/O:       IO=[x]xxxxxxxx
```

BV PC, 0x1E
0XB1E0 0000

1	0	1	1	x	x	x	1	1	1	1	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

```
TIME = 9750
CONTROL:   CLK=1    RST_=1
OPERATION: INSTRUCTION=[0010][0][0000000][000000000000][00000000]
          PHASE=FETCH  OPCODE=0010 ADDR=[1d]11101  I_DATA=[0]00000000
STORAGE:   MEM[0]=1 MEM[1]=128  MEM[2]=129
REGISTERS: A_REG=127    B_REG=127   RDR_REG=129 DIR_REG=1   PORT_REG=x
SIGNALS:   RAMDATA=x    ALUOUT=z    BUS=xxxxxxxx
FLAGS:     CF=0 ZF=0    SF=1    OF=1    IF=0
CONTROLS:  IR_EN=1  A_EN=0  B_EN=0  PDR_EN=0    PORT_EN=0   PORT_RD=1
          PC_EN=0  PC_LOAD=0   ALU_EN=0    ALU_OE=0    RAM_OE=0    RDR_EN=0
RAM_CS=1
I/O:       IO=[x]xxxxxxxx
```

```
TIME = 9850
CONTROL:   CLK=1    RST_=1
OPERATION: INSTRUCTION=[1011][0][0011110][000000000000][00000000]
          PHASE=DECODE OPCODE=1011 ADDR=[1d]11101  I_DATA=[0]00000000
STORAGE:   MEM[0]=1 MEM[1]=128  MEM[2]=129
REGISTERS: A_REG=127    B_REG=127   RDR_REG=129 DIR_REG=1   PORT_REG=x
SIGNALS:   RAMDATA=x    ALUOUT=z    BUS=xxxxxxxx
FLAGS:     CF=0 ZF=0    SF=1    OF=1    IF=0
CONTROLS:  IR_EN=0  A_EN=0  B_EN=0  PDR_EN=0    PORT_EN=0   PORT_RD=1
          PC_EN=0  PC_LOAD=0   ALU_EN=0    ALU_OE=0    RAM_OE=0    RDR_EN=0
RAM_CS=1
I/O:       IO=[x]xxxxxxxx
```

```
TIME = 9950
CONTROL:   CLK=1    RST_=1
OPERATION: INSTRUCTION=[1011][0][0011110][000000000000][00000000]
           PHASE=EXECUTE    OPCODE=1011 ADDR=[1d]11101  I_DATA=[0]00000000
STORAGE:   MEM[0]=1 MEM[1]=128  MEM[2]=129
REGISTERS: A_REG=127    B_REG=127   RDR_REG=129 DIR_REG=1   PORT_REG=x
SIGNALS:   RAMDATA=x    ALUOUT=z    BUS=xxxxxxxx
FLAGS:     CF=0 ZF=0    SF=1    OF=1    IF=0
CONTROLS:  IR_EN=0  A_EN=0  B_EN=0  PDR_EN=0    PORT_EN=0   PORT_RD=1
           PC_EN=0  PC_LOAD=0   ALU_EN=0    ALU_OE=0    RAM_OE=0    RDR_EN=0
RAM_CS=1
I/O:       IO=[x]xxxxxxxx
```

```
TIME = 10050
CONTROL:   CLK=1    RST_=1
OPERATION: INSTRUCTION=[1011][0][0011110][000000000000][00000000]
           PHASE=UPDATE OPCODE=1011 ADDR=[1d]11101  I_DATA=[0]00000000
STORAGE:   MEM[0]=1 MEM[1]=128  MEM[2]=129
REGISTERS: A_REG=127    B_REG=127   RDR_REG=129 DIR_REG=1   PORT_REG=x
SIGNALS:   RAMDATA=x    ALUOUT=z    BUS=xxxxxxxx
FLAGS:     CF=0 ZF=0    SF=1    OF=1    IF=0
CONTROLS:  IR_EN=0  A_EN=0  B_EN=0  PDR_EN=0    PORT_EN=0   PORT_RD=1
           PC_EN=1  PC_LOAD=1   ALU_EN=0    ALU_OE=0    RAM_OE=0    RDR_EN=0
RAM_CS=1
I/O:       IO=[x]xxxxxxxx
```

LDI PORT, 42

0x0C30 002A

0	0	0	0	1	1	0	0	0	0	1	1	x	x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	0	1	0

```
TIME = 10150
CONTROL:   CLK=1    RST_=1
OPERATION: INSTRUCTION=[1011][0][0011110][000000000000][00000000]
           PHASE=FETCH  OPCODE=1011 ADDR=[1e]11110  I_DATA=[0]00000000
STORAGE:   MEM[0]=1 MEM[1]=128  MEM[2]=129
```

```
REGISTERS: A_REG=127    B_REG=127   RDR_REG=129 DIR_REG=1   PORT_REG=x
SIGNALS:   RAMDATA=x    ALUOUT=z    BUS=xxxxxxxx
FLAGS:     CF=0 ZF=0    SF=1    OF=1    IF=0
CONTROLS:  IR_EN=1  A_EN=0  B_EN=0  PDR_EN=0    PORT_EN=0   PORT_RD=1
          PC_EN=0  PC_LOAD=0   ALU_EN=0    ALU_OE=0    RAM_OE=0    RDR_EN=0
RAM_CS=1
I/O:       IO=[x]xxxxxxxx
```

```
TIME = 10250
CONTROL:   CLK=1    RST_=1
OPERATION: INSTRUCTION=[0000][1][1000011][000000000000][00101010]
          PHASE=DECODE OPCODE=0000 ADDR=[1e]11110  I_DATA=[42]00101010
STORAGE:   MEM[0]=1 MEM[1]=128  MEM[2]=129
REGISTERS: A_REG=127    B_REG=127   RDR_REG=129 DIR_REG=1   PORT_REG=x
SIGNALS:   RAMDATA=x    ALUOUT=z    BUS=xxxxxxxx
FLAGS:     CF=0 ZF=0    SF=1    OF=1    IF=1
CONTROLS:  IR_EN=0  A_EN=0  B_EN=0  PDR_EN=0    PORT_EN=1   PORT_RD=1
          PC_EN=0  PC_LOAD=0   ALU_EN=0    ALU_OE=0    RAM_OE=0    RDR_EN=0
RAM_CS=1
I/O:       IO=[x]xxxxxxxx
TIME = 10350
CONTROL:   CLK=1    RST_=1
OPERATION: INSTRUCTION=[0000][1][1000011][000000000000][00101010]
          PHASE=EXECUTE    OPCODE=0000 ADDR=[1e]11110  I_DATA=[42]00101010
STORAGE:   MEM[0]=1 MEM[1]=128  MEM[2]=129
REGISTERS: A_REG=127    B_REG=127   RDR_REG=129 DIR_REG=1   PORT_REG=42
SIGNALS:   RAMDATA=42   ALUOUT=z    BUS=00101010
FLAGS:     CF=0 ZF=0    SF=1    OF=1    IF=1
CONTROLS:  IR_EN=0  A_EN=0  B_EN=0  PDR_EN=0    PORT_EN=1   PORT_RD=1
          PC_EN=0  PC_LOAD=0   ALU_EN=0    ALU_OE=0    RAM_OE=0    RDR_EN=0
RAM_CS=1
I/O:       IO=[42]00101010
```

```
TIME = 10450
CONTROL:   CLK=1    RST_=1
OPERATION: INSTRUCTION=[0000][1][1000011][000000000000][00101010]
          PHASE=UPDATE OPCODE=0000 ADDR=[1e]11110  I_DATA=[42]00101010
```

```
STORAGE:    MEM[0]=1 MEM[1]=128  MEM[2]=129
REGISTERS: A_REG=127    B_REG=127   RDR_REG=129 DIR_REG=1   PORT_REG=42
SIGNALS:    RAMDATA=42   ALUOUT=z    BUS=00101010
FLAGS:      CF=0 ZF=0    SF=1    OF=1    IF=1
CONTROLS:   IR_EN=0  A_EN=0  B_EN=0  PDR_EN=0    PORT_EN=0   PORT_RD=1
           PC_EN=1  PC_LOAD=0   ALU_EN=0    ALU_OE=0    RAM_OE=0    RDR_EN=0
RAM_CS=1
I/O:        IO=[42]00101010
```

IV. Conclusion

The ability to create a simulated, simple RISC machine in Verilog / SystemVerilog has been a highly rewarding endeavor and has given me a deep appreciation for abstraction. There were 4 issues encountered during the testing of this design, 3 of which involved changing the output of the memories and ALU to a combinational output. Once that was resolved, the last issue was encountered when outputting to the I/O. This was due to the testbench initialization of the inputs at the beginning of the program, and was remedied by bringing the port read signal into the testbench and using it as a flag for the assign statement.

A good portion of time was spent on writing the program and instructions themselves, and a full suit of test vectors were loaded onto the ROM via 4 program files. Each function of the RISC machine was tested under normal operating procedures, to success. As stated in the specifications, further improvements could be made to the design by creating a pipelined structure with branch flushing capabilities. Since the data processed is 8-bits wide and the clock period is an arbitrary 100ns, a pipelined design would improve the throughput of the machine from its current value of $\frac{8bits}{400ns} = 20Mb/s$ to $\frac{8}{100ns} = 80Mb/s$, which is a 120% improvement over my current implementation to output the answer of life, the universe, and everything.

Appendix

Note: Only modules created explicitly for this experiment have been documented in this appendix. Remaining modules remain the same as their previous iterations, except where explained in the report. A zip file has been included with this report, with the full design and output.

Code:

Top Module: RISCY.sv

```
/**********************************************************************
ECE 526/L
Experiment 10: RISC-Y
Developer: Joel Bailey
**********************************************************************
File Name: RISCY.sv
Date Created: 20201130
Date Last Modified: 20201203
```

```
Module Purpose: Top level of a reduced instruction set computer (RISC).
This top level instantiates the following modules:
   - AASD Reset
   - Phase Generator, with phaser
   - Program Counter
   - Instruction Register
   - Port Direction Register
   - Read-only Memory
   - Random Access Memory
   - (2) Tri-state Buffers
   - Port Data Register
   - A Register
   - B Register
   - 2 to 1 Multiplexer
   - Arithmetic Unit (ALU)
   - Ram Data Register
**************************************************************************/

`timescale 1 ns / 100 ps
module RISCY (CLK, RST_, IO);
input CLK, RST_;
inout [7:0] IO;

   reg EN, CF, OF, SF, ZF;
   reg [31:0] ROM_OUT, CMD;
   reg [7:0] RDR_OUT, DATA, AOUT, BOUT, PORT_OUT;
   wire [7:0] BUS;
   reg [6:0] ADDR;
   reg [4:0] ROM_ADDR;
   reg AASD_RESET_;
   reg IR_EN, A_EN, B_EN, PDR_EN, PORT_EN, PORT_RD, PC_EN,
      PC_LOAD, ALU_EN, ALU_OE, RAM_OE, RDR_EN, RAM_CS, DIR;

   AASD RESETTER(
       .CLK(CLK),
       .RST_(RST_),
       .AASD_OUT_(AASD_RESET_)
   );
```

```
PHASE_GENERATOR PHASEGEN(
    .CLK(CLK),
    .RST_(AASD_RESET_),
    .EN(1'b1),
    .ADDR(CMD[26:20]),
    .OPCODE(CMD[31:28]),
    .ZF(ZF),
    .OF(OF),
    .SF(SF),
    .CF(CF),
    .IF(CMD[27]),
    .IR_EN(IR_EN),
    .A_EN(A_EN),
    .B_EN(B_EN),
    .PDR_EN(PDR_EN),
    .PORT_EN(PORT_EN),
    .PORT_RD(PORT_RD),
    .PC_EN(PC_EN),
    .PC_LOAD(PC_LOAD),
    .ALU_EN(ALU_EN),
    .ALU_OE(ALU_OE),
    .RAM_OE(RAM_OE),
    .RAM_CS(RAM_CS),
    .RDR_EN(RDR_EN)
);

COUNTER #(.WIDTH(5)) PC (
    .CLK(CLK),
    .RST_(AASD_RESET_),
    .EN(PC_EN),
    .LD(PC_LOAD),
    .DATA(CMD[24:20]),
    .COUNT(ROM_ADDR)
);

ROM #(.WIDTH(32), .DEPTH(32)) ROM0 (
    .CS_(1'b0),
```

```
    .OE(1'b1),
    .ADDR(ROM_ADDR),
    .DOUT(ROM_OUT)
);

REG #(.WIDTH(32)) IR (
    .CLK(CLK),
    .EN(IR_EN),
    .D(ROM_OUT),
    .Q(CMD)
);

RAM #(.WIDTH(8), .DEPTH(32)) RAM0 (
    .CLK(CLK),
    .WS(CLK),
    .OE(RAM_OE),
    .CS_(RAM_CS),
    .ADDR(CMD[4:0]),
    .DATA(BUS)
);

REG #(.WIDTH(8)) RDR (
    .CLK(CLK),
    .EN(RDR_EN),
    .D(BUS),
    .Q(RDR_OUT)
);

MUX2_1 #(.WIDTH(8)) DATAMUX (
    .A(CMD[7:0]),
    .B(RDR_OUT),
    .SEL(RAM_OE),
    .OUT(DATA)
);

RESET_REG #(.WIDTH(8)) AREG (
    .CLK(CLK),
    .RST_(AASD_RESET_),
```

```
    .EN(A_EN),
    .D(DATA),
    .Q(AOUT)
);

RESET_REG #(.WIDTH(8)) BREG (
    .CLK(CLK),
    .RST_(AASD_RESET_),
    .EN(B_EN),
    .D(DATA),
    .Q(BOUT)
);

ALU #(.WIDTH(8)) ALUNIT (
    .CLK(CLK),
    .EN(ALU_EN),
    .OE(ALU_OE),
    .OPCODE(CMD[31:28]),
    .A(AOUT),
    .B(BOUT),
    .ALU_OUT(BUS),
    .CF(CF),
    .OF(OF),
    .SF(SF),
    .ZF(ZF)
);

RESET_REG #(.WIDTH(1)) PDR ( //RESETS TO 0, READ IO
    .CLK(CLK),
    .RST_(AASD_RESET_),
    .EN(PDR_EN),
    .D(DATA[0]),
    .Q(DIR)
);

REG #(.WIDTH(8)) PORTDATA (
    .CLK(CLK),
    .EN(PORT_EN),
```

```
        .D(DATA),
        .Q(PORT_OUT)
    );

    TRISTATE #(.WIDTH(8)) INNOUT (
        .DIN(PORT_OUT),
        .CTRL(DIR),
        .DOUT(IO)
    );

    TRISTATE #(.WIDTH(8)) IO_BUS (
        .DIN(IO),
        .CTRL(PORT_RD),
        .DOUT(BUS)
    );

endmodule
```

Module: TRISTATE.sv

```
/*************************************************************************
ECE 526/L
Experiment 10: RISC-Y
Developer: Joel Bailey
*************************************************************************
File Name: TRISTATE.sv
Date Created: 20201130
Date Last Modified: 20201203
Module Purpose: Scalable Tristate Buffer
*************************************************************************/

`timescale 1 ns / 100 ps

module TRISTATE(DIN, CTRL, DOUT);
parameter WIDTH = 8;

input [WIDTH - 1 : 0] DIN;
```

```
input CTRL;
output reg [WIDTH - 1 : 0] DOUT;

   always_comb begin
       if (CTRL)
           DOUT = DIN;
       else
           DOUT = {WIDTH{1'bz}};
   end

endmodule
```

Module: RESET_REG.sv

```
/**********************************************************************
ECE 526/L
Experiment 6: Sum of products
Developer: Joel Bailey
**********************************************************************
File Name: RESISTER.sv
Date Created: 20201019
Date Last Modified: 20201022

Module Purpose:
AASD D-FF
**********************************************************************/
`timescale 1 ns / 100 ps

module RESET_REG(CLK, RST_, EN, D, Q);
parameter WIDTH = 4;

   input CLK, EN, RST_;
   input [WIDTH - 1 : 0] D;
   output reg [WIDTH - 1 : 0] Q;

   always @(posedge CLK, negedge RST_) begin
       if (!RST_)
           Q <= 0;
```

```
        else
            if (EN)
                Q <= D;
    end

endmodule
```

Module: REG.sv

```
/**********************************************************************
ECE 526/L
Experiment 6: Sum of products
Developer: Joel Bailey
**********************************************************************
File Name: RESISTER.sv
Date Created: 20201019
Date Last Modified: 20201022

Module Purpose:
D-FF NO RESET
**********************************************************************/
`timescale 1 ns / 100 ps

module REG(CLK, EN, D, Q);
parameter WIDTH = 4;

    input CLK, EN;
    input [WIDTH - 1 : 0] D;
    output reg [WIDTH - 1 : 0] Q;

    always @(posedge CLK) begin
        if (EN)
            Q <= D;
    end

endmodule
```

Test bench:

```
 `timescale 1 ns / 100 ps

module TESTBENCH;

   reg CLK, RST_;
   wire [7:0] IO;
   reg [7:0] INPUT;

   RISCY RISC (
       .CLK(CLK),
       .RST_(RST_),
       .IO(IO)
   );

   initial
   $monitorb ("\nTIME = %0d\n", $time,
              "CONTROL:   CLK=%0b\tRST_=%0b\n", CLK, RST_,
              "OPERATION: INSTRUCTION=[%b][%b][%b][%b][%b]\n", RISC.CMD[31:28], RISC.CMD[27],
RISC.CMD[26:20], RISC.CMD[19:8], RISC.CMD[7:0],
              "           PHASE=%s\tOPCODE=%b\tADDR=[%h]%b\tI_DATA=[%0d]%b\n",  RISC.PHASEGEN.PSIG,
RISC.CMD[31:28], RISC.ROM_ADDR, RISC.ROM_ADDR, RISC.DATA, RISC.DATA,
              "STORAGE:   MEM[0]=%0d\tMEM[1]=%0d\tMEM[2]=%0d\n", RISC.RAM0.MEM[0],
RISC.RAM0.MEM[1], RISC.RAM0.MEM[2],
              "REGISTERS: A_REG=%0d\tB_REG=%0d  \tRDR_REG=%0d\tDIR_REG=%0d\tPORT_REG=%0d\n",
RISC.AREG.Q, RISC.BREG.Q, RISC.RDR.Q, RISC.PDR.Q, RISC.PORTDATA.Q,
              "SIGNALS:   RAMDATA=%0d\tALUOUT=[%0d]%b\tBUS=%b\n", RISC.RAM0.DATA, RISC.ALUNIT.TMP
,RISC.ALUNIT.TMP, RISC.BUS,
              "FLAGS:     CF=%b\tZF=%b\tSF=%b\tOF=%b\tIF=%b\n", RISC.CF, RISC.ZF, RISC.SF, RISC.OF,
RISC.CMD[27],
              "CONTROLS:  IR_EN=%b\tA_EN=%b\tB_EN=%b\tPDR_EN=%b\tPORT_EN=%b\tPORT_RD=%b\n",
RISC.IR_EN, RISC.A_EN, RISC.B_EN, RISC.PDR_EN, RISC.PORT_EN, RISC.PORT_RD,
              "
PC_EN=%b\tPC_LOAD=%b\tALU_EN=%b\tALU_OE=%b\tRAM_OE=%b\tRDR_EN=%b\tRAM_CS=%b\n", RISC.PC_EN,
RISC.PC_LOAD, RISC.ALU_EN, RISC.ALU_OE, RISC.RAM_OE, RISC.RDR_EN, RISC.RAM_CS,
              "I/O:       IO=[%0d]%b\n", RISC.IO, RISC.IO,
               );
```

```
    //begin clock
    initial begin
        CLK <= 0;
        forever begin
        #50 CLK <= ~CLK;
        end
    end

    assign IO = (RISC.PDR.Q == 1'b0) ? INPUT : {8{1'bz}};

    //reset
    initial begin
        RST_ <= 0; INPUT = 8'b00000001;
        #100;
        RST_ <= 1;
        #400;
        INPUT = 8'b10000000;
        #10000;
        $finish;
    end

endmodule
```

ROM Files:

Prog1.mem: 14300000 14300001 04000000 04100001 20000000 10000002 A0800000

Prog2.mem: 0C100001 30000000 10000003 90F00000

Prog3.mem: 04000002 40000000 50000000 60000000 70000000 81600000

Prog4.mem: 0C200001 0C0000FF 0C10007F 20000000 C1B00000 0C00007F 20000000
B1E00000 0C30002A