TPS763 Low-Power 150-mA Low-Dropout Linear Regulators

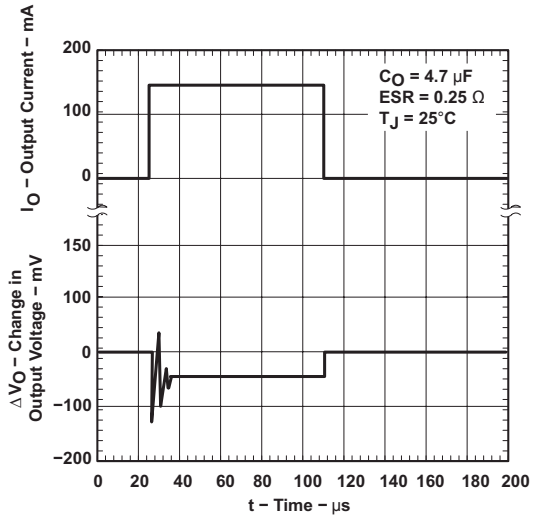
1 Features

- 150-mA Low-Dropout Regulator
- Output Voltage: 5 V, 3.8 V, 3.3 V, 3 V, 2.8 V, 2.7 V, 2.5 V, 1.8 V, 1.6 V, and Variable
- Dropout Voltage, Typically 300 mV at 150 mA
- Thermal Protection
- Over Current Limitation
- Less Than 2-µA Quiescent Current in Shutdown Mode
- –40°C to 125°C Operating Junction Temperature Range
- 5-Pin SOT-23 (DBV) Package

2 Applications

- Electricity Meters
- Solar Inverters
- HVAC Systems
- Servo Drives and Motion Control
- Sensor Transmitters

TPS76350 Load Transient Response



3 Description

The TPS763xx family of low-dropout (LDO) voltage regulators offers the benefits of low-dropout voltage, low-power operation, and miniaturized packaging. These regulators feature low dropout voltages and quiescent currents compared to conventional LDO regulators. Offered in a 5-pin, small outline integrated-circuit SOT-23 package, the TPS763xx series devices are ideal for cost-sensitive designs and for applications where board space is at a premium.

A combination of new circuit design and process innovation has enabled the usual pnp pass transistor to be replaced by a PMOS pass element. Because the PMOS pass element behaves as a low-value resistor, the dropout voltage is low—typically 300 mV at 150 mA of load current (TPS76333)—and is directly proportional to the load current. Because the PMOS pass element is a voltage-driven device, the quiescent current is low (140 µA maximum) and is stable over the entire range of output load current (0 mA to 150 mA). Intended for use in portable systems such as laptops and cellular phones, the low-dropout voltage feature and low-power operation result in a significant increase in system battery operating life.

The TPS763xx also features a logic-enabled sleep mode to shut down the regulator, reducing quiescent current to 1 µA maximum at T_J = 25°C.The TPS763xx is offered in 1.6-V ,1.8-V, 2.5-V, 2.7-V, 2.8-V, 3-V, 3.3-V, 3.8-V, and 5-V fixed-voltage versions and in a variable version (programmable over the range of 1.5 V to 6.5 V).

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS763xx	SOT-23 (5)	2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

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4 Revision History

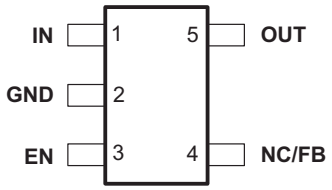
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision H (January 2004) to Revision I **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Deleted Legacy Applications and Non-Ceramic Capacitor Stability from *Applications* ... 1
- Added Electricity Meters, Solar Inverters, HVAC Systems, Servo Drives and Motion Control, and Sensor Transmitters to *Applications* ... 1
- Deleted *Dissipation Ratings* table ... 3
- Added *Thermal Information* table ... 4

5 Pin Configuration and Functions

DBV Package
5-Pin SOT-23
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	IN	I	Input supply voltage
2	GND	—	Ground
3	EN	I	Enable input
4	NC/FB	—/I	No connection (fixed-voltage option only) or feedback voltage (TPS76301 only)
5	OUT	O	Regulated output voltage

6 Specifications

7 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Input voltage	–0.3	10	V
Voltage at EN	–0.3	V_I + 0.3	V
Voltage on OUT, FB		7	V
Peak output current	Internally limited		
Operating junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

8 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

9 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_I	Input voltage(1)	2.7	10	V
I_O	Continuous output current	0	150	mA
T_J	Operating junction temperature	–40	125	°C

(1) To calculate the minimum input voltage for your maximum output current, use the following equation: $V_{I(min)} = V_{O(max)} + V_{DO(max\ load)}$

10 Thermal Information

THERMAL METRIC[1]		TPS763xx DBV (SOT-23) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	205.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	125.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	34.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	15.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	33.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

11 Electrical Characteristics

over recommended operating free-air temperature range, $V_I = V_{O(typ)} + 1$ V, $I_O = 1$ mA, EN = IN, and $C_O = 4.7$ µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_O	Output voltage	TPS76301	3.25 V > V_I ≥ 2.7 V, 2.5 V ≥ V_O ≥ 1.5 V, I_O = 1 mA to 75 mA, T_J = 25°C	0.98 × V_O	V_O	1.02 × V_O	V
			3.25 V > V_I ≥ 2.7 V, 2.5 V ≥ V_O ≥ 1.5 V, I_O = 1 mA to 75 mA	0.97 × V_O	V_O	1.03 × V_O	
			V_I ≥ 3.25 V, 5 V ≥ V_O ≥ 1.5 V, I_O = 1 mA to 100 mA, T_J = 25°C	0.98 × V_O	V_O	1.02 × V_O	
			V_I ≥ 3.25 V, 5 V ≥ V_O ≥ 1.5 V, I_O = 1 mA to 100 mA	0.97 × V_O	V_O	1.03 × V_O	
			V_I ≥ 3.25 V, 5 V ≥ V_O ≥ 1.5 V, I_O = 1 mA to 150 mA, T_J = 25°C	0.975 × V_O	V_O	1.025 × V_O	
			V_I ≥ 3.25 V, 5 V ≥ V_O ≥ 1.5 V, I_O = 1 mA to 150 mA	0.9625 × V_O	V_O	1.0375 × V_O	
		TPS76316	V_I = 2.7 V, 1 mA < I_O < 75 mA, T_J = 25°C	1.568	1.6	1.632	
			V_I = 2.7 V, 1 mA < I_O < 75 mA	1.552	1.6	1.648	
			V_I = 3.25 V, 1 mA < I_O < 100 mA, T_J = 25°C	1.568	1.6	1.632	
			V_I = 3.25 V, 1 mA < I_O < 100 mA	1.552	1.6	1.648	
			V_I = 3.25 V, 1 mA < I_O < 150 mA, T_J = 25°C	1.56	1.6	1.64	
			V_I = 3.25 V, 1 mA < I_O < 150 mA	1.536	1.6	1.664	
		TPS76318	V_I = 2.7 V, 1 mA < I_O < 75 mA, T_J = 25°C	1.764	1.8	1.836	
			V_I = 2.7 V, 1 mA < I_O < 75 mA	1.746	1.8	1.854	
			V_I = 3.25 V, 1 mA < I_O < 100 mA, T_J = 25°C	1.764	1.8	1.836	
			V_I = 3.25 V, 1 mA < I_O < 100 mA	1.746	1.8	1.854	
			V_I = 3.25 V, 1 mA < I_O < 150 mA, T_J = 25°C	1.755	1.8	1.845	
			V_I = 3.25 V, 1 mA < I_O < 150 mA	1.733	1.8	1.867	

Electrical Characteristics (continued)

over recommended operating free-air temperature range, $V_I = V_{O(typ)} + 1$ V, $I_O = 1$ mA, EN = IN, and $C_O = 4.7$ µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_O	Output voltage (continued)	TPS76325	I_O = 1 mA to 100 mA, T_J = 25°C	2.45	2.5	2.55	V
			I_O = 1 mA to 100 mA	2.425	2.5	2.575	
			I_O = 1 mA to 150 mA, T_J = 25°C	2.438	2.5	2.562	
			I_O = 1 mA to 150 mA	2.407	2.5	2.593	
		TPS76327	I_O = 1 mA to 100 mA, T_J = 25°C	2.646	2.7	2.754	
			I_O = 1 mA to 100 mA	2.619	2.7	2.781	
			I_O = 1 mA to 150 mA, T_J = 25°C	2.632	2.7	2.767	
			I_O = 1 mA to 150 mA	2.599	2.7	2.801	
		TPS76328	I_O = 1 mA to 100 mA, T_J = 25°C	2.744	2.8	2.856	
			I_O = 1 mA to 100 mA	2.716	2.8	2.884	
			I_O = 1 mA to 150 mA, T_J = 25°C	2.73	2.8	2.87	
			I_O = 1 mA to 150 mA	2.695	2.8	2.905	
		TPS76330	I_O = 1 mA to 100 mA, T_J = 25°C	2.94	3	3.06	
			I_O = 1 mA to 100 mA	2.91	3	3.09	
			I_O = 1 mA to 150 mA, T_J = 25°C	2.925	3	3.075	
			I_O = 1 mA to 150 mA	2.888	3	3.112	
		TPS76333	I_O = 1 mA to 100 mA, T_J = 25°C	3.234	3.3	3.366	
			I_O = 1 mA to 100 mA	3.201	3.3	3.399	
			I_O = 1 mA to 150 mA, T_J = 25°C	3.218	3.3	3.382	
			I_O = 1 mA to 150 mA	3.177	3.3	3.423	
		TPS76338	I_O = 1 mA to 100 mA, T_J = 25°C	3.724	3.8	3.876	
			I_O = 1 mA to 100 mA	3.705	3.8	3.895	
			I_O = 1 mA to 150 mA, T_J = 25°C	3.686	3.8	3.914	
			I_O = 1 mA to 150 mA	3.667	3.8	3.933	
		TPS76350	I_O = 1 mA to 100 mA, T_J = 25°C	4.875	5	5.125	
			I_O = 1 mA to 100 mA	4.825	5	5.175	
			I_O = 1 mA to 150 mA, T_J = 25°C	4.75	5	5.15	
			I_O = 1 mA to 150 mA	4.8	5	5.2	
$I_{(Q)}$	Quiescent current (GND pin current)	I_O = 1 mA to 150 mA, T_J = 25°C(1)			85	100	µA
		I_O = 1 mA to 150 mA(2)				140	
	Standby current	EN < 0.5 V, T_J = 25°C			0.5	1	µA
		EN < 0.5 V				2	
V_n	Output noise voltage	BW = 300 Hz to 50 kHz, T_J = 25°C, C_O = 10 µF(2)			140		µV
PSRR	Ripple rejection	f = 1 kHz, C_O = 10 µF, T_J = 25°C(2)			60		dB
	Current limit	T_J = 25°C(3)		0.5	0.8	1.5	A
	Output voltage line regulation ($\Delta V_O/V_O$)(3)	V_O + 1 V < V_I ≤ 10 V, V_I ≥ 3.5 V, T_J = 25°C			0.04%	0.07%	V
		V_O + 1 V < V_I ≤ 10 V, V_I ≥ 3.5 V				0.1%	
V_{IH}	EN high level input(2)				1.4	2	V
V_{IL}	EN low level input(2)			0.5	1.2		V

(1) Minimum IN operating voltage is 2.7 V or $V_{O(typ)} + 1$ V, whichever is greater.
(2) Test conditions includes output voltage $V_O = 0$ V (for variable device FB is shorted to V_O), and pulse duration = 10 mS.
(3) If V_O < 2.5 V and V_{Imax} = 10 V, V_{Imin} = 3.5 V:

$$\text{Line Reg. (mV)} = (\%/\text{V}) \times \frac{V_O(V_{Imax} - 3.5\ \text{V})}{100} \times 1000$$

If V_O > 2.5 V and V_{Imax} = 10 V, V_{Imin} = VO + 1 V:

$$\text{Line Reg. (mV)} = (\%/\text{V}) \times \frac{V_O(V_{Imax} - (V_O + 1))}{100} \times 1000$$

Electrical Characteristics (continued)

over recommended operating free-air temperature range, $V_I = V_{O(typ)} + 1$ V, $I_O = 1$ mA, EN = IN, and $C_O = 4.7$ µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_I	EN input current	EN = 0 V			–0.01	–0.5	µA
		EN = IN			–0.01	–0.5	
V_{DO}	Dropout voltage	TPS76325	I_O = 0 mA, T_J = 25°C		0.2		mV
			I_O = 1 mA, T_J = 25°C		3		
			I_O = 50 mA, T_J = 25°C		120	150	
			I_O = 50 mA			200	
			I_O = 75 mA, T_J = 25°C		180	225	
			I_O = 75 mA			300	
			I_O = 100 mA, T_J = 25°C		240	300	
			I_O = 100 mA			400	
			I_O = 150 mA, T_J = 25°C		360	450	
			I_O = 150 mA			600	
		TPS76333	I_O = 0 mA, T_J = 25°C		0.2		
			I_O = 1 mA, T_J = 25°C		3		
			I_O = 50 mA, T_J = 25°C		100	125	
			I_O = 50 mA			166	
			I_O = 75 mA, T_J = 25°C		150	188	
			I_O = 75 mA			250	
			I_O = 100 mA, T_J = 25°C		200	250	
			I_O = 100 mA			333	
			I_O = 150 mA, T_J = 25°C		300	375	
			I_O = 150 mA			500	
		TPS76350	I_O = 0 mA, T_J = 25°C		0.2		
			I_O = 1 mA, T_J = 25°C		2		
			I_O = 50 mA, T_J = 25°C		60	75	
			I_O = 50 mA			100	
			I_O = 75 mA, T_J = 25°C		90	113	
			I_O = 75 mA			150	
			I_O = 100 mA, T_J = 25°C		120	150	
			I_O = 100 mA			200	
			I_O = 150 mA, T_J = 25°C		180	225	
			I_O = 150 mA			300	

11.1 Typical Characteristics

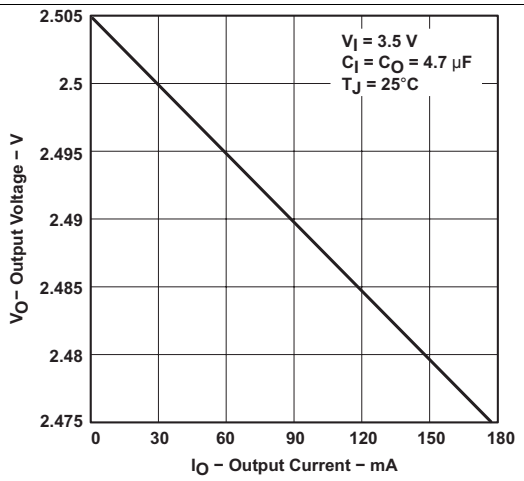


Figure 1. TPS76325 Output Voltage vs Output Current

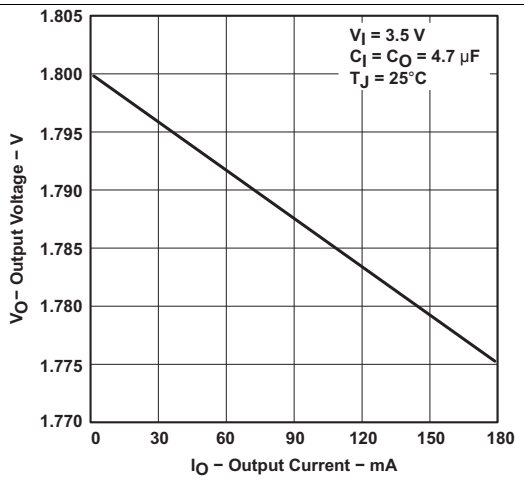


Figure 2. TPS76318 Output Voltage vs Output Current

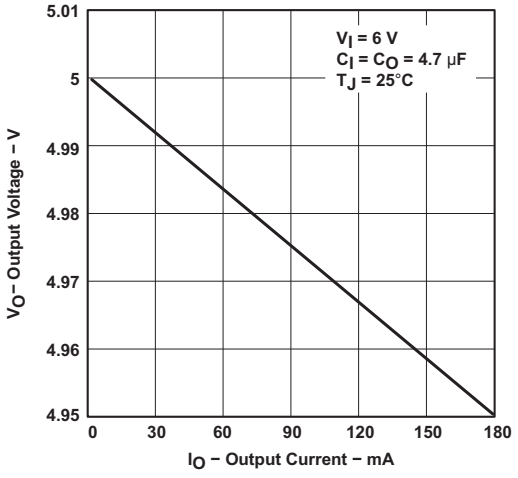


Figure 3. TPS76350 Output Voltage vs Output Current

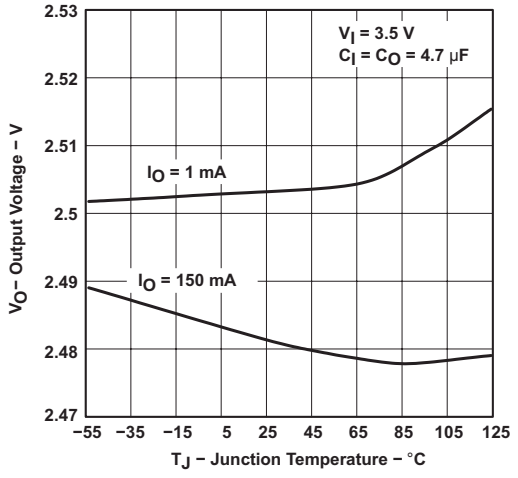


Figure 4. TPS76325 Output Voltage vs Output Current

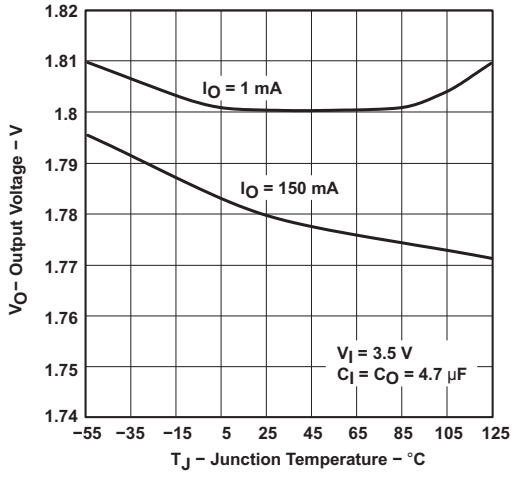


Figure 5. TPS76318 Output Voltage vs Free-Air Temperature

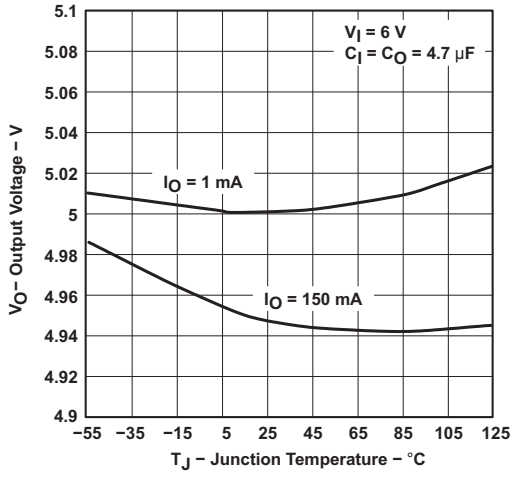


Figure 6. TPS76350 Output Voltage vs Free-Air Temperature

Typical Characteristics (continued)

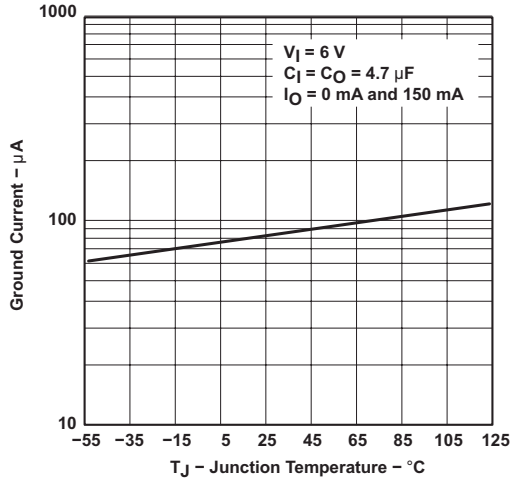


Figure 7. TPS76350 Ground Current vs Free-Air Temperature

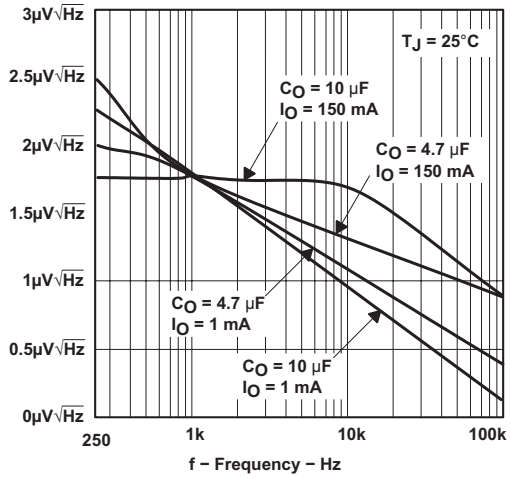


Figure 8. Output Noise vs Frequency

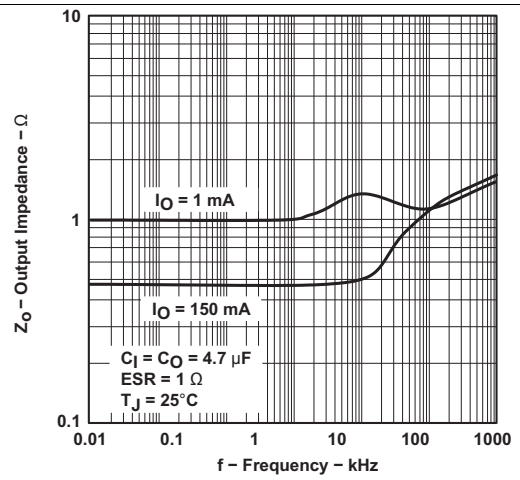


Figure 9. Output Impedance vs Frequency

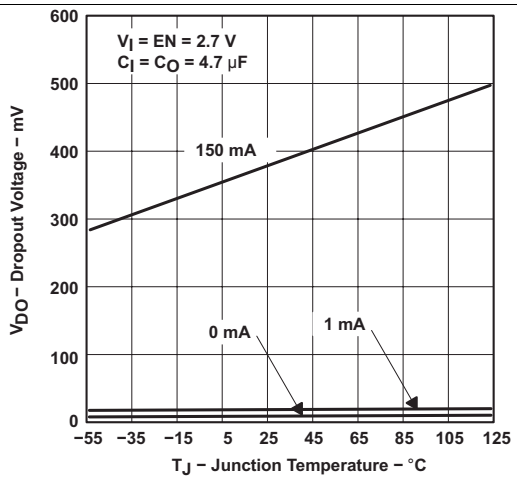


Figure 10. TPS76325 Dropout Voltage vs Free-Air Temperature

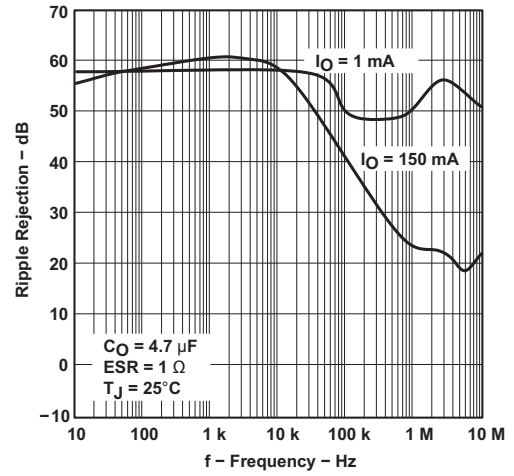


Figure 11. TPS76325 Ripple Rejection vs Frequency

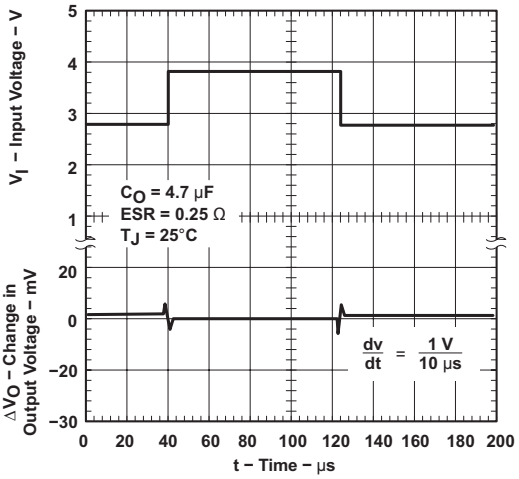


Figure 12. TPS76318 Line Transient Response

Typical Characteristics (continued)

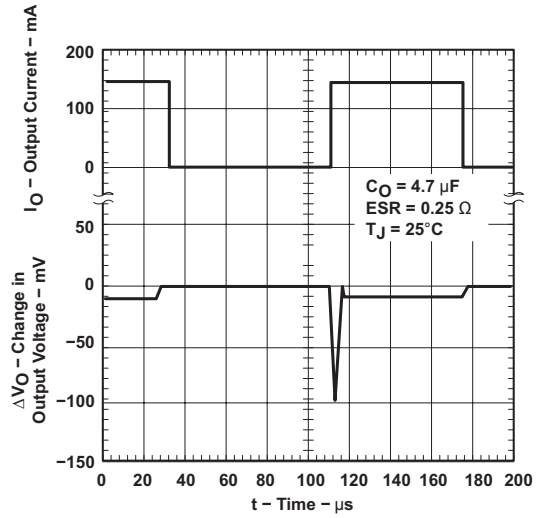


Figure 13. TPS76318 Load Transient Response

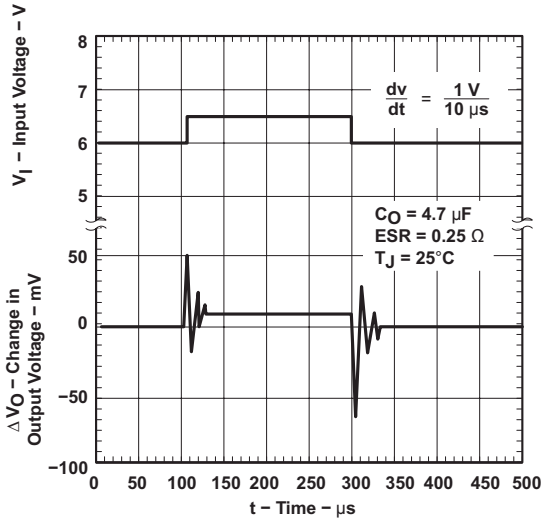


Figure 14. TPS76350 Line Transient Response

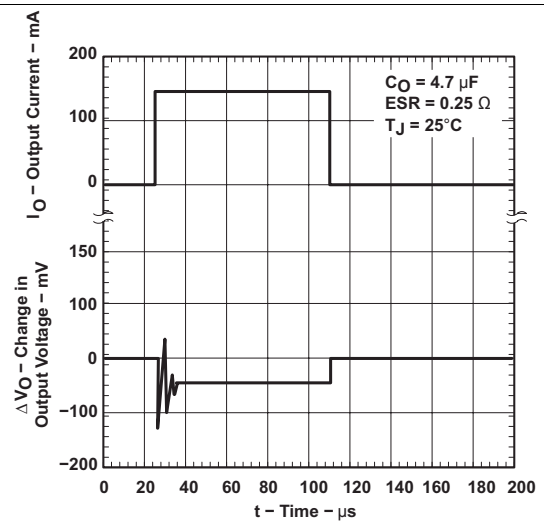


Figure 15. TPS76350 Load Transient Response

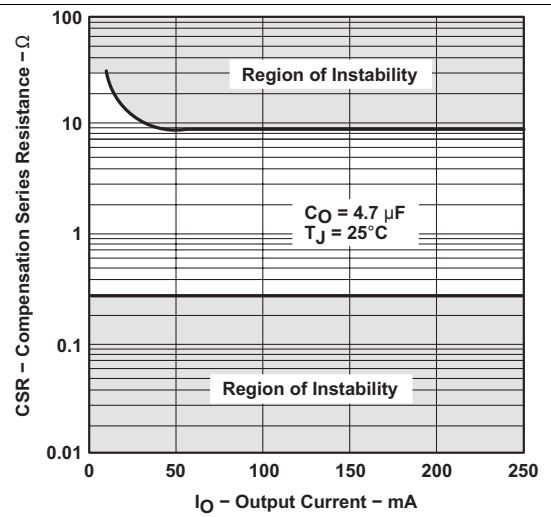


Figure 16. Compensation Series Resistance (CSR) vs Output Current

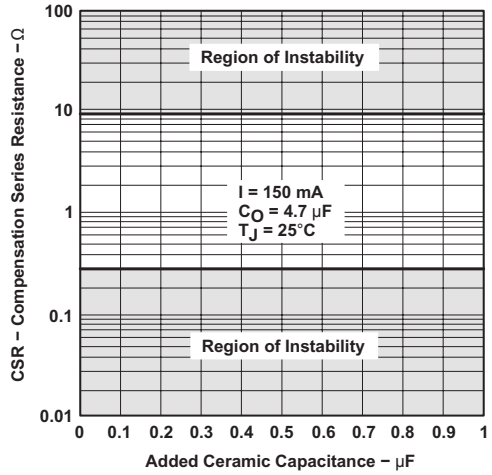


Figure 17. Compensation Series Resistance (CSR) vs Added Ceramic Capacitance

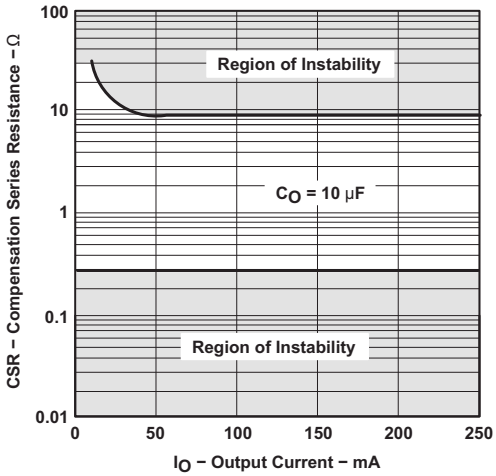


Figure 18. Compensation Series Resistance (CSR) vs Output Current

Typical Characteristics (continued)

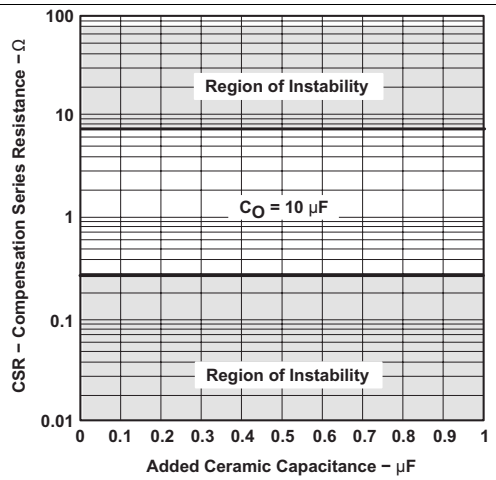


Figure 19. Compensation Series Resistance (CSR) vs Added Ceramic Capacitance

12 Detailed Description

12.1 Overview

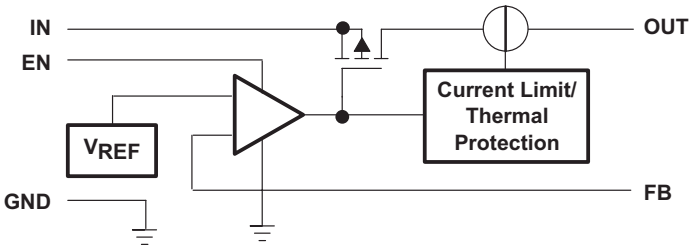
The TPS763xx devices uses a PMOS pass element to dramatically reduce both dropout voltage and supply current over more conventional PNP pass element LDO designs. The PMOS pass element is a voltage-controlled device that, unlike a PNP transistor, does not require increased drive current as output current increases. Supply current in the TPS763xx is essentially constant from no-load to maximum load.

Current limiting and thermal protection prevent damage by excessive output current and/or power dissipation. The device switches into a constant-current mode at approximately 1 A; further load reduces the output voltage instead of increasing the output current. The thermal protection shuts the regulator off if the junction temperature rises above 165°C. Recovery is automatic when the junction temperature drops approximately 25°C below the high temperature trip point. The PMOS pass element includes a back diode that safely conducts reverse current when the input voltage level drops below the output voltage level.

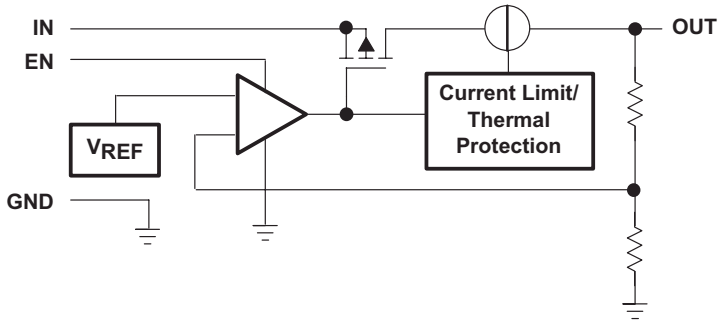
A logic low on the enable input, EN shuts off the output and reduces the supply current to less than 2 µA. EN must be tied high in applications where the shutdown feature is not used.

12.2 Functional Block Diagram

TPS76301



TPS76316/ 18/ 25/ 27/ 28/ 30/ 33/ 38/ 50



12.3 Feature Description

12.3.1 Regulator Protection

The TPS763xx features internal current limiting and thermal protection. During normal operation, the TPS763xx limits output current to approximately 800 mA. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, take care not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 165°C, thermal-protection circuitry shuts it down. Once the device has cooled down to below 140°C, regulator operation resumes.

Feature Description (continued)

12.3.2 Enable

The enable signal (V_{EN}) is an active-high digital control that enables the LDO when the enable voltage is past the rising threshold ($V_{EN} \geq V_{IH(EN)}$) and disables the LDO when the enable voltage is below the falling threshold ($V_{EN} \leq V_{IL(EN)}$). The exact enable threshold is between $V_{IH(EN)}$ and $V_{IL(EN)}$ because EN is a digital control. In applications that do not use the enable control, connect EN to V_{IN}.

12.4 Device Functional Modes

Table 1 provides a quick comparison between the regulation and disabled operation.

Table 1. Device Functional Modes Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	EN	I_{OUT}	T_J
Regulation(1)	$V_{IN} > V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{IH(EN)}$	$I_{OUT} < I_{CL}$	$T_J < T_{sd}$
Disabled(2)	—	$V_{EN} < V_{IL(EN)}$	—	$T_J > T_{sd}$

(1) All table conditions must be met.
(2) The device is disabled when any condition is met.

12.4.1 Regulation

The device regulates the output to the targeted output voltage when all the conditions in Table 1 are met.

12.4.2 Disabled

When disabled, the pass device is turned off, the internal circuits are shutdown.

13 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

13.1 Application Information

The TPS763xx low-dropout (LDO) regulators are part of a family of regulators which have been optimized for use in battery-operated equipment and feature extremely low dropout voltages, low quiescent current (140 µA), and an enable input to reduce supply currents to less than 2 µA when the regulator is turned off.

13.2 Typical Application

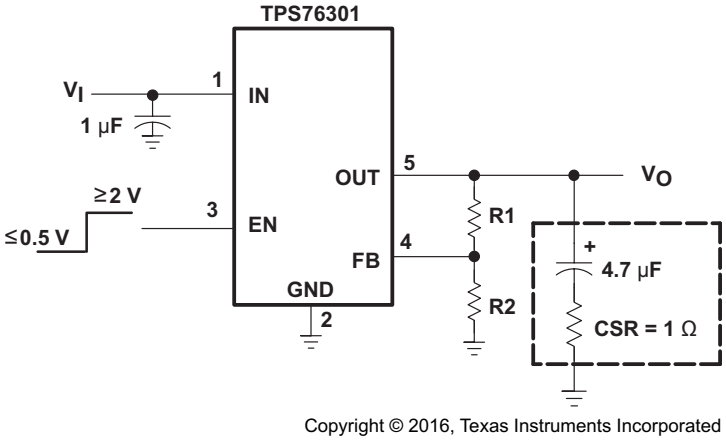


Figure 20. Typical Application Circuit

13.2.1 Design Requirements

Although not required, TI recommends a 0.047-µF or larger ceramic bypass input capacitor, connected between IN and GND and placed close to the TPS763xx, to improve transient response and noise rejection. A higher-value electrolytic input capacitor may be necessary if large, fast-rise-time load transients are anticipated and the device is placed several inches from the power source. Follow the programming guidelines from Table 2.

Table 2. Output Voltage Programming Guide

OUTPUT VOLTAGE (V)	DIVIDER RESISTANCE (kΩ)(1)	
	R1	R2
2.5	187	169
3.3	301	169
3.6	348	169
4	402	169
5	549	169
6.45	750	169

(1) 1% values shown

13.2.2 Detailed Design Procedure

13.2.2.1 Capacitor Selection

Like all low dropout regulators, the TPS763xx requires an output capacitor connected between OUT and GND to stabilize the internal loop control. The minimum recommended capacitance value is 4.7 µF and the ESR (equivalent series resistance) must be between 0.3 Ω and 10 Ω. Capacitor values 4.7 µF or larger are acceptable, provided the ESR is less than 10 Ω. Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the requirements described above. Most of the commercially available 4.7 µF surface-mount solid tantalum capacitors, including devices from Sprague, Kemet, and Nichico, meet the ESR requirements stated above (see Table 3).

Table 3. Capacitor Selection

PART NO.	MFR	VALUE	MAX ESR	SIZE (H × L × W)
T494B475K016AS	Kemet	4.7 µF	1.5 Ω	1.9 × 3.5 × 2.8
195D106x0016x2T	Sprague	10 µF	1.5 Ω	1.3 × 7 × 2.7
695D106x003562T	Sprague	10 µF	1.3 Ω	2.5 × 7.6 × 2.5
TPSC475K035R0600	AVX	4.7 µF	0.6 Ω	2.6 × 6 × 3.2

13.2.2.2 Output Voltage Programming

The output voltage of the TPS76301 adjustable regulator is programmed using an external resistor divider as shown in Figure 21. The output voltage is calculated using Equation 1.

$$V_O = 0.995 \times V_{ref} \times \left(1 + \frac{R1}{R2}\right) \quad (1)$$

where

- Vref = 1.192 V typical (the internal reference voltage)
- 0.995 is a constant used to center the load regulator (1%)

Resistors R1 and R2 must be chosen for approximately 7-µA divider current. Lower value resistors can be used but offer no inherent advantage and waste more power. Higher values must be avoided as leakage currents at FB increase the output voltage error. TI recommends choosing a design procedure of R2 = 169 kΩ to set the divider current at 7 µA and then calculate R1 using Equation 2.

$$R1 = \left(\frac{V_O}{0.995 \times V_{ref}} - 1\right) \times R2 \quad (2)$$

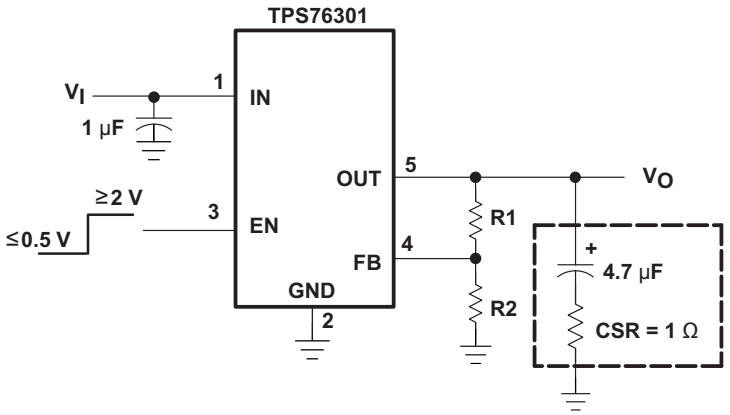


Figure 21. TPS76301 Adjustable LDO Regulator Programming

13.2.2.3 Reverse Current

The TPS763xx pass element has a built-in back diode that safely conducts reverse currents when the input voltage drops below the output voltage (for example, during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage is anticipated, external limiting might be appropriate.

13.2.3 Application Curves

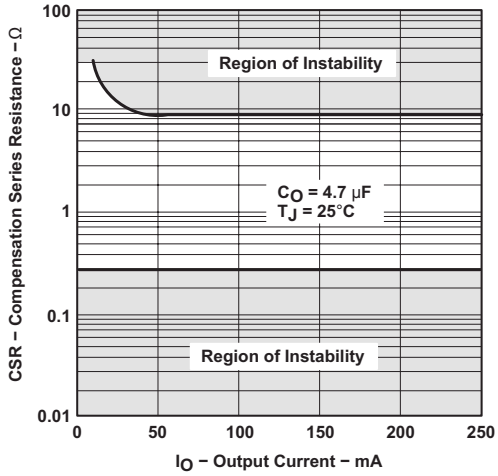


Figure 22. Compensation Series Resistance (CSR) vs Output Current

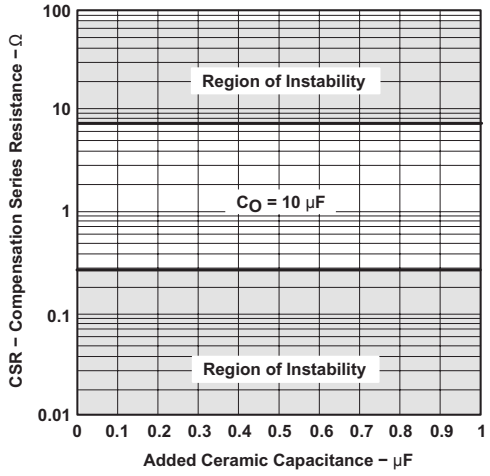


Figure 23. Compensation Series Resistance (CSR) vs Added Ceramic Capacitance

14 Power Supply Recommendations

A 1-µF or larger input capacitor must be used.

14.1 Power Dissipation and Junction Temperature

Specified regulator operation is assured to a junction temperature of 125°C; the maximum junction temperature allowable to avoid damaging the device is 150°C. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D, which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using Equation 3.

$$P_{D(max)} = \frac{T_J max - T_A}{R_{\theta JA}} \quad (3)$$

where

- $T_J$max is the maximum allowable junction temperature
- $R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package, see *Thermal Information*
- T_A is the ambient temperature

The regulator dissipation is calculating using Equation 4.

$$P_D = (V_I - V_O) \times I_O \quad (4)$$

Power dissipation resulting from quiescent current is negligible.

15 Layout

15.1 Layout Guidelines

- Place input and output capacitors as close to the device as possible.
- Use copper planes for device connections to optimize thermal performance.
- Place thermal vias around the device to distribute the heat.

15.2 Layout Example

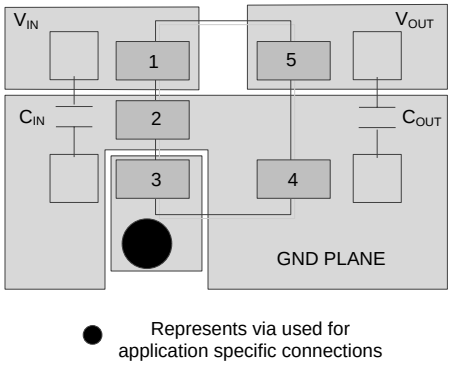


Figure 24. Layout Example for DBV Package

16 Device and Documentation Support

16.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

16.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

16.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

16.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

16.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

17 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS76301DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PAZI	Samples
TPS76301DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PAZI	Samples
TPS76301DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PAZI	Samples
TPS76316DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBHI	Samples
TPS76316DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBHI	Samples
TPS76316DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBHI	Samples
TPS76318DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBAI	Samples
TPS76318DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBAI	Samples
TPS76318DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBAI	Samples
TPS76318DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBAI	Samples
TPS76325DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		PBBI	Samples
TPS76325DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		PBBI	Samples
TPS76325DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		PBBI	Samples
TPS76327DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		PBCI	Samples
TPS76327DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		PBCI	Samples
TPS76327DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		PBCI	Samples
TPS76328DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		PBDI	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS76328DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		PBDI	Samples
TPS76330DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		PBII	Samples
TPS76330DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		PBII	Samples
TPS76333DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBEI	Samples
TPS76333DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBEI	Samples
TPS76333DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBEI	Samples
TPS76333DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBEI	Samples
TPS76338DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		PBFI	Samples
TPS76338DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		PBFI	Samples
TPS76350DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		PBGI	Samples
TPS76350DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		PBGI	Samples
TPS76350DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		PBGI	Samples
TPS76350DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		PBGI	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPS763 :

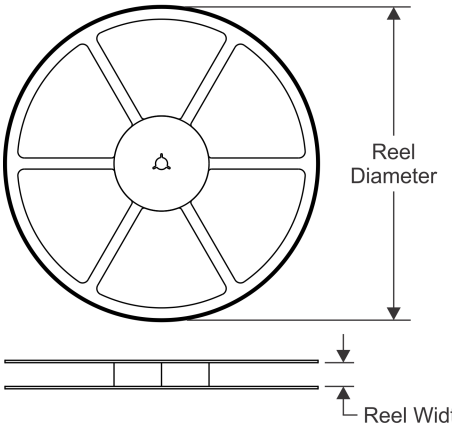
- Automotive: TPS763-Q1

NOTE: Qualified Version Definitions:

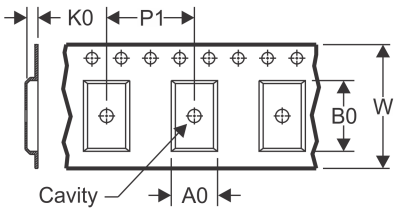
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

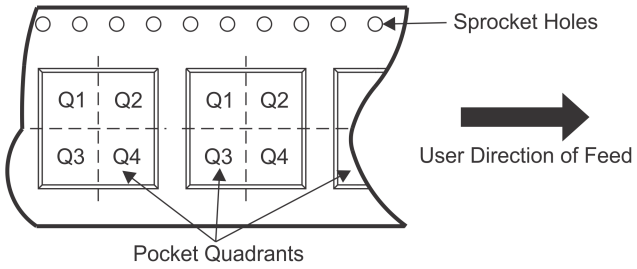


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

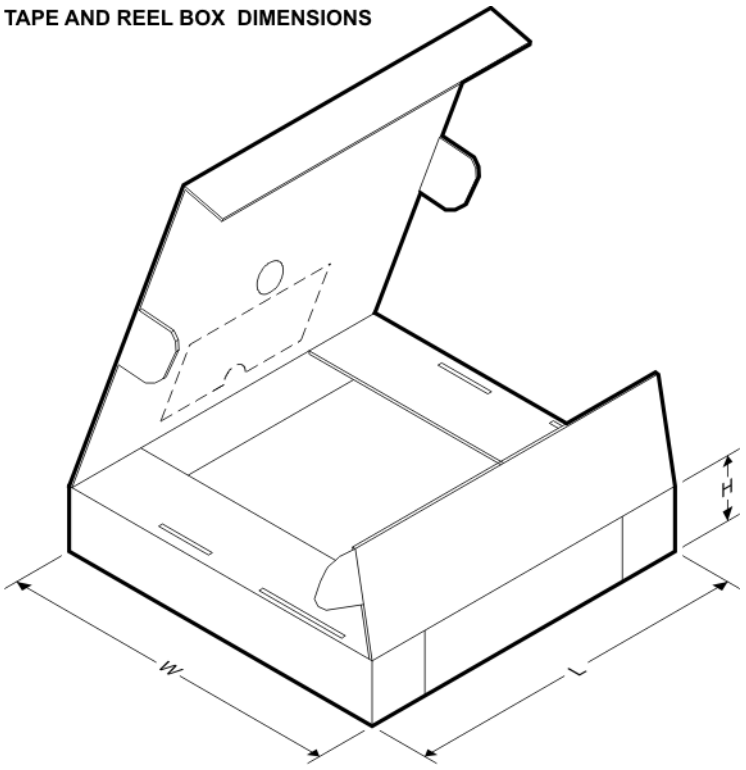


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS76301DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS76301DBVR	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS76301DBVT	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS76301DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS76316DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS76316DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS76318DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS76318DBVR	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS76318DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS76318DBVT	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS76325DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS76325DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS76327DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS76327DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS76328DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS76328DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS76330DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS76330DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS76333DBVR	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS76333DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS76333DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS76333DBVT	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS76338DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS76338DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS76350DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS76350DBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



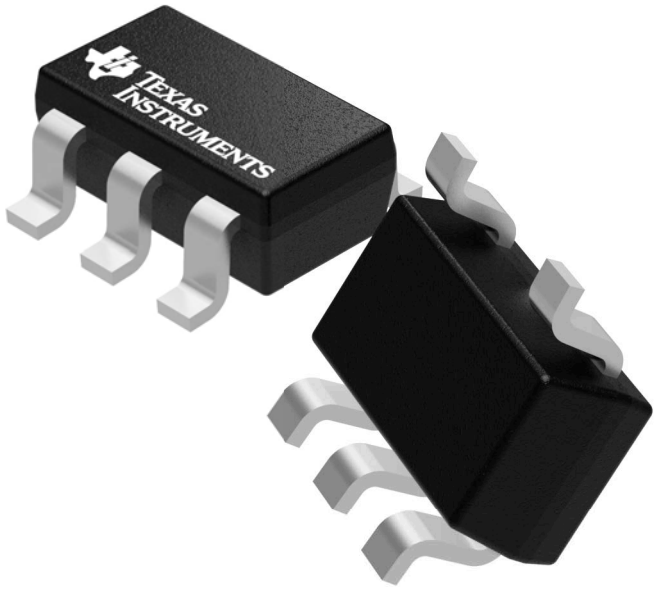
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS76301DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS76301DBVR	SOT-23	DBV	5	3000	203.0	203.0	35.0
TPS76301DBVT	SOT-23	DBV	5	250	203.0	203.0	35.0
TPS76301DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS76316DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS76316DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS76318DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS76318DBVR	SOT-23	DBV	5	3000	203.0	203.0	35.0
TPS76318DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS76318DBVT	SOT-23	DBV	5	250	203.0	203.0	35.0
TPS76325DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS76325DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS76327DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS76327DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS76328DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS76328DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS76330DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS76330DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS76333DBVR	SOT-23	DBV	5	3000	203.0	203.0	35.0
TPS76333DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS76333DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS76333DBVT	SOT-23	DBV	5	250	203.0	203.0	35.0
TPS76338DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS76338DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS76350DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS76350DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0

DBV 5 SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



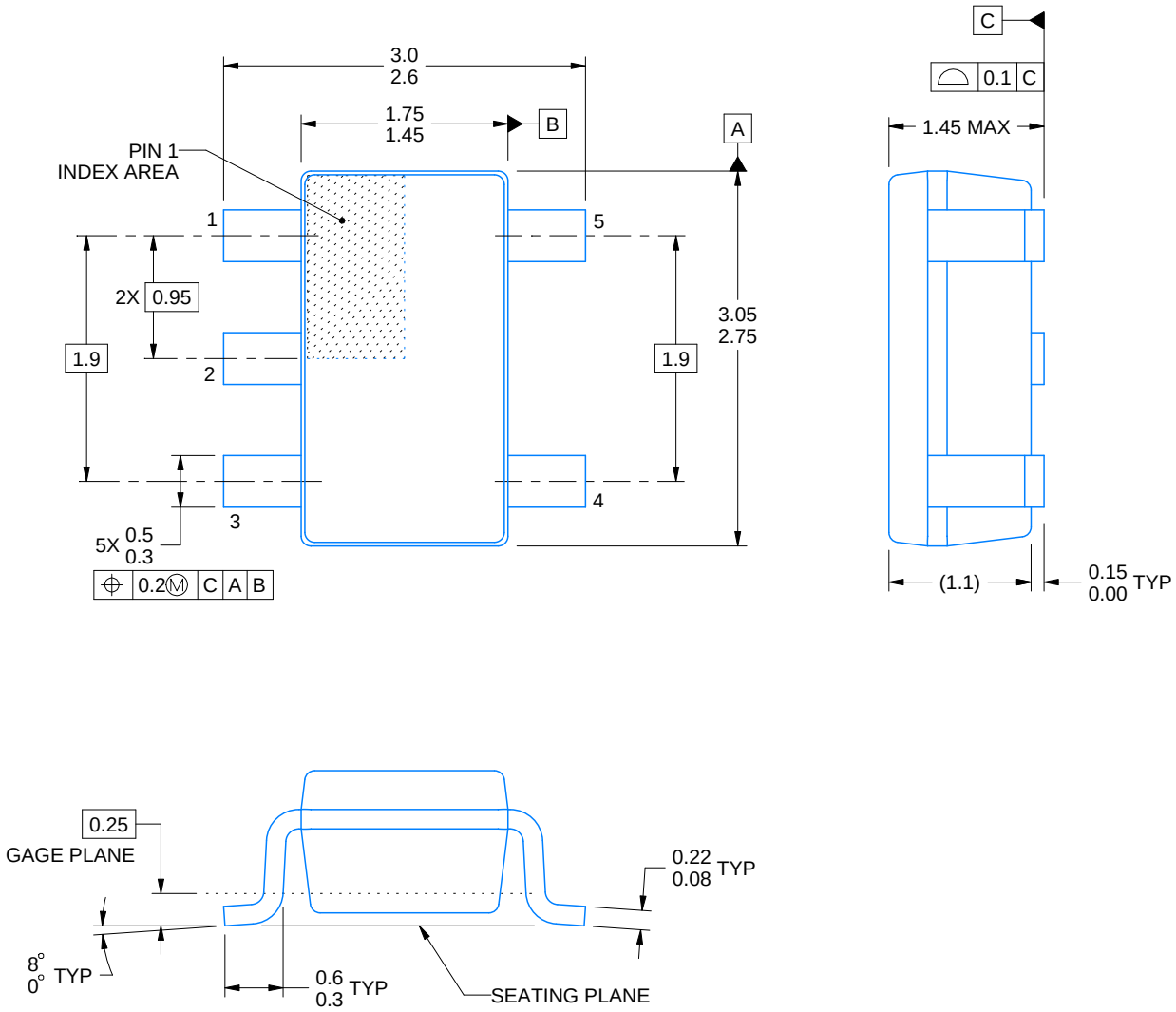
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

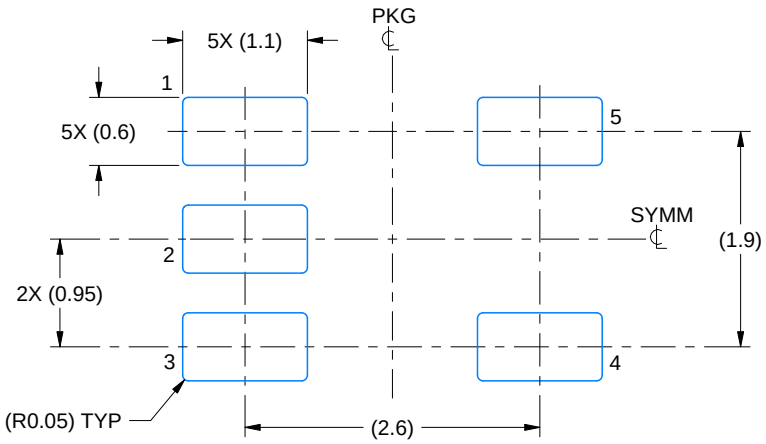
SMALL OUTLINE TRANSISTOR



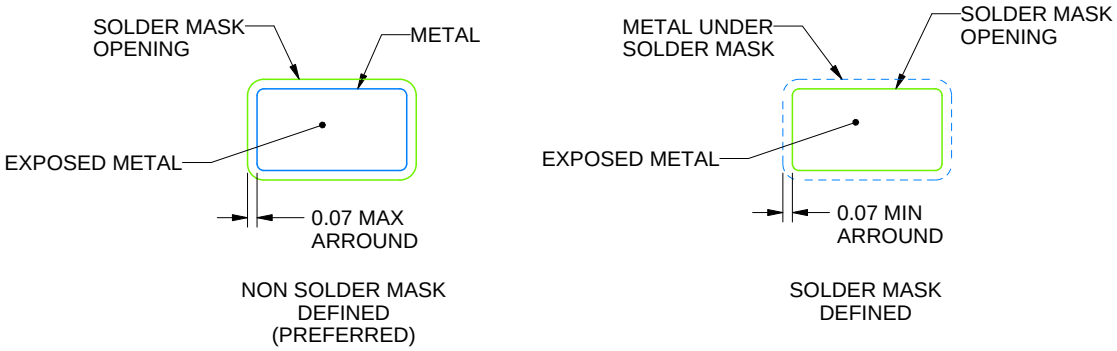
4214839/C 04/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

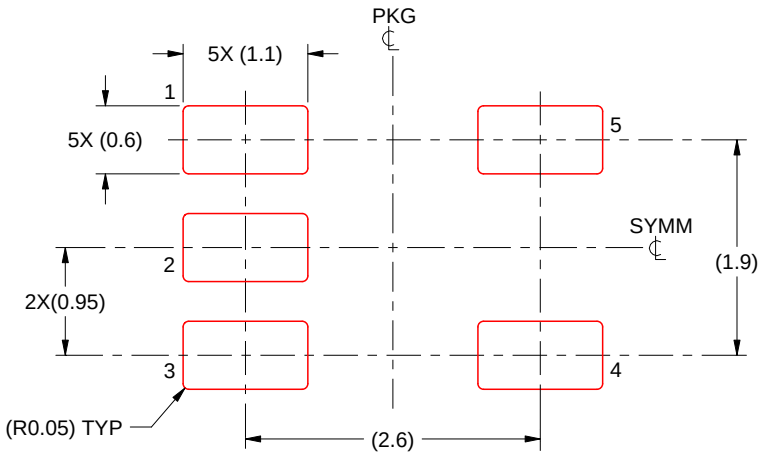


SOLDER MASK DETAILS

4214839/C 04/2017

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/C 04/2017

NOTES: (continued)

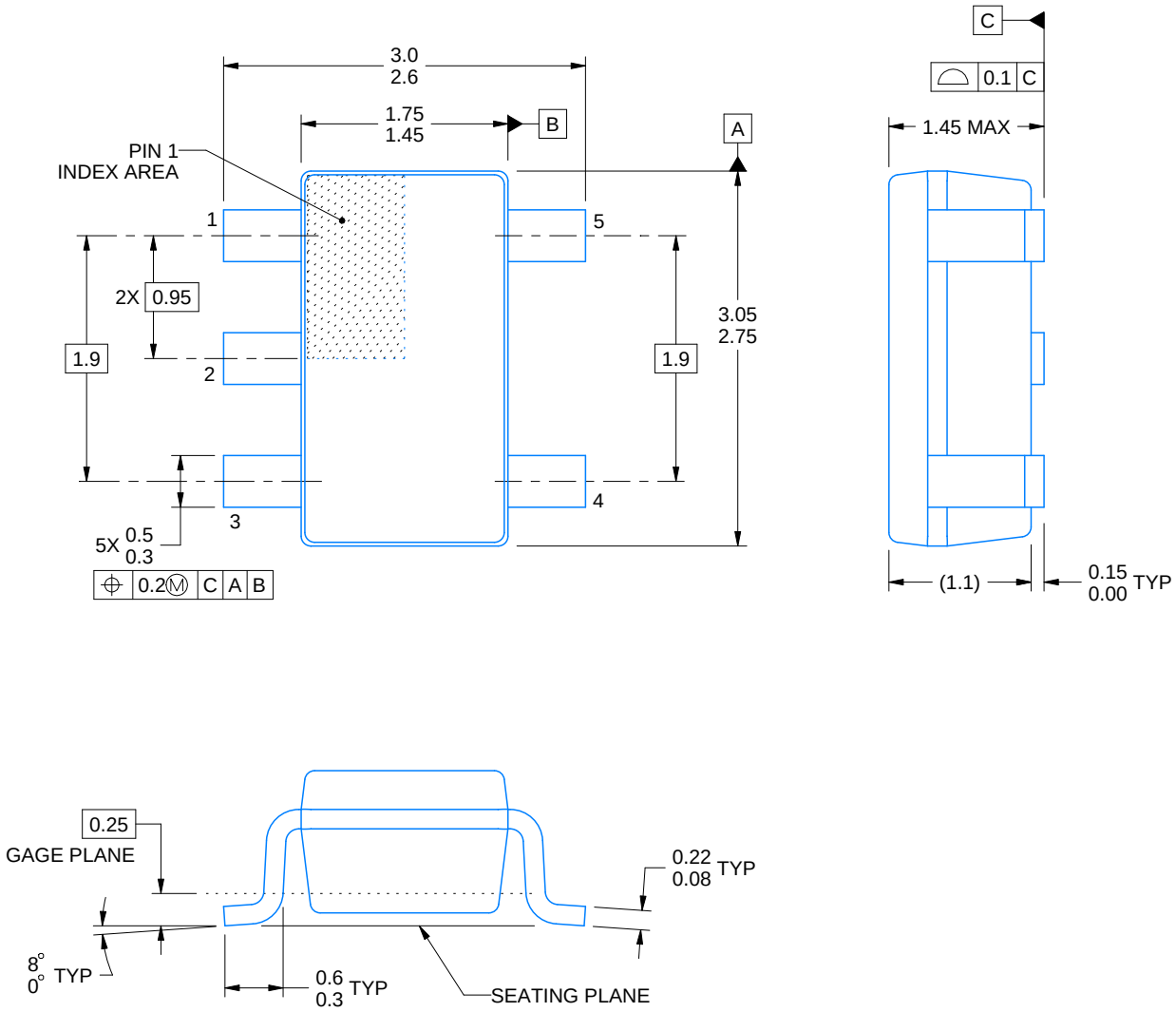
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

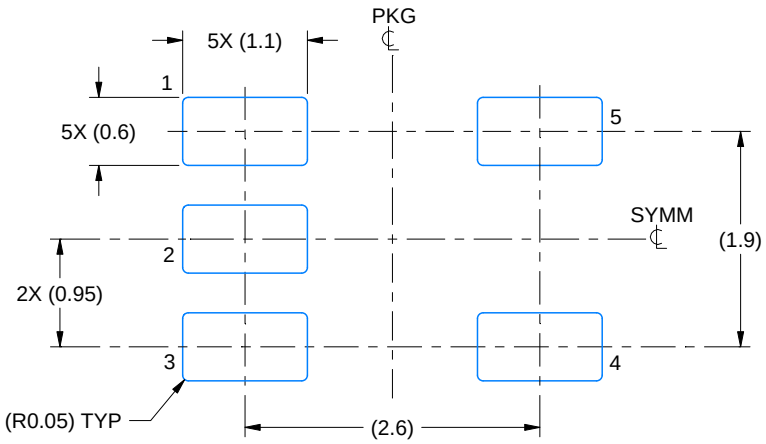
SMALL OUTLINE TRANSISTOR



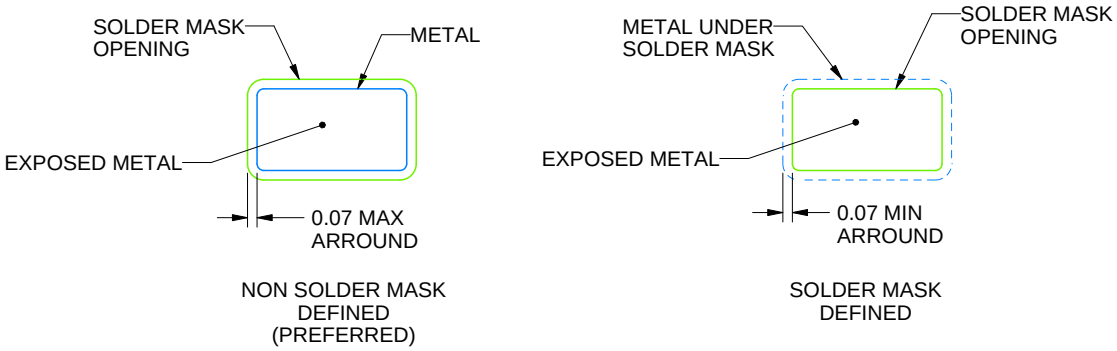
4214839/D 11/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

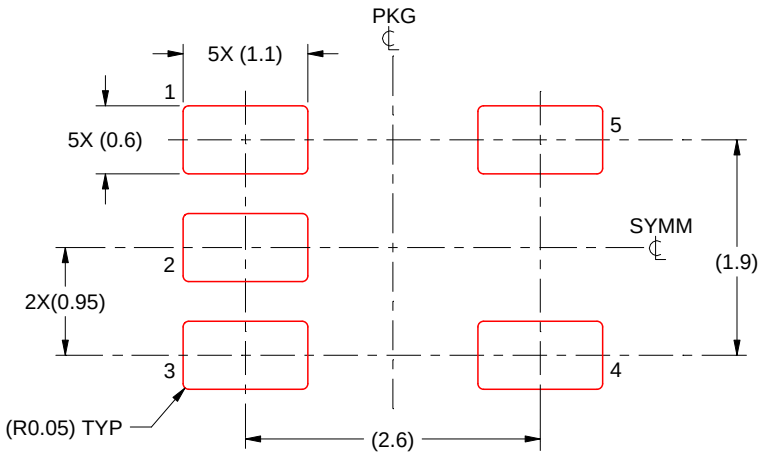


SOLDER MASK DETAILS

4214839/D 11/2018

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/D 11/2018

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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