A.5 M8739 LESI ADAPTER

The M8739 LESI UNIBUS Adapter is a quad height module which plugs into any small peripheral controller slot in the UNIBUS backplane. It interfaces the UNIBUS to the intelligent controller in the transport. The M8739 performs the following functions:

1. Enables the I/O controller to send and receive data (via Direct memory access) to and from the Host's memory.

2. Enables the I/O controller to interrupt the Host.

3. Enables access to two UNIBUS registers - Initialization and Polling (IP), and Status, Address and Purge (SA).

In the LESI Interconnect, the M8739 is always a slave to the controller. The controller initiates all operations and the adapter response upon completion of the command or data block transfer.

Figure A-4 is the M8739 Block Diagram.

A.5.1 Data Transfers

Before initiating an NPR, the controller writes the host starting address for the NPR into the address register. The controller initiates the NPR by writing into the command register: Do an NPR, with a direction bit and the word count. The address register increments with each data transfer occuring on the host interface.

The M8739 transfers data to and from the controller in blocks of 16 words. Multiple block transfers occur without reissuing the command or rewriting the starting address (except in Byte Mode). This is done by transferring 16 more data words into or from the adapter RAM. The DO NPR command restarts when an overflow of the word count is detected by the adapter. Each successive block transfer must start at RAM address 0 and be 16 words long. If a shorter block has to be transmitted at the end of the burst, DO NPR is cleared first, then the word count is modified before the controller reissues DO NPR and sets up the RAM. Multiple block transfers can be prevented by clearing DO NPR at the end of each block transfer.

Byte operation occurs in single byte transfers at the beginning and end of a record. All data inside the record is in word format and all word transfers are executed in block sizes specified by the Host. The adapter gives up the Host bus at the end of every byte transfer. Therefore, after each single byte transfer, the controller writes the starting address and issues a new command.

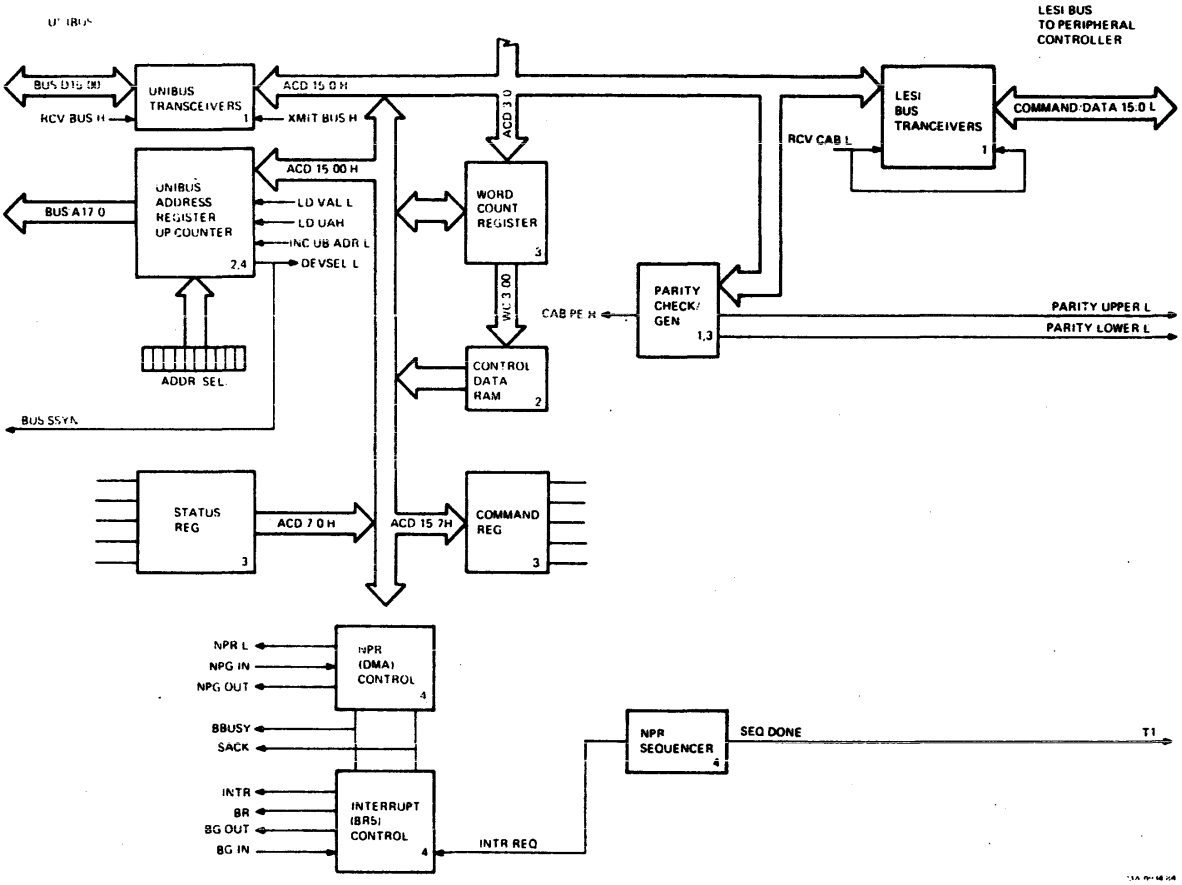

Figure A-4. M8739 LESI ADAPTER BLOCK DIAGRAM

Parity is generated and checked on both the controller and the host interfaces. The adapter informs the controller of the completion of the data block transfer by asserting ATTENTION.

A.5.2 Interrupts

The adapter card also executes Host interrupts. First, the controller writes the interrupt vector into RAM location zero, then initiates the interrupt by writing into the command register the DO INTERRUPT command with zero address and word count bits.

A.5.3 UNIBUS Registers

The M8739 adapter also operates as a slave device to the host when it runs from the TMSCP Controller. The adapter holds the addresses of two UNIBUS registers, Initialization and Polling (IP) and Status, Address and Purge (SA) which are used for control of the port.

- IP Register Function

  1. Host write to IP causes a "hard" initialization of the port and controller.

  2. Host read from IP (when the port is operating) sets POLL bit in the adapter status register.

- SA Register Function

  1. Host write to SA during initialization sends host specific parameters to the port (adapter and controller).

  2. Host read from SA during initialization gets data/error information relating to the initialization process.

  3. Host read from SA during normal operation gets status and fatal errors.

  4. Host write zeros to SA during initialization or normal operation signifies a successful adapter purge in response to a port initiated purge request.