

ECE 424  
DUE: Wednesday, Nov 18, 12:30 pm

### Design Project #3: Single-Cycle Datapath Design (100 points)

#### COVER SHEET

**Honor Code:** \_\_\_\_\_ I have neither given or received, nor have I tolerated others' \_\_\_\_\_  
\_\_\_\_\_ use of unauthorized aid. \_\_\_\_\_

Name: \_\_\_\_\_ Joe Leveille \_\_\_\_\_ Signature: \_\_\_\_\_ *Joseph Leveille* \_\_\_\_\_

**Honor Code:** \_\_\_\_\_ I have neither given or received, nor have I tolerated \_\_\_\_\_  
\_\_\_\_\_ others' use of unauthorized aid. \_\_\_\_\_

Name: \_\_\_\_\_ Jon Bayert \_\_\_\_\_ Signature: \_\_\_\_\_ *Jonathon Bayert* \_\_\_\_\_

A complete assignment will contain:

1. This cover sheet
2. A printout of your VHDL code including your main file, modified imem.vhd, modified alu-control.vhd, and modified dmem.vhd.
3. Waveforms for the two different cases, showing the five (and only the five) signals in hex format.