Leveille
ECE 429 HW 8

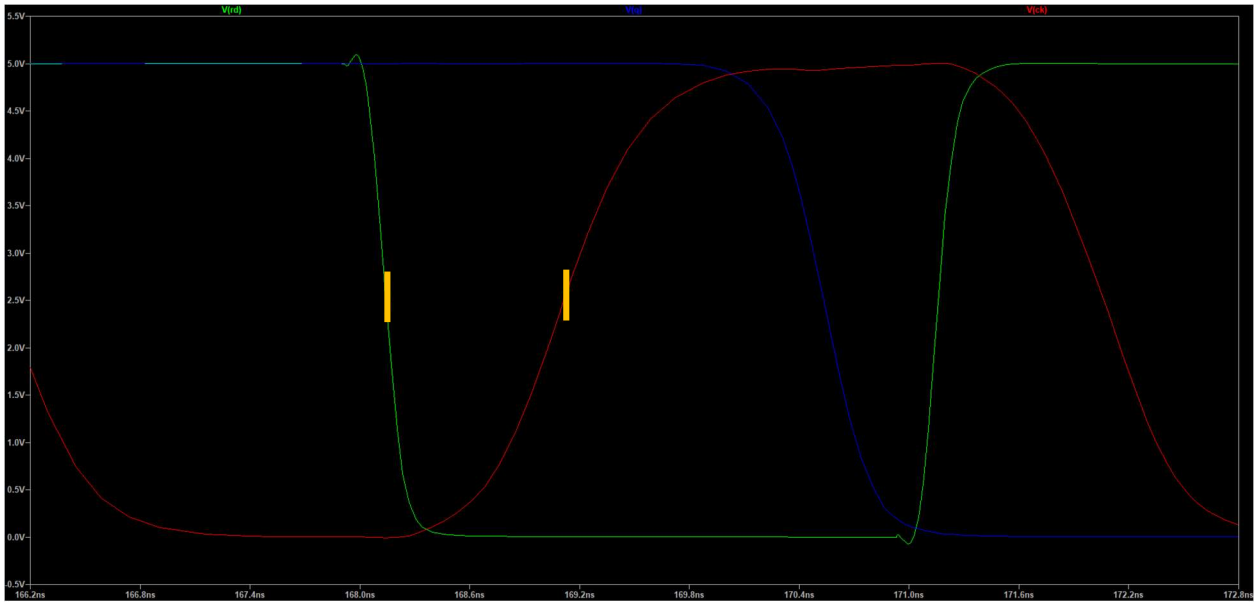
I have neither given or received, nor have I tolerated others' use of unauthorized aid.

t_{su}= 970ps (compared to 210ps from schematic simulation)

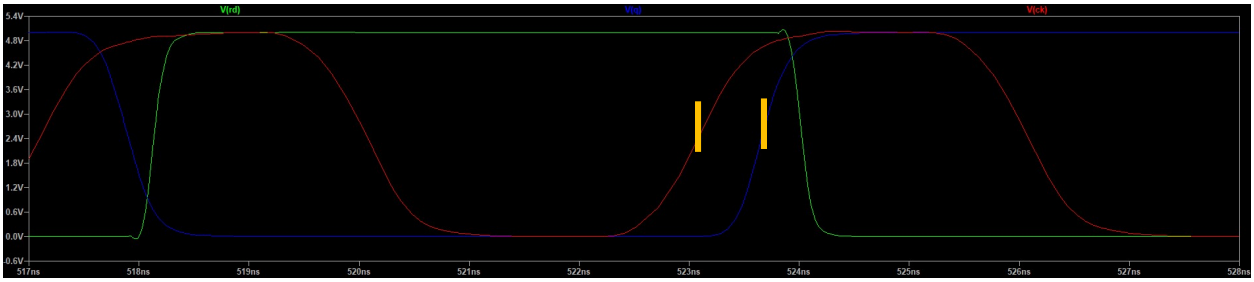
Simulation code used:

```
VGND GND 0 DC 0,VVDD VDD 0 DC 5,
VCLK CLK 0 DC 0 PULSE 0 5 0 10p 10p 3n 6n,
VIN D 0 DC 0 PULSE 5 0 200p 10p 10p 3n 5.99n,
.include c5.txt,.tran 2000n UIC,
.save v(rd) v(ck) v(q) v(qbar) v(D_FF@2:D_latch@0:x) v(D_FF@2:outbar) v(D_FF@2:D_latch@1:x) v(D_FF@2:mid) dialogbox,
*.options post
```

Screenshot of area measured:

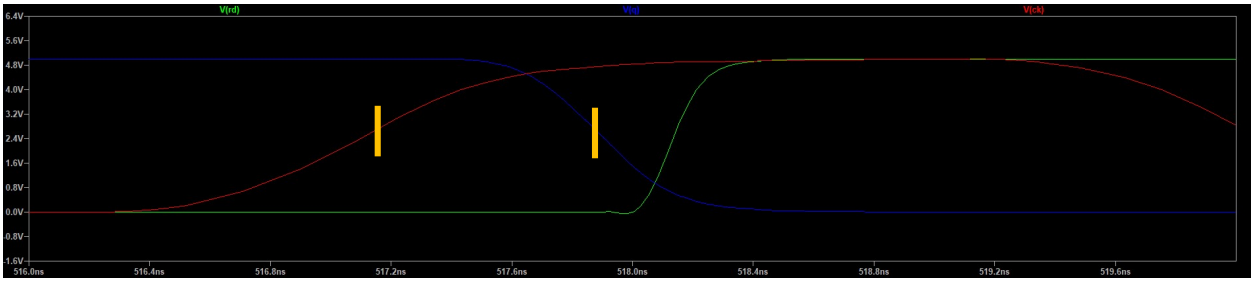


Part 2:
t_{cqr} = 565ps (compared to 282ps from schematic simulation)
Area measured:



t_{cqf} = 781ps (compared to 295ps from schematic simulation)
Area measured:

Leveille
ECE 429 HW 8



Simulation code used:

VGND GND 0 DC 0,VVDD VDD 0 DC 5,
VCLK CLK 0 DC 0 PULSE 0 5 0 10p 10p 3n 6n,
VIN D 0 DC 0 PULSE 5 0 200p 10p 10p 6n 11.99n,
.include c5.txt,.tran 2000n UIC,
.save v(rd) v(ck) v(q) v(qbar) v(D_FF@2:D_latch@0:x) v(D_FF@2:outbar) v(D_FF@2:D_latch@1:x) v(D_FF@2:mid) dialogbox,
*.options post

Measurement methods:

I used the manual plot settings to zoom in very precisely, then took the difference between the points approximated by the yellow lines above on each screenshot.

The spi file for the layout simulation was much longer than that of the schematic simulation because it included several hundred capacitance and resistance values that are only calculated for the layout simulation.