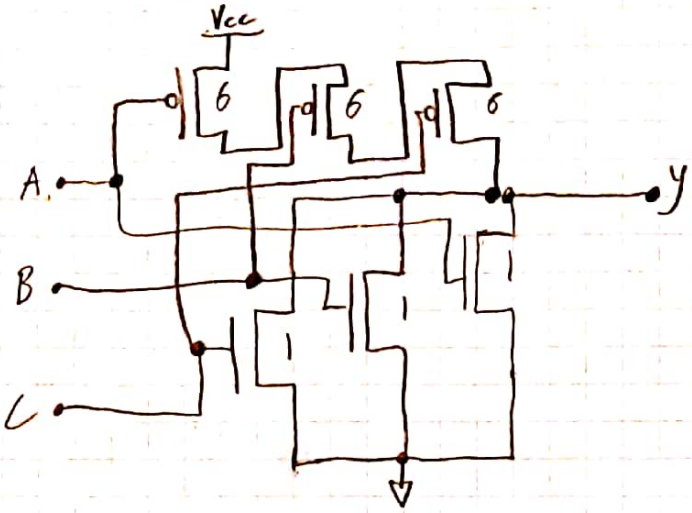
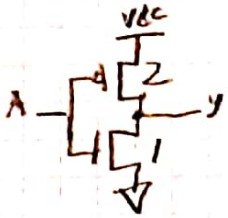
3 input NOR

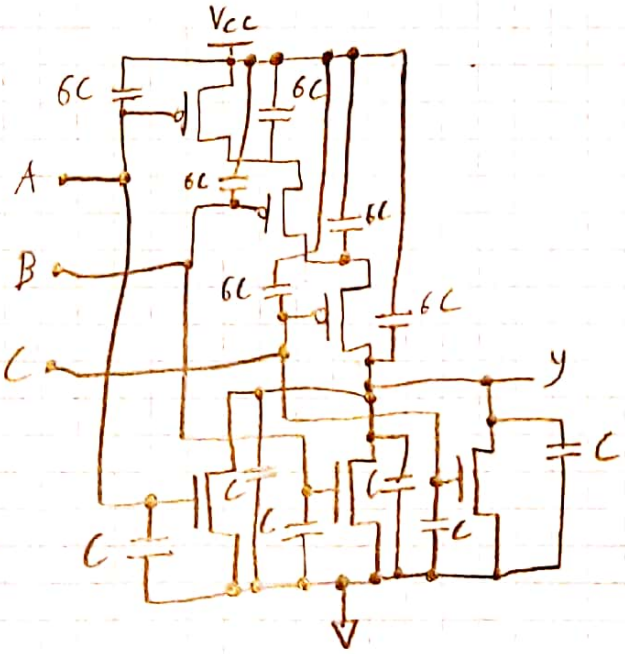
$y = \overline{A+B+C}$

$= \bar{A}\bar{B}\bar{C}$



Ref inv





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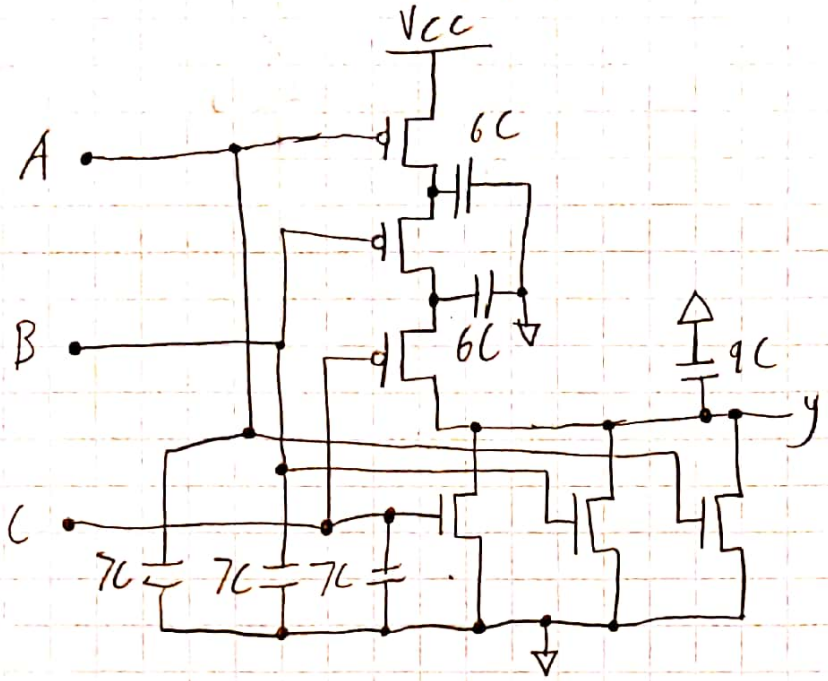
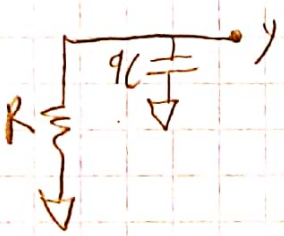
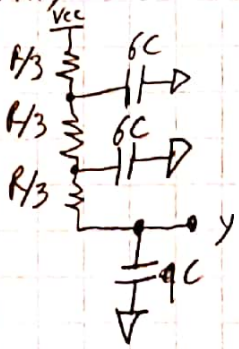


Falling Transition 000 → 001



Rising Transition 001 → 000



There are 3C capacitors because without a contact between two NMOS transistors, they can be pushed closer together & use a smaller piece of silicon between them.

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4.1

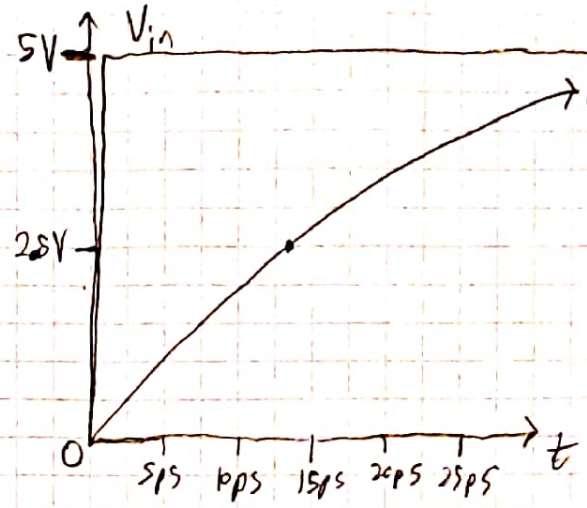
$t_{pdr} = RC\ln(2)$

$= 5k\Omega(4fF)\ln(2)$

$t_{pdr} = 13.86\ ps$

simulated: $\approx 14.92\ ps$

a)



$t_{pdr} = \tau\ln(2)$

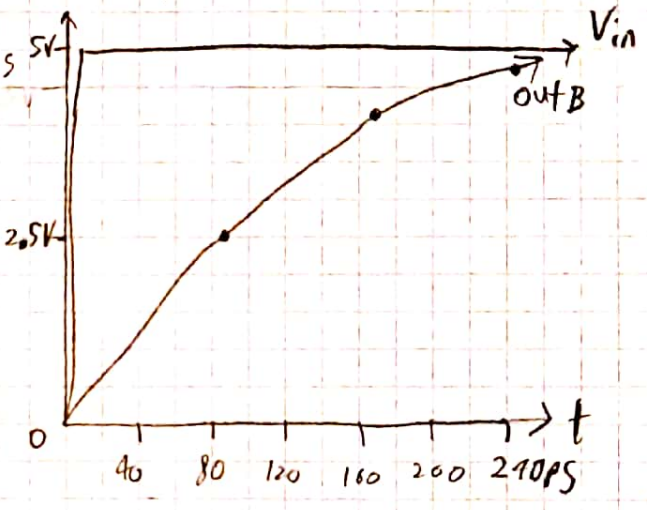
$\tau_{3rd\ order} = R_1C_1 + (R_1+R_2)C_2 + (R_1+R_2+R_3)C_3$

(10k, 15k)

$= 20ps + 40ps + 60ps = 120ps$

$t_{pdr} = 120(\ln(2)) = 83.1776\ ps$

simulated: $\approx 89.8\ ps$



4.2) I think the simulated value will always be greater than the Elmore delay estimation because of the shape of the third order response, in relation to the first order that we use as an estimation.

graph, similar to figure 4.11

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