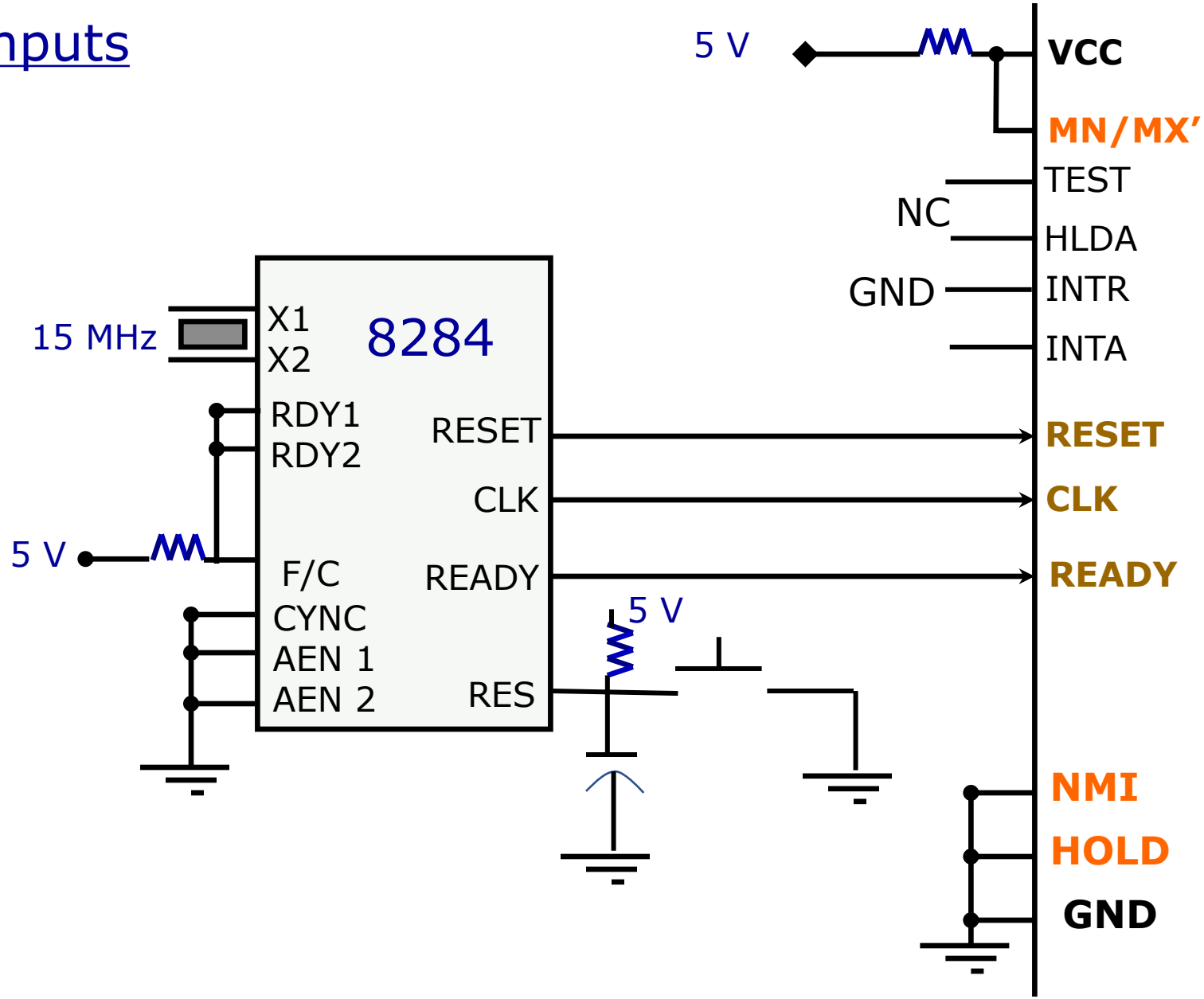
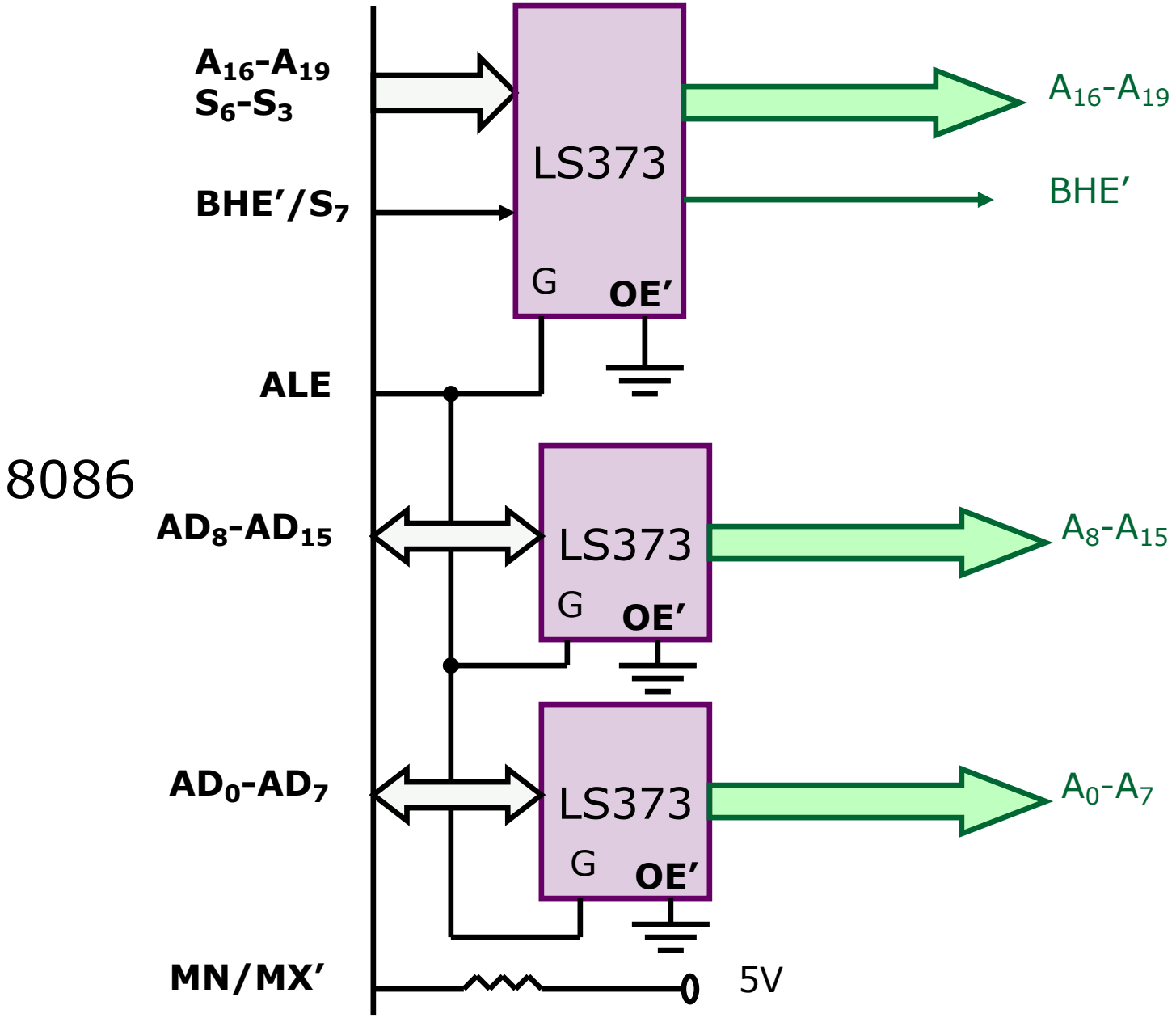
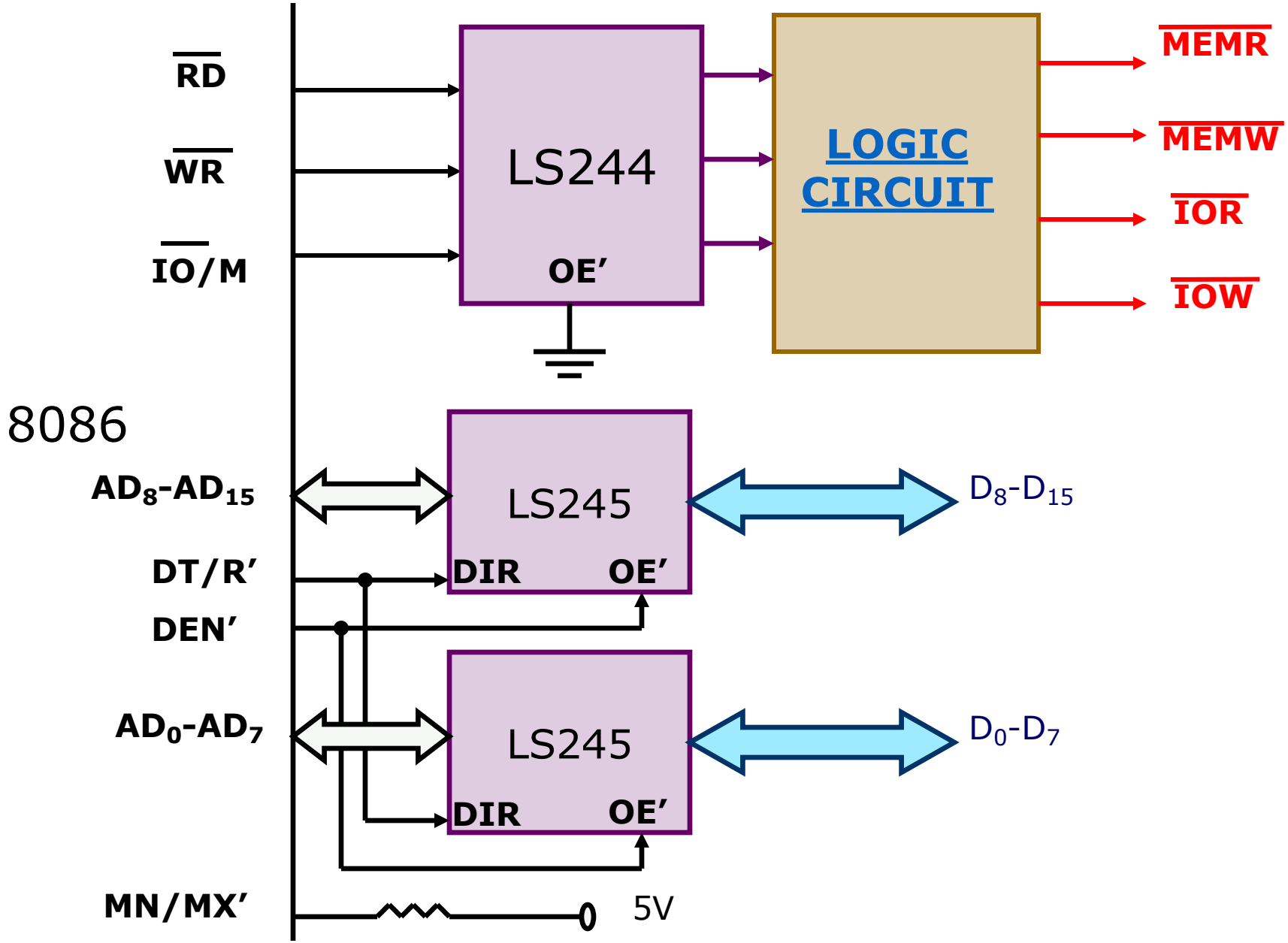
8086 Inputs


5 V
VCC
MN/MX'
TEST
NC
HLDA
GND
INTR
INTA
15 MHz
X1
X2
8284
RDY1
RDY2
RESET
CLK
5 V
F/C
READY
CYNC
AEN 1
AEN 2
5 V
RES
NMI
HOLD
GND

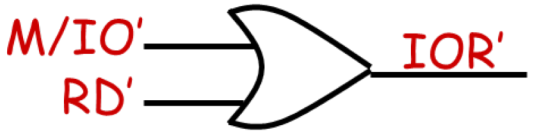
System Bus of 8086 (Address)

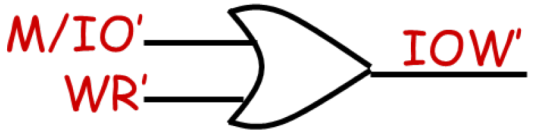


System Bus of 8086(Data + Control)

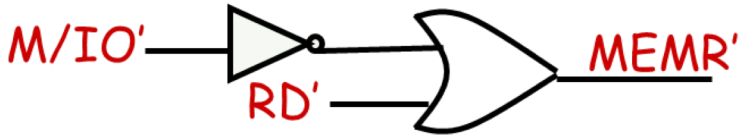


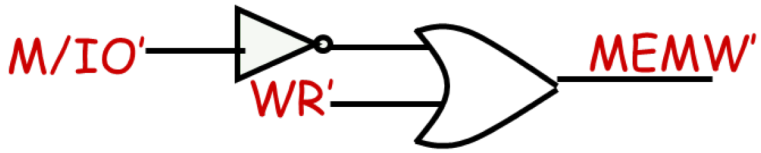
Strobe Signals



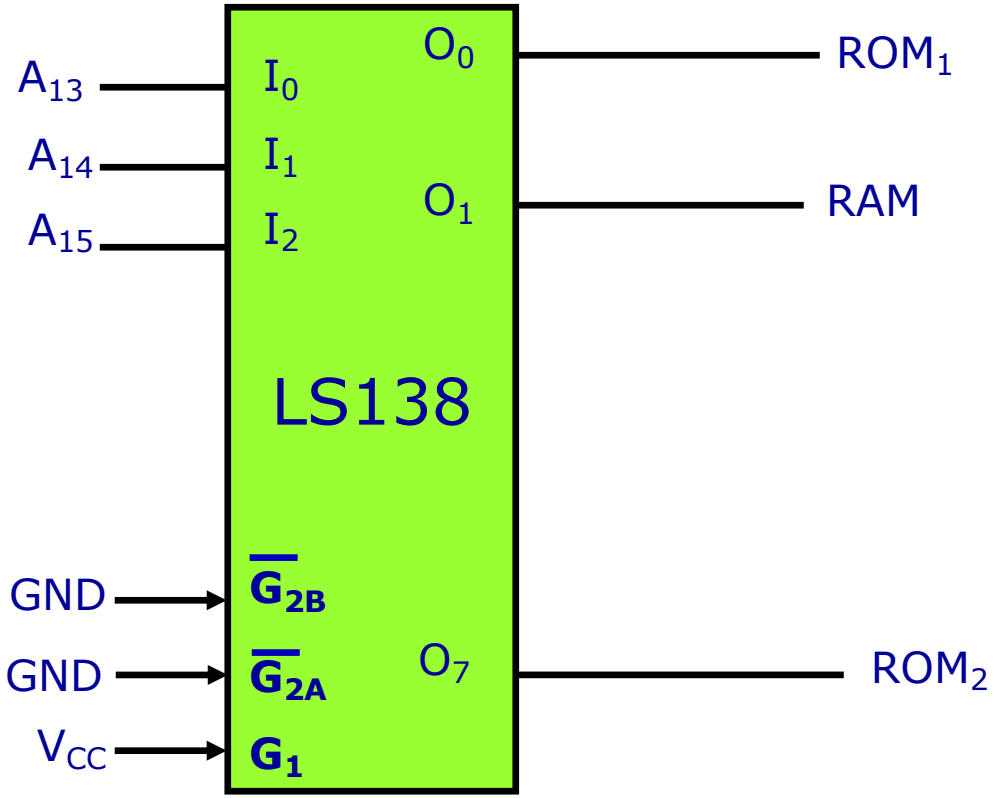


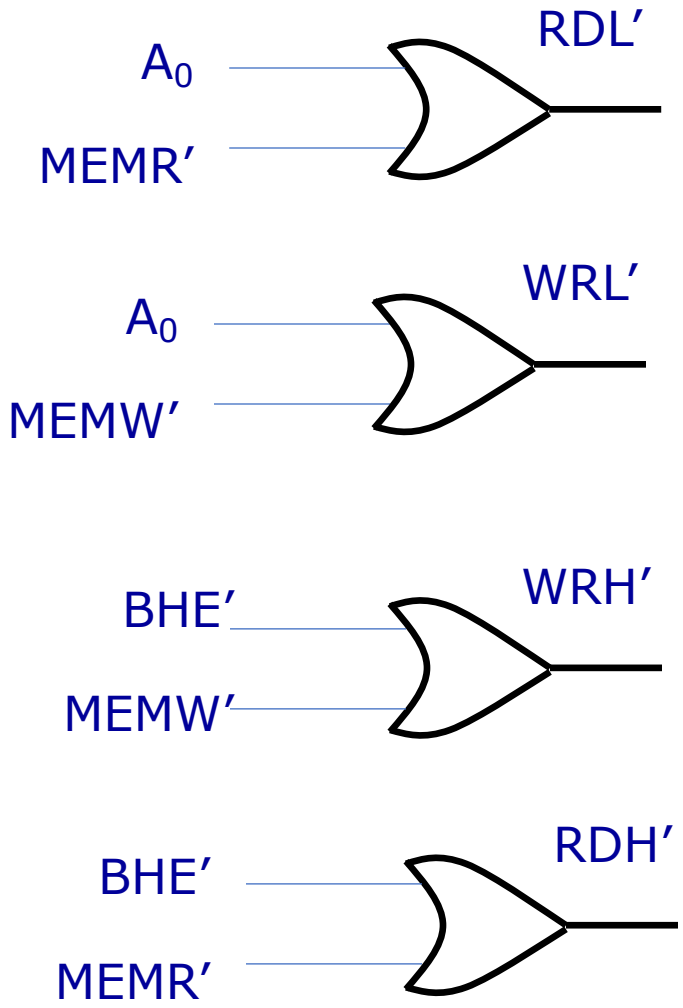
M/IO'	RD'	WR'	Bus cycle
1	0	1	MEMR'
1	1	0	MEMW'
0	0	1	IOR'
0	1	0	IOW'



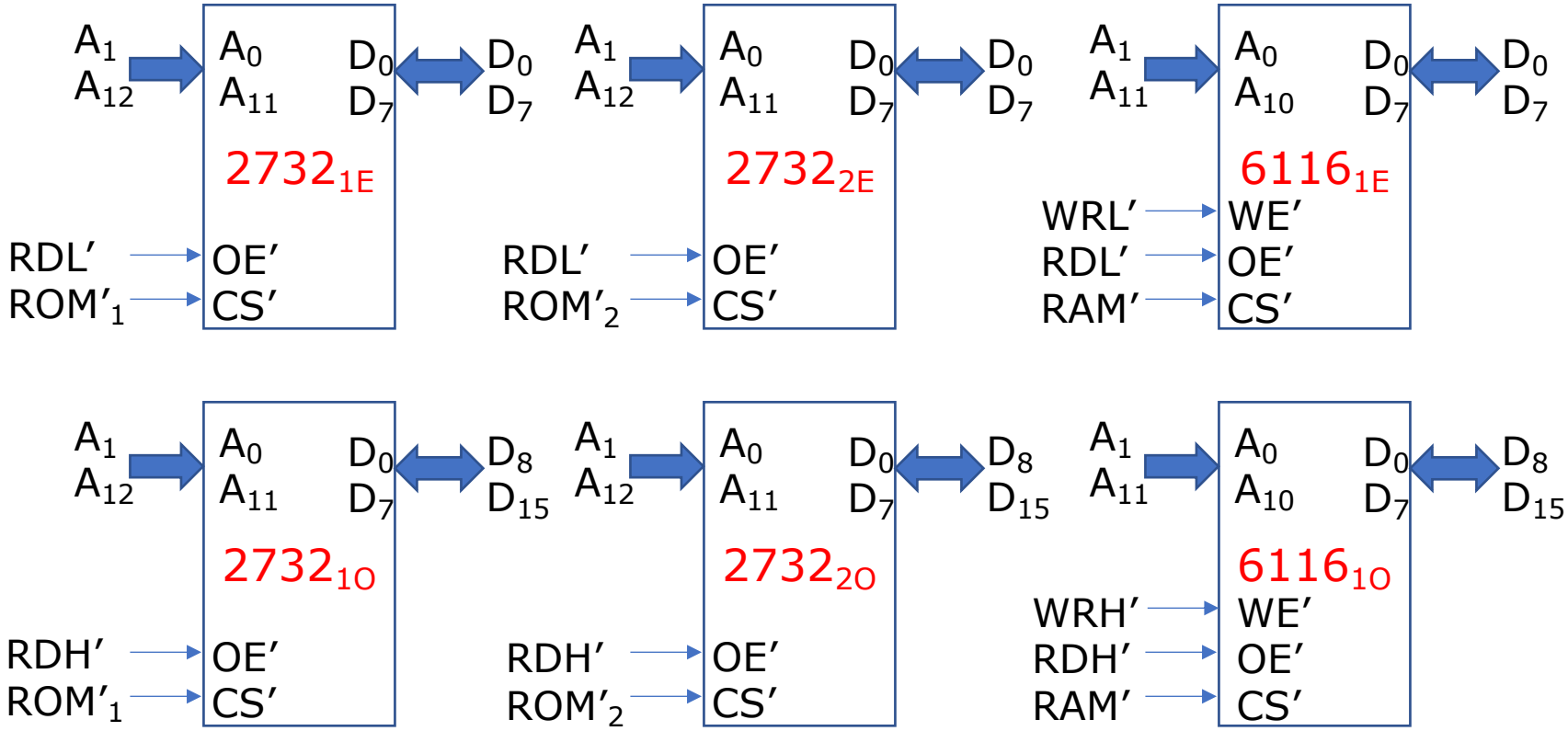


Memory Decoder

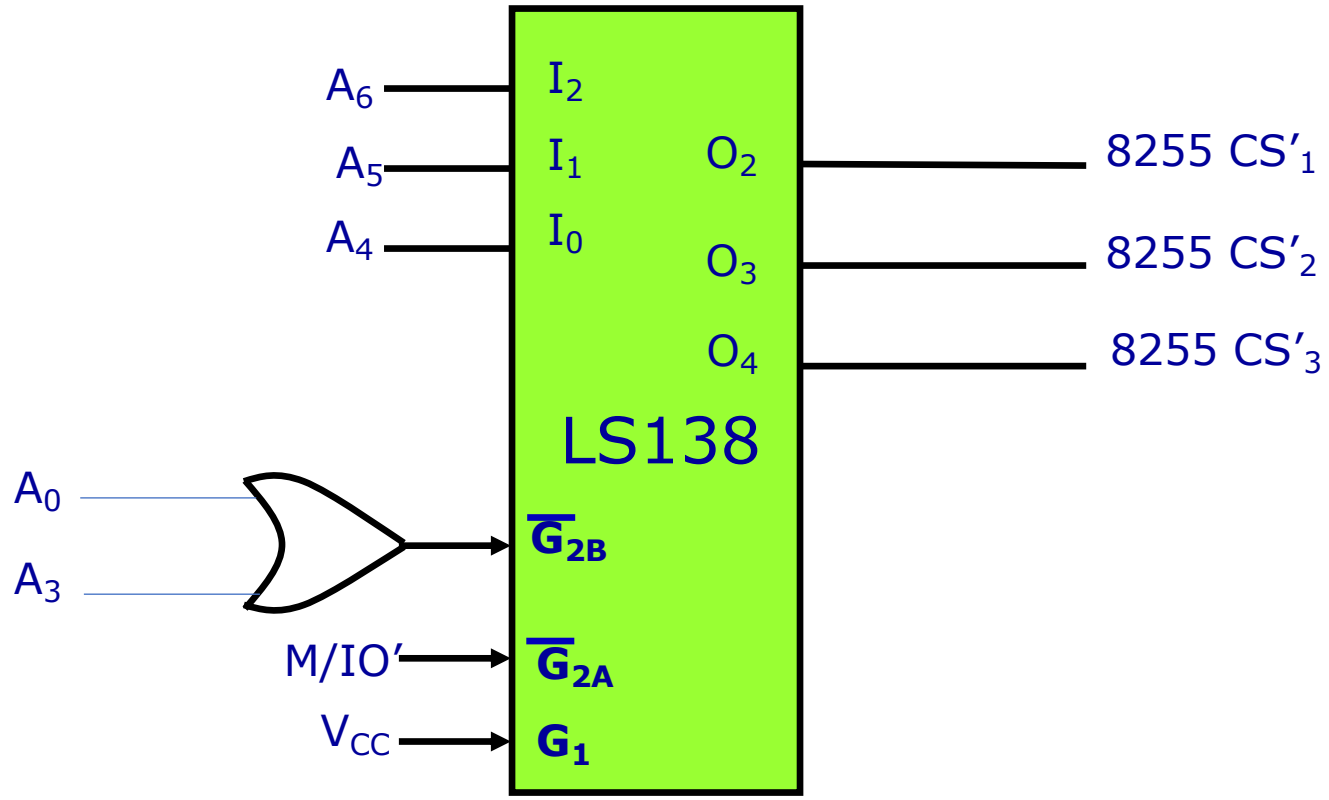




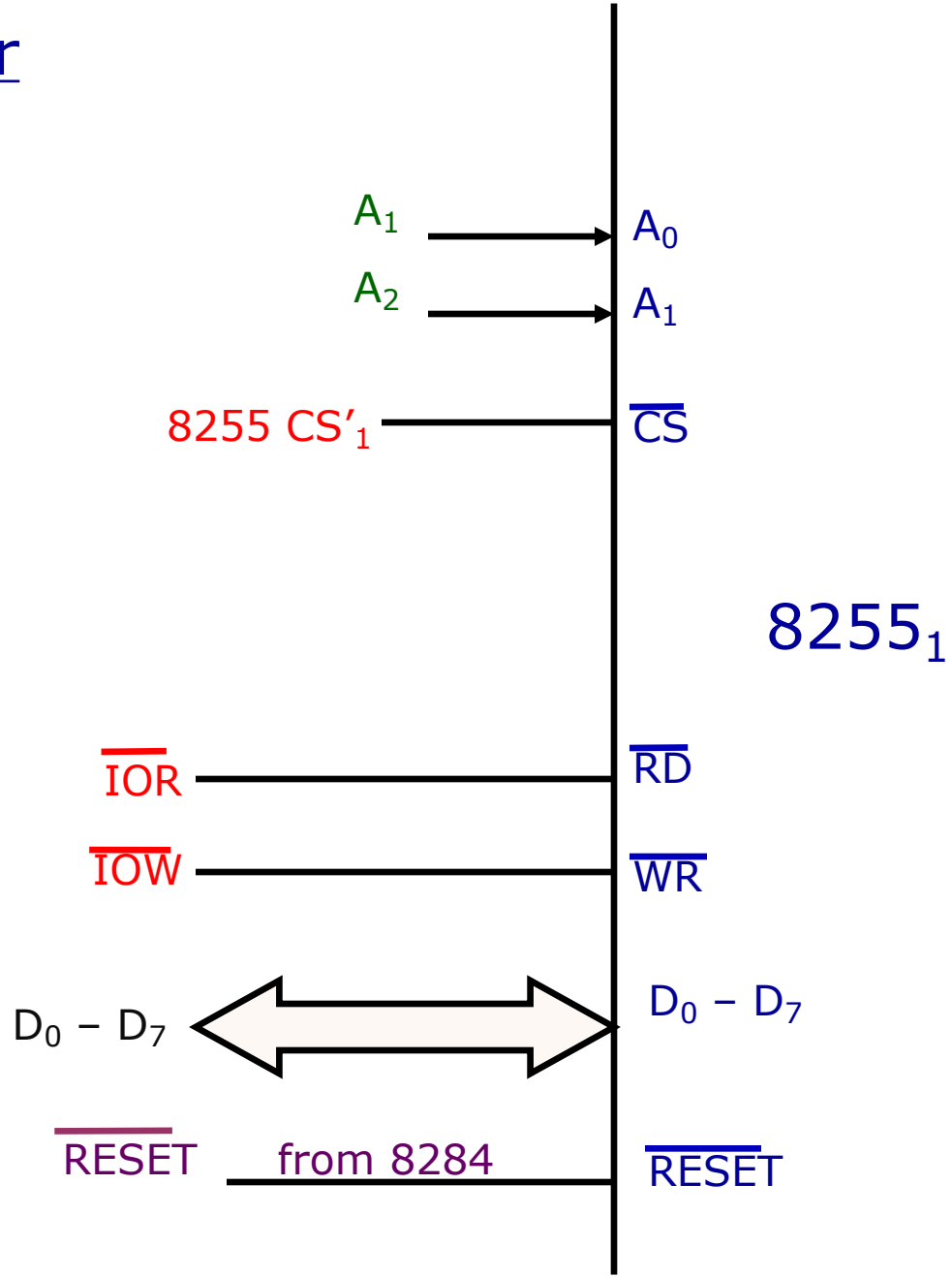
Memory Interfacing



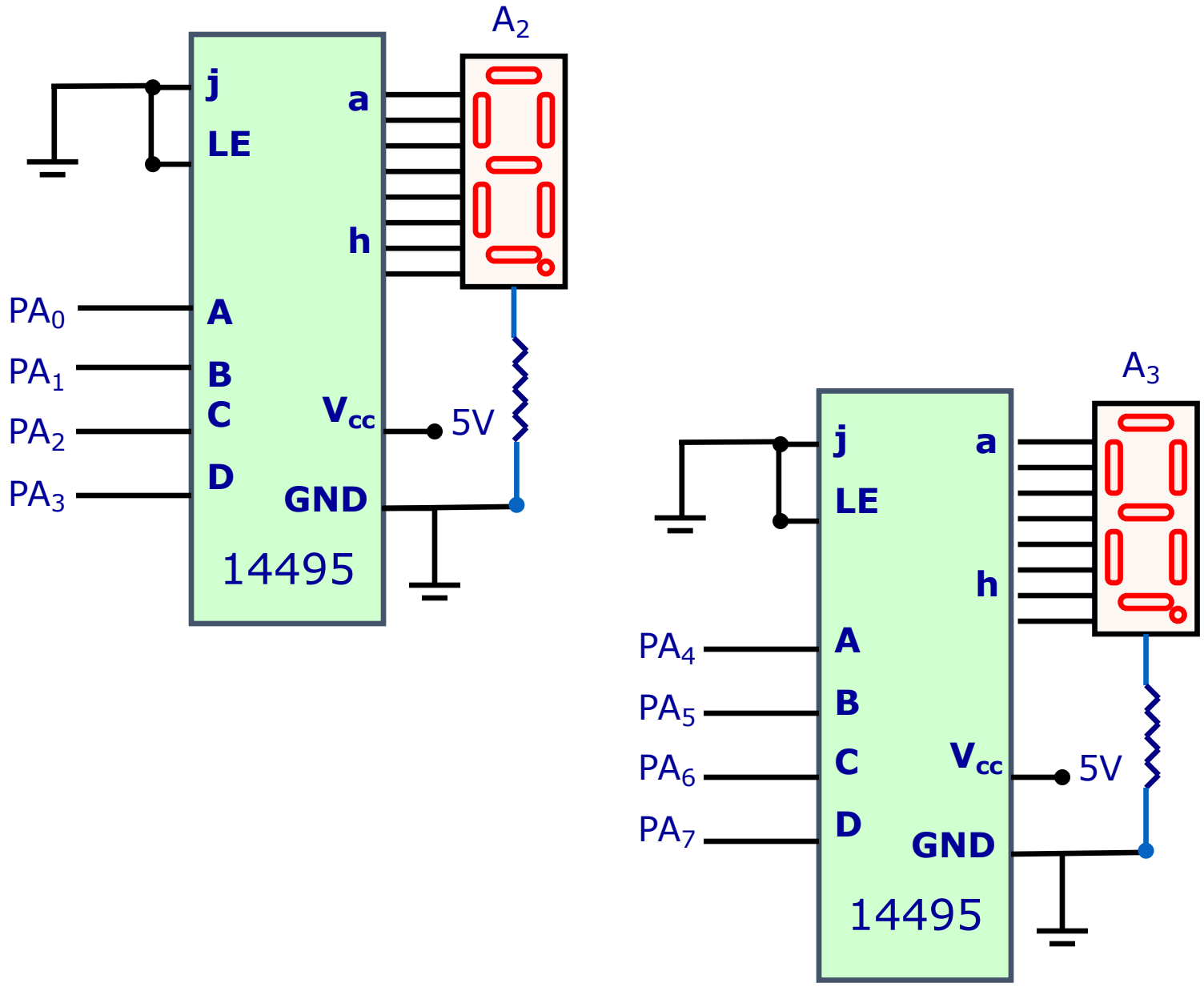
IO Decoder


A6
A5
A4
I2
I1
I0
O2
O3
O4
8255 CS'1
8255 CS'2
8255 CS'3
LS138
A0
A3
G2B
M/IO'
G2A
VCC
G1

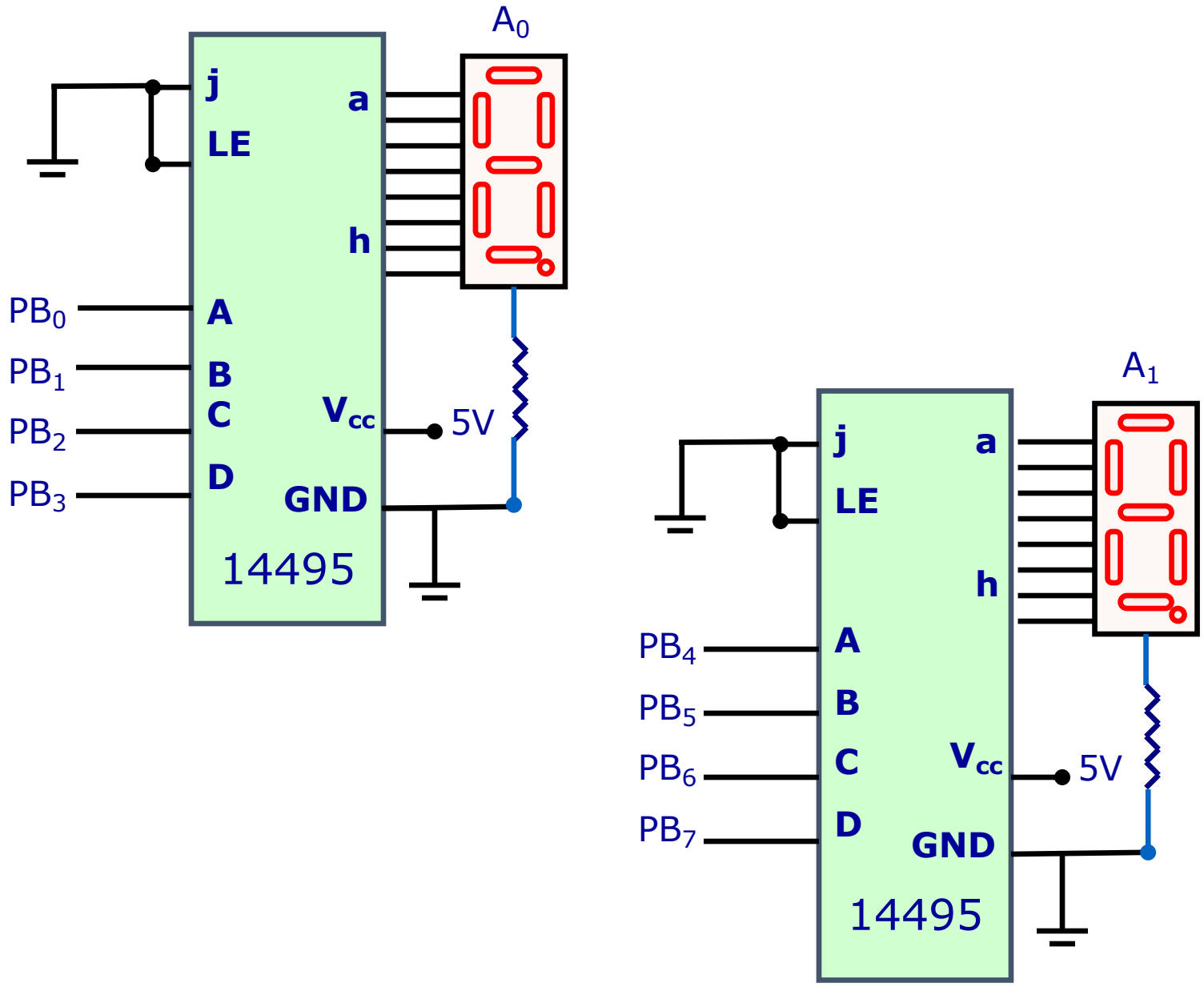
8255_1 Interface to the processor



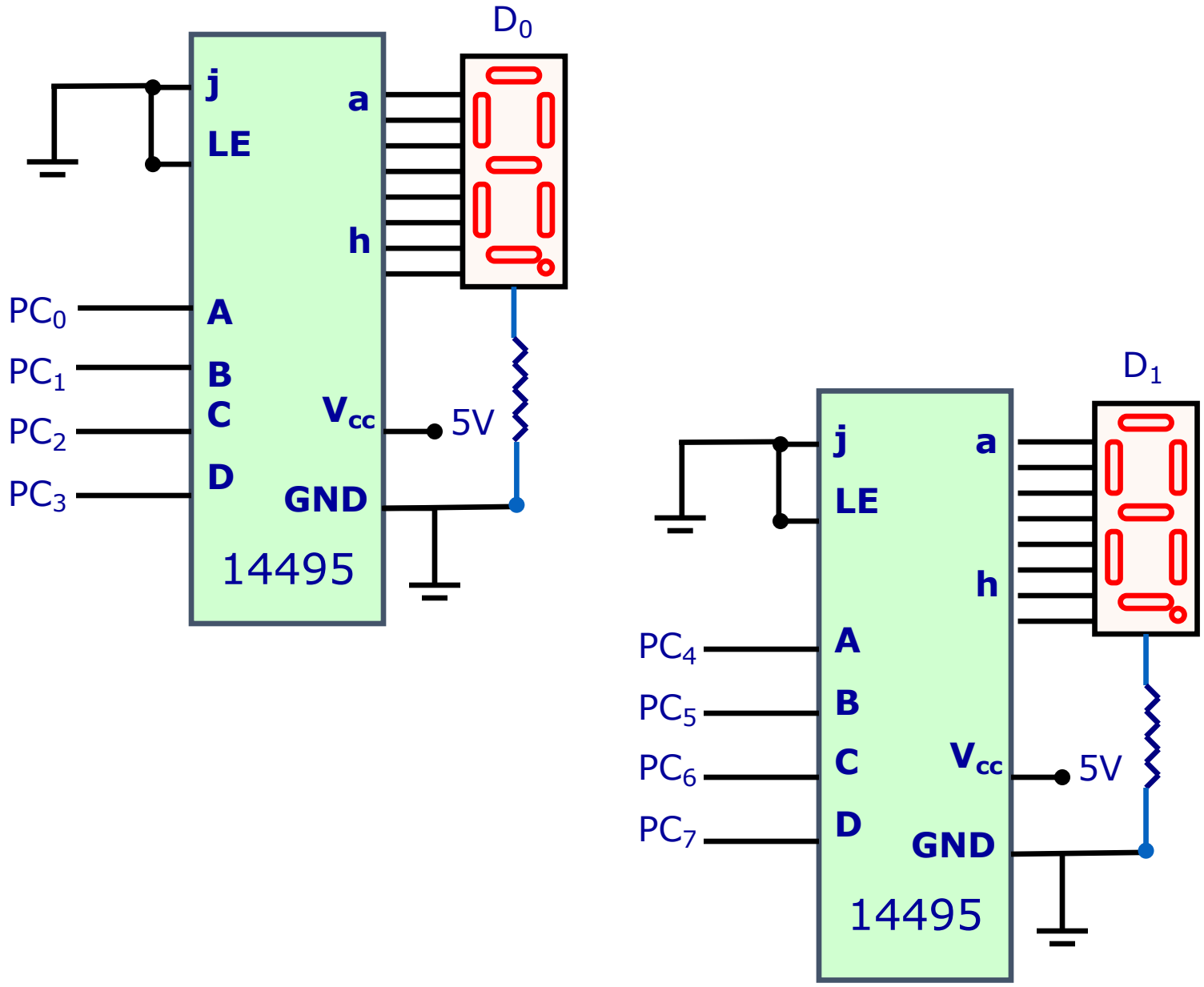
8255_1 to 14495 (for 7-seg display)



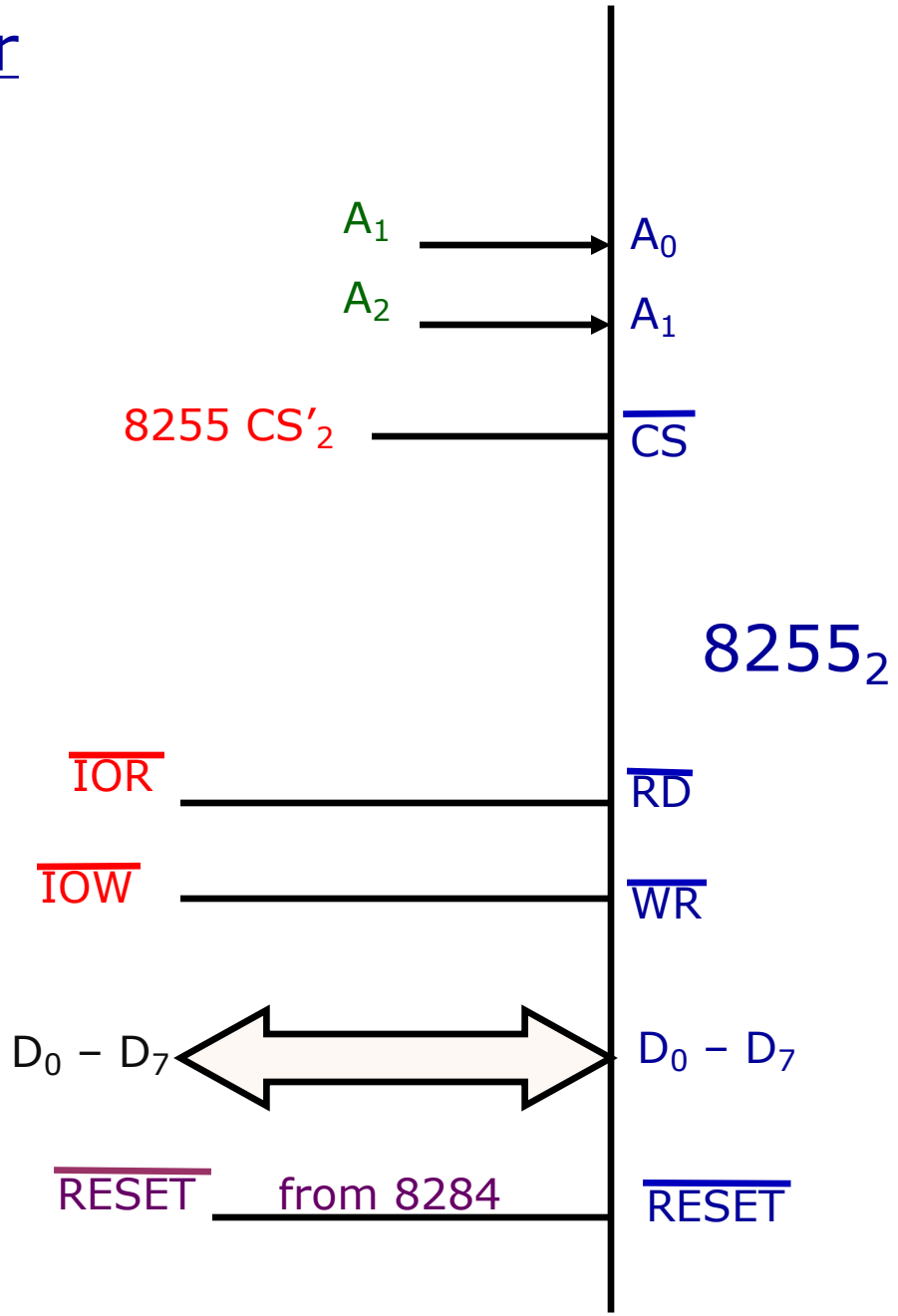
8255$_1$ to 14495 (for 7-seg display)

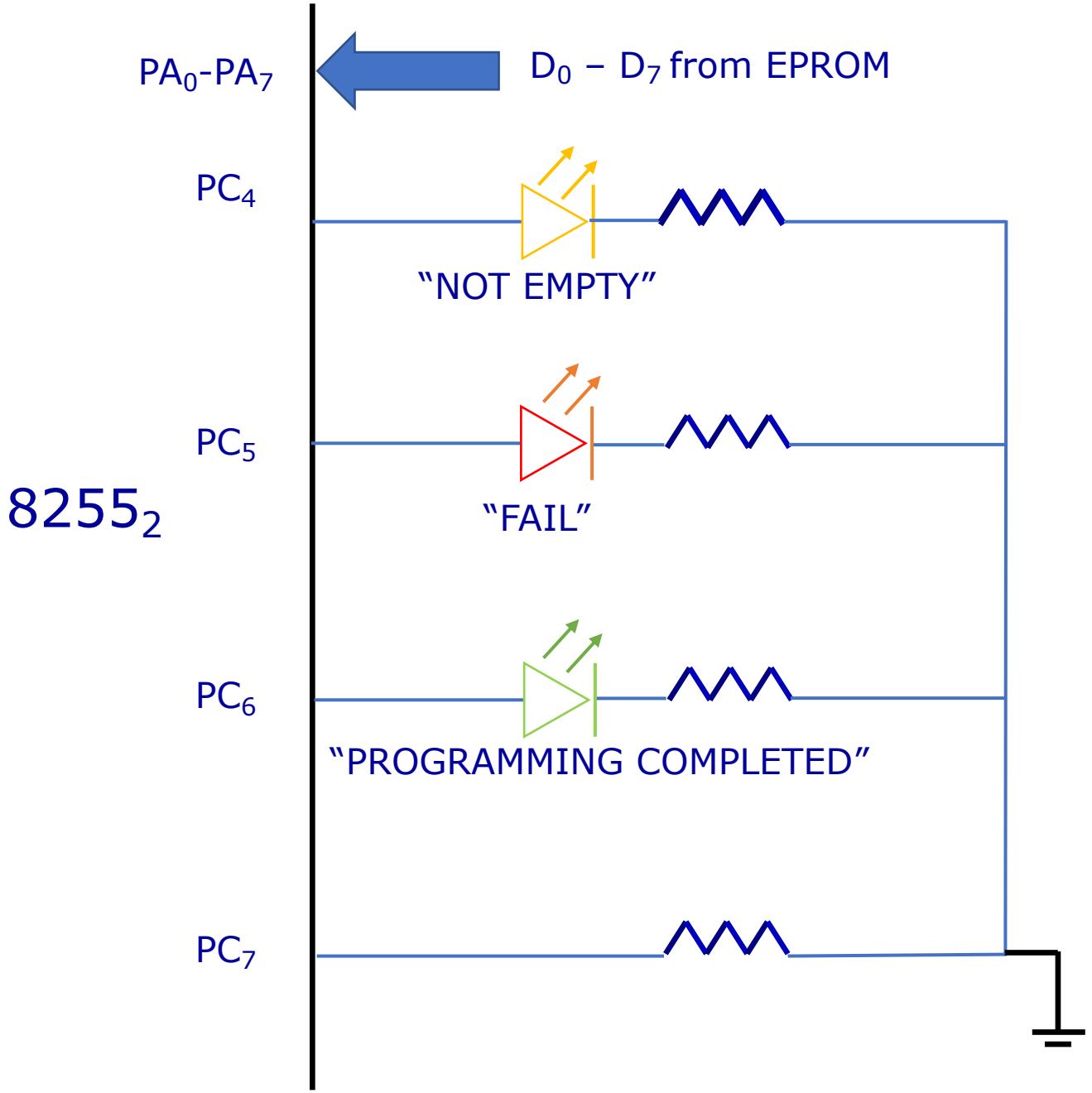


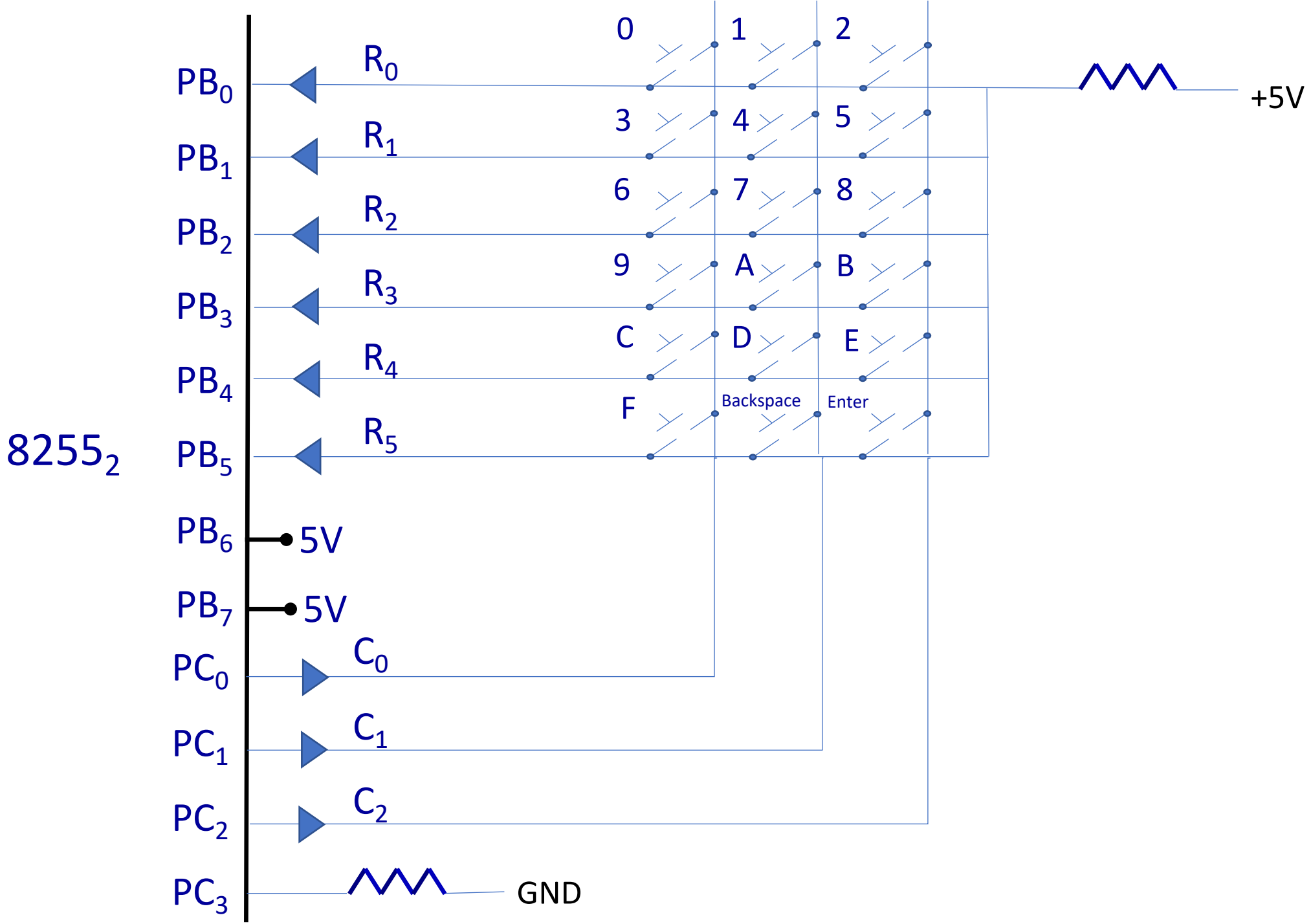
8255$_1$ to 14495 (for 7-seg display)



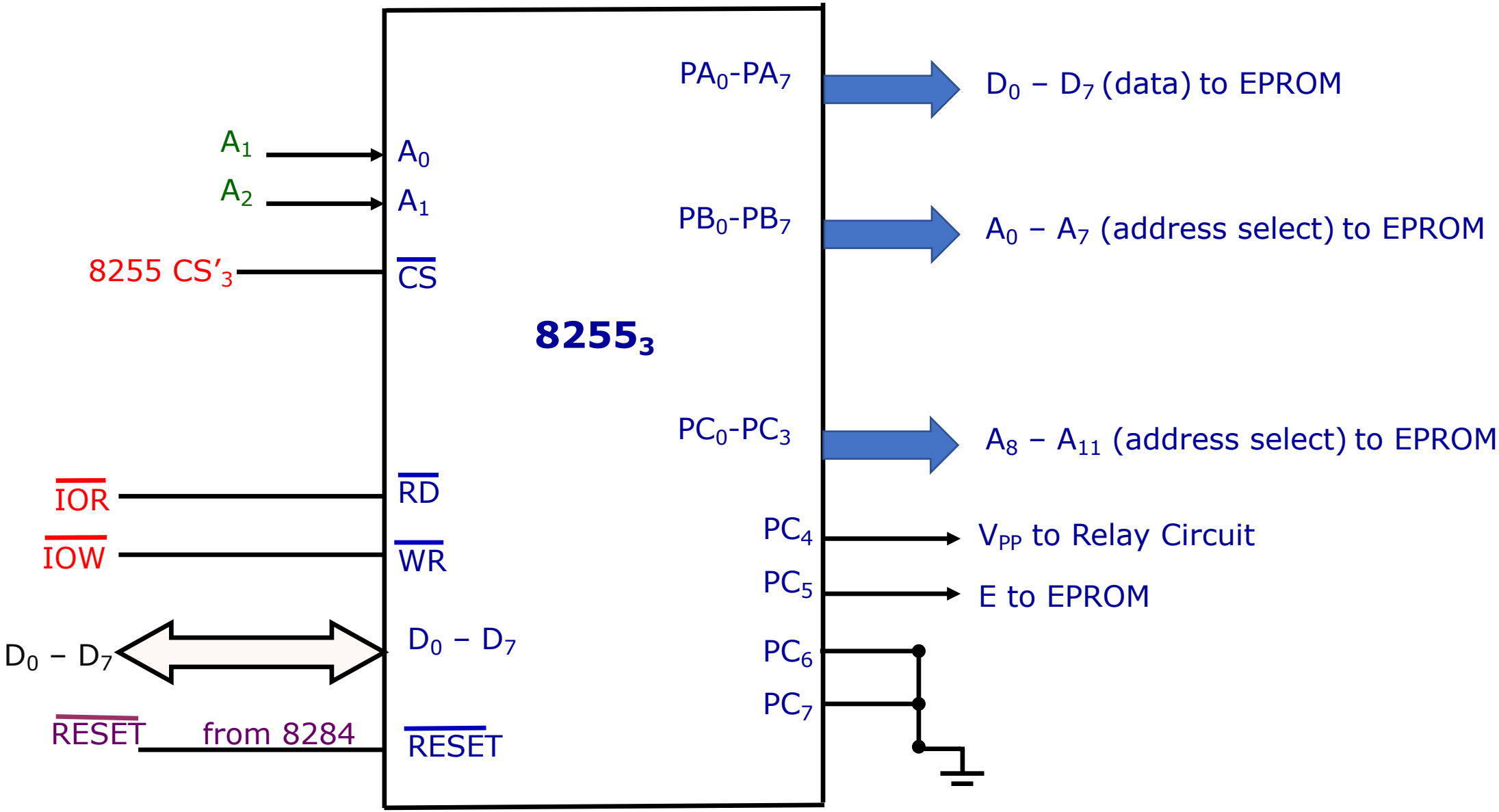
8255_2 Interface to the processor



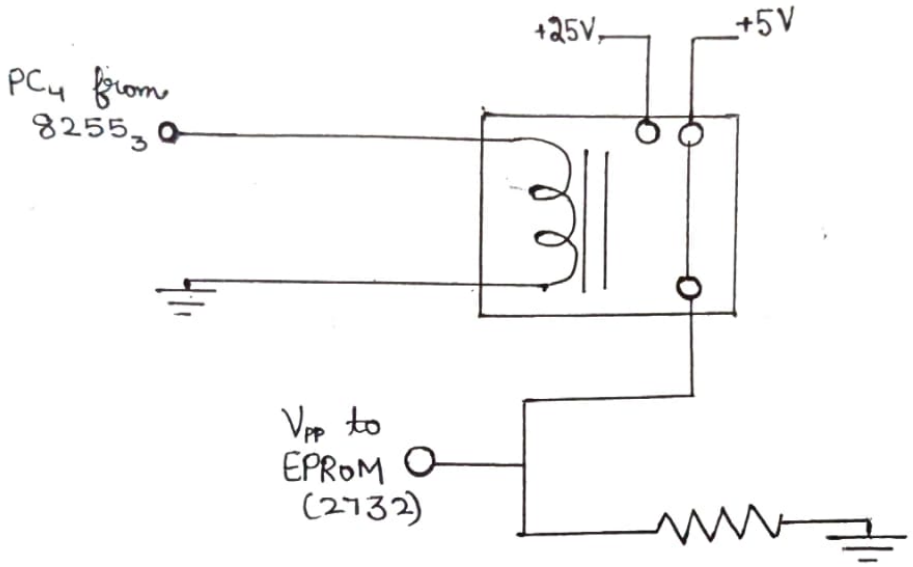

PA0-PA7
D0 – D7 from EPROM
PC4
"NOT EMPTY"
PC5
8255 2
"FAIL"
PC6
"PROGRAMMING COMPLETED"
PC7

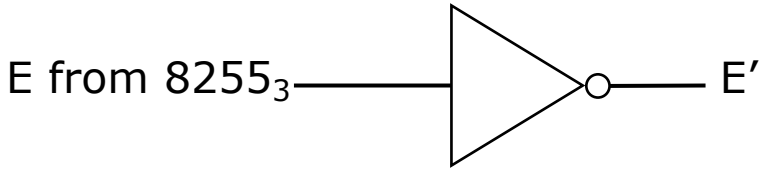

8255₂
PB0
PB1
PB2
PB3
PB4
PB5
PB6
PB7
PC0
PC1
PC2
PC3
R0
R1
R2
R3
R4
R5
5V
5V
C0
C1
C2
GND
0
1
2
3
4
5
6
7
8
9
A
B
C
D
E
F
Backspace
Enter
+5V

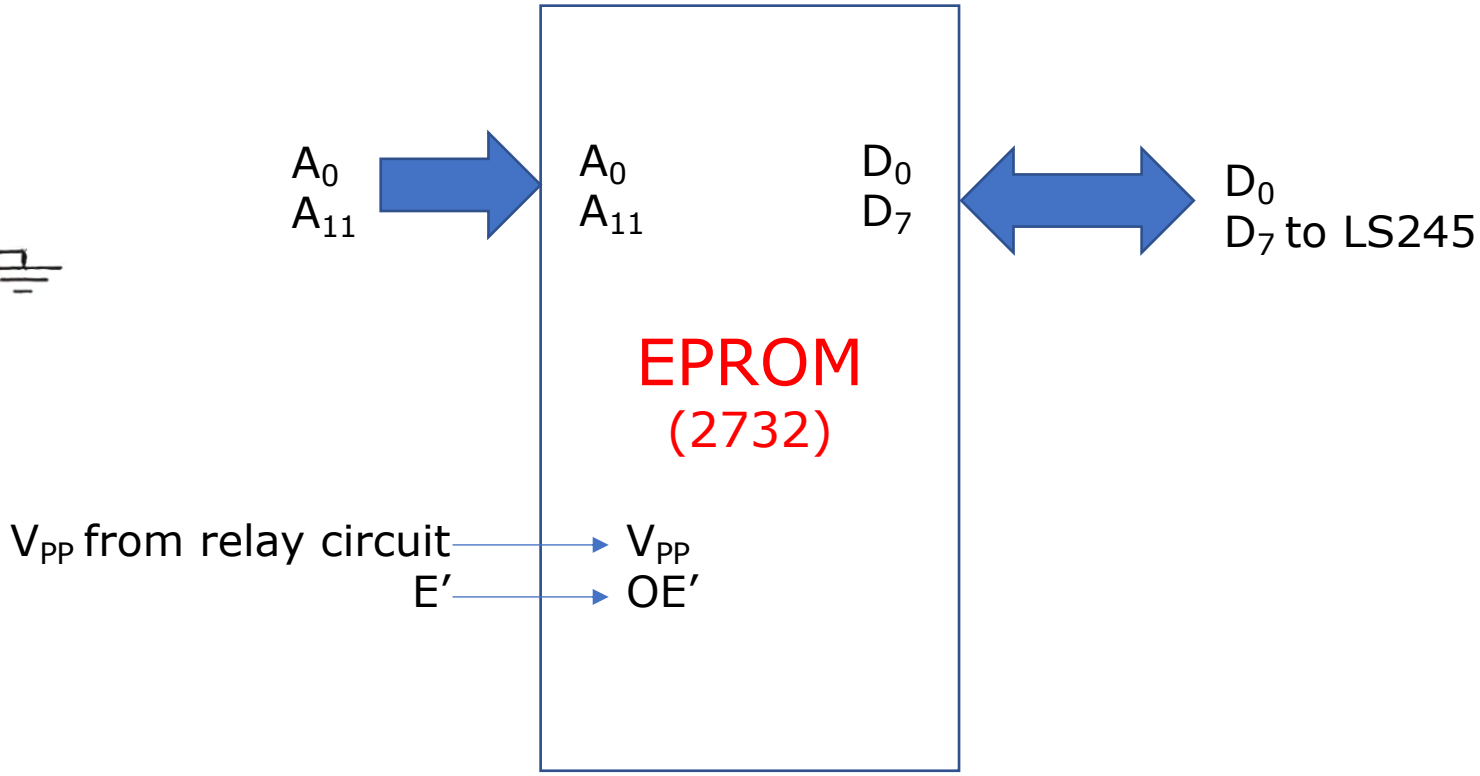
8255_3 Interface to the processor (left) and EPROM (right)



Relay circuit and EPROM







EPROM Data Lines Interfacing