Course: BCT 2408 COMPUTER ARCHITECTURE
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A. Direct-Mapped Cache with Consecutive Allocation

System Configuration:

- Cache size: 16 KB = 16,384 bytes
- Cache type: Direct-mapped
- Line size: 64 bytes
- Addressing: Physical
- Array element size: 4 bytes (single-precision float)
- Arrays `X` and `Y`: 4096 elements each, stored consecutively in memory

Loop Behavior:

- Iterates 4096 times
- Each iteration performs:
  - Load `X[i]`
  - Load `Y[i]`
  - Store `X[i]`
- Total memory operations: `3 × 4096 = 12,288`

Memory Layout & Cache Mapping:

- `X`: 4096 × 4 = 16 KB
- `Y`: 16 KB

- Total: 32 KB (exceeds cache size)
- Cache lines: 16 KB / 64 = 256 lines
- Each cache line holds: 64 / 4 = 16 elements
- Both `X` and `Y` span 256 cache lines

Since the cache is direct-mapped and the arrays are stored back-to-back, `X[i]` and `Y[i]` map to the **same cache lines**, leading to **conflict misses**.

Cache Miss Analysis:

- **Compulsory Misses**:

    - 256 blocks for `X` + 256 for `Y` = **512 misses**
- **Conflict Misses**:
    - Every access after the first causes a miss:
        - Load `X[i]`: miss (conflicted by `Y[i]`)
        - Load `Y[i]`: miss (conflicted with `X[i]`)
        - Store `X[i]`: miss (block evicted by `Y[i]`)
    - Total: 3 × 4096 = 12,288 accesses
    - Subtract compulsory: 12,288 - 512 = **11,776 conflict misses**
- **Capacity Misses**: None — active working set is only two elements at any time

Final Stats:

- Total cache misses: **12,288**
- Miss rate: **100% (1.0)**

B. Optimization: Padding to Avoid Conflicts

Goal: Eliminate conflict misses by ensuring `X` and `Y` map to **different cache lines**

Strategy:

- Introduce a **padding array** between `X` and `Y` in memory
- Offset `Y`'s base address by at least 16 KB so it no longer shares lines with `X`
- Result: `X` and `Y` occupy disjoint cache regions

Mapping:

- `X`: occupies cache lines 0–255
  Padding: occupies lines 256–511 (unused)
- `Y`: mapped to different cache lines, avoiding overlap

Cache Miss Analysis:

- **Compulsory Misses**:
    - `X`: 256
    - `Y`: 256
    - Total: **512**
- **Conflict Misses**: Eliminated (no line overlap)
- **Capacity Misses**: None — only a few elements used at once

Final Stats:

- Total cache misses: **512**
- Miss rate: 512 / 12,288 ≈ **4.17%**

C. Hardware-Based Optimization: 2-Way Set-Associative Cache

Upgrade:

- Cache remains 16 KB with 64-byte lines
- Switch from direct-mapped to **2-way set-associative**

New Configuration:

- Total cache lines: 16 KB / 64 B = 256
- 2 lines per set → 128 sets
- `X[i]` and `Y[i]` can now reside in the **same set without eviction**

Impact:

- Reduces conflict misses: `X` and `Y` can coexist
- No added capacity issues since working set is still minimal

Cache Miss Analysis:

- **Compulsory Misses**:
  - `X`: 256
  - `Y`: 256
  - Total: **512**
- **Conflict Misses**: None (2-way associativity resolves mapping conflict)
- **Capacity Misses**: None

Final Stats:

- Total cache misses: **512**
- Miss rate: 512 / 12,288 ≈ **4.17%**

Summary Comparison

Scenario	Compulsory Misses	Conflict Misses	Capacity Misses	Total Misses	Miss Rate
A. Direct-Mapped (No Padding)	512	11,776	0	12,288	100%
B. With Padding	512	0	0	512	4.17%
C. 2-Way Set-Associative	512	0	0	512	4.17%