MIMXRT1064-EVK

Table of Content

Revision History

Rev. Code	Date	By	Description
A	2018-7-4	Shawn Shi	Initial Release
A1	2019-2-21	Shawn Shi	Update BOM: change R126 to R129 from populate to DNP, Populate SW5, Change C88 to 2.2uF/35V. Add notes for DQS PIN
A2	2020-03-12	Shawn Shi	Update BOM: Change U32 from DNP to populate

1. Unless Otherwise Specified:

   All resistors are in ohms, 1/16 Watt,0402
   All capacitors are in uF,0402
   All voltages are DC
   All polarized capacitors are aluminum electrolytic

2. Interrupted lines coded with the same letter or letter combinations are electrically connected.

3. Device type number is for reference only. The number varies with the manufacturer.

4. Special signal usage:
   _B Denotes - Active-Low Signal
   <> or [] Denotes - Vectored Signals

5. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

ICAP Classification: CP: __ IUO: X PUBI: __

Drawing Title: MIMXRT1064-EVK

Page Title: COVER

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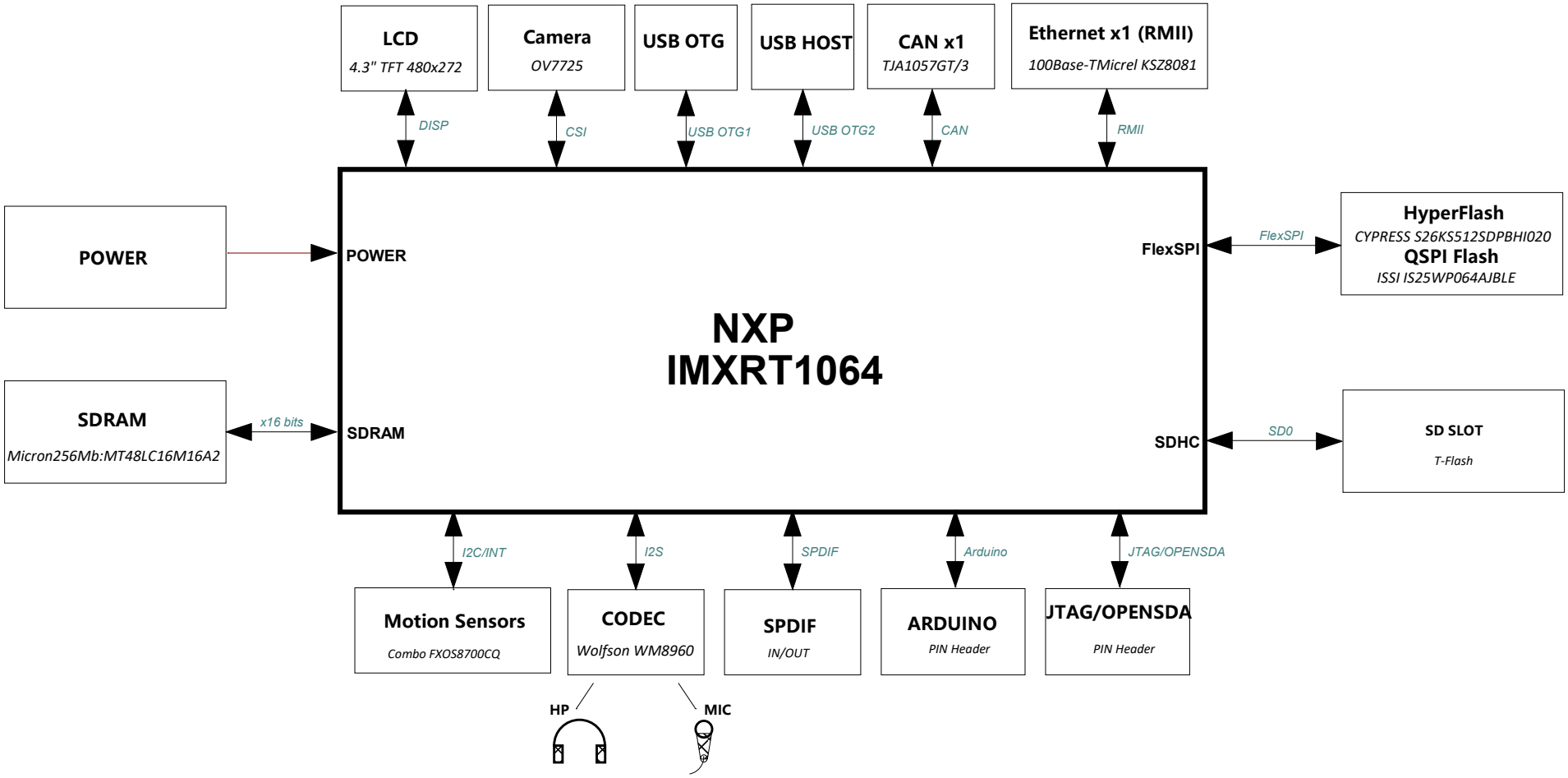
Blcok Diagram Rev A2#####

MIMXRT1064-EVK



ICAP Classification: CP: ___ IUO: X PUBI: ___

Drawing Title: MIMXRT1064-EVK

Page Title: BLOCK DIAGRAM

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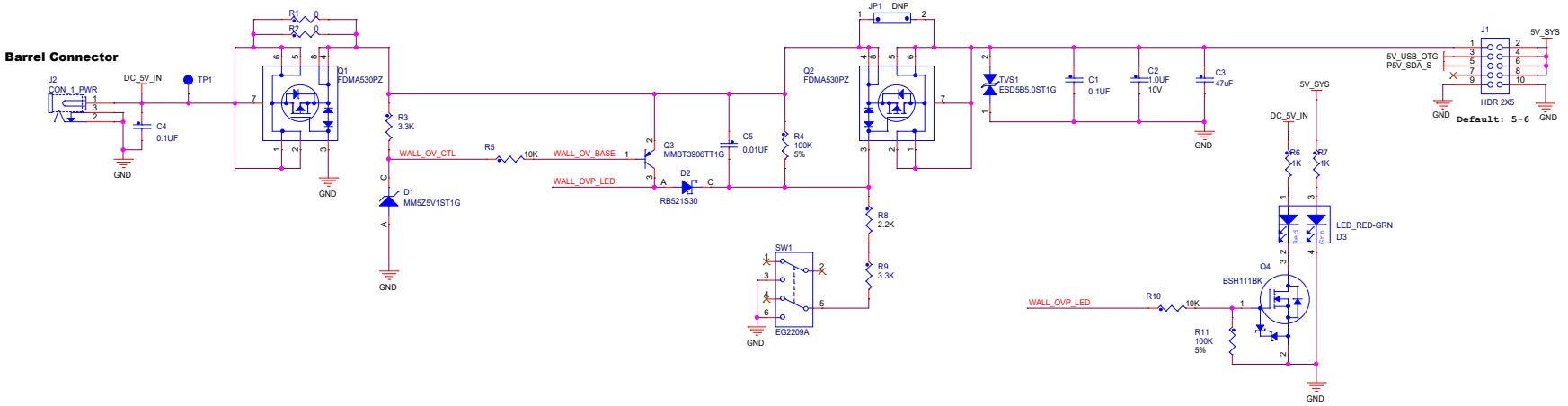
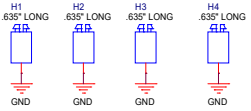
Main Power



Board Mounting Holes



Ground TPs

Layout Note: Place Ground TPs
to assist signal measurement.

ICAP Classification:	CP: ___	IUO: X	PUBI: ___
Drawing Title:	MIMXRT1064-EVK		
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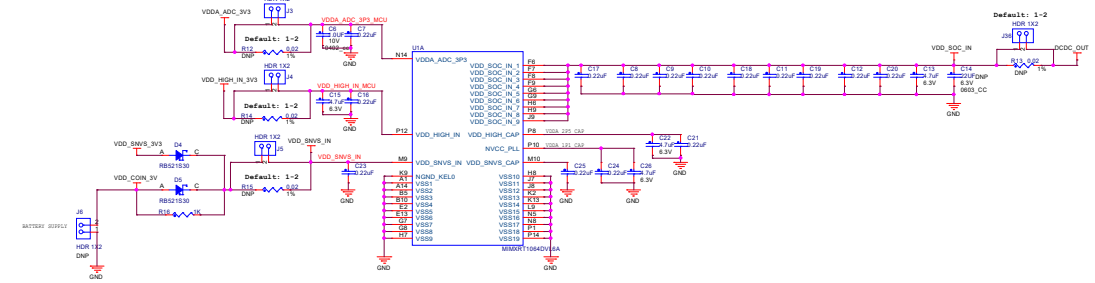
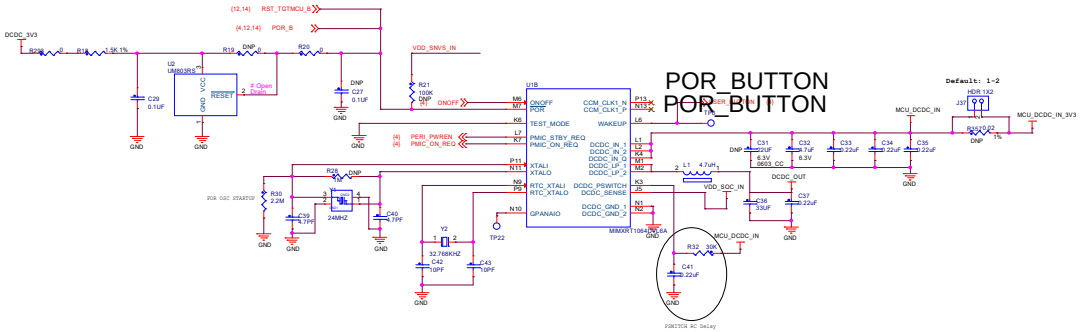
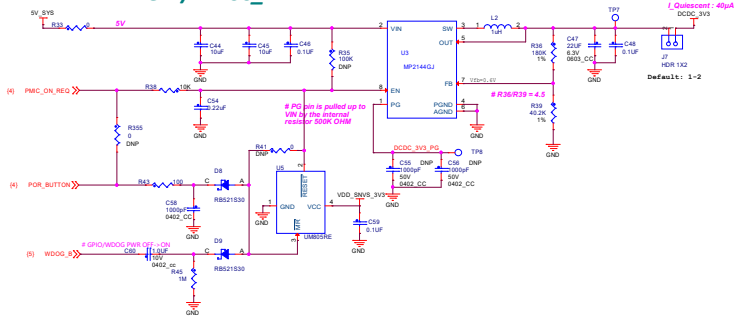


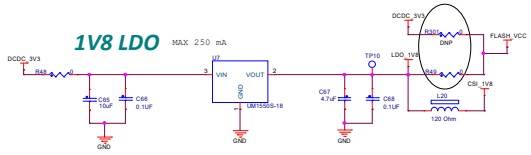


VDDHIGH / NVCC_xxx

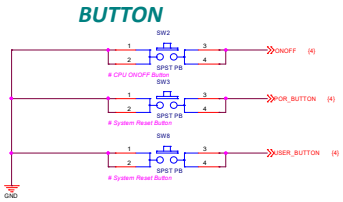


FLASH VCC

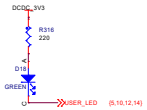
1V8 LDO MAX 250 mA



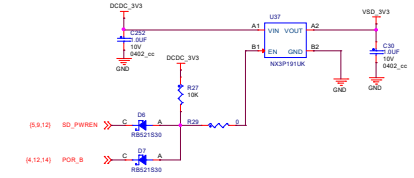
BUTTON



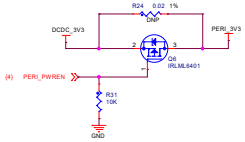
USER LED



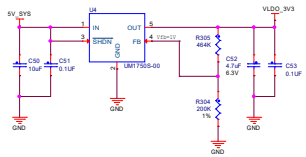
SD CARD POWER SWITCH



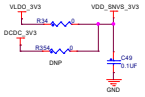
LCD 3V3 POWER SWITCH



3V3 LDO for SNVS

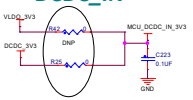


SNVS

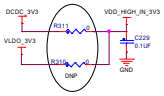


ADC

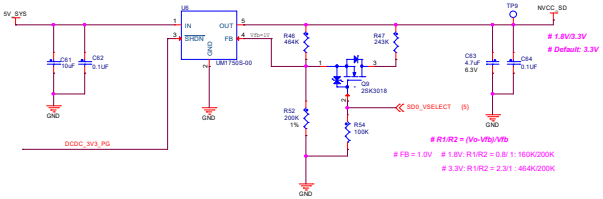
DCDC_IN



VDD_HIGH_IN



NVCC_SD <SD3.0> MAX 350 mA



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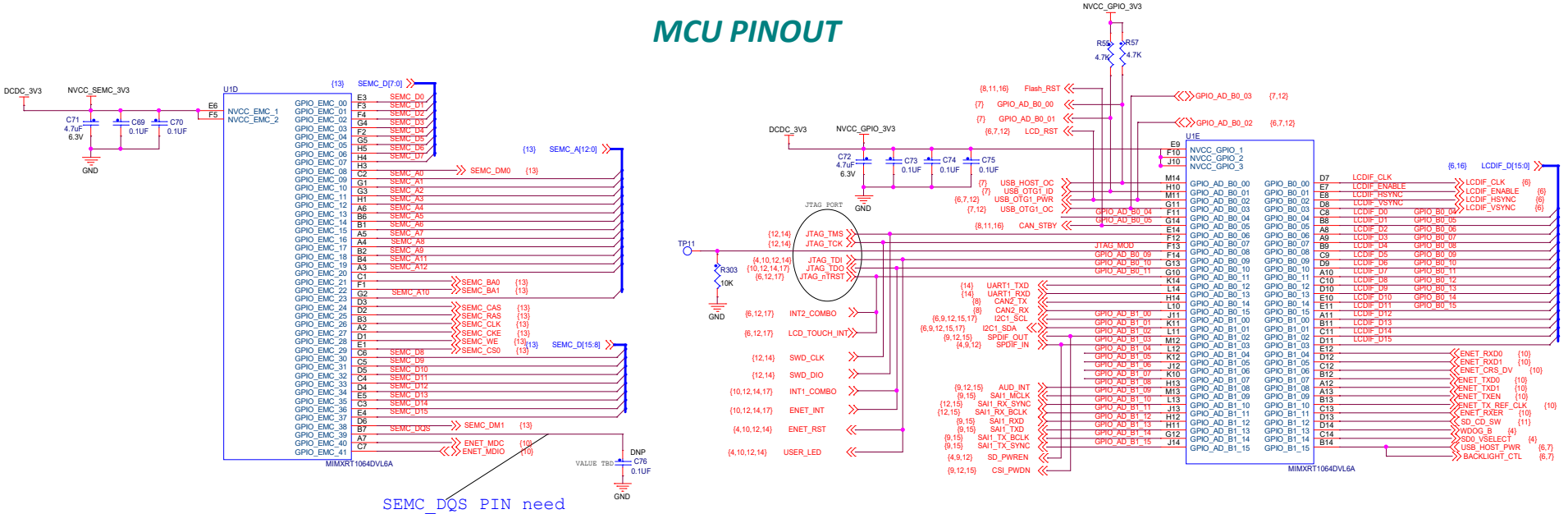
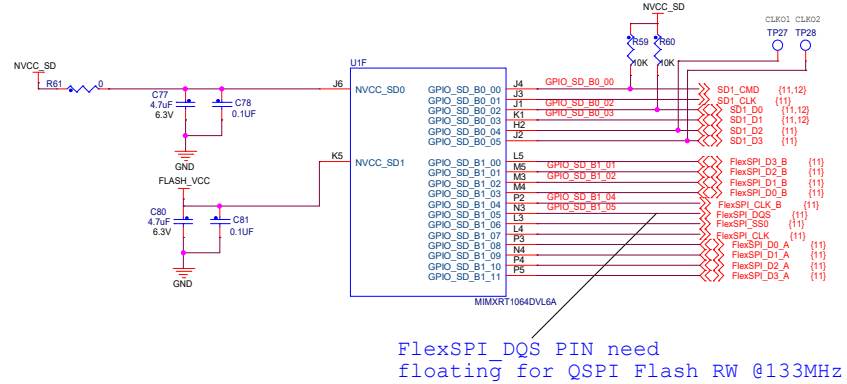
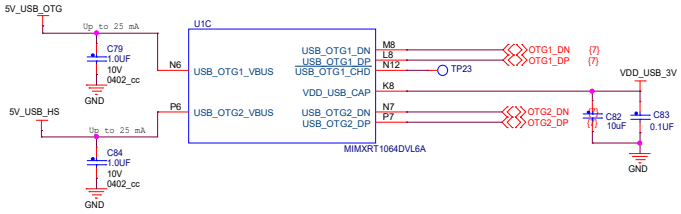
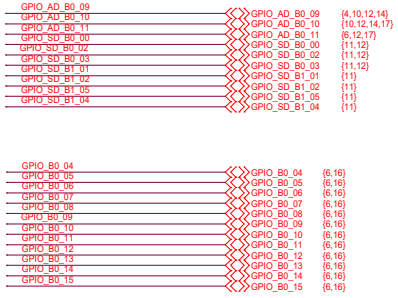
MCU PINOUT

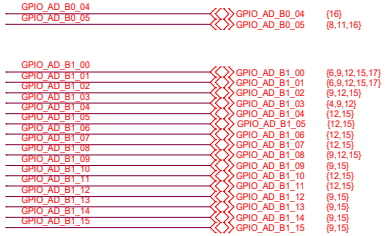

U1D
MIMXRT1064DVL6A
SEMC_DQS PIN need
floating for SDRAM RW @166MHz

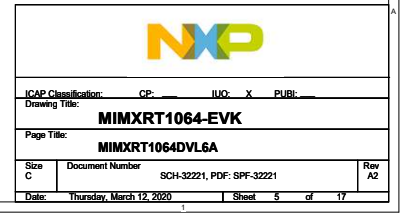

U1F
MIMXRT1064DVL6A
FlexSPI_DQS PIN need
floating for QSPI Flash RW @133MHz

U1E
MIMXRT1064DVL6A
JTAG PORT


U1C
MIMXRT1064DVL6A



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IUO: X
PUBI: ___
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MIMXRT1064-EVK
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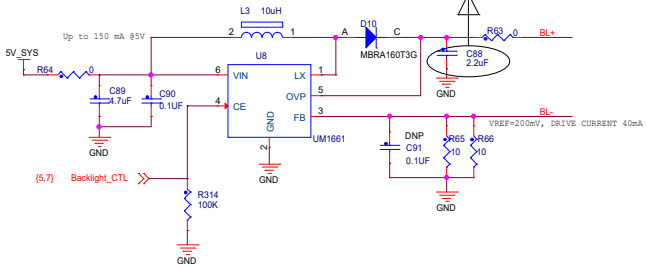
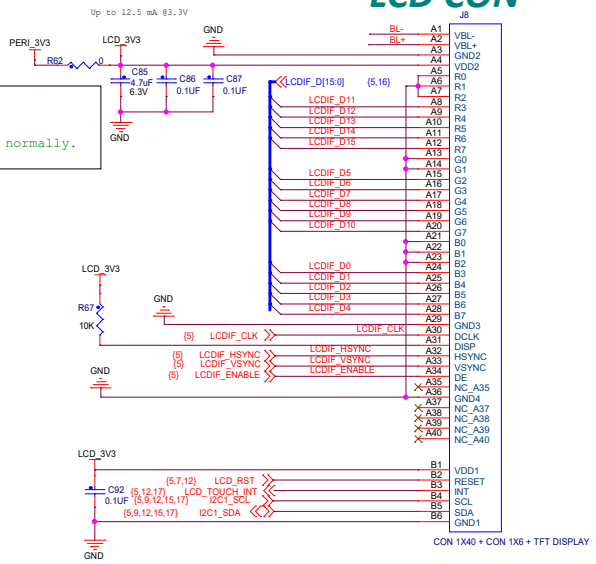
Backlight Control



Note:
If you use LCD module for Rev A, need to
change C88 to 2.2uf/35V or 1.0uf/35V
to ensure the backlight control circuits working normally.

LCD CON



CON 1X40 + CON 1X6 + TFT DISPLAY

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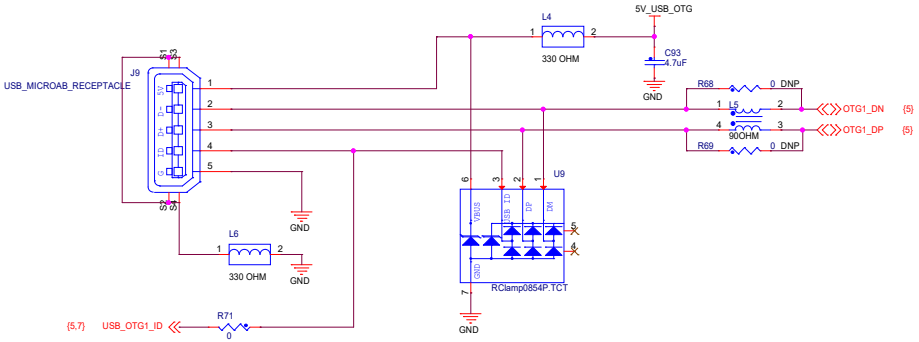
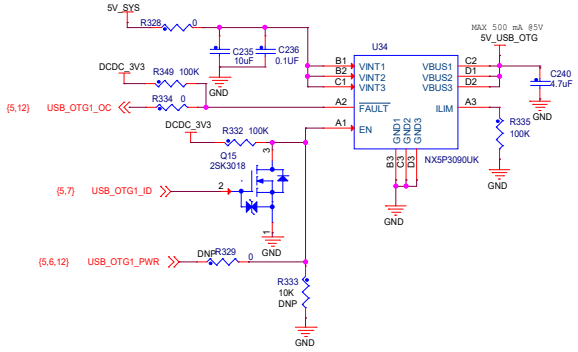
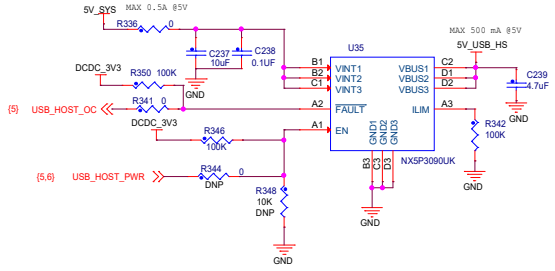
USB OTG

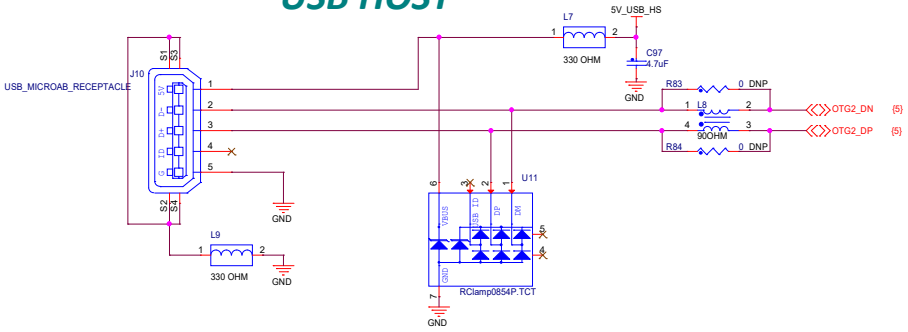


USB POWER





USB HOST



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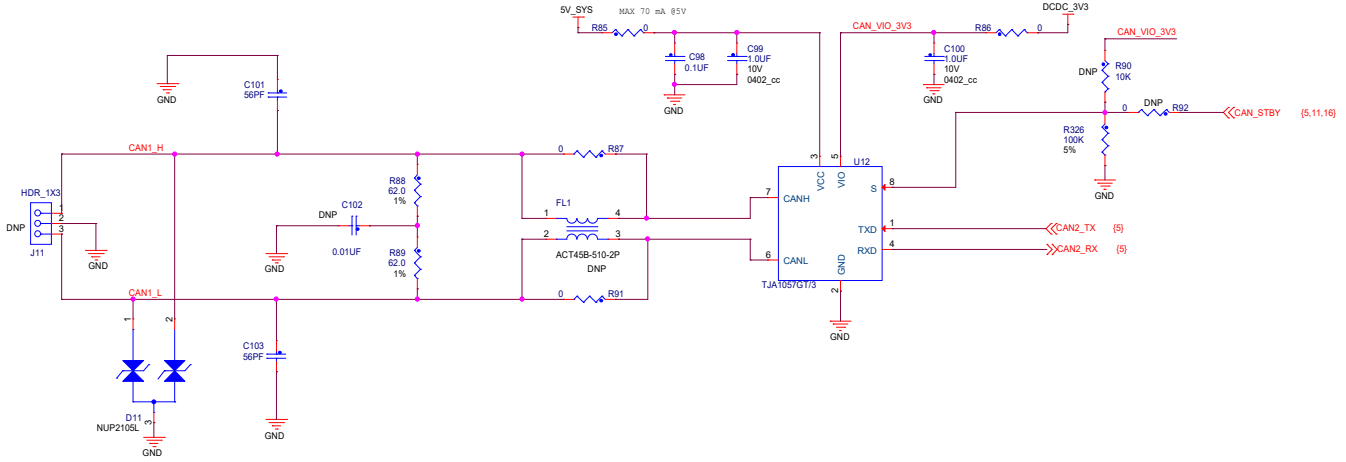
CAN BUS



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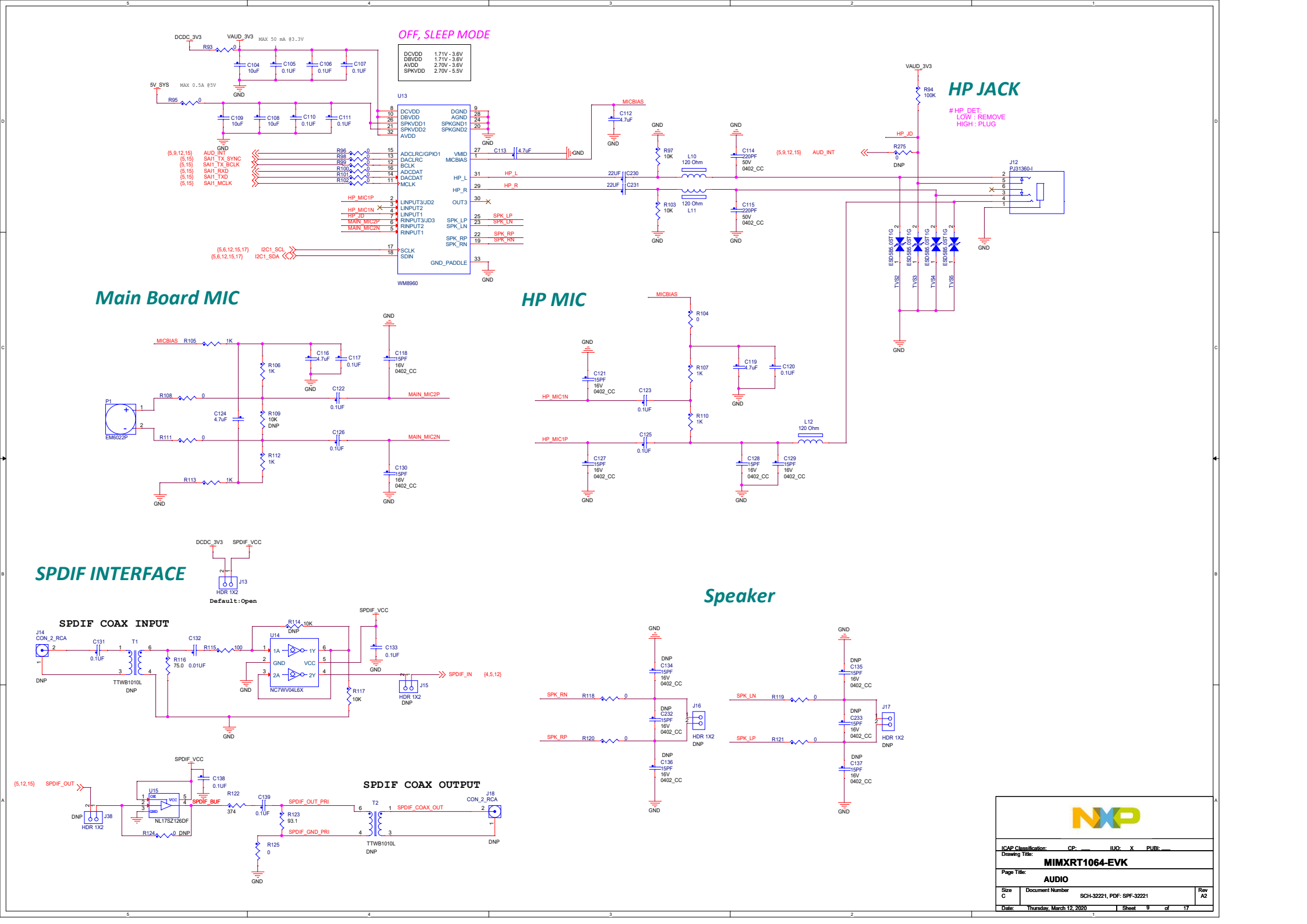
OFF, SLEEP MODE
DCVDD 1.71V - 3.6V
DBVDD 1.71V - 3.6V
AVDD 2.70V - 3.6V
SPKVDD 2.70V - 5.5V
HP JACK
HP_DET:
LOW : REMOVE
HIGH : PLUG
Main Board MIC
HP MIC
SPDIF INTERFACE
Speaker
SPDIF COAX INPUT
SPDIF COAX OUTPUT
WM8960
NC7WV04L6X
NL17SZ126DF
TTWB1010L
EM6022P
ESD585_0ST1G
ICAP Classification: CP: ___ IUO: X PUBI: ___
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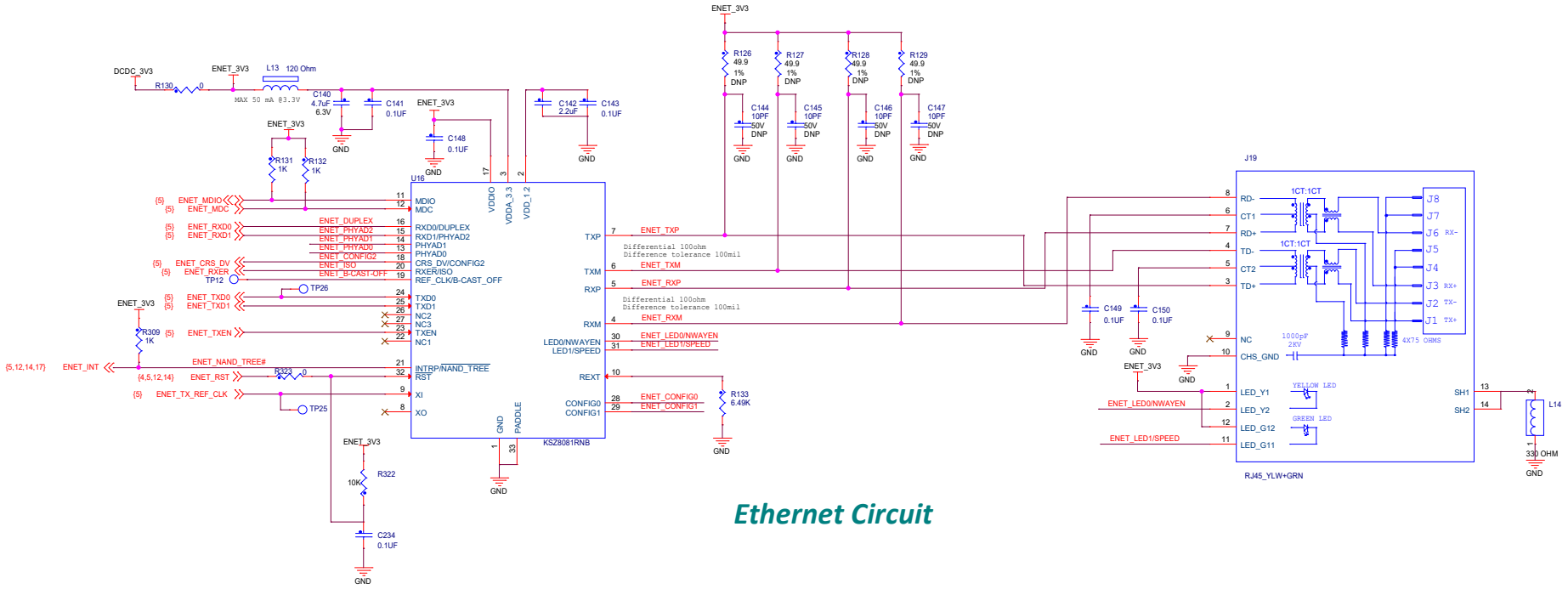
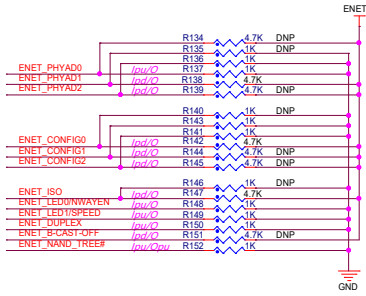


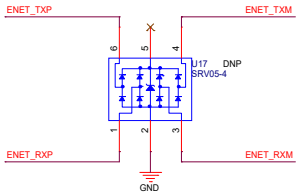
Ethernet Circuit



# CFG	Description
PHYAD[2:0]	PHY ADDR 00-XXX (00010 DEFAULT)
CONFIG[2:0]	IF MODE 001 RMII 101 RMII Back-to-Back xxx Reserved-not used
ISO	ISOLATE mode Pull-up = Enable Pull-down (default) = Disable
SPEED	SPEED mode Pull-up (default) = 100Mbps Pull-down = 10Mbps

# CFG	Description
DUPLEX	DUPLEX mode Pull-up (default) = Half Duplex Pull-down = Full Duplex
NWAYEN	Nway Auto-Negotiation Pull-up (default) = Enable Pull-down = Disable
B_CAST_OFF	Broadcast Off - for PHY Address 0 Pull-up = PHY Address 0 set as unique PHY addr Pull-down (default) = PHY Address 0 set as broadcast PHY addr
NAND_TREE#	NAND Tree Mode Pull-up (default) = Disable Pull-down = Enable

ESD PROTECTION



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Page Title: **ETHERNET**

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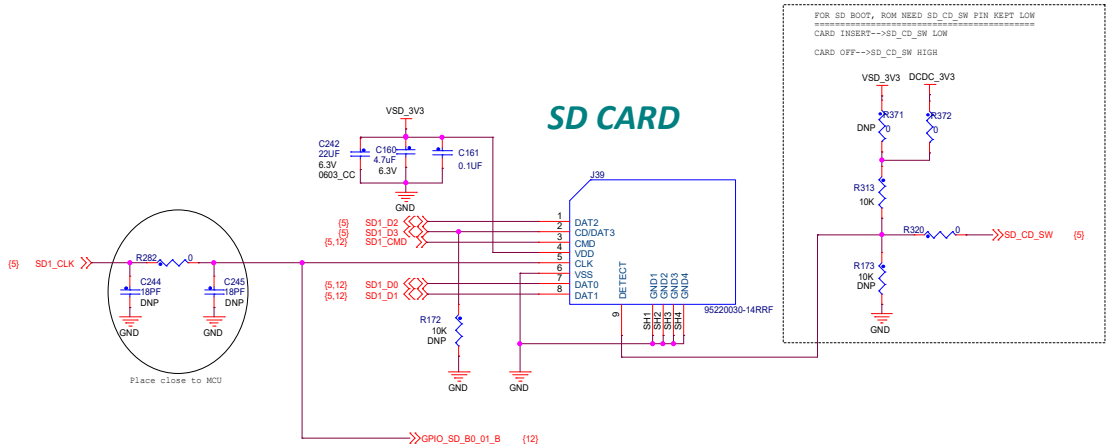
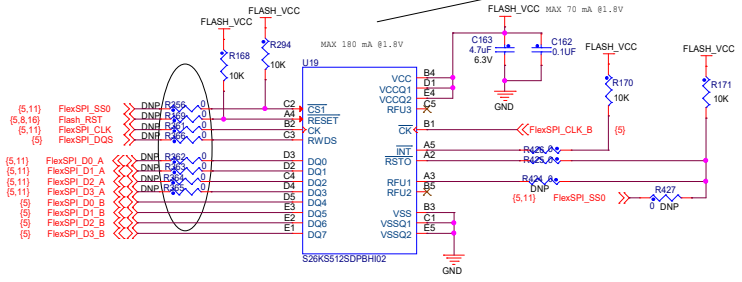
SD CARD



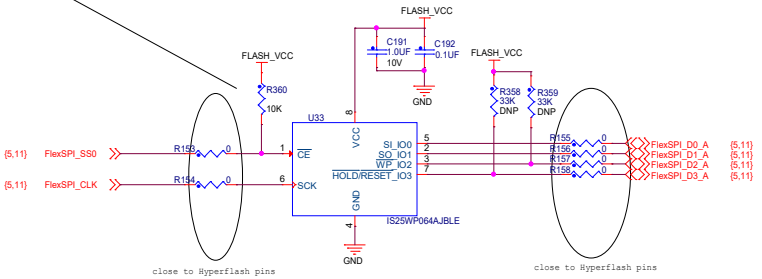
OPTION1: USE Hyperflash(DNP R153~R158, Mount R356,R361~R366)
OPTION2: USE QSPI FLASH(Mount R153~R158, DNP R356,R361~R366)

1V8 HyperFlash



Share the same package with S27KS0641DPBHI023
(if HYPERRAM is replaced, then DNP R425,R426,Mount R424,R427)

1V8 QSPI Flash



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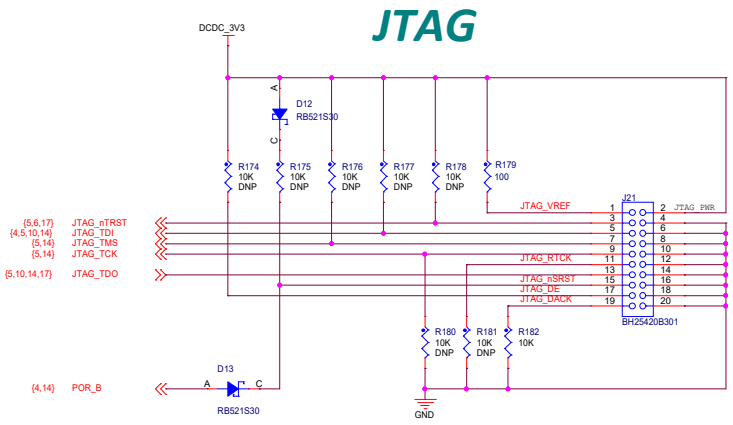
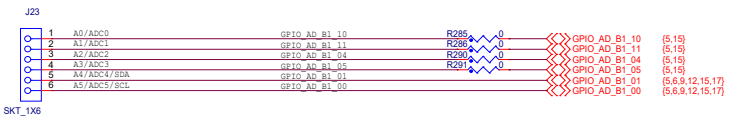
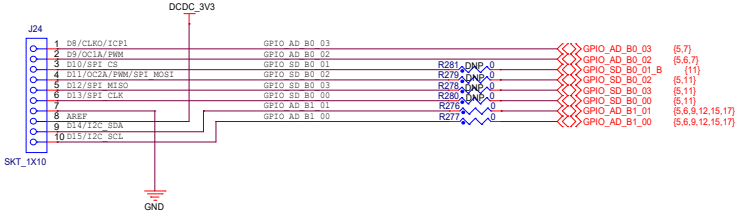
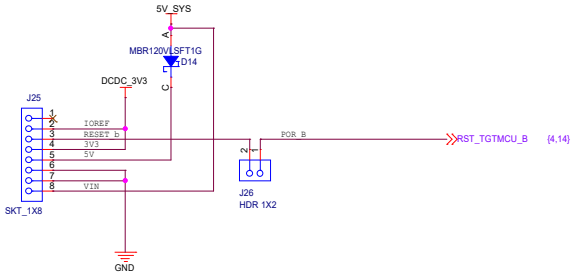


Arduino Interface







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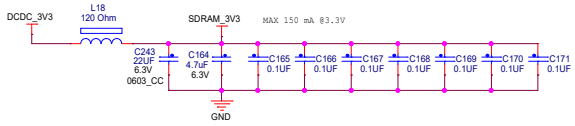
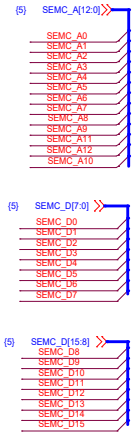
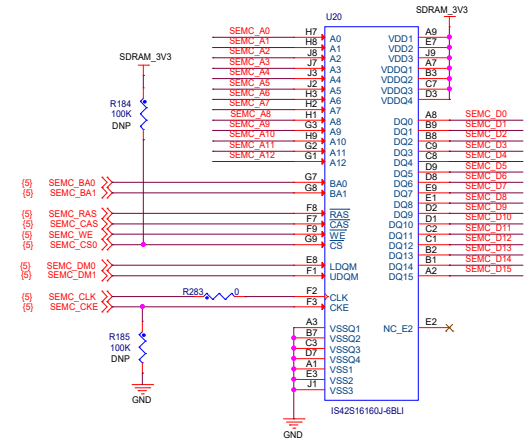
SDRAM







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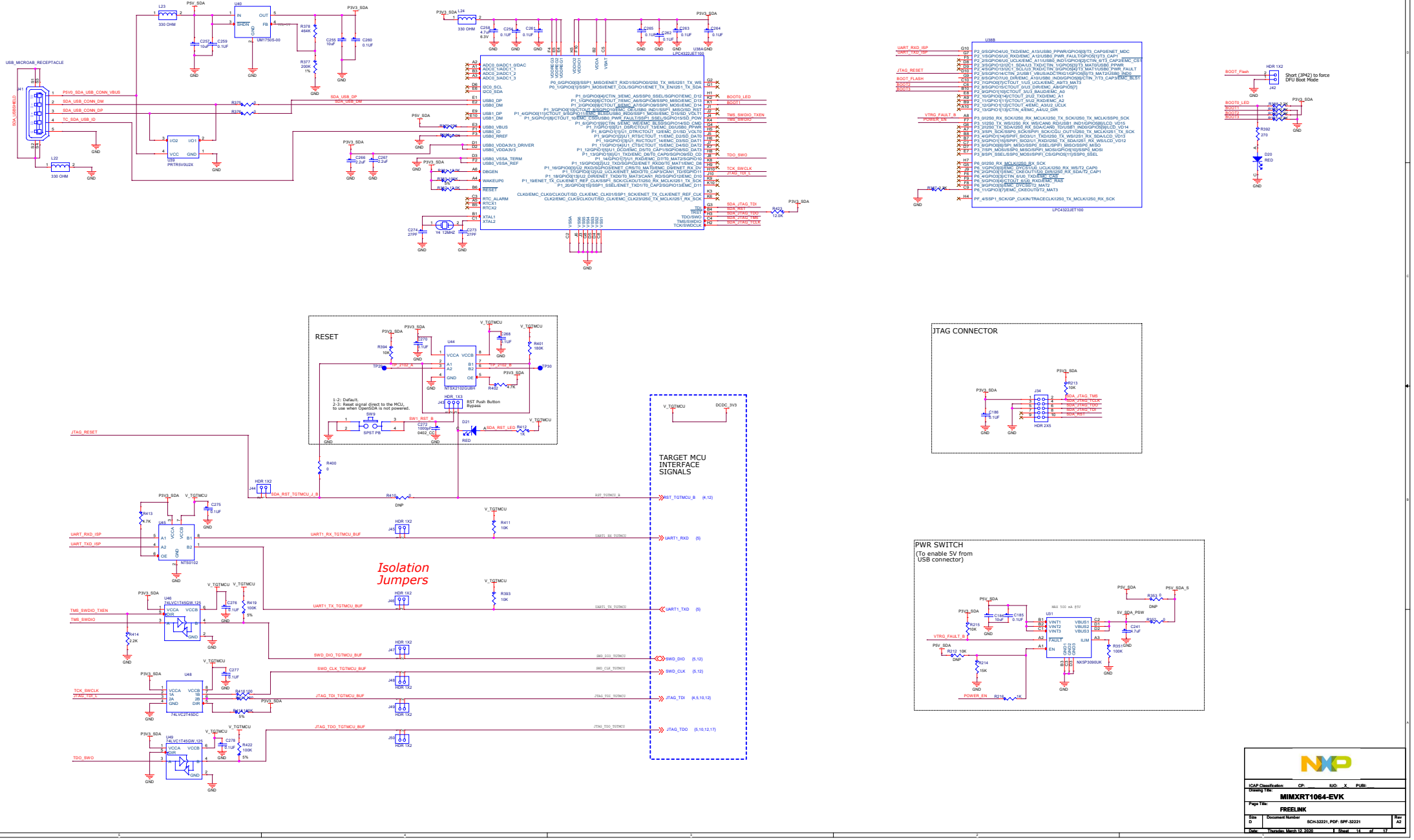
Freelink Interface



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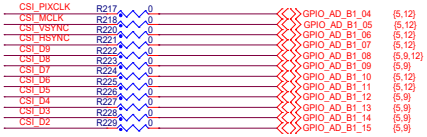
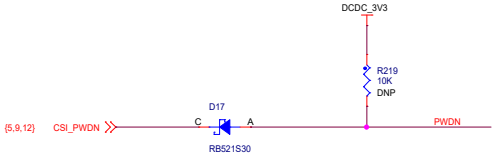
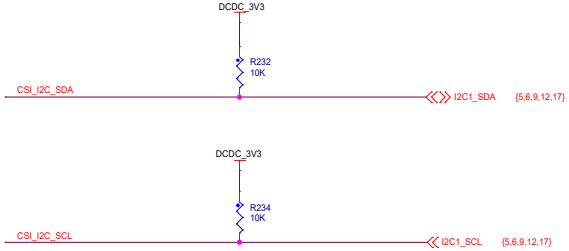
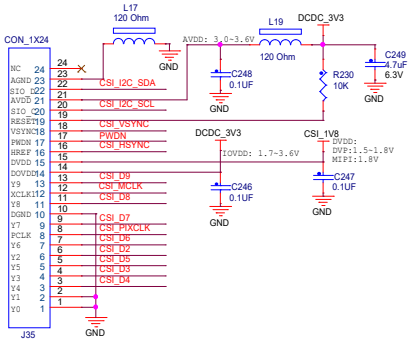
Camera Signals







FPC FOR MT9M114/OV7725 MODULE



ICAP Classification:	CP: ___	IUO: X	PUBI: ___
Drawing Title:	MIMXRT1064-EVK		
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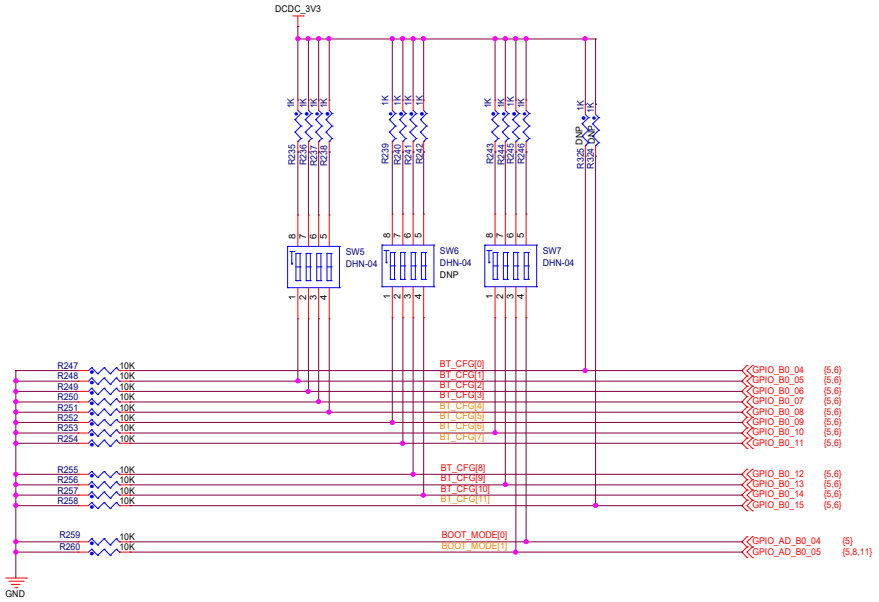
FUSE MAP

TYPE	BOOT_CFG[11]	BOOT_CFG[10]	BOOT_CFG[9]	BOOT_CFG[8]	BOOT_CFG[7]	BOOT_CFG[6]	BOOT_CFG[5]	BOOT_CFG[4]	BOOT_CFG[3]	BOOT_CFG[2]	BOOT_CFG[1]	BOOT_CFG[0]
	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
FlexSPI1 - Serial NOR	Infinit-Loop: (Debug USE only) 0 - Disable 1- Enable	FLASH_TYPE 000-Device supports 3B read by default 001-Device supports 4B read by default 010-HyperFlash 1V8 011-HyperFlash 3V3 100-MXIC Octal DDR			0	0	0	0	HOLD TIME: 00 - 500us 01 - 1ms 10 - 3ms 11 - 10ms		EncryptedXIP 0 - Disabled 1- Enabled	Reserved
SD	Infinit-Loop: (Debug USE only) 0 - Disable 1- Enable	Reserved	Bus Width: 0 - 1-bit 1 - 4-bit	SD1 VOLTAGE SELECTION: 0 - 3.3V 1 - 1.8V	0	1	SD/SDXC Speed: 00 - Normal/SDR12 01 - High/SDR25 10 - SDR50 11 - SDR104		SD Power Cycle Enable: '0' - No power cycle '1' - Enabled via USDHC_RST pad	SD Loopback Clock Source Sel: (for SDR50 and SDR104 only) '0' - through SD '1' - direct	Port Select: 0 - eSDHC1 1 - eSDHC2	Fast Boot: 0 - Regular 1 - Fast Boot



ICAP Classification: CP: ___ IUO: X PUBI: ___

Drawing Title: **MIMXRT1064-EVK**

Page Title: **BOOT**

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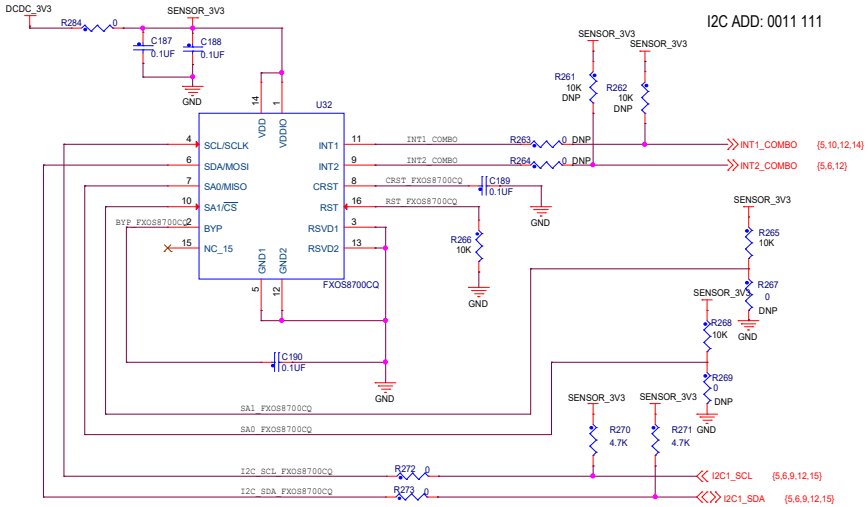
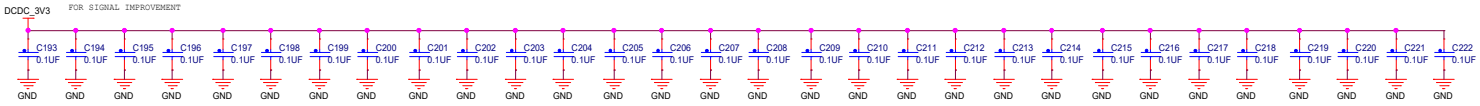
COMBO SENSOR



FXOS8700CQ COMBO SENSOR



ICAP Classification: CP: ___ IUO: X PUBI: ___

Drawing Title: **MIMXRT1064-EVK**

Page Title: **MISC**

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