VSC8257-01 Registers
Quad Channel 1G/10GBASE-KR to SFI Ethernet WIS PHY with VeriTime™

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Contents

1 Revision History

This section describes the changes that were implemented in this document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 2.0

Revision 2.0 of this document was published in September 2018. This was the first publication of the registers.

2 Registers

This section provides information about the programming interface, register maps, register descriptions, and register tables of the device.

Note: This register map is provided as a reference only. It is intended for use as a reference during debug activity. Unless expressly indicated, production designs that include the VSC8254-01, VSC8256-01, VSC8257-01, or VSC8258-01 devices should utilize the API for configuration and all device interaction.

Important Not all register functionality is tested, supported, or guaranteed.

Note: Registers pertaining to feature additions such as 1588 and MACsec are excluded at this time.

Use the following addresses to access a register using the SPI/I2C interface. Append the address offset to the port address to get the absolute address as follows:

- Channel 0: 0x000000 + address offset per register
- Channel 1: 0x200000 + address offset per register
- Channel 2: 0x400000 + address offset per register
- Channel 3: 0x600000 + address offset per register

For information about register addresses when using the MDIO interface, see the Management Interfaces functional descriptions in the VSC8257-01 datasheet and the API or contact your Microsemi representative.

2.1 LINE_PMA (Device 0x1)

Table 1 • **DEV1_IEEE_PMA_CONTROL**

Address	Short Description	Register Name	Details
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Table 2 • **DEV1_IEEE_PMA_STATUS**

Address	Short Description	Register Name	Details
0x10001	PMA Status Register 1	PMA_STATUS_1	Page 8

Table 3 • **DEV1_IEEE_PMA_DEVICE_ID**

Address	Short Description	Register Name	Details
0x10002	PMA Device Identifier 1	PMA_DEVICE_ID_1	Page 9
0x10003	PMA Device Identifier 2	PMA_DEVICE_ID_2	Page 9
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Table 4 • **DEV1_IEEE_PMA_PMD_STATUS**

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Table 5 • **DEV1_IEEE_PMD_CONTROL_AND_STATUS**

Address	Short Description	Register Name	Details
0x10009	PMD Transmit Disable	PMD_TRANSMIT_DISABLE	Page 13
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Table 6 • **DEV1_IEEE_PMA_PMD_PACKAGE_ID**

Address	Short Description	Register Name	Details
0x1001E	PMA/PMD Package Identifier 1	PMA_PMD_PACKAGE_ID_1	Page 14
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Table 7 • **KR_FEC_ABILITY**

Address	Short Description	Register Name	Details
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Table 8 • **KR_FEC_CONTROL_1**

Address	Short Description	Register Name	Details
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Table 9 • **KR_FEC_STATUS**

Address	Short Description	Register Name	Details
0x100AC	KR FEC Corrected Lower	KR_FEC_CORRECTED_LOWER	Page 15
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0x100AE	KR FEC Uncorrected Lower	KR_FEC_UNCORRECTED_LOWER	Page 16
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Table 10 • **KR FEC Control 2**

Address	Short Description	Register Name	Details
0x18300	KR FEC Control 2	KR_FEC_Control_2	Page 17

Table 11 • **Rx Alarm Control**

Address	Short Description	Register Name	Details
0x19000	Rx Alarm Control	RX_ALARM_Control_Register	Page 17

Table 12 • **Tx Alarm Control**

Address	Short Description	Register Name	Details
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Table 13 • **Rx Alarm Status**

Address	Short Description	Register Name	Details
0x19003	Rx Alarm Status	RX_ALARM_Status_Register	Page 18

Table 14 • **Tx Alarm Status**

Address	Short Description	Register Name	Details
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Table 15 • **Datapath Control**

Address	Short Description	Register Name	Details
0x1A002	10G or 1G mode in Datapath	DATAPATH_MODE	Page 20

Table 16 • **Enable MAC Datapath**

Address	Short Description	Register Name	Details
0x1A006	Enable MAC in the Datapath	MAC_ENA	Page 21

Table 17 • **BYPASS_CONFIG_STAT**

Address	Short Description	Register Name	Details
0x1A020	Repeater Mode Configuration	BYPASS_CFG1	Page 21
0x1A021	Bypass Status	BYPASS_STATUS	Page 22
0x1A022	Bypass Interrupt Enable	BYPASS_INTR_EN	Page 22
0x1A023	Bypass Interrupt	BYPASS_INTR	Page 22

Table 18 • **Vendor_Specific_PMA_Control_2**

Address	Short Description	Register Name	Details
0x1A100	Vendor Specific PMA Control 2	Vendor_Specific_PMA_Control_2	Page 23

Table 19 • **PMA_INTR**

Address	Short Description	Register Name	Details
0x1A202	PMA Status	PMA_STAT	Page 24
0x1A203	PMA Interrupt Mask	PMA_INTR_MASK	Page 25
0x1A204	PMA Interrupt Status	PMA_INTR_STAT	Page 25

Table 20 • **SPARE_RW_REGISTERS**

Address	Short Description	Register Name	Details
0x1AEF0	Device1 Spare R/W 0	DEV1_SPARE_RW0	Page 29
0x1AEF1	Device1 Spare R/W 1	DEV1_SPARE_RW1	Page 30
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0x1AEF3	Device1 Spare R/W 3	DEV1_SPARE_RW3	Page 30
0x1AEF4	Device1 Spare R/W 4	DEV1_SPARE_RW4	Page 30
0x1AEF5	Device1 Spare R/W 5	DEV1_SPARE_RW5	Page 30
0x1AEF6	Device1 Spare R/W 6	DEV1_SPARE_RW6	Page 31
0x1AEF7	Device1 Spare R/W 7	DEV1_SPARE_RW7	Page 31
0x1AEF8	Device1 Spare R/W 8	DEV1_SPARE_RW8	Page 31
0x1AEF9	Device1 Spare R/W 9	DEV1_SPARE_RW9	Page 31
0x1AEFA	Device1 Spare R/W 10	DEV1_SPARE_RW10	Page 31
0x1AEFB	Device1 Spare R/W 11	DEV1_SPARE_RW11	Page 32
0x1AEFC	Device1 Spare R/W 12	DEV1_SPARE_RW12	Page 32
0x1AEFD	Device1 Spare R/W 13	DEV1_SPARE_RW13	Page 32
0x1AEFE	Device1 Spare R/W 14	DEV1_SPARE_RW14	Page 32
0x1AEFF	Device1 Spare R/W 15	DEV1_SPARE_RW15	Page 32

Table 21 • **SD10G65_VScope2**

Address	Short Description	Register Name	Details
0x1B000	VScope Main Config A	VSCOPE_MAIN_CFG_A	Page 33
0x1B001	VScope Main Config B	VSCOPE_MAIN_CFG_B	Page 33
0x1B002	VScope Main Config C	VSCOPE_MAIN_CFG_C	Page 34
0x1B003	VScope Pattern Lock Config A	VSCOPE_PAT_LOCK_CFG_A	Page 34
0x1B004	VScope Pattern Lock Config B	VSCOPE_PAT_LOCK_CFG_B	Page 35
0x1B005	VScope HW Scan Config 1A	VSCOPE_HW_SCAN_CFG_1A	Page 35
0x1B006	VScope HW Scan Config 1B	VSCOPE_HW_SCAN_CFG_1B	Page 35
0x1B007	VScope HW Config 2A	VSCOPE_HW_SCAN_CFG_2A	Page 36
0x1B008	VScope HW Config 2B	VSCOPE_HW_SCAN_CFG_2B	Page 36

Table 21 • **SD10G65_VScope2 *(continued)***

Address	Short Description	Register Name	Details
0x1B009	VScope Status	VSCOPE_STAT	Page 36
0x1B00A	VScope Counter A	VSCOPE_CNT_A	Page 37
0x1B00B	VScope Counter B	VSCOPE_CNT_B	Page 37
0x1B00C	VScope General Purpose A	VSCOPE_DBG_LSB_A	Page 37
0x1B00D	VScope General Purpose B	VSCOPE_DBG_LSB_B	Page 37

Table 22 • **SD10G65_DFT**

Address	Short Description	Register Name	Details
0x1B100	SD10G65 DFT Main Configuration 1	DFT_RX_CFG_1	Page 38
0x1B101	SD10G65 DFT Main Configuration 2	DFT_RX_CFG_2	Page 39
0x1B102	SD10G65 DFT Pattern Mask Configuration 1	DFT_RX_MASK_CFG_1	Page 40
0x1B103	SD10G65 DFT Pattern Mask Configuration 2	DFT_RX_MASK_CFG_2	Page 40
0x1B104	SD10G65 DFT Pattern Checker Configuration 1	DFT_RX_PAT_CFG_1	Page 40
0x1B105	SD10G65 DFT Pattern Checker Configuration 2	DFT_RX_PAT_CFG_2	Page 40
0x1B106	SD10G65 DFT BIST Configuration A	DFT_BIST_CFG0A	Page 40
0x1B107	SD10G65 DFT BIST Configuration B	DFT_BIST_CFG0B	Page 41
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0x1B10A	SD10G65 DFT BIST Configuration A	DFT_BIST_CFG2A	Page 41
0x1B10B	SD10G65 DFT BIST Configuration B	DFT_BIST_CFG2B	Page 42
0x1B10C	SD10G65 DFT BIST Configuration A	DFT_BIST_CFG3A	Page 42
0x1B10D	SD10G65 DFT BIST Configuration B	DFT_BIST_CFG3B	Page 42
0x1B10E	SD10G65 DFT Error Status 1	DFT_ERR_STAT_1	Page 42
0x1B10F	SD10G65 DFT Error Status 2	DFT_ERR_STAT_2	Page 43
0x1B110	SD10G65 DFT PRBS Status 1	DFT_PRBS_STAT_1	Page 43
0x1B111	SD10G65 DFT PRBS Status 2	DFT_PRBS_STAT_2	Page 43
0x1B112	SD10G65 DFT Miscellaneous Status 1	DFT_MAIN_STAT_1	Page 43
0x1B113	SD10G65 DFT Miscellaneous Status 2	DFT_MAIN_STAT_2	Page 43
0x1B114	SD10G65 DFT Main Configuration	DFT_TX_CFG	Page 44
0x1B115	SD10G65 DFT Tx Constant Pattern Configuration1	DFT_TX_PAT_CFG_1	Page 45
0x1B116	SD10G65 DFT Tx Constant Pattern Configuration2	DFT_TX_PAT_CFG_2	Page 45
0x1B117	SD10G65 DFT Tx Constant Pattern Status	DFT_TX_CMP_DAT_STAT	Page 45
0x1B118	DFT Clock Compare Config	DFT_CLK_CMP_CFG	Page 46
0x1B119	DFT Clock Compare Timer A	DFT_CLK_CMP_TIMERA	Page 46
0x1B11A	DFT Clock Compare Timer B	DFT_CLK_CMP_TIMERB	Page 47
0x1B11B	DFT Clock Comparison Value A	DFT_CLK_CMP_VALUEA	Page 47
0x1B11C	DFT Clock Comparison Value B	DFT_CLK_CMP_VALUEB	Page 47

Table 22 • **SD10G65_DFT *(continued)***

Address	Short Description	Register Name	Details
0x1B11D	DFT Clock Comparison Maximum Value A	DFT_CLK_CMP_MAXVALA	Page 47
0x1B11E	DFT Clock Comparison Maximum Value B	DFT_CLK_CMP_MAXVALB	Page 48
0x1B11F	DFT Tx Error Insertion Configuration 1	DFT_TX_ERR_INSERT_CFG_1	Page 48
0x1B120	DFT Tx Error Insertion Configuration 2	DFT_TX_ERR_INSERT_CFG_2	Page 48
0x1B121	DFT Clock Generator Configuration 1	DFT_CLK_GEN_CFG_1	Page 49
0x1B122	DFT Clock Generator Configuration 2	DFT_CLK_GEN_CFG_2	Page 49
0x1B123	DFT Clock Generator Configuration 3	DFT_CLK_GEN_CFG_3	Page 49

Table 23 • **ROMENG_1**

Address	Short Description	Register Name	Details
0x1B200 - 0x1B286	SPI address field of ROM table entry (x135)	spi_adr	Page 50
0x1B300 - 0x1B386	Lower 16 bits of SPI Data Field of ROM Table Entry (x135)	data_lsw	Page 50
0x1B400 - 0x1B486	Upper 16 bits of SPI Data Field of ROM Table Entry (x135)	data_msw	Page 50

Table 24 • **ROMENG_2**

Address	Short Description	Register Name	Details
0x1B600	ROM Table Start/End Addresses of Tx 10G Setting Routine	adr_tx10g	Page 50
0x1B601	ROM Table Start/End Addresses of Rx 10G Setting Routine	adr_rx10g	Page 51
0x1B602	ROM Table Start/End Addresses of Tx 1G Setting Routine	adr_tx1g	Page 51
0x1B603	ROM Table Start/End Addresses of Rx 1G Setting Routine	adr_rx1g	Page 51
0x1B604	ROM Table Start/End Addresses of WAN Setting Routine	adr_wan	Page 51

Table 25 • **ROMENG_STATUS**

Address	Short Description	Register Name	Details
0x1B6FF	ROM Engine Status	ROMENG_STATUS	Page 52

2.1.1 PMA IEEE Configuration and Status

Configuration and status register set for Device 1 IEEE MDIO

2.1.1.1 PMA Control Register 1

Short Name:PMA_CONTROL_1

Address:0x10000

PMA Control Register 1

Table 26 • **PMA Control Register 1**

Bit	Name	Access	Description	Default
15	RST	One-shot	MDIO Manageable Device (MMD) software reset. This register resets functions associated exclusively with the line side PMA. Data path logic and configuration registers are reset. This register is self-clearing. 0: Normal operation 1: Reset	0x0
13	SPEED_SEL_A	R/O	Indicates whether the device operates at 10 Gbps and above. 0: Unspecified 1: Operation at 10 Gbps and above	0x1
11	LOW_PWR_PMA	R/W	The channel's data path is placed into low power mode with this register. The PMA in this channel is also placed into low power mode regardless of the channel cross connect configuration. The PMD_TRANSMIT_DISABLE.GLOBAL_PMD_TRANSMIT_DISABLE register state can can be transmitted from a GPIO pin to shut off an optics module's Tx driver. 1: Low Power Mode. 0: Normal Operation.	0x0
6	SPEED_SEL_B	R/O	Indicates whether the device operates at 10 Gbps and above. 0: Unspecified 1: 10 Gbps an above	0x1
5:2	SPEED_SEL_C	R/O	Device speed selection 1xxx: Reserved x1xx: Reserved xx1x: Reserved 0001: Reserved 0000: 10 Gbps	0x0
0	EN_PAD_LOOP	R/W	Enable PMA Pad Loopback H5 0: Disable 1: Enable	0x0

2.1.1.2 PMA Status Register 1

Short Name:PMA_STATUS_1

Address:0x10001

PMA Status Register 1

Table 27 • **PMA Status Register 1**

Bit	Name	Access	Description	Default
7	FAULT	R/O	Indicates a fault condition for this interface in either the transmit or the receive paths. 0: Fault condition not detected. Latch-high alarm status bits TRANSMIT_FAULT=0 AND RECEIVE_FAULT=0. 1: Fault condition detected. Latch-high alarm status bits TRANSMIT_FAULT=1 OR RECEIVE_FAULT=1.	0x0
2	RECEIVE_LINK_STATUS	R/O	Indicates the receive link status for this interface This is a sticky bit that latches the low state. The latch-low bit is cleared when the register is read. 0: PMA/PMD receive link down 1: PMA/PMD receive link up	0x1
1	LOW_POWER_ABILITY	R/O	Indicates PMA/PMD supports Low Power Mode 0: PMA/PMD does not support low power mode 1: PMA/PMD supports low power mode	0x1

2.1.1.3 PMA Device Identifier 1

Short Name:PMA_DEVICE_ID_1

Address:0x10002

PMA Device Identifier 1

Table 28 • **PMA Device Identifier 1**

Bit	Name	Access	Description	Default
15:0	PMA_DEVICE_ID_1	R/O	Upper 16 bits of a 32-bit unique PMA device identifier. Bits 3-18 of the device manufacturer's OUI.	0x0007

2.1.1.4 PMA Device Identifier 2

Short Name:PMA_DEVICE_ID_2

Address:0x10003

PMA Device Identifier 2

Table 29 • **PMA Device Identifier 2**

Bit	Name	Access	Description	Default
15:0	PMA_DEVICE_ID_2	R/O	Lower 16 bits of a 32-bit unique PMA device identifier. Bits 19-24 of the device manufacturer's OUI. Six-bit model number, and a four-bit revision number.	0x0400

2.1.1.5 PMA/PMD Speed Ability

Short Name:PMA_PMD_SPEED_ABILITY

Address:0x10004

PMA/PMD Speed Ability

Table 30 • **PMA/PMD Speed Ability**

Bit	Name	Access	Description	Default
0	ETH_10G_CAPABLE	R/O	Indicates PMA/PMD capability to run at 10 Gbps 0: PMA/PMD is not capable of operating at 10 Gbps 1: PMA/PMD is capable of operating at 10 Gbps	0x1

2.1.1.6 PMA/PMD Devices In Package 1

Short Name:PMA_PMD_DEV_IN_PACKAGE_1

Address:0x10005

PMA/PMD Devices In Package 1

Table 31 • **PMA/PMD Devices In Package 1**

Bit	Name	Access	Description	Default
5	DTE_XS_PRESENT	R/O	Indicates if the DTE XS is present 0: DTE XS is not present in package 1: DTE XS is present in package	0x0
4	PHY_XS_PRESENT	R/O	Indicates if the PHY XS is present 0: PHY XS is not present in package 1: PHY iXS is present in package	0x1
3	PCS_PRESENT	R/O	Indicates if the PCS is present 0: PCS is not present in package 1: PCS is present in package	0x1
2	WIS_PRESENT	R/O	Indicates if the WIS is present 0: WIS is not present in package 1: WIS is present in package	0x1
1	PMD_PMA_PRESENT	R/O	Indicates if the PMA/PMD is present 0: PMD/PMA is not present in package 1: PMD/PMA is present in package	0x1
0	CLAUSE_22_REG_PRESENT	R/O	Indicates if the clause 22 registers are present 0: Clause 22 registers are not present in package 1: Clause 22 registers are present in package	0x0

2.1.1.7 PMA/PMD Devices In Package 2

Short Name:PMA_PMD_DEV_IN_PACKAGE_2

Address:0x10006

PMA/PMD Devices In Package 2

Table 32 • **PMA/PMD Devices In Package 2**

Bit	Name	Access	Description	Default
15	VENDOR_SPECIFIC_DEV2_PRESENT	R/O	Indicates if the vendor specific device 2 is present 0: Vendor specific device 2 is not present in package 1: Vendor specific device 2 is present in package	0x0

Table 32 • **PMA/PMD Devices In Package 2 *(continued)***

Bit	Name	Access	Description	Default
14	VENDOR_SPECIFIC_DEV 1_PRESENT	R/O	Indicates if the vendor specific device 1 is present 0: Vendor specific device 1 is not present in package 1: Vendor specific device 1 is present in package	0x0

2.1.1.8 PMA/PMD Control 2

Short Name:PMA_PMD_CONTROL_2

Address:0x10007

PMA/PMD Control 2

Table 33 • **PMA/PMD Control 2**

Bit	Name	Access	Description	Default
3:0	VENDOR_SPECIFIC_DEV 2_PRESENT_CTRL	R/W	Indicates the PMA type selected WAN mode is enabled when 10GBASE-SW, 10GBASE-LW or 10GBASE-EW is selected. 1111: 10BASE-T (not supported) 1110: 100BASE-Tx (not supported) 1101: 1000BASE-KX 1100: 1000BASE-T (not supported) 1011: 10GBASE-KR 1010: 10GBASE-KX4 (not supported) 1001: 10GBASE-T (not supported) 1000: 10GBASE-LRM 0111: 10GBASE-SR 0110: 10GBASE-LR 0101: 10GBASE-ER 0100: 10GBASE-LX-4 0011: 10GBASE-SW 0010: 10GBASE-LW 0001: 10GBASE-EW 0000: Reserved	0x7

2.1.1.9 PMA/PMD Status 2

Short Name:PMA_PMD_STATUS_2

Address:0x10008

PMA/PMD Status 2

Table 34 • **PMA/PMD Status 2**

Bit	Name	Access	Description	Default
15:14	DEVICE_PRESENT	R/O	Indicates if the PMA device is present 00: Device not Present 01: Reserved 10: Device Present 11: Reserved	0x2

Table 34 • **PMA/PMD Status 2 *(continued)***

Bit	Name	Access	Description	Default
13	TRANSMIT_FAULT_ABILITY	R/O	PMA/PMD transmit path fault detection ability 0: PMA/PMD does not have the ability to detect a fault condition on the transmit path 1: PMA/PMD has the ability to detect a fault condition on the transmit path	0x1
12	RECEIVE_FAULT_ABILITY	R/O	PMA/PMD receive path fault detection ability 0: PMA/PMD does not have the ability to detect a fault condition on the receive path 1: PMA/PMD has the ability to detect a fault condition on the receive path	0x1
11	TRANSMIT_FAULT	R/O	Indicates a fault condition on this interface's transmit path. This is a sticky bit that latches the high state. The latch-high bit is cleared when the register is read. 0: No fault condition on transmit path 1: Fault condition on transmit path	0x0
10	RECEIVE_FAULT	R/O	Indicates a fault condition on this interface's receive path. This is a sticky bit that latches the high state. The latch-high bit is cleared when the register is read. 0: No fault condition on receive path 1: Fault condition on receive path	0x0
8	PMD_TRANSMIT_DISABLE_ABILITY	R/O	Disable the PMA/PMD transmit path ability 0: PMD does not have the ability to disable the transmit path 1: PMD has the ability to disable the transmit path	0x1
7	ETH_10GBASE_SR_ABILITY	R/O	10GBASE-SR ability 0: PMA/PMD is not able to perform 10GBASE-SR 1: PMA/PMD is able to perform 10GBASE-SR	0x1
6	ETH_10GBASE_LR_ABILITY	R/O	10GBASE-LR ability 0: PMA/PMD is not able to perform 10GBASE-LR 1: PMA/PMD is able to perform 10GBASE-LR	0x1
5	ETH_10GBASE_ER_ABILITY	R/O	10GBASE-ER ability 0: PMA/PMD is not able to perform 10GBASE-ER 1: PMA/PMD is able to perform 10GBASE-ER	0x1
4	ETH_10GBASE_LX4_ABILITY	R/O	10GBASE-LX4 ability 0: PMA/PMD is not able to perform 10GBASE-LX4 1: PMA/PMD is able to perform 10GBASE-LX4	0x0
3	ETH_10GBASE_SW_ABILITY	R/O	10GBASE-SW ability 0: PMA/PMD is not able to perform 10GBASE-SW 1: PMA/PMD is able to perform 10GBASE-SW	0x1

Table 34 • **PMA/PMD Status 2 *(continued)***

Bit	Name	Access	Description	Default
2	ETH_10GBASE_LW_ABILITY	R/O	10GBASE-LW ability 0: PMA/PMD is not able to perform 10GBASE-LW 1: PMA/PMD is able to perform 10GBASE-LW	0x1
1	ETH_10GBASE_EW_ABILITY	R/O	10GBASE-EW ability 0: PMA/PMD is not able to perform 10GBASE-EW 1: PMA/PMD is able to perform 10GBASE-EW	0x1
0	PMA_LOOPBACK_ABILITY	R/O	Ability to perform a loopback function 0: PMA does not have the ability to perform a loopback function 1: PMA has the ability to perform a loopback function	0x1

2.1.1.10 PMD Transmit Disable

Short Name:PMD_TRANSMIT_DISABLE

Address:0x10009

PMD Transmit Disable

Table 35 • **PMD Transmit Disable**

Bit	Name	Access	Description	Default
4	PMD_TRANSMIT_DISABLE_3	R/O	Value always 0, writes ignored. 0: Normal operation 1: Transmit disable	0x0
3	PMD_TRANSMIT_DISABLE_2	R/O	Value always 0, writes ignored 0: Normal operation 1: Transmit disable	0x0
2	PMD_TRANSMIT_DISABLE_1	R/O	Value always 0, writes ignored. 0: Normal operation 1: Transmit disable	0x0
1	PMD_TRANSMIT_DISABLE_0	R/O	Value always 0, writes ignored. 0: Normal operation 1: Transmit disable	0x0
0	GLOBAL_PMD_TRANSMIT_DISABLE	R/W	PMD Transmit Disable. This register bit can be transmitted from a GPIO pin to shut off an optics module's Tx driver. This TXEN signal automatically disables the Tx driver when the channel is in low power mode. The GPIO configuration controls whether the transmitted signal is active high or active low. 0: Transmit enabled 1: Transmit disabled	0x0

2.1.1.11 PMD Receive Signal Detect

Short Name:PMD_RECEIVE_SIGNAL_DETECT

Address:0x1000A

PMD Receive Signal Detect

Table 36 • **PMD Receive Signal Detect**

Bit	Name	Access	Description	Default
4	PMD_RECEIVE_SIGNAL_DETECT_3	R/O	Do not support this function, value always 0	0x0
3	PMD_RECEIVE_SIGNAL_DETECT_2	R/O	Do not support this function, value always 0	0x0
2	PMD_RECEIVE_SIGNAL_DETECT_1	R/O	Do not support this function, value always 0	0x0
1	PMD_RECEIVE_SIGNAL_DETECT_0	R/O	Do not support this function, value always 0	0x0
0	GLOBAL_PMD_RECEIVE_SIGNAL_DETECT	R/O	PMD receiver signal detect 0: Signal not detected by receiver 1: Signal detected by receiver	0x0

2.1.1.12 PMA/PMD Package Identifier 1

Short Name:PMA_PMD_PACKAGE_ID_1

Address:0x1001E

PMA/PMD Package Identifier 1

Table 37 • **PMA/PMD Package Identifier 1**

Bit	Name	Access	Description	Default
15:0	PMA_PMD_PACKAGE_ID_1	R/O	PMA/PMD package identifier 1	0x0000

2.1.1.13 PMA/PMD Package Identifier 2

Short Name:PMA_PMD_PACKAGE_ID_2

Address:0x1001F

PMA/PMD package identifier 2

Table 38 • **PMA/PMD Package Identifier 2**

Bit	Name	Access	Description	Default
15:0	PMA_PMD_PACKAGE_ID_2	R/O	PMA/PMD Package Identifier 2	0x0000

2.1.2 KR FEC IEEE Configuration and Status

2.1.2.1 KR FEC Ability

Short Name:KR_FEC_ABILITY

Address:0x100AA

Table 39 • **KR FEC Ability**

Bit	Name	Access	Description	Default
1	FEC_error_indication_ability	R/O	FEC error reporting ability 0: This PHY device is not able to report FEC decoding errors to the PCS layer. 1: This PHY device is able to report FEC decoding errors to the PCS layer.	0x1
0	FEC_ability	R/O	FEC ability 0: This PHY device does not support FEC. 1: This PHY device supports FEC.	0x1

2.1.2.2 KR FEC Control 1

Short Name:KR_FEC_CONTROL_1

Address:0x100AB

Table 40 • **KR FEC Control 1**

Bit	Name	Access	Description	Default
1	FEC_enable_error_indication	R/W	0: Decoding errors have no effect on PCS sync bits 1: Enable decoder to indicate errors to PCS sync bits	0x0
0	FEC_enable	R/W	FEC enable 0: Disable FEC 1: Enable FEC	0x0

2.1.2.3 KR FEC Corrected Lower

Short Name:KR_FEC_CORRECTED_LOWER

Address:0x100AC

Table 41 • **KR FEC Corrected Lower**

Bit	Name	Access	Description	Default
15:0	FEC_CORRECTED_BLOCKS_LOWER	R/O	The FEC corrected block count is split across two registers, KR_FEC_corrected_lower and KR_FEC_corrected_upper. KR_FEC_corrected_lower contains the least significant 16 bits of the count. KR_FEC_corrected_upper contains the most significant 16 bits of the count. Reading address KR_FEC_corrected_lower latches the 16 most significant bits of the counter in KR_FEC_corrected_upper for future read out. The block count register is cleared when KR_FEC_corrected_lower is read.	0x0000

2.1.2.4 KR FEC Corrected Upper

Short Name:KR_FEC_CORRECTED_UPPER

Address:0x100AD

Table 42 • **KR FEC Corrected Upper**

Bit	Name	Access	Description	Default
15:0	FEC_CORRECTED_BLOCKS_UPPER	R/O	The FEC corrected block count is split across two registers, KR_FEC_corrected_lower and KR_FEC_corrected_upper. KR_FEC_corrected_lower contains the least significant 16 bits of the count. KR_FEC_corrected_upper contains the most significant 16 bits of the count. Reading address KR_FEC_corrected_lower latches the 16 most significant bits of the counter in KR_FEC_corrected_upper for future read out. The block count register is cleared when KR_FEC_corrected_lower is read.	0x0000

2.1.2.5 KR FEC Uncorrected Lower

Short Name:KR_FEC_UNCORRECTED_LOWER

Address:0x100AE

Table 43 • **KR FEC Uncorrected Lower**

Bit	Name	Access	Description	Default
15:0	FEC_UNCORRECTED_BLOCKS_LOWER	R/O	The FEC uncorrectable block count is split across two registers, KR_FEC_uncorrected_lower and KR_FEC_uncorrected_upper. KR_FEC_uncorrected_lower contains the least significant 16 bits of the count. KR_FEC_uncorrected_upper contains the most significant 16 bits of the count. Reading address KR_FEC_uncorrected_lower latches the 16 most significant bits of the counter in KR_FEC_uncorrected_upper for future read out. The block count register is cleared when KR_FEC_uncorrected_lower is read.	0x0000

2.1.2.6 KR FEC Uncorrected Upper

Short Name:KR_FEC_UNCORRECTED_UPPER

Address:0x100AF

Table 44 • **KR FEC Uncorrected Upper**

Bit	Name	Access	Description	Default
15:0	FEC_UNCORRECTED_BLOCKS_UPPER	R/O	The FEC uncorrectable block count is split across two registers, KR_FEC_uncorrected_lower and KR_FEC_uncorrected_upper. KR_FEC_uncorrected_lower contains the least significant 16 bits of the count. KR_FEC_uncorrected_upper contains the most significant 16 bits of the count. Reading address KR_FEC_uncorrected_lower latches the 16 most significant bits of the counter in KR_FEC_uncorrected_upper for future read out. The block count register is cleared when KR_FEC_uncorrected_lower is read.	0x0000

2.1.3 KR FEC Vendor Specific Configuration and Status

Vendor specific configuration and status register set for KR FEC Block

2.1.3.1 KR FEC Control 2

Short Name:KR_FEC_Control_2

Address:0x18300

Table 45 • **KR FEC Control 2**

Bit	Name	Access	Description	Default
1	fec_inframe	R/O	FEC in frame lock indication. This is a sticky bit that latches the low state. The latch-low bit is cleared when the register is read. 0: FEC has not achieved lock 1: FEC has achieved lock	0x1
0	fec_rstmon	R/W	FEC counters reset 0: no effect 1: reset FEC counters	0x0

2.1.4 Alarms

2.1.4.1 Rx Alarm Control

Short Name:RX_ALARM_Control_Register

Address:0x19000

Table 46 • **Rx Alarm Control**

Bit	Name	Access	Description	Default
10	Vendor_Specific	R/W	Vendor specific 0: Disable 1: Enable	0x0
9	WIS_Local_Fault_Enable	R/W	WIS Local Fault Enable 0: Disable 1: Enable	0x0

Table 46 • **Rx Alarm Control *(continued)***

Bit	Name	Access	Description	Default
8:5	Vendor_Specific_idx2	R/W	Vendor Specific 0: Disable 1: Enable	0x0
4	PMA_PMD_Receiver_Local_Fault_Enable	R/W	PMA/PMD Receiver Local Fault Enable 0: Disable 1: Enable	0x1
3	PCS_Receive_Local_Fault_Enable	R/W	PCS Receive Local Fault Enable 0: Disable 1: Enable	0x1
2:1	Vendor_Specific_idx3	R/W	Vendor Specific 0: Disable 1: Enable	0x0
0	PHY_XS_Receive_Local_Fault_Enable	R/W	PHY XS Receive Local Fault Enable 0: Disable 1: Enable	0x0

2.1.4.2 Tx Alarm Control

Short Name:TX_ALARM_Control_Register

Address:0x19001

Table 47 • **Tx Alarm Control**

Bit	Name	Access	Description	Default
10:5	Vendor_Specific	R/W	Vendor Specific 0: Disable 1: Enable	0x00
4	PMA_PMD_Transmitter_Local_Fault_Enable	R/W	PMA/PMD Transmitter Local Fault Enable 0: Disable 1: Enable	0x1
3	PCS_Transmit_Local_Fault_Enable	R/W	PCS Transmit Local Fault Enable 0: Disable 1: Enable	0x1
2:1	Vendor_Specific_idx2	R/W	Vendor Specific 0: Disable 1: Enable	0x0
0	PHY_XS_Transmit_Local_Fault_Enable	R/W	PHY XS Transmit Local Fault Enable 0: Disable 1: Enable	0x1

2.1.4.3 Rx Alarm Status

Short Name:RX_ALARM_Status_Register

Address:0x19003

Table 48 • **Rx Alarm Status**

Bit	Name	Access	Description	Default
10	Vendor_Specific	R/O	For future use.	0x0

Table 48 • **Rx Alarm Status *(continued)***

Bit	Name	Access	Description	Default
9	WIS_Local_Fault	R/O	WIS Local Fault This is a sticky bit that latches the high state. The latch-high bit is cleared when the register is read. 0: No WIS Local Fault 1: WIS Local Fault	0x0
8:5	Vendor_Specific_idx2	R/O	For future use.	0x0
4	PMA_PMD_Receiver_Local_Fault	R/O	PMA/PMD Receiver Local Fault This is a sticky bit that latches the high state. The latch-high bit is cleared when the register is read. 0: No PMA/PMD Receiver Local Fault 1: PMA/PMD Receiver Local Fault	0x0
3	PCS_Receive_Local_Fault	R/O	PCS Receive Local Fault This is a sticky bit that latches the high state. The latch-high bit is cleared when the register is read. 0: No PCS Receive Local Fault 1: PCS Receive Local Fault	0x0
2:1	Vendor_Specific_idx3	R/O	For future use.	0x0
0	PHY_XS_Receive_Local_Fault	R/O	PHY XS Receive Local Fault This is a sticky bit that latches the high state. The latch-high bit is cleared when the register is read. 0: No PHY XS Receive Local Fault 1: PHY XS Receive Local Fault	0x0

2.1.4.4 Tx Alarm Status

Short Name:TX_ALARM_Status_Register

Address:0x19004

Table 49 • **Tx Alarm Status**

Bit	Name	Access	Description	Default
10:5	Vendor_Specific	R/O	For future use.	0x00
4	PMA_PMD_Transmitter_Local_Fault	R/O	PMA/PMD Transmitter Local Fault Enable This is a sticky bit that latches the high state. The latch-high bit is cleared when the register is read. 0: No PMA/PMD Transmitter Local Fault 1: PMA/PMD Transmitter Local Fault	0x0
3	PCS_Transmit_Local_Fault	R/O	PCS Transmit Local Fault Enable This is a sticky bit that latches the high state. The latch-high bit is cleared when the register is read. 0: No PCS Transmit Local Fault 1: PCS Transmit Local Fault	0x0
2:1	Vendor_Specific_idx2	R/O	For future use.	0x0

Table 49 • **Tx Alarm Status *(continued)***

Bit	Name	Access	Description	Default
0	PHY_XS_Transmit_Local_Fault	R/O	PHY XS Transmit Local Fault Enable This is a sticky bit that latches the high state. The latch-high bit is cleared when the register is read. 0: No PHY XS Transmit Local Fault 1: PHY XS Transmit Local Fault	0x0

2.1.5 Data Path Controls

2.1.5.1 10G or 1G Mode in Datapath

Short Name:DATAPATH_MODE

Address:0x1A002

Determine the datapath mode

Table 50 • **10G or 1G mode in Datapath**

Bit	Name	Access	Description	Default
6	USR_10G_WAN	One-shot	Configure line side serdes for 10G WAN operation (9.95328 Gbps) and host side serdes for 10G LAN operation (10.3125 Gbps). This register is self-clearing. 0 = No action 1 = Initiate configuration process	0x0
5	USR_10G_LAN	One-shot	Configure line side and host side serdes for 10G LAN operation (10.3125 Gbps). This register is self-clearing. 0 = No action 1 = Initiate configuration process	0x0
4	USR_1G	One-shot	Configure line side and host side serdes for 1G LAN operation (1.250 Gbps). This register is self-clearing. 0 = No action 1 = Initiate configuration process	0x0
0	ETH_1G_ENA	R/W	Select the 10G/1G data path for the channel. In addition to this register, the serdes on the host and line side interfaces must be configured to transfer data at the desired data rate. 0 = 10G LAN or WAN 1 = 1G	0x0

2.1.5.2 Datapath Loopback Control

Short Name:PMA_LOOPBACK_CONTROL

Address:0x1A003

Datapath Loopback Control

Table 51 • **Datapath Loopback Control**

Bit	Name	Access	Description	Default
0	L3_CONTROL	R/W	Loopback L3 Enable 0 = Normal Operation 1 = Enable L3 Loopback	0x0

2.1.6 MAC Data Path Enable

2.1.6.1 Enable MAC in the Data Path

Short Name:MAC_ENA

Address:0x1A006

Enable MAC in the data path

Table 52 • **Enable MAC in the Data Path**

Bit	Name	Access	Description	Default
5	HOST_MAC_MON_ENA	R/W	Enable clock for line MAC when the non-packet data path is in use. This allows the MAC to monitor in-coming packets. The MAC's clock enable configuration register still needs to be asserted. 0 = HOST MAC monitor option disabled 1 = HOST MAC monitor option enabled	0x0
4	LINE_MAC_MON_ENA	R/W	Enable clock for line MAC when the non-packet data path is in use. This allows the MAC to monitor in-coming packets. The MAC's clock enable configuration register still needs to be asserted. 0 = LINE MAC monitor option disabled 1 = LINE MAC monitor option enabled	0x0
1	MACSEC_CLK_ENA	R/W	Clock enable for the MACsec logic. Deasserting this bit when MACsec is disabled and MACs are enabled will save power. Note: the CLK_EN register bits within the MACsec register space must be asserted along with this bit when the MACsec logic is to be used. This bit usage applies to the VSC8258 product. 0 = MACsec clock is squelched 1 = MACsec clock is enabled	0x0
0	MAC_ENA	R/W	Enable MAC in the datapath 0 = MAC is not in the datapath 1 = MAC is in the datapath	0x0

2.1.7 Repeater Mode Configuration

2.1.7.1 Repeater Mode Configuration

Short Name:BYPASS_CFG1

Address:0x1A020

Table 53 • **Repeater Mode Configuration**

Bit	Name	Access	Description	Default
8	FIFO_RESET	One-shot	Reset the bypass FIFO 0 = Normal operation 1 = RESET	0x0
7:4	RESERVED	R/W	Must be set to its default.	0x4
2	RESERVED	R/W	Must be set to its default.	0x1
1	REPEATER_FIFO_EN	R/W	Enable bypass FIFO 0 = FIFO Disabled 1 = FIFO Enabled	0x0
0	REPEATER_MODE_EN	R/W	Enable repeater mode. This causes the transmit multiplexor to select bypass data rather than data from the processing core 0 = Standard mode 1 = Repeater Mode	0x0

2.1.7.2 Bypass Status

Short Name:BYPASS_STATUS

Address:0x1A021

Table 54 •

Bit	Name	Access	Description	Default
1	FIFO_UNDERFLOW_STAT	R/O	FIFO Underflow state	0x0
0	FIFO_OVERFLOW_STAT	R/O	FIFO Overflow state	0x0

2.1.7.3 Bypass Interrupt Enable

Short Name:BYPASS_INTR_EN

Address:0x1A022

Table 55 •

Bit	Name	Access	Description	Default
1	FIFO_UNDERFLOW_INTR_EN	R/W	Allow FIFO_UNDERFLOW_STICKY to propagate to interrupt	0x0
0	FIFO_OVERFLOW_INTR_EN	R/W	Enable FIFO_OVERFLOW_STICKY to propagate to interrupt	0x0

2.1.7.4 Bypass Interrupt

Short Name:BYPASS_INTR

Address:0x1A023

Table 56 •

Bit	Name	Access	Description	Default
1	FIFO_UNDERFLOW_STICKY	Sticky		0x0

Table 56 • (continued)

Bit	Name	Access	Description	Default
0	FIFO_OVERFLOW_STICKY	Sticky	FIFO overflow occured	0x0

2.1.8 Vendor Specific PMA Controls

2.1.8.1 Vendor Specific PMA Control 2

Short Name: Vendor_Specific_PMA_Control_2

Address:0x1A100

Table 57 • **Vendor Specific PMA Control 2**

Bit	Name	Access	Description	Default
10	Suppress_LOS_detection	R/W	LOS circuitry is driven by a signal detection status signal in the line-side input buffer. The signal detection alarm driving the LOS circuitry can be squelched with this register bit. LOS detection is 0: Allowed 1: Suppressed	0x0
9	Suppress_LOL_detection	R/W	LOL circuitry is driven by a status signal in the line-side CRU. The status signal driving the LOL curcuitry can be squelched with this register bit. LOL detection is 0: Allowed 1: Suppressed	0x0
8	TX_LED_BLINK_TIME	R/W	Tx data activity LED blink time 0: 50ms interval 1: 100ms interval	0x1
7	RX_LED_BLINK_TIME	R/W	Rx data activity LED blink time 0: 50ms interval 1: 100ms interval	0x1
6:5	TX_LED_MODE	R/W	Tx LED mode control 00: Display Tx link status 01: Reserved 10: Display combination of Tx link (host Rx Link) and Tx data activity status 11: Display combination of Tx link (host Rx Link) and Tx+Rx data activity status	0x2
4:3	RX_LED_MODE	R/W	Rx LED mode control 00: Display Rx link status 01: Reserved 10: Display combination of Rx link and Rx data activity status 11: Display combination of Rx link and Rx+Tx data activity status	0x2
2	Override_system_loopback_data	R/W	System loopback data override 0: Data sent out XFI output matches default. 1: Use 'PMA system loopback data select' to select XFI ouput data.	0x0

Table 57 • **Vendor Specific PMA Control 2 *(continued)***

Bit	Name	Access	Description	Default
1:0	PMA_system_loopback_data_select	R/W	When Override system loopback data (bit 2) is set and the data channel is in 10G mode, the data transmitted from Tx PMA is determined by these register bits. 00: repeating 0x00FF pattern 01: continuously send 0's 10: continuously send 1's 11: data from Tx WIS block	0x0

2.1.8.2 Vendor Specific PMA Status 2

Short Name: Vendor_Specific_PMA_Status_2

Address:0x1A101

Table 58 • **Vendor Specific PMA Status 2**

Bit	Name	Access	Description	Default
3	WAN_ENABLED_STATUS	R/O	Indicates if the device is in WAN mode WAN mode is enable when WIS_CTRL2.WAN_MODE = 1 OR PCS_Control_2.Select_WAN_mode_or_10GBASE_R = 2 OR PMA_PMD_CONTROL_2.VENDOR_SPECIFIC_DEV2_PRESENT_CTRL = 1 OR PMA_PMD_CONTROL_2.VENDOR_SPECIFIC_DEV2_PRESENT_CTRL = 2 OR PMA_PMD_CONTROL_2.VENDOR_SPECIFIC_DEV2_PRESENT_CTRL = 3 0: Not in Wan Mode 1: WAN Mode	0x0
2	CHAN_INTR1_STATUS	R/O	State of the channel's interrupt 1 signal 0: Channel interrupt 1 signal is low 1: Channel interrupt 1 signal is high	0x0
1	CHAN_INTR0_STATUS	R/O	State of the channel's interrupt 0 signal 0: Channel interrupt 0 signal is low 1: Channel interrupt 0 signal is high	0x0
0	PMTICK_PIN_STATUS	R/O	PMTICK pin status 0: PMTICK pin is low 1: PMTICK pin is high	0x0

2.1.9 PMA Status and Interrupts

2.1.9.1 PMA Status

Short Name:PMA_STAT

Address:0x1A202

Table 59 • **PMA Status**

Bit	Name	Access	Description	Default
2	TX_LOL_STAT	R/O	Current state of Tx LOL from SerDes 0 = Tx PLL Locked 1 = Tx PLL Not locked	0x0
1	RX_LOL_STAT	R/O	Current state of Rx LOL from SerDes 0 = Rx PLL Locked 1 = Rx PLL Not locked	0x0
0	RX_LOS_STAT	R/O	LOS detected at Serdes 0 = Signal detected at input receiver 1 = No signal detected at input receiver	0x0

2.1.9.2 PMA Interrupt Mask

Short Name:PMA_INTR_MASK

Address:0x1A203

Table 60 • **PMA Interrupt Mask**

Bit	Name	Access	Description	Default
2	TX_LOL_INTR_EN	R/W	Enable interrupt when Tx LOL detected 0 = Detected Tx LOL condition not propagated to interrupt 1 = Detected Tx LOL condition is propagated to interrupt	0x0
1	RX_LOL_INTR_EN	R/W	Enable interrupt when Rx LOL detected 0 = Detected Rx LOL condition not propagated to interrupt 1 = Detected Rx LOL condition is propagated to interrupt	0x0
0	RX_LOS_INTR_EN	R/W	Enable interrupt when Rx LOS detected 0 = Detected LOS condition not propagated to interrupt 1 = Detected LOS condition is propagated to interrupt	0x0

2.1.9.3 PMA Interrupt Status

Short Name:PMA_INTR_STAT

Address:0x1A204

Table 61 • **PMA Interrupt Status**

Bit	Name	Access	Description	Default
2	TX_LOL_STICKY	Sticky	Tx LOL Detected 0 = No Tx LOL detected since last cleared 1 = Tx LOL Detected since last cleared	0x0
1	RX_LOL_STICKY	Sticky	Rx LOL Detected 0 = No Rx LOL detected since last cleared 1 = Rx LOL Detected since last cleared	0x0

Table 61 • **PMA Interrupt Status *(continued)***

Bit	Name	Access	Description	Default
0	RX_LOS_STICKY	Sticky	Rx LOS Detected 0 = No Rx LOS detected since last cleared 1 = Rx LOS Detected since last cleared	0x0

2.1.10 Block Level Reset

Reset the data path of various blocks. Configuration registers in the blocks are not reset to default states.

2.1.10.1 Block Level Soft Reset1

Short Name:BLOCK_LEVEL_RESET1

Address:0x1AE00

Table 62 • **Block Level Soft Reset1**

Bit	Name	Access	Description	Default
15	I2CM_RESET	One-shot	Reset the I2C(master) used to communicate with an optics module. 0: Normal operation 1: Reset	0x0
14	IP1588_INGR_RESET	One-shot	Reset the chip's ingress data path in the 1588 processing block 0: Normal operation 1: Reset	0x0
13	IP1588_LTC1_RESET	One-shot	Reset all 1588 LTC clock domain logic for this channel. This register resets the same logic as register IP1588_LTC2_RESET. The reset function is duplicated here in case there is a need to reset the LTC clock domain and 1588 ingress data path registers simultaneously. 0: Normal operation 1: Reset	0x0
12	IP1588_TSP_LTC1_RESET	One-shot	Reset the 1588 LTC clock domain logic within the channel's ingress and egress TSP blocks. This register resets the same logic as register IP1588_TSP_LTC2_RESET. 0: Normal operation 1: Reset	0x0
10	HOST_PMA_INGR_RESET	One-shot	Reset the chip's ingress data path in the host side PMA and PMA_INT blocks 0: Normal operation 1: Reset	0x0
9	HOST_XPT_INGR_RESET	One-shot	Reset the port's ingress data path in the cross connect blocks 0: Normal operation 1: Reset	0x0

Table 62 • **Block Level Soft Reset1** ***(continued)***

Bit	Name	Access	Description	Default
8	HOST_10G_PCS_INGR_RESET	One-shot	Reset the chip's ingress data path in the host side 10G PCS block Note: When asserting this reset, if the cross connect is in use, then HOST_XPT_INGR_RESET should also be asserted 0: Normal operation 1: Reset	0x0
7	HOST_1G_PCS_INGR_RESET	One-shot	Reset the chip's ingress data path in the host side 1G PCS block Note: When asserting this reset, if the cross connect is in use, then HOST_XPT_INGR_RESET should also be asserted 0: Normal operation 1: Reset	0x0
6	FIFO_INGR_RESET	One-shot	Reset the rate compensating FIFO in the chip's ingress data path. The FIFO is used when the MACs are disabled. 0: Normal operation 1: Reset	0x0
5	HOST_MAC_INGR_RESET	One-shot	Reset the chip's ingress data path in the host MAC and flow control buffer 0: Normal operation 1: Reset	0x0
4	LINE_MAC_INGR_RESET	One-shot	Reset the chip's ingress data path in the line MAC, MACsec (if applicable to the product SKU) and flow control buffer blocks as well as configuration registers in the MACsec decryption processor 0: Normal operation 1: Reset	0x0
3	LINE_10G_PCS_INGR_RESET	One-shot	Reset the chip's ingress data path in the line side 10G PCS block 0: Normal operation 1: Reset	0x0
2	LINE_1G_PCS_INGR_RESET	One-shot	Reset the chip's ingress data path in the line side 1G PCS block 0: Normal operation 1: Reset	0x0
1	WIS_INGR_RESET	One-shot	Reset the chip's ingress data path in the WIS block 0: Normal operation 1: Reset	0x0
0	LINE_PMA_INGR_RESET	One-shot	Reset the chip's ingress data path in the line side PMA and PMA_INT blocks 0: Normal operation 1: Reset	0x0

2.1.10.2 Block Level Soft Reset2

Short Name:BLOCK_LEVEL_RESET2

Address:0x1AE01

Table 63 • **Block Level Soft Reset2**

Bit	Name	Access	Description	Default
14	IP1588_EGR_RESET	One-shot	Reset the chip's egress data path in the 1588 processing block 0: Normal operation 1: Reset	0x0
13	IP1588_LTC2_RESET	One-shot	Reset all 1588 LTC clock domain logic for this channel. This register resets the same logic as register IP1588_LTC1_RESET. The reset function is duplicated here in case there is a need to reset the LTC clock domain and 1588 egress data path registers simultaneously. 0: Normal operation 1: Reset	0x0
12	IP1588_TSP_LTC2_RESET	One-shot	Reset the 1588 LTC clock domain logic within the channel's ingress and egress TSP blocks. This register resets the same logic as register IP1588_TSP_LTC1_RESET. 0: Normal operation 1: Reset	0x0
11	FIFO_EGR_RESET2	One-shot	Reset the 10G host interface rate compensating FIFO in the chip's egress data path. The FIFO is used only when the part is in 10G LAN or WAN mode. Note: When asserting this reset, if the cross connect is in use, then HOST_XPT_EGR_RESET should also be asserted 0: Normal operation 1: Reset	0x0
10	HOST_PMA_EGR_RESET	One-shot	Reset the chip's egress data path in the host side PMA and PMA_INT blocks 0: Normal operation 1: Reset	0x0
9	HOST_XPT_EGR_RESET	One-shot	Reset the port's egress data path in the cross connect blocks 0: Normal operation 1: Reset	0x0
8	HOST_10G_PCS_EGR_RESET	One-shot	Reset the chip's egress data path in the host side 10G PCS block Note: When asserting this reset, if the cross connect is in use, then HOST_XPT_EGR_RESET and FIFO_EGR_RESET2 should also be asserted 0: Normal operation 1: Reset	0x0

Table 63 • **Block Level Soft Reset2 *(continued)***

Bit	Name	Access	Description	Default
7	HOST_1G_PCS_EGR_RESET	One-shot	Reset the chip's egress data path in the host side 1G PCS block Note: When asserting this reset, if the cross connect is in use, then HOST_XPT_EGR_RESET should also be asserted 0: Normal operation 1: Reset	0x0
6	FIFO_EGR_RESET	One-shot	Reset the WAN mode rate compensating FIFO in the chip's egress data path. The FIFO is used when the MACs are disabled. 0: Normal operation 1: Reset	0x0
5	HOST_MAC_EGR_RESET	One-shot	Reset the chip's egress data path in the host MAC and flow control buffer 0: Normal operation 1: Reset	0x0
4	LINE_MAC_EGR_RESET	One-shot	Reset the chip's egress data path in the line MAC, MACsec (if applicable to the product SKU) and flow control buffer blocks as well as configuration registers in the MACsec encryption processor 0: Normal operation 1: Reset	0x0
3	LINE_10G_PCS_EGR_RESET	One-shot	Reset the chip's egress data path in the line side 10G PCS block 0: Normal operation 1: Reset	0x0
2	LINE_1G_PCS_EGR_RESET	One-shot	Reset the chip's egress data path in the line side 1G PCS block 0: Normal operation 1: Reset	0x0
1	WIS_EGR_RESET	One-shot	Reset the chip's egress data path in the WIS block 0: Normal operation 1: Reset	0x0
0	LINE_PMA_EGR_RESET	One-shot	Reset the chip's egress data path in the line side PMA and PMA_INT blocks 0: Normal operation 1: Reset	0x0

2.1.11 Spare R/W Registers

Spare R/W registers intended to be used by firmware.

2.1.11.1 Device1 Spare R/W 0

Short Name:DEV1_SPARE_RW0

Address:0x1AEF0

Table 64 • **Device1 Spare R/W 0**

Bit	Name	Access	Description	Default
15:0	dev1_spare_rw0	R/W	Spare	0x0000

2.1.11.2 Device1 Spare R/W 1

Short Name:DEV1_SPARE_RW1

Address:0x1AEF1

Table 65 • **Device1 Spare R/W 1**

Bit	Name	Access	Description	Default
15:0	dev1_spare_rw1	R/W	Spare	0x0000

2.1.11.3 Device1 Spare R/W 2

Short Name:DEV1_SPARE_RW2

Address:0x1AEF2

Table 66 • **Device1 Spare R/W 2**

Bit	Name	Access	Description	Default
15:0	dev1_spare_rw2	R/W	Spare	0x0000

2.1.11.4 Device1 Spare R/W 3

Short Name:DEV1_SPARE_RW3

Address:0x1AEF3

Table 67 • **Device1 Spare R/W 3**

Bit	Name	Access	Description	Default
15:0	dev1_spare_rw3	R/W	Spare	0x0000

2.1.11.5 Device1 Spare R/W 4

Short Name:DEV1_SPARE_RW4

Address:0x1AEF4

Table 68 • **Device1 Spare R/W 4**

Bit	Name	Access	Description	Default
15:0	dev1_spare_rw4	R/W	Spare	0x0000

2.1.11.6 Device1 Spare R/W 5

Short Name:DEV1_SPARE_RW5

Address:0x1AEF5

Table 69 • **Device1 Spare R/W 5**

Bit	Name	Access	Description	Default
15:0	dev1_spare_rw5	R/W	Spare	0x0000

2.1.11.7 Device1 Spare R/W 6

Short Name:DEV1_SPARE_RW6

Address:0x1AEF6

Table 70 • **Device1 Spare R/W 6**

Bit	Name	Access	Description	Default
15:0	dev1_spare_rw6	R/W	Spare	0x0000

2.1.11.8 Device1 Spare R/W 7

Short Name:DEV1_SPARE_RW7

Address:0x1AEF7

Table 71 • **Device1 Spare R/W 7**

Bit	Name	Access	Description	Default
15:0	dev1_spare_rw7	R/W	Spare	0x0000

2.1.11.9 Device1 Spare R/W 8

Short Name:DEV1_SPARE_RW8

Address:0x1AEF8

Table 72 • **Device1 Spare R/W 8**

Bit	Name	Access	Description	Default
15:0	dev1_spare_rw8	R/W	Spare	0x0000

2.1.11.10 Device1 Spare R/W 9

Short Name:DEV1_SPARE_RW9

Address:0x1AEF9

Table 73 • **Device1 Spare R/W 9**

Bit	Name	Access	Description	Default
15:0	dev1_spare_rw9	R/W	Spare	0x0000

Device1 Spare R/W 10

Short Name:DEV1_SPARE_RW10

Address:0x1AEFA

Table 74 • **Device1 Spare R/W 10**

Bit	Name	Access	Description	Default
15:0	dev1_spare_rw10	R/W	Spare	0x0000

2.1.11.11 Device1 Spare R/W 11

Short Name:DEV1_SPARE_RW11

Address:0x1AEFB

Table 75 • **Device1 Spare R/W 11**

Bit	Name	Access	Description	Default
15:0	dev1_spare_rw11	R/W	Spare	0x0000

2.1.11.12 Device1 Spare R/W 12

Short Name:DEV1_SPARE_RW12

Address:0x1AEFC

Table 76 • **Device1 Spare R/W 12**

Bit	Name	Access	Description	Default
15:0	dev1_spare_rw12	R/W	Spare	0x0000

2.1.11.13 Device1 Spare R/W 13

Short Name:DEV1_SPARE_RW13

Address:0x1AEFD

Table 77 • **Device1 Spare R/W 13**

Bit	Name	Access	Description	Default
15:0	dev1_spare_rw13	R/W	Spare	0x0000

2.1.11.14 Device1 Spare R/W 14

Short Name:DEV1_SPARE_RW14

Address:0x1AEFE

Table 78 • **Device1 Spare R/W 14**

Bit	Name	Access	Description	Default
15:0	dev1_spare_rw14	R/W	Spare	0x0000

2.1.11.15 Device1 Spare R/W 15

Short Name:DEV1_SPARE_RW15

Address:0x1AEFF

Table 79 • **Device1 Spare R/W 15**

Bit	Name	Access	Description	Default
15:0	dev1_spare_rw15	R/W	Spare	0x0000

2.1.12 SD10G65 VScope Configuration and Status

Configuration and status register set for SD10G65 VScope

2.1.12.1 VScope Main Config A

Short Name:VSCOPE_MAIN_CFG_A

Address:0x1B000

VScope main configuration register A

Table 80 • **VScope Main Config A**

Bit	Name	Access	Description	Default
8	SYN_PHASE_WR_DIS	R/W	Disables writing of synth_phase_aux in synthesizer	0x0
7	IB_AUX_OFFS_WR_DIS	R/W	Disables writing of ib_auxl_offset and ib_auxh_offset in IB	0x0
6	IB_JUMP_ENA_WR_DIS	R/W	Disables writing of ib_jumpl_ena and ib_jumph_ena in IB	0x0
5:3	CNT_OUT_SEL	R/W	Counter output selection 0-3: error counter 0-3 4: hit counter 5: clock counter 6: 8 LSBs of error counter 3-1 and hit counter 7: 8 LSBs of error counter 3-0	0x0
2:0	COMP_SEL	R/W	Comparator input selection [REF] 0 1: auxL 4 5: auxH 2 7: main; [SUB] 5 7: auxL 0 2: auxH 1 4: main (3 6: reserved)	0x0

2.1.12.2 VScope Main Config B

Short Name:VSCOPE_MAIN_CFG_B

Address:0x1B001

VScope main configuration register B

Table 81 • **VScope Main Config B**

Bit	Name	Access	Description	Default
9:8	GP_SELECT	R/W	Select GP reg input 0: rx (main)	0x0
7	GP_REG_FREEZE	R/W	Allows to freeze the GP register value to assure valid reading	0x0
6:5	SCAN_LIM	R/W	Scan limit, selects which counter saturation limits the other counters 0: clock counter 1: hit counter 2: error counters 3: no limit	0x0
4:0	PRELOAD_VAL	R/W	Preload value for error counter	0x00

2.1.12.3 VScope Main Config C

Short Name:VSCOPE_MAIN_CFG_C

Address:0x1B002

VScope main configuration register C

Table 82 • **VScope Main Config C**

Bit	Name	Access	Description	Default
12	INTR_DIS	R/W	Disable interrupt output	0x0
11	TRIG_ENA	R/W	Enable trigger	0x0
10	QUICK_SCAN	R/W	Counter enable (bit 4) implicitly done by reading the counter; unused in hw-scan mode	0x0
9:5	COUNT_PER	R/W	Counter period: preload value for clock counter	0x00
4	CNT_ENA	R/W	Enable Counting; unused in hw-scan mode	0x0
3:1	IF_MODE	R/W	Interface Width 0: 8 bit 1: 10 bit 2: 16 bit 3: 20 bit 4: 32 bit 5: 40 bit others: reserved	0x0
0	VSCOPE_ENA	R/W	Enable VScope	0x0

2.1.12.4 VScope Pattern Lock Config A

Short Name:VSCOPE_PAT_LOCK_CFG_A

Address:0x1B003

VScope pattern lock configuration register A

Table 83 • **VScope Pattern Lock Config A**

Bit	Name	Access	Description	Default
14:10	PRELOAD_HIT_CNT	R/W	Preload value for hit counter	0x00

Table 83 • **VScope Pattern Lock Config A *(continued)***

Bit	Name	Access	Description	Default
9:0	DC_MASK	R/W	Don't Care mask: Enable history mask usage. 0: enable history mask bit 1: history mask bit is "don't care"	0x3FF

2.1.12.5 VScope Pattern Lock Config B

Short Name:VSCOPE_PAT_LOCK_CFG_B

Address:0x1B004

VScope pattern lock configuration register B

Table 84 • **VScope Pattern Lock Config B**

Bit	Name	Access	Description	Default
9:0	HIST_MASK	R/W	History mask: Respective sequence is expected in reference input (comp_sel); if enabled (dc_mask) before hit and error counting is enabled	0x000

2.1.12.6 VScope HW Scan Config 1A

Short Name:VSCOPE_HW_SCAN_CFG_1A

Address:0x1B005

VScope HW scan configuration register 1A

Table 85 • **VScope HW Scan Config 1A**

Bit	Name	Access	Description	Default
13	PHASE_JUMP_INV	R/W	Invert the jumph_ena and jumpl_ena bit in HW scan mode	0x0
12:8	AMPL_OFFS_VAL	R/W	Offset between AuxL amplitude (reference) and AuxH amplitude, signed (2s-complement), +- 1/4 amplitude max.	0x00
7:0	MAX_PHASE_INCR_VAL	R/W	Maximum phase increment value before wrapping	0xFF

2.1.12.7 VScope HW Scan Config 1B

Short Name:VSCOPE_HW_SCAN_CFG_1B

Address:0x1B006

VScope HW scan configuration register 1B

Table 86 • **VScope HW Scan Config 1B**

Bit	Name	Access	Description	Default
15:10	MAX_AMPL_INCR_VAL	R/W	Maximum amplitude increment value before wrapping	0x3F
9:7	PHASE_INCR	R/W	Phase increment per scan step Increment = phase_incr + 1	0x0
6:4	AMPL_INCR	R/W	Amplitude increment per scan step Increment = ampl_incr + 1	0x0

Table 86 • **VScope HW Scan Config 1B *(continued)***

Bit	Name	Access	Description	Default
3:2	NUM_SCANS_PER_ITR	R/W	Number of scans per iteration in N-point-scan mode 0: 1 1: 2 2: 4 3: 8	0x2
1:0	HW_SCAN_ENA	R/W	Enables HW scan with N results per scan or fast-scan 0: off 1: N-point scan 2: fast-scan (sq) 3: fast-scan (diag)	0x0

2.1.12.8 VScope HW Config 2A

Short Name:VSCOPE_HW_SCAN_CFG_2A

Address:0x1B007

VScope HW scan configuration register 2A

Table 87 • **VScope HW Config 2A**

Bit	Name	Access	Description	Default
15:13	FAST_SCAN_THRES	R/W	Threshold for error_counter in fast-scan mode N+1	0x0
12:8	FS_THRES_SHIFT	R/W	Left shift for threshold of error_counter in fast-scan mode threshold = (fast_scan_thres+1) shift_left fs_thres_shift	0x00
7:0	PHASE_JUMP_VAL	R/W	Value at which jumpl_ena and jumph_ena in IB must be toggled	0x00

2.1.12.9 VScope HW Config 2B

Short Name:VSCOPE_HW_SCAN_CFG_2B

Address:0x1B008

VScope HW scan configuration register 2B

Table 88 • **VScope HW Config 2B**

Bit	Name	Access	Description	Default
15	AUX_AMPL_SYM_DIS	R/W	Disable IB amplitude symmetry compensation for AuxH and AuxL	0x0
13:8	AMPL_START_VAL	R/W	Start value for VScope amplitude in N-point-scan mode and fast-scan mode (before IB amplitude symmetry compensation)	0x00
7:0	PHASE_START_VAL	R/W	Start value for VScope phase in N-point-scan mode and fast-scan mode	0x00

2.1.12.10 VScope Status

Short Name:VSCOPE_STAT

Address:0x1B009

VScope status register

Table 89 • **VScope Status**

Bit	Name	Access	Description	Default
15:8	GP_REG_MSB	R/O	8 MSBs of general purpose register	0x00
7:4	FAST_SCAN_HIT	R/O	Fast scan mode: Indicator per cursor position whether threshold was reached	0x0
0	DONE_STICKY	R/O	Done sticky	0x0

2.1.12.11 VScope Counter A

Short Name:VSCOPE_CNT_A

Address:0x1B00A

VScope counter register A

Table 90 • **VScope Counter A**

Bit	Name	Access	Description	Default
15:0	COUNTER_MSB	R/O	Counter value higher 16-bit MSB [31:16]	0x0000

2.1.12.12 VScope Counter B

Short Name:VSCOPE_CNT_B

Address:0x1B00B

VScope counter register B

Table 91 • **VScope Counter B**

Bit	Name	Access	Description	Default
15:0	COUNTER_LSB	R/O	Counter value lower 16-bit LSB [15:0]	0x0000

2.1.12.13 VScope General Purpose A

Short Name:VSCOPE_DBG_LSB_A

Address:0x1B00C

VScope general purpose register A

Table 92 • **VScope General Purpose A**

Bit	Name	Access	Description	Default
15:0	GP_REG_LSB_A	R/O	16 bit MSB of a 32 bit general purpose register [31:16]	0x0000

2.1.12.14 VScope General Purpose B

Short Name:VSCOPE_DBG_LSB_B

Address:0x1B00D

VScope general purpose register B

Table 93 • **VScope General Purpose A**

Bit	Name	Access	Description	Default
15:0	GP_REG_LSB_B	R/O	16 bit LSB of a 32 bit general purpose register [15:0]	0x0000

2.1.13 SD10G65 DFT Configuration and Status

Configuration and status register set for SD10G65 DFT

2.1.13.1 SD10G65 DFT Main Configuration 1

Short Name:DFT_RX_CFG_1

Address:0x1B100

Main configuration register 1 for SD10G65 DFT.

Table 94 • **SD10G65 DFT Main Configuration 1**

Bit	Name	Access	Description	Default
12	STUCK_AT_PAR_MASK_CFG	R/W	Disables error generation based on stuck_at_par errors, 0: stuck_at_par error generates 63 errors per clock cycle (in PRBS mode only) 1: stuck_at_par error does not generate errors	0x1
11	STUCK_AT_01_MASK_CFG	R/W	Disables error generation based on stuck_at_01 errors, 0: stuck_at_01 error generates 63 errors per clock cycle (in PRBS mode only) 1: stuck_at_01 error does not generate errors	0x0
10	DIRECT_THROUGH_ENA_CFG	R/W	Enables data through from gearbox to gearbox	0x0
9	ERR_CNT_CAPT_CFG	R/W	Captures data from error counter to allow reading of stable data	0x0
8:7	RX_DATA_SRC_SEL	R/W	Data source selection 0: main path 1: vscope high path 2: vscope low path	0x0
6:5	BIST_CNT_CFG	R/W	States in which error counting is enabled 3:all but IDLE; 2:check 1:stable+check 0:wait_stable+stable+check	0x0
4	FREEZE_PATTERN_CFG	R/W	Disable change of stored patterns (e.g. to avoid changes during read-out)	0x0
3	CHK_MODE_CFG	R/W	Selects pattern to check 0: PRBS pattern 1: constant pattern	0x0

Table 94 • **SD10G65 DFT Main Configuration 1 *(continued)***

Bit	Name	Access	Description	Default
2:0	RX_WID_SEL_CFG	R/W	Selects DES interface width 0:8 1:10 2:16 3:20 4:32 5:40 (default)	0x4

2.1.13.2 SD10G65 DFT Main Configuration 2

Short Name:DFT_RX_CFG_2

Address:0x1B101

Main configuration register 2 for SD10G65 DFT.

Table 95 • **SD10G65 DFT Main Configuration 2**

Bit	Name	Access	Description	Default
14	RX_WORD_MODE_CFG	R/W	Pattern generator: 0:bytes mode; 1:10-bits word mode	0x0
13:11	RX_PRBS_SEL_CFG	R/W	Selects PRBS check 0: prbs7 1: prbs15 2: prbs23 3: prbs11 4: prbs31 (default) 5: prbs9	0x4
10	INV_ENA_CFG	R/W	Enables PRBS checker input inversion	0x0
9	CMP_MODE_CFG	R/W	Selects compare mode 0: compare mode possible 1 learn mode is forced	0x0
8:6	LRN_CNT_CFG	R/W	Number of consecutive errors/non-errors before transitioning to respective state value = num-40-bits-words + 1	0x0
5	CNT_RST	R/W	SW reset of error counter; rising edge activates reset	0x0
4:3	CNT_CFG	R/W	Selects modes in which error counter is active 0:learn and compare mode 1:transition between modes 2:learn mode 3:compare mode	0x0
2:1	BIST_MODE_CFG	R/W	BIST mode 0: off 1: BIST 2: BER 3:CONT (infinite mode)	0x3
0	DFT_RX_ENA	R/W	Enable Rx DFT capability 0: Disable DFT 1: Enable DFT	0x0

2.1.13.3 SD10G65 DFT Pattern Mask Configuration 1

Short Name:DFT_RX_MASK_CFG_1

Address:0x1B102

Configuration register 1 for SD10G65 DFT to mask data bits preventing error counting for these bits.

Table 96 • **SD10G65 DFT Pattern Mask Configuration 1**

Bit	Name	Access	Description	Default
15:0	LSB_MASK_CFG_1	R/W	Mask out (active high) errors in 16 bit MSB data bits [31:16]	0x0000

2.1.13.4 SD10G65 DFT Pattern Mask Configuration 2

Short Name:DFT_RX_MASK_CFG_2

Address:0x1B103

Configuration register 2 for SD10G65 DFT to mask data bits preventing error counting for these bits.

Table 97 • **SD10G65 DFT Pattern Mask Configuration 2**

Bit	Name	Access	Description	Default
15:0	LSB_MASK_CFG_2	R/W	Mask out (active high) errors in 16 LSB data bits [15:0]	0x0000

2.1.13.5 SD10G65 DFT Pattern Checker Configuration 1

Short Name:DFT_RX_PAT_CFG_1

Address:0x1B104

Pattern checker configuration register 1 for SD10G65 DFT.

Table 98 • **SD10G65 DFT Pattern Checker Configuration 1**

Bit	Name	Access	Description	Default
15:8	MSB_MASK_CFG	R/W	Mask out (active high) errors in 8 MSB data bits	0x00
0	PAT_READ_CFG	R/W	Pattern read enable	0x0

2.1.13.6 SD10G65 DFT Pattern Checker Configuration 2

Short Name:DFT_RX_PAT_CFG_2

Address:0x1B105

Pattern checker configuration register 2 for SD10G65 DFT.

Table 99 • **SD10G65 DFT Pattern Checker Configuration 2**

Bit	Name	Access	Description	Default
11:8	MAX_ADDR_CHK_CFG	R/W	Maximum address in Checker (before continuing with address 0)	0x0
3:0	READ_ADDR_CFG	R/W	Address to read patterns from used by SW	0x0

2.1.13.7 SD10G65 DFT BIST Configuration 0A

Short Name:DFT_BIST_CFG0A

Address:0x1B106

BIST configuration register A for SD10G65 DFT controlling 'check and wait-stable' mode.

Table 100 • **SD10G65 DFT BIST Configuration 0A**

Bit	Name	Access	Description	Default
15:0	WAKEUP_DLY_CFG	R/W	BIST FSM: threshold to leave DOZE state	0x0000

2.1.13.8 SD10G65 DFT BIST Configuration 0B

Short Name:DFT_BIST_CFG0B

Address:0x1B107

BIST configuration register B for SD10G65 DFT controlling 'check and wait-stable' mode.

Table 101 • **SD10G65 DFT BIST Configuration 0B**

Bit	Name	Access	Description	Default
15:0	MAX_BIST_FRAMES_CFG	R/W	BIST FSM: threshold to enter FINISHED state	0x0000

2.1.13.9 SD10G65 DFT BIST Configuration 1A

Short Name:DFT_BIST_CFG1A

Address:0x1B108

BIST configuration register A for SD10G65 DFT controlling 'stable' mode.

Table 102 • **SD10G65 DFT BIST Configuration 1A**

Bit	Name	Access	Description	Default
15:0	MAX_UNSTABLE_CYC_CFG	R/W	BIST FSM: threshold to iterate counter for max_stable_attempts	0x0000

2.1.13.10 SD10G65 DFT BIST Configuration 1B

Short Name:DFT_BIST_CFG1B

Address:0x1B109

BIST configuration register B for SD10G65 DFT controlling 'stable' mode.

Table 103 • **SD10G65 DFT BIST Configuration 1B**

Bit	Name	Access	Description	Default
15:0	STABLE_THRES_CFG	R/W	BIST FSM: threshold to enter CHECK state	0x0000

2.1.13.11 SD10G65 DFT BIST Configuration 2A

Short Name:DFT_BIST_CFG2A

Address:0x1B10A

BIST configuration register B for SD10G65 DFT controlling frame length in 'check' mode.

Table 104 • **SD10G65 DFT BIST Configuration 2A**

Bit	Name	Access	Description	Default
15:0	FRAME_LEN_CFG_MSB	R/W	BIST FSM: threshold to iterate counter for max_bist_frames [31:16]	0x0000

2.1.13.12 SD10G65 DFT BIST Configuration B

Short Name:DFT_BIST_CFG2B

Address:0x1B10B

BIST configuration register B for SD10G65 DFT controlling frame length in 'check' mode.

Table 105 • **SD10G65 DFT BIST Configuration 2B**

Bit	Name	Access	Description	Default
15:0	FRAME_LEN_CFG_LSB	R/W	BIST FSM: threshold to iterate counter for max_bist_frames [15:0]	0x0000

2.1.13.13 SD10G65 DFT BIST Configuration 3A

Short Name:DFT_BIST_CFG3A

Address:0x1B10C

BIST configuration register A for SD10G65 DFT controlling stable attempts in ' wait-stable' mode.

Table 106 • **SD10G65 DFT BIST Configuration 3A**

Bit	Name	Access	Description	Default
15:0	MAX_STABLE_ATTEMPTS_CFG_MSB	R/W	BIST FSM: threshold to enter SYNC_ERR state [31:16]	0x0000

2.1.13.14 SD10G65 DFT BIST Configuration 3B

Short Name:DFT_BIST_CFG3B

Address:0x1B10D

BIST configuration register B for SD10G65 DFT controlling stable attempts in ' wait-stable' mode.

Table 107 • **SD10G65 DFT BIST Configuration B**

Bit	Name	Access	Description	Default
15:0	MAX_STABLE_ATTEMPTS_CFG_LSB	R/W	BIST FSM: threshold to enter SYNC_ERR state [15:0]	0x0000

2.1.13.15 SD10G65 DFT Error Status 1

Short Name:DFT_ERR_STAT_1

Address:0x1B10E

Status register 1 for SD10G65 DFT containing the error counter value

Table 108 • **SD10G65 DFT Error Status 1**

Bit	Name	Access	Description	Default
15:0	ERR_CNT_MSB	R/O	Counter output depending on cnt_cfg [31:16]	0x0000

2.1.13.16 SD10G65 DFT Error Status 2

Short Name:DFT_ERR_STAT_2

Address:0x1B10F

Status register B2 for SD10G65 DFT containing the error counter value

Table 109 • **SD10G65 DFT Error Status 2**

Bit	Name	Access	Description	Default
15:0	ERR_CNT_LSB	R/O	Counter output depending on cnt_cfg [15:0]	0x0000

2.1.13.17 SD10G65 DFT PRBS Status 1

Short Name:DFT_PRBS_STAT_1

Address:0x1B110

Status register 1 for SD10G65 DFT containing the PRBS data related to 1st sync lost event

Table 110 • **SD10G65 DFT PRBS Status 1**

Bit	Name	Access	Description	Default
15:0	PRBS_DATA_STAT_MSB	R/O	PRBS data after first sync lost [31:16]	0x0000

2.1.13.18 SD10G65 DFT PRBS Status 2

Short Name:DFT_PRBS_STAT_2

Address:0x1B111

Status register 2 for SD10G65 DFT containing the PRBS data related to 1st sync lost event

Table 111 • **SD10G65 DFT PRBS Status 2**

Bit	Name	Access	Description	Default
15:0	PRBS_DATA_STAT_LSB	R/O	PRBS data after first sync lost [15:0]	0x0000

2.1.13.19 SD10G65 DFT Miscellaneous Status 1

Short Name:DFT_MAIN_STAT_1

Address:0x1B112

Status register 1 for SD10G65 DFT

Table 112 • **SD10G65 DFT Miscellaneous Status 1**

Bit	Name	Access	Description	Default
9:0	CMP_DATA_STAT	R/O	10 bits data word at address 'read_addr_cfg' used for further observation by SW	0x000

2.1.13.20 SD10G65 DFT Miscellaneous Status 2

Short Name:DFT_MAIN_STAT_2

Address:0x1B113

Status register 2 for SD10G65 DFT

Table 113 • **SD10G65 DFT Miscellaneous Status 2**

Bit	Name	Access	Description	Default
5	STUCK_AT_PAR	R/O	Data input is unchanged for all 40 parallel bits for at least 7 clock cycles (defined by c_STCK_CNT_THRES)	0x0
4	STUCK_AT_01	R/O	Data input is constantly 0 or constantly 1 for all 40 parallel bits for at least 7 clock cycles (defined by c_STCK_CNT_THRES)	0x0
3	NO_SYNC	R/O	BIST: no sync found since BIST enabled	0x0
2	INSTABLE	R/O	BIST: input data not stable	0x0
1	INCOMPLETE	R/O	BIST not complete (i.e. not reached stable state or following)	0x0
0	ACTIVE	R/O	BIST is active (i.e. left DOZE but did not enter a final state)	0x0

2.1.13.21 SD10G65 DFT Main Configuration

Short Name:DFT_TX_CFG

Address:0x1B114

Main configuration register for SD10G65 DFT.

Table 114 • **SD10G65 DFT Main Configuration**

Bit	Name	Access	Description	Default
12	RST_ON_STUCK_AT_CFG	R/W	Enables (1) reset of PRBS generator in case of unchanged data ('stuck-at') for at least 511 clock cycles. Can be disabled (0) e.g. in scrambler mode to avoid the very rare case that input patterns allow to keep the generator's shift register filled with a constant value.	0x1
11:9	TX_WID_SEL_CFG	R/W	Selects SER interface width 0:8 1:10 2:16 3:20 4:32 5:40 (default)	0x4
8:6	TX_PRBS_SEL_CFG	R/W	Selects PRBS generator 0: prbs7 1: prbs15 2: prbs23 3: prbs11 4: prbs31 (default) 5: prbs9	0x4
5	SCRAM_INV_CFG	R/W	Inverts the scrambler output	0x0
4	IPATH_CFG	R/W	Selects PRBS generator input 0:pat-gen 1:core	0x0

Table 114 • **SD10G65 DFT Main Configuration**

Bit	Name	Access	Description	Default
3:2	OPATH_CFG	R/W	Selects DFT-Tx output 0:PRBS/scrambler (default) 1:bypass	0x0
1	TX_WORD_MODE_CFG	R/W	Word width of constant pattern generator 0:bytes mode; 1:10-bits word mode	0x0
0	DFT_TX_ENA	R/W	Enable Tx DFT capability 0: Disable DFT 1: Enable DFT	0x0

2.1.13.22 SD10G65 DFT Tx Constant Pattern Configuration 1

Short Name:DFT_TX_PAT_CFG_1

Address:0x1B115

Tx Constant MSB pattern configuration register 1 for SD10G65 DFT.

Table 115 • **SD10G65 DFT Tx Constant Pattern Configuration 1**

Bit	Name	Access	Description	Default
4	PAT_VLD_CFG	R/W	Constant patterns are valid to store	0x0
3:0	MAX_ADDR_GEN_CFG	R/W	Maximum address in generator (before continuing with address 0)	0x0

2.1.13.23 SD10G65 DFT Tx Constant Pattern Configuration 2

Short Name:DFT_TX_PAT_CFG_2

Address:0x1B116

Tx Constant MSB pattern configuration register 2 for SD10G65 DFT.

Table 116 • **SD10G65 DFT Tx Constant Pattern Configuration 2**

Bit	Name	Access	Description	Default
13:10	STORE_ADDR_CFG	R/W	Current storage address for patterns in generator	0x0
9:0	PATTERN_CFG	R/W	10 bits word of constant patterns for transmission	0x000

2.1.13.24 SD10G65 DFT Tx Constant Pattern Status

Short Name:DFT_TX_CMP_DAT_STAT

Address:0x1B117

Status register for SD10G65 DFT containing the constant patterns used for comparison (last in LEARN mode)

Table 117 • **SD10G65 DFT Tx Constant Pattern Status**

Bit	Name	Access	Description	Default
12	TX_STUCK_AT_STICKY	Sticky	Scrambler/PRBS generator output unchanged for at least 511 clock cycles. The high state is cleared by writing a 1 to the bit.	0x0
9:0	PAT_STAT	R/O	10 bits data word at address 'store_addr_cfg' used for further observation by SW	0x000

2.1.13.25 DFT Clock Compare Config

Short Name:DFT_CLK_CMP_CFG

Address:0x1B118

Configuration register for Clock Compare logic. Compared clocks are always divided by 4 before any further processing. A clock edge on tx_clk increments the counter, a clock edge on rx_clk decrements the counter. If only one clock is selected for clock comparison, the number of clock cycles within a given time can be measured.

Table 118 • **DFT Clock Compare Config**

Bit	Name	Access	Description	Default
12	CLK_CMP_UPDTOG	R/O	Clock compare value updated toggle bit. Toggles on each update of CLK_CMP_VALUE	0x0
8	CLK_CMP_WRAP_ENA	R/W	Enable clock comparison counter wrap 0: counter saturates 1: counter wraps	0x0
7:6	CLK_CMP_DIV_TX	R/W	Clock compare divider for Tx clock 0: tx clk 1: tx_clk/2 2: tx_clk/4 3: tx_clk/8	0x3
5:4	CLK_CMP_DIV_RX	R/W	Clock compare divider for Rx clock 0: rx clk 1: rx_clk/2 2: rx_clk/4 3: rx_clk/8	0x3
3:2	CLK_CMP_SEL	R/W	Clock compare selection 0: rx_clk vs. tx_clk 1: rx_clk 2: tx_clk 3: Reserved	0x0
1	CLK_CMP_MODE	R/W	Clock comparison mode 0: single shot 1: continuous	0x0
0	CLK_CMP_ENA	R/W	Enable clock comparison (enabling automatically clears comparison counter)	0x0

2.1.13.26 DFT Clock Compare Timer

Short Name:DFT_CLK_CMP_TIMERA

Address:0x1B119

Upper half of clock comparison timer. After timer has expired, current clock comparison value is stored. The timer is clocked at 156.25 MHz.

Table 119 • **DFT Clock Compare Timer**

Bit	Name	Access	Description	Default
15:0	CLK_CMP_TIMER_MSB	R/W	Clock comparison timer, bits [31:16]. Counter interval is N + 1 clock cycles where the clock frequency is 156.25 MHz.	0x0950

2.1.13.27 DFT Clock Compare Timer

Short Name:DFT_CLK_CMP_TIMERB

Address:0x1B11A

Lower half of clock comparison timer. After timer has expired, current clock comparison value is stored. The timer is clocked at 156.25 MHz.

Table 120 • **DFT Clock Compare Timer**

Bit	Name	Access	Description	Default
15:0	CLK_CMP_TIMER_LSB	R/W	Clock comparison timer, bits [15:0]. Counter interval is N + 1 clock cycles where the clock frequency is 156.25 MHz.	0x2F8F

2.1.13.28 DFT Clock Comparison Value A

Short Name:DFT_CLK_CMP_VALUEA

Address:0x1B11B

Upper half of clock comparison result. This register is updated after clock comparison timer has expired. In continuous mode this register is periodically updated.

Table 121 • **DFT Clock Comparison Value A**

Bit	Name	Access	Description	Default
15:0	CLK_CMP_VALUE_MSB	R/O	Clock comparison value (difference between clk0 and clk1), bits [31:16]	0x0000

2.1.13.29 DFT Clock Comparison Value B

Short Name:DFT_CLK_CMP_VALUEB

Address:0x1B11C

Lower half of clock comparison result. This register is updated after clock comparison timer has expired. In continuous mode this register is periodically updated.

Table 122 • **DFT Clock Comparison Value B**

Bit	Name	Access	Description	Default
15:0	CLK_CMP_VALUE_LSB	R/O	Clock comparison value (difference between clk0 and clk1), bits [15:0]	0x0000

2.1.13.30 DFT Clock Comparison Maximum Value A

Short Name:DFT_CLK_CMP_MAXVALA

Address:0x1B11D

Upper half of clock comparison max result. Can be used to judge e.g. SSC clock deviation. This register is updated after clock comparison timer has expired. In continuous mode this register is periodically updated.

Table 123 • **DFT Clock Comparison Maximum Value A**

Bit	Name	Access	Description	Default
15:0	CLK_CMP_MAXVAL_MSB	R/O	Clock comparison max value (maximum measured difference between clk0 and clk1), bits [31:16]	0x0000

2.1.13.31 DFT Clock Comparison Maximum Value B

Short Name:DFT_CLK_CMP_MAXVALB

Address:0x1B11E

Lower half of clock comparison max result. Can be used to judge e.g. SSC clock deviation. This register is updated after clock comparison timer has expired. In continuous mode this register is periodically updated.

Table 124 • **DFT Clock Comparison Maximum Value B**

Bit	Name	Access	Description	Default
15:0	CLK_CMP_MAXVAL_LSB	R/O	Clock comparison max value (maximum measured difference between clk0 and clk1), bits [15:0]	0x0000

2.1.13.32 DFT Tx Error Insertion Configuration

Short Name:DFT_TX_ERR_INSERT_CFG_1

Address:0x1B11F

Configuration register for explicit error insertion into DFT driven data stream. Allows to insert expected errors to check e.g. Tx/Rx connectivity

Table 125 • **DFT Tx Error Insertion Configuration**

Bit	Name	Access	Description	Default
15:6	CG_TIMER_CFG	R/W	Preload value for clock generator timer	0x000
4	ERR_TRIG_ONESHOT_CFG	R/W	Trigger a single error or a burst of errors (refer to num_err_cfg) 0 to 1 (edge) activates this function	0x0
3:0	ERR_FREQ_CFG	R/W	Frequency of continous/limited error insertion in steps of 40 bits 0: disable continous insertion 1-15: step between 2 errors = 2^(err_freq_cfg + 5) 40 bit words (refer also to err_posit_offs_cfg)	0x0

2.1.13.33 DFT Tx Error Insertion Configuration

Short Name:DFT_TX_ERR_INSERT_CFG_2

Address:0x1B120

Configuration register for explicit error insertion into DFT driven data stream. Allows to insert expected errors to check e.g. Tx/Rx connectivity

Table 126 • **DFT Tx Error insertion Configuration**

Bit	Name	Access	Description	Default
15:10	ERR_POSIT_CFG	R/W	Position within 40 bit word where an error is inserted by inverting the bit value 0: LSB 39: MSB 40-63: reserved	0x00

Table 126 • **DFT Tx Error insertion Configuration *(continued)***

Bit	Name	Access	Description	Default
9:4	ERR_POSIT_OFFS_CFG	R/W	Offset of bit position increased per inserted error; allows 'walking' error. Offset is reset when continuous/limited error insertion is disabled or burst mode is enabled and burst insertion is finished or err_posit_offs_cfg = 0 0: disabled 1: move 1 bit (from LSB to MSB) ... 39: move 39 bit (from LSB to MSB) 40-63: reserved	0x00
3:0	NUM_ERR_CFG	R/W	limited error insertion: burst mode (err_freq_cfg must be > 0) 0: burst mode is disabled 1-15: number of errors after each error triggering = 2^(num_err_cfg + 5)	0x0

2.1.13.34 DFT Clock Generator Configuration 1

Short Name:DFT_CLK_GEN_CFG_1

Address:0x1B121

Configuration register for clock generator to build a low speed clock signal of variable length and variable duty cycle provided on all data bits simultaneously

Table 127 • **DFT Clock Generator Configuration 1**

Bit	Name	Access	Description	Default
9:0	CG_PER_CFG	R/W	(Half) clock period cfg in normal mode: high period = cg_per_cfg + cg_dcd_cfg, low period = cg_per_cfg - cg_dcd_cfg	0x000

2.1.13.35 DFT Clock Generator Configuration 2

Short Name:DFT_CLK_GEN_CFG_2

Address:0x1B122

Configuration register for clock generator to build a low speed clock signal of variable length and variable duty cycle provided on all data bits simultaneously

Table 128 • **DFT Clock Generator Configuration 2**

Bit	Name	Access	Description	Default
9:0	CG_PER_JUMP_CFG	R/W	(Half) clock period cfg in jump mode: high period = cg_per_cfg + cg_dcd_cfg, low period = cg_per_cfg - cg_dcd_cfg	0x000

2.1.13.36 DFT Clock Generator Configuration 3

Short Name:DFT_CLK_GEN_CFG_3

Address:0x1B123

Configuration register for clock generator to build a low speed clock signal of variable length and variable duty cycle provided on all data bits simultaneously

Table 129 • **DFT Clock Generator Configuration 3**

Bit	Name	Access	Description	Default
11:2	CG_DCD_CFG	R/W	Duty cycle distortion: high period = cg_per_cfg + cg_dcd_cfg, low period = cg_per_cfg - cg_dcd_cfg	0x000
1:0	CG_MODE_CFG	R/W	clock generator mode 0: normal operation cg_per_cfg controls period; 0->1 transition: after current period has finished (only) the next period is controlled by cg_per_jump_cfg afterwards normal operation 2: every N'th period the high value is replaced by a low value N is defined by cg_timer_cfg 3: every N'th period the low value is replaced by a high value N is defined by cg_timer_cfg	0x0

2.1.14 ROM Engine

2.1.14.1 SPI Address Field of ROM Table Entry

Short Name:spi_adr

Addresses:0x1B200 - 0x1B286

Table 130 • **SPI Address Field of ROM Table Entry ... replication_count=135**

Bit	Name	Access	Description	Default
6:0	spi_adr	R/W	SPI address to write	0x00

2.1.14.2 Lower 16 bits of SPI Data Field Of ROM Table Entry

Short Name:data_lsw

Addresses:0x1B300 - 0x1B386

Table 131 • **Lower 16 bits of SPI Data Field of ROM Table Entry ... replication_count=135**

Bit	Name	Access	Description	Default
15:0	spi_dat_lsw	R/W	SPI data lsw	0x0000

2.1.14.3 Upper 16 bits of SPI Data Field Of ROM Table Entry

Short Name:data_msw

Addresses:0x1B400 - 0x1B486

Table 132 • **Upper 16 bits of SPI Data Field of ROM Table Entry ... replication_count=135**

Bit	Name	Access	Description	Default
15:0	spi_dat_msw	R/W	SPI data msw	0x0000

2.1.14.4 ROM Table Start/End Addresses of Tx 10G Setting Routine

Short Name:adr_tx10g

Address:0x1B600

Table 133 • **ROM Table Start/End Addresses of Tx 10G Setting Routine**

Bit	Name	Access	Description	Default
15:8	adr_tx10g_start	R/W	Starting ROM address of Tx 10G routine	0x00
7:0	adr_tx10g_end	R/W	Ending ROM address of Tx 10G routine	0x10

2.1.14.5 ROM Table Start/End Addresses of Rx 10G Setting Routine

Short Name:adr_rx10g

Address:0x1B601

Table 134 • **ROM Table Start/End Addresses of Rx 10G Setting Routine**

Bit	Name	Access	Description	Default
15:8	adr_rx10g_start	R/W	Starting ROM address of Rx 10G routine	0x11
7:0	adr_rx10g_end	R/W	Ending ROM address of Rx 10G routine	0x2C

2.1.14.6 ROM Table Start/End Addresses of Tx 1G Setting Routine

Short Name:adr_tx1g

Address:0x1B602

Table 135 • **ROM Table Start/End Addresses of Tx 1G Setting Routine**

Bit	Name	Access	Description	Default
15:8	adr_tx1g_start	R/W	Starting ROM address of Tx 1G routine	0x2D
7:0	adr_tx1g_end	R/W	Ending ROM address of Tx 1G routine	0x3D

2.1.14.7 ROM Table Start/End Addresses of Rx 1G Setting Routine

Short Name:adr_rx1g

Address:0x1B603

Table 136 • **ROM Table Start/End Addresses of Rx 1G Setting Routine**

Bit	Name	Access	Description	Default
15:8	adr_rx1g_start	R/W	Starting ROM address of Rx 1G routine	0x3E
7:0	adr_rx1g_end	R/W	Ending ROM address of Rx 1G routine	0x59

2.1.14.8 ROM Table Start/End Addresses of WAN Setting Routine

Short Name:adr_wan

Address:0x1B604

Table 137 • **ROM Table Start/End Addresses of WAN Setting Routine**

Bit	Name	Access	Description	Default
15:8	adr_wan_start	R/W	Starting ROM address of WAN routine	0x5A
7:0	adr_wan_end	R/W	Ending ROM address of WAN routine	0x86

2.1.14.9 ROM Engine Status

Short Name:ROMENG_STATUS

Address:0x1B6FF

ROM Engine Status

Table 138 • **ROM Engine Status**

Bit	Name	Access	Description	Default
5:1	exe_last	R/O	ROM Engine last routine executed 00000: 10G - configured for 10G mode 00001: TX10G - Tx configured for 10G mode 00010: RX10G - Rx configured for 10G mode 00011: 1G - configured for 1G mode 00100: TX1G - Rx configured for 1G mode 00101: RX1G - Rx configured for 1G mode 00110: 3G - configured for 3G mode 00111: TX3G - Rx configured for 3G mode 01000: RX3G - Rx configured for 3G mode 01001: WAN - configured for WAN mode 01010: RST - configured to Reset condition 01011: LBON - configured for Loopback enabled 01100: LBOFF - configured for Loopback disabled 01101: LPON - LowPower mode enabled 01110: LPOFF - LowPower mode disabled 01111: RC - RCOMP routine 10000: LRON - Lock2Ref enabled 10001: LROFF - Lock2Ref disabled others: invalid	0x00
0	exe_done	R/O	ROM Engine status This is a sticky bit that latches the high state. The latch-high bit is cleared when the register is read. 0: ROM Engine has not executed a new routine since the last time this bit is read 1: ROM Engine has executed a new routine since the last time this bit is read	0x0

2.2 LINE_KR_DEV1 (Device 0x1)

Table 139 • **KR_1x0096**

Address	Short Description	Register Name	Details
0x10096	KR PMD Control	KR_1x0096	Page 56

Table 140 • **KR_1x0097**

Address	Short Description	Register Name	Details
0x10097	KR PMD Status	KR_1x0097	Page 57

Table 141 • **KR_1x0098**

Address	Short Description	Register Name	Details
0x10098	KR LP Coefficient Update	KR_1x0098	Page 57

Table 142 • **KR_1x0099**

Address	Short Description	Register Name	Details
0x10099	KR LP Status Report	KR_1x0099	Page 57

Table 143 • **KR_1x009A**

Address	Short Description	Register Name	Details
0x1009A	KR LD Coefficient Update	KR_1x009A	Page 58

Table 144 • **KR_1x009B**

Address	Short Description	Register Name	Details
0x1009B	KR LD Status Report	KR_1x009B	Page 58

Table 145 • **tr_cfg0**

Address	Short Description	Register Name	Details
0x18200	VS Training Config 0	tr_cfg0	Page 58

Table 146 • **tr_cfg1**

Address	Short Description	Register Name	Details
0x18201	VS Training Config 1	tr_cfg1	Page 58

Table 147 • **tr_cfg2**

Address	Short Description	Register Name	Details
0x18202	VS Training Config 2	tr_cfg2	Page 59

Table 148 • **tr_cfg3**

Address	Short Description	Register Name	Details
0x18203	VS Training Config 3	tr_cfg3	Page 59

Table 149 • **tr_cfg4**

Address	Short Description	Register Name	Details
0x18204	VS Training Config 4	tr_cfg4	Page 59

Table 150 • **tr_cfg5**

Address	Short Description	Register Name	Details
0x18205	VS Training Config 5	tr_cfg5	Page 59

Table 151 • **tr_cfg6**

Address	Short Description	Register Name	Details
0x18206	VS Training Config 6	tr_cfg6	Page 60

Table 152 • **tr_cfg7**

Address	Short Description	Register Name	Details
0x18207	VS Training Config 7	tr_cfg7	Page 60

Table 153 • **tr_cfg8**

Address	Short Description	Register Name	Details
0x18208	VS Training Config 8	tr_cfg8	Page 60

Table 154 • **tr_cfg9**

Address	Short Description	Register Name	Details
0x18209	VS Training Config 9	tr_cfg9	Page 60

Table 155 • **tr_gain**

Address	Short Description	Register Name	Details
0x1820A	VS Training Gain Target and Margin Values	tr_gain	Page 61

Table 156 • **tr_coef_ovrd**

Address	Short Description	Register Name	Details
0x1820B	VS Training Coefficient Update Override	tr_coef_ovrd	Page 61

Table 157 • **tr_stat_ovrd**

Address	Short Description	Register Name	Details
0x1820C	VS Training Status Report Override	tr_stat_ovrd	Page 61

Table 158 • **tr_ovrd**

Address	Short Description	Register Name	Details
0x1820D	VS Training Override	tr_ovrd	Page 61

Table 159 • **tr_step**

Address	Short Description	Register Name	Details
0x1820E	VS Training State Step	tr_step	Page 62

Table 160 • **tr_mthd**

Address	Short Description	Register Name	Details
0x1820F	VS Training Method	tr_mthd	Page 62

Table 161 • **tr_ber_thr**

Address	Short Description	Register Name	Details
0x18210	VS Training BER Threshold Settings	tr_ber_thr	Page 62

Table 162 • **tr_ber_ofs**

Address	Short Description	Register Name	Details
0x18211	VS Training BER Offset Setting	tr_ber_ofs	Page 62

Table 163 • **tr_lutsel**

Address	Short Description	Register Name	Details
0x18212	VS Training LUT Selection	tr_lutsel	Page 63

Table 164 • **tr_brkmask**

Address	Short Description	Register Name	Details
0x18213	VS Training break_mask LSW	brkmask_lsw	Page 63
0x18214	VS Training break_mask MSW	brkmask_msw	Page 63

Table 165 • **obcfg_addr**

Address	Short Description	Register Name	Details
0x18230	VS Training ROM Address for End and obcfg	obcfg_addr	Page 63

Table 166 • **apc_tmr**

Address	Short Description	Register Name	Details
0x18240	VS Training apc_timer	apc_tmr	Page 64

Table 167 • **wt_tmr**

Address	Short Description	Register Name	Details
0x18241	VS Training wait_timer	wt_tmr	Page 64

Table 168 • **mw_tmr**

Address	Short Description	Register Name	Details
0x18242	VS Training maxwait_timer LSW	mw_tmr_lsw	Page 64
0x18243	VS Training maxwait_timer MSW	mw_tmr_msw	Page 64

Table 169 • **tr_sts1**

Address	Short Description	Register Name	Details
0x18250	VS Training Status 1	tr_sts1	Page 64

Table 170 • **tr_sts2**

Address	Short Description	Register Name	Details
0x18251	VS Training Status 2	tr_sts2	Page 65

Table 171 • **tr_tapval**

Address	Short Description	Register Name	Details
0x18254	VS Tap CM Value	tr_cmval	Page 65
0x18255	VS Tap C0 Value	tr_c0val	Page 65
0x18256	VS Tap CP Value	tr_cpval	Page 65

Table 172 • **tr_frames_sent**

Address	Short Description	Register Name	Details
0x18260	VS Training frames_sent LSW	frsent_lsw	Page 66
0x18261	VS Training frames_sent MSW	frsent_msw	Page 66

Table 173 • **tr_lut**

Address	Short Description	Register Name	Details
0x18270	VS Training lut_read LSW	lut_lsw	Page 66
0x18271	VS Training lut_read MSW	lut_msw	Page 66

Table 174 • **tr_errcnt**

Address	Short Description	Register Name	Details
0x18272	VS Training prbs11 error_count	tr_errcnt	Page 66

2.2.1 KR PMD Control and Status

2.2.1.1 KR PMD Control

Short Name:KR_1x0096

Address:0x10096

Table 175 • **KR PMD Control**

Bit	Name	Access	Description	Default
1	tr_enable	R/W	Training enable 1: Enable KR start-up protocol 0: Disable KR start-up protocol	0x0
0	tr_restart	R/W	Restart training (SC) 1: Reset KR start-up protocol 0: Normal operation	0x0

2.2.1.2 KR PMD Status

Short Name:KR_1x0097

Address:0x10097

Table 176 • **KR PMD Status**

Bit	Name	Access	Description	Default
3	tr_fail	R/O	Training failure 1: Training failure has been detected 0: Training failure has not been detected	0x0
2	stprot	R/O	Startup protocol status 1: Start-up protocol in progress 0: Start-up protocol complete	0x0
1	frlock	R/O	Frame lock 1: Training frame delineation detected, 0: Training frame delineation not detected	0x0
0	rcvr_rdy	R/O	Receiver status 1: Receiver trained and ready to receive data 0: Receiver training	0x0

2.2.1.3 KR LP Coefficient Update

Short Name:KR_1x0098

Address:0x10098

Table 177 • **KR LP Coefficient Update**

Bit	Name	Access	Description	Default
15:0	lpcoef	R/O	Received coefficient update field	N/A

2.2.1.4 KR LP Status Report

Short Name:KR_1x0099

Address:0x10099

Table 178 • **KR LP Status Report**

Bit	Name	Access	Description	Default
15:0	lpstat	R/O	Received status report field	N/A

2.2.1.5 KR LD Coefficient Update

Short Name:KR_1x009A

Address:0x1009A

Table 179 • **KR LD Coefficient Update**

Bit	Name	Access	Description	Default
15:0	ldcoef	R/O	Transmitted coefficient update field	N/A

2.2.1.6 KR LD Status Report

Short Name:KR_1x009B

Address:0x1009B

Table 180 • **KR LD Status Report**

Bit	Name	Access	Description	Default
15:0	ldstat	R/O	Transmitted status report field	N/A

2.2.2 KR Vendor Specific Training

2.2.2.1 VS Training Config 0

Short Name:tr_cfg0

Address:0x18200

Table 181 • **VS Training Config 0**

Bit	Name	Access	Description	Default
15:12	tmr_dvdr	R/W	Clock divider value for timer clocks.	0x4
10	rx_inv	R/W	Invert received prbs11 within training frame	0x0
9	tx_inv	R/W	Invert transmitted prbs11 within training frame	0x0
4	ld_pre_init	R/W	Set local taps starting point 0: Set to INITIALIZE 1: Set to PRESET	0x1
3	lp_pre_init	R/W	Send first LP request 0: Send INITIALIZE 1: Send PRESET	0x1
2	nosum	R/W	Update taps regardless of v2,vp sum.	0x0
1	part_cfg_en	R/W	Enable partial OB tap configuration.	0x1
0	tapctl_en	R/W	Allow LP to to control tap settings.	0x1

2.2.2.2 VS Training Config 1

Short Name:tr_cfg1

Address:0x18201

Table 182 • **VS Training Config 1**

Bit	Name	Access	Description	Default
10:0	tmr_hold	R/W	Freeze timers. Bit set... 0: wait 1: max_wait 2: 1g 3: 3g 4: 10g 5: training 6: pgdet 7: link_pass 8: link_fail 9: an_wait 10: break_link	0x000

2.2.2.3 VS Training Config 2

Short Name:tr_cfg2

Address:0x18202

Table 183 • **VS Training Config 2**

Bit	Name	Access	Description	Default
11:6	vp_max	R/W	max settings for vp sum.	0x1F
5:0	v2_min	R/W	min settings for v2 sum.	0x01

2.2.2.4 VS Training Config 3

Short Name:tr_cfg3

Address:0x18203

Table 184 • **VS Training Config 3**

Bit	Name	Access	Description	Default
11:6	cp_max	R/W	max settings for local transmitter.	0x00
5:0	cp_min	R/W	min settings for local transmitter.	0x34

2.2.2.5 VS Training Config 4

Short Name:tr_cfg4

Address:0x18204

Table 185 • **VS Training Config 4**

Bit	Name	Access	Description	Default
11:6	c0_max	R/W	max settings for local transmitter.	0x1F
5:0	c0_min	R/W	min settings for local transmitter.	0x11

2.2.2.6 VS Training Config 5

Short Name:tr_cfg5

Address:0x18205

Table 186 • **VS Training Config 5**

Bit	Name	Access	Description	Default
11:6	cm_max	R/W	max settings for local transmitter.	0x00
5:0	cm_min	R/W	min settings for local transmitter.	0x3A

2.2.2.7 VS Training Config 6

Short Name:tr_cfg6

Address:0x18206

Table 187 • **VS Training Config 6**

Bit	Name	Access	Description	Default
11:6	cp_init	R/W	initialize settings for local transmitter.	0x38
5:0	c0_init	R/W	initialize settings for local transmitter.	0x14

2.2.2.8 VS Training Config 7

Short Name:tr_cfg7

Address:0x18207

Table 188 • **VS Training Config 7**

Bit	Name	Access	Description	Default
11:6	cm_init	R/W	initialize settings for local transmitter.	0x3E
5:0	dfe_ofs	R/W	Signed value to adjust final LP C(+1) tap position from calculated optimal setting.	0x00

2.2.2.9 VS Training Config 8

Short Name:tr_cfg8

Address:0x18208

Table 189 • **VS Training Config 8**

Bit	Name	Access	Description	Default
7:6	wt1	R/W	Weighted average calculation of DFE tap 1	0x1
5:4	wt2	R/W	Weighted average calculation of DFE tap 2	0x1
3:2	wt3	R/W	Weighted average calculation of DFE tap 3	0x1
1:0	wt4	R/W	Weighted average calculation of DFE tap 4	0x1

2.2.2.10 VS Training Config 9

Short Name:tr_cfg9

Address:0x18209

Table 190 • **VS Training Config 9**

Bit	Name	Access	Description	Default
15:0	frcnt_ber	R/W	Number of training frames used for BER calculation.	0x0014

2.2.2.11 VS Training Gain Target and Margin Values

Short Name:tr_gain

Address:0x1820A

Table 191 • **VS Training Gain Target And Margin Values**

Bit	Name	Access	Description	Default
15:10	gain_marg	R/W	LP C(0) optimized when GAIN is gain_targ +/- 2*gain_marg	0x28
9:0	gain_targ	R/W	Target value of GAIN setting during LP C(0) optimization.	0x000

2.2.2.12 VS Training Coefficient Update Override

Short Name:tr_coef_ovrd

Address:0x1820B

Table 192 • **VS Training Coefficient Update Override**

Bit	Name	Access	Description	Default
15:0	coef_ovrd	R/W	Override Coef_update field to transmit	0x0000

2.2.2.13 VS Training Status Report Override

Short Name:tr_stat_ovrd

Address:0x1820C

Table 193 • **VS Training Status Report Override**

Bit	Name	Access	Description	Default
15:0	stat_ovrd	R/W	Override Stat_report field to transmit	0x0000

2.2.2.14 VS Training Override

Short Name:tr_ovrd

Address:0x1820D

Table 194 • **VS Training Override**

Bit	Name	Access	Description	Default
4	ovrd_en	R/W	Enable manual training	0x0
3	rxtrained_ovrd	R/W	Control of rx_trained variable for training SM	0x0
2	ber_en_ovrd	R/W	Generate BER enable pulse (SC)	0x0
1	coef_ovrd_vld	R/W	Generate Coef_update_valid pulse (SC)	0x0
0	stat_ovrd_vld	R/W	Generate Stat_report_valid pulse (SC)	0x0

2.2.2.15 VS Training State Step

Short Name:tr_step

Address:0x1820E

Table 195 • **VS Training State Step**

Bit	Name	Access	Description	Default
0	step	R/W	Step to next lptrain state (if at breakpoint) (SC)	0x0

2.2.2.16 VS Training Method

Short Name:tr_mthd

Address:0x1820F

Table 196 • **VS Training Method**

Bit	Name	Access	Description	Default
11:10	mthd_cp	R/W	Training method for remote C(+1) 0: BER method 1: Gain method 2: DFE method	0x2
9:8	mthd_c0	R/W	Training method for remote C(0)	0x1
7:6	mthd_cm	R/W	Training method for remote C(-1)	0x0
5:4	ord1	R/W	remote tap to optimize first 0: C(-1) 1: C(0) 2: C(+1)	0x1
3:2	ord2	R/W	remote tap to optimize second	0x2
1:0	ord3	R/W	remote tap to optimize third	0x0

2.2.2.17 VS Training BER Threshold Settings

Short Name:tr_ber_thr

Address:0x18210

Table 197 • **VS Training BER Threshold Settings**

Bit	Name	Access	Description	Default
15:8	ber_err_th	R/W	Only consider error count > ber_err_th	0x00
7:0	ber_wid_th	R/W	Only consider errored range > ber_wid_th	0x00

2.2.2.18 VS Training BER Offset Setting

Short Name:tr_ber_ofs

Address:0x18211

Table 198 • **VS Training BER Offset Setting**

Bit	Name	Access	Description	Default
14:10	cp_ber_ofs	R/W	Signed value to adjust final cp tap position from calculated optimal setting.	0x00

Table 198 • **VS Training BER Offset Setting *(continued)***

Bit	Name	Access	Description	Default
9:5	c0_ber_ofs	R/W	Signed value to adjust final c0 tap position from calculated optimal setting.	0x00
4:0	cm_ber_ofs	R/W	Signed value to adjust final cm tap position from calculated optimal setting.	0x00

2.2.2.19 VS Training LUT Selection

Short Name:tr_lutsel

Address:0x18212

Table 199 • **VS Training LUT Selection**

Bit	Name	Access	Description	Default
8:3	lut_row	R/W	Selects LUT table entry (0 to 63).	0x00
2:0	lut_sel	R/W	Selects LUT for lut_o 0: Gain 1: DFE_1 2: DFE_2 3: DFE_avg_1 4: DFE_avg_2 5: BER_1 6: BER_2 7: BER_3	0x0

2.2.2.20 VS Training break_mask LSW

Short Name:brkmask_lsw

Address:0x18213

Table 200 • **VS Training break_mask LSW**

Bit	Name	Access	Description	Default
15:0	brkmask_lsw	R/W	Select lptrain state machine breakpoints. Each bit corresponds to a state (see design doc)	0x0000

2.2.2.21 VS Training break_mask MSW

Short Name:brkmask_msw

Address:0x18214

Table 201 • **VS Training break_mask MSW**

Bit	Name	Access	Description	Default
15:0	brkmask_msw	R/W	Select lptrain state machine breakpoints. Each bit corresponds to a state (see design doc)	0x0000

2.2.2.22 VS Training ROM Address for End and obcfg

Short Name:obcfg_addr

Address:0x18230

Table 202 • **VS Training ROM Address for End and obcfg**

Bit	Name	Access	Description	Default
6:0	obcfg_addr	R/W	Address of OB tap configuration settings	0x00

2.2.2.23 VS Training apc_timer

Short Name:apc_tmr

Address:0x18240

Table 203 • **VS Training apc_timer**

Bit	Name	Access	Description	Default
15:0	apc_tmr	R/W	Delay between LP tap update, and capture of direct-connect apc values	0x0000

2.2.2.24 VS Training wait_timer

Short Name:wt_tmr

Address:0x18241

Table 204 • **VS Training wait_timer**

Bit	Name	Access	Description	Default
15:0	wt_tmr	R/W	wait_timer for training state machine to allow extra training frames to be exchanged	0x0A08

2.2.2.25 VS Training maxwait_timer LSW

Short Name:mw_tmr_lsw

Address:0x18242

Table 205 • **VS Training maxwait_timer LSW**

Bit	Name	Access	Description	Default
15:0	mw_tmr_lsw	R/W	maxwait_timer, when training expires and failure declared. 500ms	0xA30A

2.2.2.26 VS Training maxwait_timer MSW

Short Name:mw_tmr_msw

Address:0x18243

Table 206 • **VS Training maxwait_timer MSW**

Bit	Name	Access	Description	Default
15:0	mw_tmr_msw	R/W	maxwait_timer, when training expires and failure declared. 500ms	0x0133

2.2.2.27 VS Training Status 1

Short Name:tr_sts1

Address:0x18250

Table 207 • **VS Training Status 1**

Bit	Name	Access	Description	Default
12	ber_busy	R/O	Indicates prbs11 checker is active	N/A
11:9	tr_sm	R/O	Training state machine	N/A
8:4	lptrain_sm	R/O	LP training state machine	N/A
3	gain_fail	R/O	Indicates gain_target was not reached during LP training	N/A
2	training	R/O	training variable from training state machine	N/A
1	dme_viol	R/O	Indicates a DME violation has occurred (LH)	N/A
0	tr_done	R/O	Indicates that local and remote training has completed	N/A

2.2.2.28 VS Training Status 2

Short Name:tr_sts2

Address:0x18251

Table 208 • **VS Training Status 2**

Bit	Name	Access	Description	Default
2	cp_range_err	R/O	CP range error (LH)	N/A
1	c0_range_err	R/O	C0 range error (LH)	N/A
0	cm_range_err	R/O	CM range error (LH)	N/A

2.2.3 Vendor Specific Tap Value

2.2.3.1 VS Tap CM Value

Short Name:tr_cmval

Address:0x18254

Table 209 • **VS Tap CM Value**

Bit	Name	Access	Description	Default
6:0	cm_val	R/O	CM value	0x00

2.2.3.2 VS Tap C0 Value

Short Name:tr_c0val

Address:0x18255

Table 210 • **VS Tap C0 Value**

Bit	Name	Access	Description	Default
6:0	c0_val	R/O	C0 value	0x00

2.2.3.3 VS Tap CP Value

Short Name:tr_cpval

Address:0x18256

Table 211 • **VS Tap CP value**

Bit	Name	Access	Description	Default
6:0	cp_val	R/O	CP value	0x00

2.2.4 Vendor Specific Counters

2.2.4.1 VS Training frames_sent LSW

Short Name:frsent_lsw

Address:0x18260

Table 212 • **VS Training frames_sent LSW**

Bit	Name	Access	Description	Default
15:0	frsent_lsw	R/O	Number of training frames sent to complete training.	N/A

2.2.4.2 VS Training frames_sent LSW

Short Name:frsent_msw

Address:0x18261

Table 213 • **VS Training frames_sent MSW**

Bit	Name	Access	Description	Default
15:0	frsent_msw	R/O	Number of training frames sent to complete training.	N/A

2.2.4.3 VS Training lut_read LSW

Short Name:lut_lsw

Address:0x18270

Table 214 • **VS Training lut_read LSW**

Bit	Name	Access	Description	Default
15:0	lut_lsw	R/O	Measured value of selected LUT.	0x0000

2.2.4.4 VS Training lut_read MSW

Short Name:lut_msw

Address:0x18271

Table 215 • **VS Training lut_read MSW**

Bit	Name	Access	Description	Default
15:0	lut_msw	R/O	Measured value of selected LUT.	0x0000

2.2.4.5 VS Training PRBS11 error_count

Short Name:tr_errcnt

Address:0x18272

Table 216 • **VS Training PRBS11 error_count**

Bit	Name	Access	Description	Default
15:0	errcnt	R/O	bit error count of prbs11 checker	0x0000

2.3 SFP_TWS (Device 0x1)

Table 217 • **I2C_BUS_STAT**

Address	Short Description	Register Name	Details
0x1C003	I2C Bus Status	I2C_BUS_STATUS	Page 68

Table 218 • **I2C_READ_ADDRESS**

Address	Short Description	Register Name	Details
0x1C004	I2C Read Address	I2C_READ_ADDR	Page 68

Table 219 • **I2C_READ_STATUS_AND_DATA**

Address	Short Description	Register Name	Details
0x1C005	I2C Read Status And Data	I2C_READ_STATUS_DATA	Page 69

Table 220 • **I2C_RESET_SEQUENCE**

Address	Short Description	Register Name	Details
0x1C006	I2C Reset Sequence	I2C_RESET_SEQ	Page 69

2.3.1 I2C Master Interface for SFP Modules

2.3.1.1 I2C Slave ID

Short Name:SLAVE_ID

Address:0x1C000

I2C Slave ID

Table 221 • **I2C Slave ID**

Bit	Name	Access	Description	Default
6:0	SLAVE_ID	R/W	I2C Slave ID	0x50

2.3.1.2 I2C Prescale (I2C Speed)

Short Name:PRESACLE

Address:0x1C001

I2C Prescale (I2C Speed)

Table 222 • **I2C Prescale (I2C Speed)**

Bit	Name	Access	Description	Default
15:0	PRESCALE	R/W	SCL Frequency = 156.25 MHz/5*(Prescale+1). 0 to 0x4C are invalid settings.	0x004D

2.3.1.3 I2C Write Control

Short Name:I2C_WRITE_CTRL

Address:0x1C002

I2C Write Control Register

Table 223 • **I2C Write Control**

Bit	Name	Access	Description	Default
15:8	WRITE_DATA	R/W	I2C Write Data. A write to I2C_WRITE_CTRL register will trigger I2C master to write the value in WRITE_DATA register to address specified in WRITE_ADDR register of slave ID specified in SLAVE_ID register	0x00
7:0	WRITE_ADDR	R/W	I2C Write Address. A write to I2C_WRITE_CTRL register will trigger I2C master to write the value in WRITE_DATA register to address specified in WRITE_ADDR register of slave ID specified in SLAVE_ID register	0x00

2.3.1.4 I2C Bus Status

Short Name:I2C_BUS_STATUS

Address:0x1C003

I2C Bus Status

Table 224 • **I2C Bus Status**

Bit	Name	Access	Description	Default
1	I2C_WRITE_ACK	R/O	I2C Write Acknowledge 0: Idle 1: Write Acknowledge	0x0
0	I2C_BUS_BUSY	R/O	I2C Bus Busy 0: I2C bus is not busy 1: I2C bus is busy	0x0

2.3.1.5 I2C Read Address

Short Name:I2C_READ_ADDR

Address:0x1C004

I2C Read Address Register

Table 225 • **I2C Read Address**

Bit	Name	Access	Description	Default
7:0	READ_ADDR	R/W	I2C Read Address. A write to READ_ADDR register will trigger I2C master to read the value from the address specified in READ_ADDR register of slave ID specified in SLAVE_ID register, and stores the value at READ_DATA register	0x00

2.3.1.6 I2C Read Status And Data

Short Name:I2C_READ_STATUS_DATA

Address:0x1C005

I2C Read Status And Data

Table 226 • **I2C Read Status And Data**

Bit	Name	Access	Description	Default
15	I2C_BUS_BUSY	R/O	I2C Bus Busy 0: I2C bus is not busy, data updated 1: I2C bus is busy, data not updated	0x0
7:0	READ_DATA	R/O	I2C Read Data. A write to READ_ADDR register will trigger I2C master to read the value from the address specified in READ_ADDR register of slave ID specified in SLAVE_ID register, and stores the value at READ_DATA register	0x00

2.3.1.7 I2C Reset Sequence

Short Name:I2C_RESET_SEQ

Address:0x1C006

I2C Reset Sequence

Table 227 • **I2C Reset Sequence**

Bit	Name	Access	Description	Default
0	RESET_SEQ	R/W	I2C Reset Sequence. A write to RESET_SEQ register (any value) will trigger I2C master to issue a Reset Sequence.	0x0

2.4 GPIO_INTR_CTRL (Device 0x1)

Table 228 • **GPIO_INTR**

Address	Short Description	Register Name	Details
0x1C010	GPIO Output Selection 0	GPIO0_OUT	Page 70
0x1C011	GPIO Output Selection 1	GPIO1_OUT	Page 71
0x1C012	GPIO Output Selection 2	GPIO2_OUT	Page 73
0x1C013	GPIO Output Selection 3	GPIO3_OUT	Page 75

Table 228 • **GPIO_INTR *(continued)***

Address	Short Description	Register Name	Details
0x1C014	GPIO Output Selection 4	GPIO4_OUT	Page 77
0x1C015	GPIO Output Selection 5	GPIO5_OUT	Page 79
0x1C016	GPIO Output Selection 6	GPIO6_OUT	Page 81
0x1C017	GPIO Output Selection 7	GPIO7_OUT	Page 83
0x1C018 - 0x1C019	Interrupt	INTR	Page 85
0x1C01A - 0x1C01B	Interrupt Status	INTR_STAT	Page 87

2.4.1 GPIO Configuration

2.4.1.1 GPIO Output Selection 0

Short Name:GPIO0_OUT

Address:0x1C010

Selects which internal signal is routed to the corresponding output line

Table 229 • **GPIO Output Selection**

Bit	Name	Access	Description	Default
5:0	SEL0	R/W	Selects which internal signal is routed to the corresponding output line 0 = i2c_mstr_module_dataout_o 1 = i2c_mstr_module_clkout_o 2 = led_tx_o 3 = led_rx_o 4 = rxalarm_o 5 = txalarm_o 6 = host_link_up_o 7 = line_link_up_o 8 = line_kr_sync8b10b_2gpio 9 = line_kr_sync10g_2gpio 10 = rosi_frm_pulse_o 11 = rosi_sdat_o 12 = rosi_sclk_o 13 = tosi_frm_pulse_o 14 = tosi_sclk_o 15 = line_pcs1g_link_status 16 = line_pcs_rx_status_o 17 = client_pcs1g_link_status 18 = host_pcs_rx_status 19 = host_sd10g_ib_signal_detect_i 20 = line_sd10g_ib_signal_detect_i 21 = hpcs10g_intr 22 = lpcs10g_intr 23 = client_pcs1g_intr 24 = line_pcs1g_intr 25 = wis_interrupt0 26 = host_pmaint_intr 27 = line_pmaint_intr 28 = data_activity_tx 29 = data_activity_rx 30 = host_data_activity_tx	0x00

Table 229 • **GPIO Output Selection *(continued)***

Bit	Name	Access	Description	Default
5:0	SEL0	R/W	*(continued)* Selects which internal signal is routed to the corresponding output line 31 = host_data_activity_rx 32 = xgmii_pause_egr_bist_exp4_o 33 = xgmii_pause_igr_bist_exp4_o 34 = rx_pcs_pause_o 35 = tx_pcs_pause_o 36 = rx_wis_pause_o 37 = tx_wis_pause_o 38 = eth_channel_dis_o 39 = msec_ip1588_sfd_lane_o 40 = line_s_tx_fault 41 = (eth_1g_ena ? line_pcs1g_ass_latency_o[0] : ewis_fr_bitpos_o[0]); 42 = (eth_1g_ena ? line_pcs1g_ass_latency_o[1] : ewis_fr_bitpos_o[1]); 43 = (eth_1g_ena ? line_pcs1g_char_pos_o[0] : ewis_fr_bitpos_o[2]); 44 = (eth_1g_ena ? line_pcs1g_char_pos_o[1] : ewis_fr_wordpos_o[0]); 45 = (eth_1g_ena ? line_pcs1g_char_pos_o[2] : ewis_fr_wordpos_o[1]); 46 = (eth_1g_ena ? line_pcs1g_char_pos_o[3] : ewis_fr_wordpos_o[2]); 47 = macsec_igr_pred_var_lat_o[0] 48 = macsec_igr_pred_var_lat_o[1] 49 = kr_active_2gpio 50 = dft_tx_ena_2gpio 51 = reserved 52 = exe_last_2gpio[0] 53 = exe_last_2gpio[1] 54 = exe_last_2gpio[2] 55 = exe_last_2gpio[3] 56 = exe_last_2gpio[4] 57 = link_hcd_2gpio[0] 58 = link_hcd_2gpio[1] 59 = link_hcd_2gpio[2] 60 = eth_1g_ena 61 = host_kr_sync8b10b_2gpio 62 = host_kr_sync10g_2gpio 63 = host_kr_active_2gpio	0x00

2.4.1.2 GPIO Output Selection 1

Short Name:GPIO1_OUT

Address:0x1C011

Selects which internal signal is routed to the corresponding output line

Table 230 • **GPIO Output Selection**

Bit	Name	Access	Description	Default
5:0	SEL1	R/W	Selects which internal signal is routed to the corresponding output line 0 = i2c_mstr_module_dataout_o 1 = i2c_mstr_module_clkout_o 2 = led_tx_o 3 = led_rx_o 4 = rxalarm_o 5 = txalarm_o 6 = host_link_up_o 7 = line_link_up_o 8 = line_kr_sync8b10b_2gpio 9 = line_kr_sync10g_2gpio 10 = rosi_frm_pulse_o 11 = rosi_sdat_o 12 = rosi_sclk_o 13 = tosi_frm_pulse_o 14 = tosi_sclk_o 15 = line_pcs1g_link_status 16 = line_pcs_rx_status_o 17 = client_pcs1g_link_status 18 = host_pcs_rx_status 19 = host_sd10g_ib_signal_detect_i 20 = line_sd10g_ib_signal_detect_i 21 = hpcs10g_intr 22 = lpcs10g_intr 23 = client_pcs1g_intr 24 = line_pcs1g_intr 25 = wis_interrupt0 26 = host_pmaint_intr 27 = line_pmaint_intr 28 = data_activity_tx 29 = data_activity_rx 30 = host_data_activity_tx	0x01

Table 230 • **GPIO Output Selection *(continued)***

Bit	Name	Access	Description	Default
5:0	SEL1	R/W	*(continued)* Selects which internal signal is routed to the corresponding output line 31 = host_data_activity_rx 32 = xgmii_pause_egr_bist_exp4_o 33 = xgmii_pause_igr_bist_exp4_o 34 = rx_pcs_pause_o 35 = tx_pcs_pause_o 36 = rx_wis_pause_o 37 = tx_wis_pause_o 38 = eth_channel_dis_o 39 = msec_ip1588_sfd_lane_o 40 = line_s_tx_fault 41 = (eth_1g_ena ? line_pcs1g_ass_latency_o[0] : ewis_fr_bitpos_o[0]); 42 = (eth_1g_ena ? line_pcs1g_ass_latency_o[1] : ewis_fr_bitpos_o[1]); 43 = (eth_1g_ena ? line_pcs1g_char_pos_o[0] : ewis_fr_bitpos_o[2]); 44 = (eth_1g_ena ? line_pcs1g_char_pos_o[1] : ewis_fr_wordpos_o[0]); 45 = (eth_1g_ena ? line_pcs1g_char_pos_o[2] : ewis_fr_wordpos_o[1]); 46 = (eth_1g_ena ? line_pcs1g_char_pos_o[3] : ewis_fr_wordpos_o[2]); 47 = macsec_igr_pred_var_lat_o[0] 48 = macsec_igr_pred_var_lat_o[1] 49 = kr_active_2gpio 50 = dft_tx_ena_2gpio 51 = reserved 52 = exe_last_2gpio[0] 53 = exe_last_2gpio[1] 54 = exe_last_2gpio[2] 55 = exe_last_2gpio[3] 56 = exe_last_2gpio[4] 57 = link_hcd_2gpio[0]	0x01

2.4.1.3 GPIO Output Selection 2

Short Name:GPIO2_OUT

Address:0x1C012

Selects which internal signal is routed to the corresponding output line

Table 231 • **GPIO Output Selection**

Bit	Name	Access	Description	Default
5:0	SEL2	R/W	Selects which internal signal is routed to the corresponding output line 0 = i2c_mstr_module_dataout_o 1 = i2c_mstr_module_clkout_o 2 = led_tx_o 3 = led_rx_o 4 = rxalarm_o 5 = txalarm_o 6 = host_link_up_o 7 = line_link_up_o 8 = line_kr_sync8b10b_2gpio 9 = line_kr_sync10g_2gpio 10 = rosi_frm_pulse_o 11 = rosi_sdat_o 12 = rosi_sclk_o 13 = tosi_frm_pulse_o 14 = tosi_sclk_o 15 = line_pcs1g_link_status 16 = line_pcs_rx_status_o 17 = client_pcs1g_link_status 18 = host_pcs_rx_status 19 = host_sd10g_ib_signal_detect_i 20 = line_sd10g_ib_signal_detect_i 21 = hpcs10g_intr 22 = lpcs10g_intr 23 = client_pcs1g_intr 24 = line_pcs1g_intr 25 = wis_interrupt0 26 = host_pmaint_intr 27 = line_pmaint_intr 28 = data_activity_tx 29 = data_activity_rx 30 = host_data_activity_tx	0x02

Table 231 • **GPIO Output Selection *(continued)***

Bit	Name	Access	Description	Default
5:0	SEL2	R/W	*(continued)* Selects which internal signal is routed to the corresponding output line 31 = host_data_activity_rx 32 = xgmii_pause_egr_bist_exp4_o 33 = xgmii_pause_igr_bist_exp4_o 34 = rx_pcs_pause_o 35 = tx_pcs_pause_o 36 = rx_wis_pause_o 37 = tx_wis_pause_o 38 = eth_channel_dis_o 39 = msec_ip1588_sfd_lane_o 40 = line_s_tx_fault 41 = (eth_1g_ena ? line_pcs1g_ass_latency_o[0] : ewis_fr_bitpos_o[0]); 42 = (eth_1g_ena ? line_pcs1g_ass_latency_o[1] : ewis_fr_bitpos_o[1]); 43 = (eth_1g_ena ? line_pcs1g_char_pos_o[0] : ewis_fr_bitpos_o[2]); 44 = (eth_1g_ena ? line_pcs1g_char_pos_o[1] : ewis_fr_wordpos_o[0]); 45 = (eth_1g_ena ? line_pcs1g_char_pos_o[2] : ewis_fr_wordpos_o[1]); 46 = (eth_1g_ena ? line_pcs1g_char_pos_o[3] : ewis_fr_wordpos_o[2]); 47 = macsec_igr_pred_var_lat_o[0] 48 = macsec_igr_pred_var_lat_o[1] 49 = kr_active_2gpio 50 = dft_tx_ena_2gpio 51 = reserved 52 = exe_last_2gpio[0] 53 = exe_last_2gpio[1] 54 = exe_last_2gpio[2] 55 = exe_last_2gpio[3] 56 = exe_last_2gpio[4] 57 = link_hcd_2gpio[0]	0x02

2.4.1.4 GPIO Output Selection 3

Short Name:GPIO3_OUT

Address:0x1C013

Selects which internal signal is routed to the corresponding output line

Table 232 • **GPIO Output Selection**

Bit	Name	Access	Description	Default
5:0	SEL3	R/W	Selects which internal signal is routed to the corresponding output line 0 = i2c_mstr_module_dataout_o 1 = i2c_mstr_module_clkout_o 2 = led_tx_o 3 = led_rx_o 4 = rxalarm_o 5 = txalarm_o 6 = host_link_up_o 7 = line_link_up_o 8 = line_kr_sync8b10b_2gpio 9 = line_kr_sync10g_2gpio 10 = rosi_frm_pulse_o 11 = rosi_sdat_o 12 = rosi_sclk_o 13 = tosi_frm_pulse_o 14 = tosi_sclk_o 15 = line_pcs1g_link_status 16 = line_pcs_rx_status_o 17 = client_pcs1g_link_status 18 = host_pcs_rx_status 19 = host_sd10g_ib_signal_detect_i 20 = line_sd10g_ib_signal_detect_i 21 = hpcs10g_intr 22 = lpcs10g_intr 23 = client_pcs1g_intr 24 = line_pcs1g_intr 25 = wis_interrupt0 26 = host_pmaint_intr 27 = line_pmaint_intr 28 = data_activity_tx 29 = data_activity_rx 30 = host_data_activity_tx	0x03

Table 232 • **GPIO Output Selection *(continued)***

Bit	Name	Access	Description	Default
5:0	SEL3	R/W	*(continued)* Selects which internal signal is routed to the corresponding output line 31 = host_data_activity_rx 32 = xgmii_pause_egr_bist_exp4_o 33 = xgmii_pause_igr_bist_exp4_o 34 = rx_pcs_pause_o 35 = tx_pcs_pause_o 36 = rx_wis_pause_o 37 = tx_wis_pause_o 38 = eth_channel_dis_o 39 = msec_ip1588_sfd_lane_o 40 = line_s_tx_fault 41 = (eth_1g_ena ? line_pcs1g_ass_latency_o[0] : ewis_fr_bitpos_o[0]); 42 = (eth_1g_ena ? line_pcs1g_ass_latency_o[1] : ewis_fr_bitpos_o[1]); 43 = (eth_1g_ena ? line_pcs1g_char_pos_o[0] : ewis_fr_bitpos_o[2]); 44 = (eth_1g_ena ? line_pcs1g_char_pos_o[1] : ewis_fr_wordpos_o[0]); 45 = (eth_1g_ena ? line_pcs1g_char_pos_o[2] : ewis_fr_wordpos_o[1]); 46 = (eth_1g_ena ? line_pcs1g_char_pos_o[3] : ewis_fr_wordpos_o[2]); 47 = macsec_igr_pred_var_lat_o[0] 48 = macsec_igr_pred_var_lat_o[1] 49 = kr_active_2gpio 50 = dft_tx_ena_2gpio 51 = reserved 52 = exe_last_2gpio[0] 53 = exe_last_2gpio[1] 54 = exe_last_2gpio[2] 55 = exe_last_2gpio[3] 56 = exe_last_2gpio[4] 57 = link_hcd_2gpio[0]	0x03

2.4.1.5 GPIO Output Selection 4

Short Name:GPIO4_OUT

Address:0x1C014

Selects which internal signal is routed to the corresponding output line

Table 233 • **GPIO Output Selection**

Bit	Name	Access	Description	Default
5:0	SEL4	R/W	Selects which internal signal is routed to the corresponding output line 0 = i2c_mstr_module_dataout_o 1 = i2c_mstr_module_clkout_o 2 = led_tx_o 3 = led_rx_o 4 = rxalarm_o 5 = txalarm_o 6 = host_link_up_o 7 = line_link_up_o 8 = line_kr_sync8b10b_2gpio 9 = line_kr_sync10g_2gpio 10 = rosi_frm_pulse_o 11 = rosi_sdat_o 12 = rosi_sclk_o 13 = tosi_frm_pulse_o 14 = tosi_sclk_o 15 = line_pcs1g_link_status 16 = line_pcs_rx_status_o 17 = client_pcs1g_link_status 18 = host_pcs_rx_status 19 = host_sd10g_ib_signal_detect_i 20 = line_sd10g_ib_signal_detect_i 21 = hpcs10g_intr 22 = lpcs10g_intr 23 = client_pcs1g_intr 24 = line_pcs1g_intr 25 = wis_interrupt0 26 = host_pmaint_intr 27 = line_pmaint_intr 28 = data_activity_tx 29 = data_activity_rx 30 = host_data_activity_tx	0x06

Table 233 • **GPIO Output Selection *(continued)***

Bit	Name	Access	Description	Default
5:0	SEL4	R/W	*(continued)* Selects which internal signal is routed to the corresponding output line 31 = host_data_activity_rx 32 = xgmii_pause_egr_bist_exp4_o 33 = xgmii_pause_igr_bist_exp4_o 34 = rx_pcs_pause_o 35 = tx_pcs_pause_o 36 = rx_wis_pause_o 37 = tx_wis_pause_o 38 = eth_channel_dis_o 39 = msec_ip1588_sfd_lane_o 40 = line_s_tx_fault 41 = (eth_1g_ena ? line_pcs1g_ass_latency_o[0] : ewis_fr_bitpos_o[0]); 42 = (eth_1g_ena ? line_pcs1g_ass_latency_o[1] : ewis_fr_bitpos_o[1]); 43 = (eth_1g_ena ? line_pcs1g_char_pos_o[0] : ewis_fr_bitpos_o[2]); 44 = (eth_1g_ena ? line_pcs1g_char_pos_o[1] : ewis_fr_wordpos_o[0]); 45 = (eth_1g_ena ? line_pcs1g_char_pos_o[2] : ewis_fr_wordpos_o[1]); 46 = (eth_1g_ena ? line_pcs1g_char_pos_o[3] : ewis_fr_wordpos_o[2]); 47 = macsec_igr_pred_var_lat_o[0] 48 = macsec_igr_pred_var_lat_o[1] 49 = kr_active_2gpio 50 = dft_tx_ena_2gpio 51 = reserved 52 = exe_last_2gpio[0] 53 = exe_last_2gpio[1] 54 = exe_last_2gpio[2] 55 = exe_last_2gpio[3] 56 = exe_last_2gpio[4] 57 = link_hcd_2gpio[0]	0x06

2.4.1.6 GPIO Output Selection 5

Short Name:GPIO5_OUT

Address:0x1C015

Selects which internal signal is routed to the corresponding output line

Table 234 • **GPIO Output Selection**

Bit	Name	Access	Description	Default
5:0	SEL5	R/W	Selects which internal signal is routed to the corresponding output line 0 = i2c_mstr_module_dataout_o 1 = i2c_mstr_module_clkout_o 2 = led_tx_o 3 = led_rx_o 4 = rxalarm_o 5 = txalarm_o 6 = host_link_up_o 7 = line_link_up_o 8 = line_kr_sync8b10b_2gpio 9 = line_kr_sync10g_2gpio 10 = rosi_frm_pulse_o 11 = rosi_sdat_o 12 = rosi_sclk_o 13 = tosi_frm_pulse_o 14 = tosi_sclk_o 15 = line_pcs1g_link_status 16 = line_pcs_rx_status_o 17 = client_pcs1g_link_status 18 = host_pcs_rx_status 19 = host_sd10g_ib_signal_detect_i 20 = line_sd10g_ib_signal_detect_i 21 = hpcs10g_intr 22 = lpcs10g_intr 23 = client_pcs1g_intr 24 = line_pcs1g_intr 25 = wis_interrupt0 26 = host_pmaint_intr 27 = line_pmaint_intr 28 = data_activity_tx 29 = data_activity_rx 30 = host_data_activity_tx	0x07

Table 234 • **GPIO Output Selection *(continued)***

Bit	Name	Access	Description	Default
5:0	SEL5	R/W	*(continued)* Selects which internal signal is routed to the corresponding output line 31 = host_data_activity_rx 32 = xgmii_pause_egr_bist_exp4_o 33 = xgmii_pause_igr_bist_exp4_o 34 = rx_pcs_pause_o 35 = tx_pcs_pause_o 36 = rx_wis_pause_o 37 = tx_wis_pause_o 38 = eth_channel_dis_o 39 = msec_ip1588_sfd_lane_o 40 = line_s_tx_fault 41 = (eth_1g_ena ? line_pcs1g_ass_latency_o[0] : ewis_fr_bitpos_o[0]); 42 = (eth_1g_ena ? line_pcs1g_ass_latency_o[1] : ewis_fr_bitpos_o[1]); 43 = (eth_1g_ena ? line_pcs1g_char_pos_o[0] : ewis_fr_bitpos_o[2]); 44 = (eth_1g_ena ? line_pcs1g_char_pos_o[1] : ewis_fr_wordpos_o[0]); 45 = (eth_1g_ena ? line_pcs1g_char_pos_o[2] : ewis_fr_wordpos_o[1]); 46 = (eth_1g_ena ? line_pcs1g_char_pos_o[3] : ewis_fr_wordpos_o[2]); 47 = macsec_igr_pred_var_lat_o[0] 48 = macsec_igr_pred_var_lat_o[1] 49 = kr_active_2gpio 50 = dft_tx_ena_2gpio 51 = reserved 52 = exe_last_2gpio[0] 53 = exe_last_2gpio[1] 54 = exe_last_2gpio[2] 55 = exe_last_2gpio[3] 56 = exe_last_2gpio[4] 57 = link_hcd_2gpio[0]	0x07

2.4.1.7 GPIO Output Selection 6

Short Name:GPIO6_OUT

Address:0x1C016

Selects which internal signal is routed to the corresponding output line

Table 235 • **GPIO Output Selection**

Bit	Name	Access	Description	Default
5:0	SEL6	R/W	Selects which internal signal is routed to the corresponding output line 0 = i2c_mstr_module_dataout_o 1 = i2c_mstr_module_clkout_o 2 = led_tx_o 3 = led_rx_o 4 = rxalarm_o 5 = txalarm_o 6 = host_link_up_o 7 = line_link_up_o 8 = line_kr_sync8b10b_2gpio 9 = line_kr_sync10g_2gpio 10 = rosi_frm_pulse_o 11 = rosi_sdat_o 12 = rosi_sclk_o 13 = tosi_frm_pulse_o 14 = tosi_sclk_o 15 = line_pcs1g_link_status 16 = line_pcs_rx_status_o 17 = client_pcs1g_link_status 18 = host_pcs_rx_status 19 = host_sd10g_ib_signal_detect_i 20 = line_sd10g_ib_signal_detect_i 21 = hpcs10g_intr 22 = lpcs10g_intr 23 = client_pcs1g_intr 24 = line_pcs1g_intr 25 = wis_interrupt0 26 = host_pmaint_intr 27 = line_pmaint_intr 28 = data_activity_tx 29 = data_activity_rx 30 = host_data_activity_tx	0x13

Table 235 • **GPIO Output Selection *(continued)***

Bit	Name	Access	Description	Default
5:0	SEL6	R/W	*(continued)* Selects which internal signal is routed to the corresponding output line 31 = host_data_activity_rx 32 = xgmii_pause_egr_bist_exp4_o 33 = xgmii_pause_igr_bist_exp4_o 34 = rx_pcs_pause_o 35 = tx_pcs_pause_o 36 = rx_wis_pause_o 37 = tx_wis_pause_o 38 = eth_channel_dis_o 39 = msec_ip1588_sfd_lane_o 40 = line_s_tx_fault 41 = (eth_1g_ena ? line_pcs1g_ass_latency_o[0] : ewis_fr_bitpos_o[0]); 42 = (eth_1g_ena ? line_pcs1g_ass_latency_o[1] : ewis_fr_bitpos_o[1]); 43 = (eth_1g_ena ? line_pcs1g_char_pos_o[0] : ewis_fr_bitpos_o[2]); 44 = (eth_1g_ena ? line_pcs1g_char_pos_o[1] : ewis_fr_wordpos_o[0]); 45 = (eth_1g_ena ? line_pcs1g_char_pos_o[2] : ewis_fr_wordpos_o[1]); 46 = (eth_1g_ena ? line_pcs1g_char_pos_o[3] : ewis_fr_wordpos_o[2]); 47 = macsec_igr_pred_var_lat_o[0] 48 = macsec_igr_pred_var_lat_o[1] 49 = kr_active_2gpio 50 = dft_tx_ena_2gpio 51 = reserved 52 = exe_last_2gpio[0] 53 = exe_last_2gpio[1] 54 = exe_last_2gpio[2] 55 = exe_last_2gpio[3] 56 = exe_last_2gpio[4] 57 = link_hcd_2gpio[0]	0x13

2.4.1.8 GPIO Output Selection 7

Short Name:GPIO7_OUT

Address:0x1C017

Selects which internal signal is routed to the corresponding output line

Table 236 • **GPIO Output Selection**

Bit	Name	Access	Description	Default
5:0	SEL7	R/W	Selects which internal signal is routed to the corresponding output line 0 = i2c_mstr_module_dataout_o 1 = i2c_mstr_module_clkout_o 2 = led_tx_o 3 = led_rx_o 4 = rxalarm_o 5 = txalarm_o 6 = host_link_up_o 7 = line_link_up_o 8 = line_kr_sync8b10b_2gpio 9 = line_kr_sync10g_2gpio 10 = rosi_frm_pulse_o 11 = rosi_sdat_o 12 = rosi_sclk_o 13 = tosi_frm_pulse_o 14 = tosi_sclk_o 15 = line_pcs1g_link_status 16 = line_pcs_rx_status_o 17 = client_pcs1g_link_status 18 = host_pcs_rx_status 19 = host_sd10g_ib_signal_detect_i 20 = line_sd10g_ib_signal_detect_i 21 = hpcs10g_intr 22 = lpcs10g_intr 23 = client_pcs1g_intr 24 = line_pcs1g_intr 25 = wis_interrupt0 26 = host_pmaint_intr 27 = line_pmaint_intr 28 = data_activity_tx 29 = data_activity_rx 30 = host_data_activity_tx	0x14

Table 236 • **GPIO Output Selection *(continued)***

Bit	Name	Access	Description	Default
5:0	SEL7	R/W	*(continued)* Selects which internal signal is routed to the corresponding output line 31 = host_data_activity_rx 32 = xgmii_pause_egr_bist_exp4_o 33 = xgmii_pause_igr_bist_exp4_o 34 = rx_pcs_pause_o 35 = tx_pcs_pause_o 36 = rx_wis_pause_o 37 = tx_wis_pause_o 38 = eth_channel_dis_o 39 = msec_ip1588_sfd_lane_o 40 = line_s_tx_fault 41 = (eth_1g_ena ? line_pcs1g_ass_latency_o[0] : ewis_fr_bitpos_o[0]); 42 = (eth_1g_ena ? line_pcs1g_ass_latency_o[1] : ewis_fr_bitpos_o[1]); 43 = (eth_1g_ena ? line_pcs1g_char_pos_o[0] : ewis_fr_bitpos_o[2]); 44 = (eth_1g_ena ? line_pcs1g_char_pos_o[1] : ewis_fr_wordpos_o[0]); 45 = (eth_1g_ena ? line_pcs1g_char_pos_o[2] : ewis_fr_wordpos_o[1]); 46 = (eth_1g_ena ? line_pcs1g_char_pos_o[3] : ewis_fr_wordpos_o[2]); 47 = macsec_igr_pred_var_lat_o[0] 48 = macsec_igr_pred_var_lat_o[1] 49 = kr_active_2gpio 50 = dft_tx_ena_2gpio 51 = reserved 52 = exe_last_2gpio[0] 53 = exe_last_2gpio[1] 54 = exe_last_2gpio[2] 55 = exe_last_2gpio[3] 56 = exe_last_2gpio[4] 57 = link_hcd_2gpio[0]	0x14

2.4.1.9 Interrupt

Short Name:INTR

Addresses:0x1C018 - 0x1C019

Table 237 • **Interrupt**

Bit	Name	Access	Description	Default
15	HPMA_INTR_EN	R/W	Host PMA interrupt interrupt enable. Enables Host PMA interrupt to propagate to corresponding channel interrupt 0 = Host PMA interrupt will not affect the corresponding channel interrupt 1 = Host PMA interrupt will propagate to the corresponding channel interrupt	0x1
14	LPMA_INTR_EN	R/W	Line PMA interrupt interrupt enable. Enables Line PMA interrupt to propagate to corresponding channel interrupt 0 = Line PMA interrupt will not affect the corresponding channel interrupt 1 = Line PMA interrupt will propagate to the corresponding channel interrupt	0x1

Table 237 • **Interrupt *(continued)***

Bit	Name	Access	Description	Default
13	HEGR_FIFO_INTR_EN	R/W	Host Egress FIFO interrupt interrupt enable. Enables Host Egress FIFO interrupt to propagate to corresponding channel interrupt 0 = Host Egress FIFO interrupt will not affect the corresponding channel interrupt 1 = Host Egress FIFO interrupt will propagate to the corresponding channel interrupt	0x1
12	LEGR_FIFO_INTR_EN	R/W	Line Egress FIFO interrupt interrupt enable. Enables Line Egress FIFO interrupt to propagate to corresponding channel interrupt 0 = Line Egress FIFO interrupt will not affect the corresponding channel interrupt 1 = Line Egress FIFO interrupt will propagate to the corresponding channel interrupt	0x1
11	LIGR_FIFO_INTR_EN	R/W	Line Ingress FIFO interrupt interrupt enable. Enables Line Ingress FIFO interrupt to propagate to corresponding channel interrupt 0 = Line Ingress FIFO interrupt will not affect the corresponding channel interrupt 1 = Line Ingress FIFO interrupt will propagate to the corresponding channel interrupt	0x1
10	FCBUF_INTR_EN	R/W	Flow Control Buffer interrupt interrupt enable. Enables Flow Control Buffer interrupt to propagate to corresponding channel interrupt 0 = Flow Control Buffer interrupt will not affect the corresponding channel interrupt 1 = Flow Control Buffer interrupt will propagate to the corresponding channel interrupt	0x1
9	HMAC_INTR_EN	R/W	Host MAC interrupt interrupt enable. Enables Host MAC interrupt to propagate to corresponding channel interrupt 0 = Host MAC interrupt will not affect the corresponding channel interrupt 1 = Host MAC interrupt will propagate to the corresponding channel interrupt	0x1
8	LMAC_INTR_EN	R/W	Line MAC interrupt interrupt enable. Enables Line MAC interrupt to propagate to corresponding channel interrupt 0 = Line MAC interrupt will not affect the corresponding channel interrupt 1 = Line MAC interrupt will propagate to the corresponding channel interrupt	0x1
7	MSEC_IGR_INTR_EN	R/W	MACSEC Ingress interrupt interrupt enable. Enables MACSEC Ingress interrupt to propagate to corresponding channel interrupt 0 = MACSEC Ingress interrupt will not affect the corresponding channel interrupt 1 = MACSEC Ingress interrupt will propagate to the corresponding channel interrupt	0x1

Table 237 • **Interrupt *(continued)***

Bit	Name	Access	Description	Default
6	MSEC_EGR_INTR_EN	R/W	MACSEC Egress interrupt interrupt enable. Enables MACSEC Egress interrupt to propagate to corresponding channel interrupt 0 = MACSEC Egress interrupt will not affect the corresponding channel interrupt 1 = MACSEC Egress interrupt will propagate to the corresponding channel interrupt	0x1
5	HPCS1G_INTR_EN	R/W	Host PCS1G interrupt interrupt enable. Enables Host PCS1G interrupt to propagate to corresponding channel interrupt 0 = Host PCS1G interrupt will not affect the corresponding channel interrupt 1 = Host PCS1G interrupt will propagate to the corresponding channel interrupt	0x1
4	LPCS1G_INTR_EN	R/W	Line PCS1G interrupt interrupt enable. Enables Line PCS1G interrupt to propagate to corresponding channel interrupt 0 = Line PCS1G interrupt will not affect the corresponding channel interrupt 1 = Line PCS1G interrupt will propagate to the corresponding channel interrupt	0x1
3	HPCS10G_INTR_EN	R/W	Host PCS10G interrupt interrupt enable. Enables Host PCS10G interrupt to propagate to corresponding channel interrupt 0 = Host PCS10G interrupt will not affect the corresponding channel interrupt 1 = Host PCS10G interrupt will propagate to the corresponding channel interrupt	0x1
2	LPCS10G_INTR_EN	R/W	Line PCS10G interrupt interrupt enable. Enables Line PCS10G interrupt to propagate to corresponding channel interrupt 0 = Line PCS10G interrupt will not affect the corresponding channel interrupt 1 = Line PCS10G interrupt will propagate to the corresponding channel interrupt	0x1
1	WIS1_INTR_EN	R/W	WIS 2nd interrupt interrupt enable. Enables WIS 2nd interrupt to propagate to corresponding channel interrupt 0 = WIS 2nd interrupt will not affect the corresponding channel interrupt 1 = WIS 2nd interrupt will propagate to the corresponding channel interrupt	0x1
0	WIS0_INTR_EN	R/W	WIS first interrupt interrupt enable. Enables WIS first interrupt to propagate to corresponding channel interrupt 0 = WIS first interrupt will not affect the corresponding channel interrupt 1 = WIS first interrupt will propagate to the corresponding channel interrupt	0x1

2.4.1.10 Interrupt Status

Short Name:INTR_STAT

Addresses:0x1C01A - 0x1C01B

Table 238 • **Interrupt Status**

Bit	Name	Access	Description	Default
15	HPMA_INTR_STAT	R/O	Host PMA interrupt status. Indicates Host PMA interrupt is pending or is masked. 0 = Host PMA interrupt not pending or corresponding INTR_EN is cleared 1 = Host PMA interrupt pending and corresponding INTR_EN is set	0x0
14	LPMA_INTR_STAT	R/O	Line PMA interrupt status. Indicates Line PMA interrupt is pending or is masked 0 = Line PMA interrupt not pending or corresponding INTR_EN is cleared 1 = Line PMA interrupt pending and corresponding INTR_EN is set	0x0
13	HEGR_FIFO_INTR_STAT	R/O	Host Egress FIFO interrupt status. Indicates Host Egress FIFO interrupt is pending or is masked 0 = Host Egress FIFO interrupt not pending or corresponding INTR_EN is cleared 1 = Host Egress FIFO interrupt pending and corresponding INTR_EN is set	0x0
12	LEGR_FIFO_INTR_STAT	R/O	Line Egress interrupt status. Indicates Line Egress interrupt is pending or is masked 0 = Line Egress interrupt not pending or corresponding INTR_EN is cleared 1 = Line Egress interrupt pending and corresponding INTR_EN is set	0x0
11	LIGR_FIFO_INTR_STAT	R/O	Line Ingress interrupt status. Indicates Line Ingress interrupt is pending or is masked 0 = Line Ingress interrupt not pending or corresponding INTR_EN is cleared 1 = Line Ingress interrupt pending and corresponding INTR_EN is set	0x0
10	FCBUF_INTR_STAT	R/O	Flow Control Buffer interrupt status. Indicates Flow Control Buffer interrupt is pending or is masked 0 = Flow Control Buffer interrupt not pending or corresponding INTR_EN is cleared 1 = Flow Control Buffer interrupt pending and corresponding INTR_EN is set	0x0
9	HMAC_INTR_STAT	R/O	Host MAC interrupt status. Indicates Host MAC interrupt is pending or is masked 0 = Host MAC interrupt not pending or corresponding INTR_EN is cleared 1 = Host MAC interrupt pending and corresponding INTR_EN is set	0x0
8	LMAC_INTR_STAT	R/O	Line MAC interrupt status. Indicates Line MAC interrupt is pending or is masked 0 = Line MAC interrupt not pending or corresponding INTR_EN is cleared 1 = Line MAC interrupt pending and corresponding INTR_EN is set	0x0

Table 238 • (continued) **Interrupt Status**

Bit	Name	Access	Description	Default
7	MSEC_IGR_INTR_STAT	R/O	MACSEC Ingress interrupt status. Indicates MACSEC Ingress interrupt is pending or is masked 0 = MACSEC Ingress interrupt not pending or corresponding INTR_EN is cleared 1 = MACSEC Ingress interrupt pending and corresponding INTR_EN is set	0x0
6	MSEC_EGR_INTR_STAT	R/O	MACSEC Egress interrupt status. Indicates MACSEC Egress interrupt is pending or is masked 0 = MACSEC Egress interrupt not pending or corresponding INTR_EN is cleared 1 = MACSEC Egress interrupt pending and corresponding INTR_EN is set	0x0
5	HPCS1G_INTR_STAT	R/O	Host PCS1G interrupt status. Indicates Host PCS1G interrupt is pending or is masked 0 = Host PCS1G interrupt not pending or corresponding INTR_EN is cleared 1 = Host PCS1G interrupt pending and corresponding INTR_EN is set	0x0
4	LPCS1G_INTR_STAT	R/O	Line PCS1G interrupt status. Indicates Line PCS1G interrupt is pending or is masked 0 = Line PCS1G interrupt not pending or corresponding INTR_EN is cleared 1 = Line PCS1G interrupt pending and corresponding INTR_EN is set	0x0
3	HPCS10G_INTR_STAT	R/O	Host PCS10G interrupt status. Indicates Host PCS10G interrupt is pending or is masked 0 = Host PCS10G interrupt not pending or corresponding INTR_EN is cleared 1 = Host PCS10G interrupt pending and corresponding INTR_EN is set	0x0
2	LPCS10G_INTR_STAT	R/O	Line PCS10G interrupt status. Indicates Line PCS10G interrupt is pending or is masked 0 = Line PCS10G interrupt not pending or corresponding INTR_EN is cleared 1 = Line PCS10G interrupt pending and corresponding INTR_EN is set	0x0
1	WIS1_INTR_STAT	R/O	2nd WIS interrupt status. Indicates 2nd WIS interrupt is pending or is masked 0 = 2nd WIS interrupt not pending or corresponding INTR_EN is cleared 1 = 2nd WIS interrupt pending and corresponding INTR_EN is set	0x0
0	WIS0_INTR_STAT	R/O	1st WIS interrupt status. Indicates 1st WIS interrupt is pending or is masked 0 = 1st WIS interrupt not pending or corresponding INTR_EN is cleared 1 = 1st WIS interrupt pending and corresponding INTR_EN is set	0x0

2.5 LINE_PMA_32BIT (Device 0x1)

Table 239 • **SD10G65_APC**

Address	Short Description	Register Name	Details
0x1F000	APC Top Control Configuration	APC_TOP_CTRL_CFG	Page 93
0x1F001	APC Common Configuration 0	APC_COMMON_CFG0	Page 93
0x1F002	APC Parameter Control Synchronization	APC_PARCTRL_SYNC_CFG	Page 95
0x1F003	APC parctrl FSM1 Timer Config	APC_PARCTRL_FSM1_TIMER_CFG	Page 96
0x1F004	APC parctrl FSM2 Timer Config	APC_PARCTRL_FSM2_TIMER_CFG	Page 97
0x1F005	APC FLEXCTRL Read Counter	APC_FLEXCTRL_CNT_STATUS	Page 97
0x1F006	APC Level Detect Calibration Configuration	APC_LD_CAL_CFG	Page 97
0x1F007	APC Sampling Stage Calibration Configuration 0	APC_IS_CAL_CFG0	Page 98
0x1F008	APC Sampling Stage Calibration Configuration 1	APC_IS_CAL_CFG1	Page 98
0x1F009	APC EQZ CTRL Config	APC_EQZ_COMMON_CFG	Page 99
0x1F00A	APC EQZ CTRL Configuration	APC_EQZ_GAIN_CTRL_CFG	Page 100
0x1F00B	APC EQZ ADJ CTRL Configuration	APC_EQZ_GAIN_ADJ_CTRL_CFG	Page 100
0x1F00C	APC EQZ CTRL Status	APC_EQZ_CTRL_STATUS	Page 101
0x1F00D	APC EQZ LD Control	APC_EQZ_LD_CTRL	Page 101
0x1F00E	APC EQZ LD CTRL Config0	APC_EQZ_LD_CTRL_CFG0	Page 102
0x1F00F	APC EQZ LD CTRL Config1	APC_EQZ_LD_CTRL_CFG1	Page 102
0x1F010	APC EQZ Pattern Matching Cfg 0	APC_EQZ_PAT_MATCH_CFG0	Page 102
0x1F011	APC EQZ Pattern Matching Cfg 1	APC_EQZ_PAT_MATCH_CFG1	Page 103
0x1F012	APC EQZ_OFFS Control	APC_EQZ_OFFS_CTRL	Page 103
0x1F013	APC EQZ_OFFS Timer Config	APC_EQZ_OFFS_TIMER_CFG	Page 104
0x1F014	APC EQZ_OFFS Parameter Control	APC_EQZ_OFFS_PAR_CFG	Page 104
0x1F015	APC EQZ_C Control	APC_EQZ_C_CTRL	Page 105
0x1F016	APC EQZ_C Timer Config	APC_EQZ_C_TIMER_CFG	Page 106
0x1F017	APC EQZ_C Parameter Control	APC_EQZ_C_PAR_CFG	Page 106
0x1F018	APC EQZ_L Control	APC_EQZ_L_CTRL	Page 107
0x1F019	APC EQZ_L Timer Config	APC_EQZ_L_TIMER_CFG	Page 108
0x1F01A	APC EQZ_L Parameter Control	APC_EQZ_L_PAR_CFG	Page 108
0x1F01B	APC EQZ_AGC Control	APC_EQZ_AGC_CTRL	Page 109
0x1F01C	APC EQZ_AGC Timer Config	APC_EQZ_AGC_TIMER_CFG	Page 110
0x1F01D	APC EQZ_AGC Parameter Control	APC_EQZ_AGC_PAR_CFG	Page 110
0x1F01E	APC DFE1 Control	APC_DFE1_CTRL	Page 111
0x1F01F	APC DFE1 Timer Config	APC_DFE1_TIMER_CFG	Page 112
0x1F020	APC DFE1 Parameter Control	APC_DFE1_PAR_CFG	Page 112

Table 239 • **SD10G65_APC *(continued)***

Address	Short Description	Register Name	Details
0x1F021	APC DFE2 Control	APC_DFE2_CTRL	Page 113
0x1F022	APC DFE2 Timer Config	APC_DFE2_TIMER_CFG	Page 114
0x1F023	APC DFE2 Parameter Control	APC_DFE2_PAR_CFG	Page 114
0x1F024	APC DFE3 Control	APC_DFE3_CTRL	Page 115
0x1F025	APC DFE3 Timer Config	APC_DFE3_TIMER_CFG	Page 116
0x1F026	APC DFE3 Parameter Control	APC_DFE3_PAR_CFG	Page 116
0x1F027	APC DFE4 Control	APC_DFE4_CTRL	Page 117
0x1F028	APC DFE4 Timer Config	APC_DFE4_TIMER_CFG	Page 118
0x1F029	APC DFE4 Parameter Control	APC_DFE4_PAR_CFG	Page 118
0x1F02A	APC LC softcontrol Configuration	APC_LC_SOFTCTRL_CFG	Page 119

Table 240 • **SD10G65_DES**

Address	Short Description	Register Name	Details
0x1F100	SD10G65 DES Configuration 0	SD10G65_DES_CFG0	Page 120
0x1F101	SD10G65 MOEBDIV Configuration 0	SD10G65_MOEBDIV_CFG0	Page 121

Table 241 • **SD10G65_OB**

Address	Short Description	Register Name	Details
0x1F110	SD10G65 OB Configuration 0	SD10G65_OB_CFG0	Page 121
0x1F111	SD10G65 OB Configuration 1	SD10G65_OB_CFG1	Page 122
0x1F112	SD10G65 OB Configuration 2	SD10G65_OB_CFG2	Page 123
0x1F113	SD10G65 OB Configuration 3	SD10G65_OB_CFG3	Page 124

Table 242 • **SD10G65_IB**

Address	Short Description	Register Name	Details
0x1F120	SD10G65 IB Configuration 0	SD10G65_IB_CFG0	Page 124
0x1F121	SD10G65 IB Configuration 1	SD10G65_IB_CFG1	Page 126
0x1F122	SD10G65 IB Configuration 2	SD10G65_IB_CFG2	Page 127
0x1F123	SD10G65 IB Configuration 3	SD10G65_IB_CFG3	Page 127
0x1F124	SD10G65 IB Configuration 4	SD10G65_IB_CFG4	Page 129
0x1F125	SD10G65 IB Configuration 5	SD10G65_IB_CFG5	Page 130
0x1F126	SD10G65 IB Configuration 6	SD10G65_IB_CFG6	Page 132
0x1F127	SD10G65 IB Configuration 7	SD10G65_IB_CFG7	Page 132
0x1F128	SD10G65 IB Configuration 8	SD10G65_IB_CFG8	Page 133
0x1F129	SD10G65 IB Configuration 9	SD10G65_IB_CFG9	Page 133

Table 242 • **SD10G65_IB *(continued)***

Address	Short Description	Register Name	Details
0x1F12A	SD10G65 IB Configuration 10 JTAG Related Setting	SD10G65_IB_CFG10	Page 134
0x1F12B	SD10G65 IB Configuration 11 JTAG Related Setting	SD10G65_IB_CFG11	Page 135
0x1F12C	SD10G65 SBUS Rx CFG Service-Bus Related Setting	SD10G65_SBUS_RX_CFG	Page 135

Table 243 • **SD10G65_RX_RCPLL**

Address	Short Description	Register Name	Details
0x1F130	SD10G65 Rx RCPLL Configuration 0	SD10G65_RX_RCPLL_CFG0	Page 136
0x1F131	SD10G65 Rx RCPLL Configuration 1	SD10G65_RX_RCPLL_CFG1	Page 137
0x1F132	SD10G65 Rx RCPLL Configuration 2	SD10G65_RX_RCPLL_CFG2	Page 137
0x1F133	SD10G65 Rx RCPLL Status 0	SD10G65_RX_RCPLL_STAT0	Page 138

Table 244 • **SD10G65_RX_SYNTH**

Address	Short Description	Register Name	Details
0x1F140	SD10G65 Rx Synthesizer Configuration 0	SD10G65_RX_SYNTH_CFG0	Page 138
0x1F141	SD10G65 Rx Synthesizer Configuration 1	SD10G65_RX_SYNTH_CFG1	Page 139
0x1F142	SD10G65 Rx Synthesizer Configuration 2	SD10G65_RX_SYNTH_CFG2	Page 139
0x1F143	SD10G65 Rx Synthesizer Configuration 3	SD10G65_RX_SYNTH_CFG3	Page 140
0x1F144	SD10G65 Rx Synthesizer Configuration 4	SD10G65_RX_SYNTH_CFG4	Page 140
0x1F145	SD10G65 Rx Synthesizer CDR Loopfilter Control	SD10G65_RX_SYNTH_CDRLF	Page 140
0x1F146	SD10G65 Rx Synthesizer 0 for Qualifier Access	SD10G65_RX_SYNTH_QUALIFIER0	Page 141
0x1F147	SD10G65 Rx Synthesizer 1 for Qualifier Access	SD10G65_RX_SYNTH_QUALIFIER1	Page 141
0x1F148	SD10G65 Rx Synthesizer for Sync Control Data	SD10G65_RX_SYNTH_SYNC_CTRL	Page 142
0x1F149	F2DF Configuration / status	F2DF_CFG_STAT	Page 142

Table 245 • **SD10G65_TX_SYNTH**

Address	Short Description	Register Name	Details
0x1F150	SD10G65 Tx Synthesizer Configuration 0	SD10G65_TX_SYNTH_CFG0	Page 143
0x1F151	SD10G65 Tx Synthesizer Configuration 1	SD10G65_TX_SYNTH_CFG1	Page 143
0x1F152	SD10G65 Tx Synthesizer Configuration 3	SD10G65_TX_SYNTH_CFG3	Page 143
0x1F153	SD10G65 Tx Synthesizer Configuration 4	SD10G65_TX_SYNTH_CFG4	Page 144
0x1F154	SD10G65 SSC Generator Configuration 0	SD10G65_SSC_CFG0	Page 144
0x1F155	SD10G65 SSC Generator Configuration 1	SD10G65_SSC_CFG1	Page 144

Table 246 • **SD10G65_TX_RCPLL**

Address	Short Description	Register Name	Details
0x1F160	SD10G65 Tx RCPLL Configuration 0	SD10G65_TX_RCPLL_CFG0	Page 145
0x1F161	SD10G65 Tx RCPLL Configuration 1	SD10G65_TX_RCPLL_CFG1	Page 145
0x1F162	SD10G65 Tx RCPLL Configuration 2	SD10G65_TX_RCPLL_CFG2	Page 145
0x1F163	SD10G65 Tx RCPLL Status 0	SD10G65_TX_RCPLL_STAT0	Page 146

2.5.1 SD10G65 APC Configuration and Status

Configuration and status register set for SD10G65 APC

2.5.1.1 APC Top Control Configuration

Short Name:APC_TOP_CTRL_CFG

Address:0x1F000

Configuration register for top control logic

Table 247 • **APC Top Control Configuration**

Bit	Name	Access	Description	Default
31:24	PWR_UP_TIME	R/W	Delay time required to power up auxiliary channels	0x0F
23:16	PWR_DN_TIME	R/W	Delay time required to power down auxiliary channels	0x05
15:0	SLEEP_TIME	R/W	APC top-control sleep-time (power-down). Given in number of clock cycles (typically 2.5 ... 5 ns)	0xC350

2.5.1.2 APC Common Configuration 0

Short Name:APC_COMMON_CFG0

Address:0x1F001

Common configurations 0 for APC logic. Note: For HML error correction logic HML=000/001/011/111 are considered valid, 010 and 101 are considered correctable (010 correctable to 011; 101 correctable to 001) and 100 and 110 are considered uncorrectable.

Table 248 • **APC Common Configuration 0**

Bit	Name	Access	Description	Default
31	HML_CLR_CNT	R/W	Clear HML sampling error counter 1: Clear counter	0x0
30	HML_ERRCORR_MODE	R/W	HML sampling error correction mode. Correctable sampling errors can be automatically corrected. 0: Disable auto-correction 1: Enable auto-correction	0x1
29	HML_ERRCORR_ENA	R/W	HML sampling error correction enable. Invalid samples are not used for parameter control (smart sampling). 0: Disable smart sampling 1: Enable smart sampling	0x0

Table 248 • **APC Common Configuration 0** ***(continued)***

Bit	Name	Access	Description	Default
28	HML_SWAP_HL	R/W	H/L swapping in HML sampling error correction logic 0: No H/L swapping 1: H/L swapped	0x1
27:26	APC_FSM_RECOVER_MODE	R/W	Top-ctrl FSM recovery behavior 0: No auto-recovery 1: Auto-restart on missing input signal after Restart-Delay-Timer has expired 2: Auto-restart on missing input signal	0x0
25	SIG_DET_VALID_CFG	R/W	Signal detect valid configuration (Offs/AGC/L/C/DFE) 0: Signal_detect input directly used 1: Signal_detect input gated with gain_ctrl ramp-up done (EQZ_GAIN_CTRL_DONE)	0x0
24:20	SIG_LOST_DELAY_TIME	R/W	Signal lost delay timer configuration used for APC recovery. The signal lost delay time specifies the time when a missing input signal is considered a lost input signal on sig_det = 0. The delay time is T = (2^sig_lost_delay_time) * T_rx_clk_per	0x14
19:16	TOP_CTRL_STATE	R/O	Current state of APC top control state machine 0: Off 1: Power-up 2: Power-down 3: Manual mode 4: Calibrate IS 5: Calibrate LD 6: Not used 7: Gain-control ramp-up 8: Mission mode (FSM1 controlled) 9: Mission mode (FSM2 controlled) 10-12: Debug states 13: Snooze 14-15: Not used	0x0
15:12	BLOCK_READ_SEL	R/W	Select flexctrl block in order to read internal counters. Counter values readable from APC_FLEXCTRL_CNT_STATUS. 0: Offset-ctrl 1: L-ctrl 2: C-ctrl 3: AGC-ctrl 4: DFE1-ctrl 5: DFE2-ctrl 6: DFE3-ctrl 7: DFE4-ctrl 8: SAM_Offset-cal 9: Level-cal 10: HML sampling errors	0x0
11	RESET_APC	R/W	Reset APC core logic (configuration registers are not reset) 1: Reset APC 0: Normal operation (mission mode)	0x0

Table 248 • **APC Common Configuration 0 *(continued)***

Bit	Name	Access	Description	Default
10	FREEZE_APC	R/W	Freeze current state 0: Normal operation 1: Freeze APC	0x0
8:6	IF_WIDTH	R/W	Interface bit-width 0: 8-bit 1: 10-bit 2: 16-bit 3: 20-bit 4: 32-bit 5: 40-bit	0x4
5	RESERVED	R/W	Must be set to its default.	0x1
4	THROTTLE_MODE	R/W	APC throttling mode 0: Disable, no power reduction (continuous operation) 1: Enable, power reduced operation (pulsed operation)	0x0
3	APC_DIRECT_ENA	R/W	Enable APC direct connections instead of local IB configuration registers.	0x0
2:0	APC_MODE	R/W	APC operation mode 0: Off 1: Manual mode 2: Perform calibrarion and run FSM1 3: Perform calibration and run FSM2 4: Perform calibration and run FSM1 and FSM2 in ping-pong operation 5: Perform calibration and then enter manual mode	0x0

2.5.1.3 APC Parameter Control Synchronization

Short Name:APC_PARCTRL_SYNC_CFG

Address:0x1F002

Configuration register for common flexible parameter control FSMs

Table 249 • **APC Parameter Control Synchronization**

Bit	Name	Access	Description	Default
31:28	RESERVED	R/W	Must be set to its default.	0x3
15	FSM2_CTRL_MODE	R/W	Parameter control mode for FSM2 0: Discrete 1: Continuous	0x1
14	FSM1_CTRL_MODE	R/W	Parameter control mode for FSM1 0: Discrete 1: Continuous	0x1

Table 249 • **APC Parameter Control Synchronization**

Bit	Name	Access	Description	Default
13:11	FSM2_RECOVER_MODE	R/W	FSM2 recovery behavior 0: No auto-recovery 1: Freeze FSM2 on weak (eqz_gain > eqz_gain_freeze_thres) or missing input signal 2: Freeze FSM2 on weak signal and restart on missing input signal 3: Freeze FSM2 on missing input signal 4: Freeze FSM2 on missing input signal and auto-restart after Restart-Delay-Timer has expired 5: Auto-restart FSM2 on missing input signal 6-7: Reserved	0x0
10:8	FSM1_RECOVER_MODE	R/W	FSM1 recovery behavior 0: No auto-recovery 1: Freeze FSM1 on weak (eqz_gain > eqz_gain_freeze_thres) or missing input signal 2: Freeze FSM1 on weak signal and restart on missing input signal 3: Freeze FSM1 on missing input signal 4: Freeze FSM1 on missing input signal and auto-restart after Restart-Delay-Timer has expired 5: Auto-restart FSM1 on missing input signal 6-7: Reserved	0x0
7	FSM2_CTRL_DONE	R/O	Parameter control state of FSM2 in one-time mode 1: finished	0x0
6	FSM2_START_CTRL	R/W	Start operation of FSM2 (parameter update). Should be cleared afterwards in One-time mode and stay set in Non-stop and Paused mode	0x0
5:4	FSM2_OP_MODE	R/W	Operation mode of FSM2 0: Off 1: One-time 2: Non-stop 3: Paused	0x0
3	FSM1_CTRL_DONE	R/O	Parameter control state of FSM1 in one-time mode 1: finished	0x0
2	FSM1_START_CTRL	R/W	Start operation of FSM1 (parameter update). Should be cleared afterwards in One-time mode and stay set in Non-stop and Paused mode	0x0
1:0	FSM1_OP_MODE	R/W	Operation mode of FSM1 0: Off 1: One-time 2: Non-stop 3: Paused	0x0

2.5.1.4 APC parctrl FSM1 Timer Config

Short Name:APC_PARCTRL_FSM1_TIMER_CFG

Address:0x1F003

Timing configuration register for common flexible parameter control FSM1

Table 250 • **APC parctrl FSM1 Timer Config**

Bit	Name	Access	Description	Default
31:16	FSM1_PS_TIME	R/W	FSM1 Pause time (in number of rx_clk cycles)	0x0064
15:0	FSM1_OP_TIME	R/W	FSM1 Operation time (in number of rx_clk cycles)	0x03E8

2.5.1.5 APC parctrl FSM2 Timer Config

Short Name:APC_PARCTRL_FSM2_TIMER_CFG

Address:0x1F004

Timing configuration register for common flexible parameter control FSM2

Table 251 • **APC parctrl FSM2 Timer Config**

Bit	Name	Access	Description	Default
31:16	FSM2_PS_TIME	R/W	FSM2 Pause time (in number of rx_clk cycles)	0x0064
15:0	FSM2_OP_TIME	R/W	FSM2 Operation time (in number of rx_clk cycles)	0x03E8

2.5.1.6 APC FLEXCTRL Read Counter

Short Name:APC_FLEXCTRL_CNT_STATUS

Address:0x1F005

Observation register for multiple counters. The selection is done via APC_COMMON_CFG.BLOCK_READ_SEL (select flexctrl block to be read) and APC_XXX_CTRL.XXX_READ_CNT_SEL (counter within flexctrl block XXX) or APC_COMMON_CFG.OFFSCAL_READ_CNT_SEL. Note that the EQZ and DFE counters hit_cnt and err_cnt make only sense in DISCRETE control mode.

Table 252 • **APC FLEXCTRL Read Counter**

Bit	Name	Access	Description	Default
31:0	APC_CTRL_CNTVAL	R/O	Current counter value	0x00000000

2.5.1.7 APC Level Detect Calibration Configuration

Short Name:APC_LD_CAL_CFG

Address:0x1F006

Configuration register for APC level detect calibrations logic

Table 253 • **APC Level Detect Calibration Configuration**

Bit	Name	Access	Description	Default
30:28	CAL_CLK_DIV	R/W	Calibration clock divider. Clock used in calibration blocks is divided by 2^(2*CAL_CLK_DIV) 0: No clock division 1: Clock is divided by 4 2: Clock is divided by 16 ... 7: Clock is divided by 16384	0x2
19	DETLEV_CAL_DONE	R/O	Detect level calibration state 1: finished	0x0
12	SKIP_SDET_CAL	R/W	Skip signal detect calibration	0x0
11	SKIP_LD_CAL	R/W	Skip level detect calibration	0x0
10:5	IE_SDET_LEVEL	R/W	Level for IE signal detect (when controlled by APC) 0: 20mV	0x02
4:1	DETLVL_TIMER	R/W	Timer for calibration process 14: Use for 400MHz rx_clk	0xE
0	START_DETLVL_CAL	R/W	Start signal and level detect calibration process (sampling stage; only in manual mode, see apc_mode)	0x0

2.5.1.8 APC Sampling Stage Calibration Configuration 0

Short Name:APC_IS_CAL_CFG0

Address:0x1F007

Configuration register 0 for APC sampling stage calibrations logic

Table 254 • **APC Sampling Stage Calibration Configuration 0**

Bit	Name	Access	Description	Default
25:20	IB_DFE_GAIN_ADJ	R/W	Gain adjustment for DFE amplifier	0x24
19:14	CPMD_THRES_INIT	R/W	Initial value for CP/MD FF threshold calibration.	0x00
13:8	VSC_THRES_INIT	R/W	Initial value for VScope FF threshold calibration.	0x00
7	SKIP_OBSERVE_INIT	R/W	Skip observe block initialization	0x0
6	SKIP_OFFSET_INIT	R/W	Skip sample FF offset initialization	0x0
5	SKIP_THRESHOLD_INIT	R/W	Skip sample FF threshold initialization	0x0
4	SKIP_DFE_BUFFER_INIT	R/W	Skip DFE buffer 0db initialization	0x0
3	SKIP_OBSERVE_CAL	R/W	Skip observe block calibration	0x0
2	SKIP_OFFSET_CAL	R/W	Skip sample FF offset calibration	0x0
1	SKIP_THRESHOLD_CAL	R/W	Skip sample FF threshold calibration	0x0
0	SKIP_DFE_BUFFER_CAL	R/W	Skip DFE buffer 0db calibration	0x0

2.5.1.9 APC Sampling Stage Calibration Configuration 1

Short Name:APC_IS_CAL_CFG1

Address:0x1F008

Configuration register 1 for APC sampling stage calibrations logic

Table 255 • **APC Sampling Stage Calibration Configuration 1**

Bit	Name	Access	Description	Default
31:24	EQZ_AGC_DAC_VAL	R/W	AGC-DAC value used for DFE 0dB calibration during IB-calibration process	0x58
23	USE_AGC_DAC_VAL	R/W	Enable use of EQZ_AGC_DAC_VAL instead of EQZ_AGC_INI during DFE 0dB IB calibration	0x0
19:16	CAL_NUM_ITERATIONS	R/W	Controls number of calibrations iterations to settle values that depend on each other (offset vs threshold). Coding number of iterations = cal_num_iterations + 1.	0xF
13:9	PAR_DATA_NUM_ONES_THRES	R/W	Selects the number of ones threshold when using parallel data. Value for rising ramp from zero to one. The value for the falling ramp (one -> zero) is half the interface width minus par_data_num_ones_thres.	0x10
8	PAR_DATA_SEL	R/W	Controls whether the parallel data from the deserializer or the signal from the observe multiplexer in the sample stage is used. Coding: 0: observe multiplexer, 1: parallel data.	0x1
7:3	OFFSCAL_READ_CNT_SEL	R/W	Select offset calibration result to be read (BLOCK_READ_SEL = 8 required)	0x00
2	OFFSCAL_DIS_SWAP	R/W	Swaps disp with disn used during calibration	0x0
1	OFFSCAL_DONE	R/O	Offset calibration state 1: finished	0x0
0	START_OFFSCAL	R/W	Start offset calibration process (sampling stage; only in manual mode, see apc_mode)	0x0

2.5.1.10 APC EQZ CTRL Config

Short Name:APC_EQZ_COMMON_CFG

Address:0x1F009

Configuration register for gain control logic

Table 256 • **APC EQZ CTRL Config**

Bit	Name	Access	Description	Default
22:13	EQZ_GAIN_FREEZE_THRES	R/W	Gain freeze threshold, used in APC recovery mode for low input signals	0x37A
12:11	EQZ_GAIN_RECOVER_MODE	R/W	Gain recovery behavior 0: No auto-recovery 1: Freeze gain on missing input signal and auto-restart after Restart-Delay-Timer has expired 2: Auto-restart Gain control on missing input signal 3: Reserved	0x0
10	EQZ_GAIN_ADJ_HALT	R/W	Stop update of gain_adj	0x0

Table 256 • **APC EQZ CTRL Config *(continued)***

Bit	Name	Access	Description	Default
9	EQZ_GAIN_CAL_MODE	R/W	Gain calibration mode 0: Use successive approximation to find required gain 1: use max gain and reduce linearly to find required gain	0x0
8	EQZ_GAIN_ADJ_START_UPDATE	R/W	Start (initiate) gain_adj update process (on rising edge of cfg bit)	0x0
7	EQZ_GAIN_START_UPDATE	R/W	Start (initiate) gain update process (on rising edge of cfg bit)	0x0
6	EQZ_GAIN_START_CTRL	R/W	(Re-)start (initiate) main gain/gain_adj calibration process (on rising edge of cfg bit)	0x0
5:4	EQZ_GAIN_OP_MODE	R/W	Operation mode (only when EQZ_GAIN_STOP_CTRL = 1) 0: Idle 1: Calibrate and work 2: Work	0x0
3	EQZ_GAIN_STOP_CTRL	R/W	Stop main gain control machine immediately	0x0
2	EQZ_GAIN_AUTO_RESTART	R/W	Restart gain/gain_adj calibration automatically on rising edge of signal_detect	0x1
1:0	EQZ_GAIN_CHG_MODE	R/W	Parameter change mode 0: Automatic update 1: Preset (use PAR_INI as fix value internal processing continues) 2: Freeze (internal processing stops parameter stays at current value) 3: No update (internal processing continues but parameter is not updated)	0x0

2.5.1.11 APC EQZ CTRL Configuration

Short Name:APC_EQZ_GAIN_CTRL_CFG

Address:0x1F00A

Configuration register for gain

Table 257 • **APC EQZ CTRL Configuration**

Bit	Name	Access	Description	Default
29:20	EQZ_GAIN_MAX	R/W	Maximum gain in normal operation (should be not greater then 895 (512+3*128-1)	0x37F
19:10	EQZ_GAIN_MIN	R/W	Minimum gain in normal operation	0x000
9:0	EQZ_GAIN_INI	R/W	Gain initial value (used if EQZ_GAIN_CHG_MODE = 1)	0x000

2.5.1.12 APC EQZ ADJ CTRL Configuration

Short Name:APC_EQZ_GAIN_ADJ_CTRL_CFG

Address:0x1F00B

Configuration register for gain_adj

Table 258 • **APC EQZ ADJ CTRL Configuration**

Bit	Name	Access	Description	Default
26:20	EQZ_GAIN_ADJ_MAX	R/W	Maximum gain_adj in normal operation	0x7F
16:10	EQZ_GAIN_ADJ_MIN	R/W	Minimum gain_adj in normal operation	0x00
6:0	EQZ_GAIN_ADJ_INI	R/W	Gain_adj initial value (used if EQZ_GAIN_CHG_MODE = 1)	0x00

2.5.1.13 APC EQZ CTRL Status

Short Name:APC_EQZ_CTRL_STATUS

Address:0x1F00C

Observation register for controlled settings

Table 259 • **APC EQZ CTRL Status**

Bit	Name	Access	Description	Default
23	EQZ_GAIN_CTRL_DONE	R/O	Status flag indicating main gain/gain_adj ramp-up process has finished	0x0
22:16	EQZ_GAIN_ADJ_ACTVAL	R/O	Parameter value (controlled/computed gain adjustment value)	0x00
15:6	EQZ_GAIN_ACTVAL	R/O	Parameter value (controlled/computed gain value)	0x000
5:0	LD_LEV_ACTVAL	R/O	Parameter value (controlled/computed level for level-detect logic)	0x00

2.5.1.14 APC EQZ LD Control

Short Name:APC_EQZ_LD_CTRL

Address:0x1F00D

Configuration register for level-detect (LD) control, timing and behavior (timing: number of rx_clk cycles, used for LD toggling)

Table 260 • **APC EQZ LD Control**

Bit	Name	Access	Description	Default
31	LD_EQ_TOGGLE	R/O	Captured toggling of LD-EQ	0x0
30	LD_IB_TOGGLE	R/O	Captured toggling of LD-IB	0x0
29	LD_CATCH_BYPASS	R/W	Bypass LD catch circuitry (allows capturing pulses shorter then one rx_clk cycle)	0x1
28:26	LD_WD_CNT_MAX	R/W	Max value for LD updates in gain_adjust (watch-dog; prevent endless loop of LD adjustment; max is 2^value - 1)	0x3
25:22	LD_TOG_THRESHOLD	R/W	Number of required toggles before toggling is considered valid	0x2
21:14	LD_T_TOGGLE_DEADTIME	R/W	Sensitivity deadtime between two toggles (value is multiplied by 2)	0x02
8	LD_LEV_UPDATE	R/W	Update internal LD_lev value with LD_LEV_INI	0x0

Table 260 • **APC EQZ LD Control *(continued)***

Bit	Name	Access	Description	Default
7	LD_EQ_START_TOG_CHK	R/W	Start (initiate) a LD-EQ toggle check (for present LD-level)	0x0
6	LD_IB_START_TOG_CHK	R/W	Start (initiate) a LD-IB toggle check (for present LD-level)	0x0
5:0	LD_LEV_INI	R/W	LD_lev initial value (used as preset value if EQZ_GAIN_CHG_MODE = 1)	0x28

2.5.1.15 APC EQZ LD CTRL Config0

Short Name:APC_EQZ_LD_CTRL_CFG0

Address:0x1F00E

Configuration register 0 for level-detect (LD) controller timing (number of rx_clk cycles, used for operation timing). Important note: For small ld_t_* values it might be necessary to change IB configuration bit-group IB_LDSD_DIVSEL to higher values!

Table 261 • **APC EQZ LD CTRL Config0**

Bit	Name	Access	Description	Default
31:16	LD_T_DEADTIME_WRK	R/W	Minimum activity for LD in work mode (value is multiplied by 8)	0x0064
15:0	LD_T_TIMEOUT_WRK	R/W	Activity timeout threshold for LD in work mode (value is multiplied by 8)	0x03E8

2.5.1.16 APC EQZ LD CTRL Config1

Short Name:APC_EQZ_LD_CTRL_CFG1

Address:0x1F00F

Configuration register 1 for level-detect (LD) controller timing (number of rx_clk cycles, used for calibration timing). Important note: For small ld_t_* values it might be necessary to change IB configuration bit-group IB_LDSD_DIVSEL to higher values!

Table 262 • **APC EQZ LD CTRL Config1**

Bit	Name	Access	Description	Default
31:16	LD_T_DEADTIME_CAL	R/W	Minimum activity for LD in calibration mode (value is multiplied by 8)	0x0064
15:0	LD_T_TIMEOUT_CAL	R/W	Activity timeout threshold for LD in calibration mode (value is multiplied by 8)	0x03E8

2.5.1.17 APC EQZ Pattern Matching Cfg 0

Short Name:APC_EQZ_PAT_MATCH_CFG0

Address:0x1F010

Pattern matching configuration register for eqz_c and eqz_l control

Table 263 • **APC EQZ Pattern Matching Cfg 0**

Bit	Name	Access	Description	Default
31:24	EQZ_C_PAT_MASK	R/W	EQZ-C-control pattern mask (only those bits are used for pattern matching whose mask bit is set)	0x00

Table 263 • **APC EQZ Pattern Matching Cfg 0 *(continued)***

Bit	Name	Access	Description	Default
23:16	EQZ_C_PAT_MATCH	R/W	EQZ-C-control pattern used for pattern matching (corresponding mask bits must be set)	0x00
15:8	EQZ_L_PAT_MASK	R/W	EQZ-L-control pattern mask (only those bits are used for pattern matching whose mask bit is set)	0x00
7:0	EQZ_L_PAT_MATCH	R/W	EQZ-L-control pattern used for pattern matching (corresponding mask bits must be set)	0x00

2.5.1.18 APC EQZ Pattern Matching Cfg 1

Short Name:APC_EQZ_PAT_MATCH_CFG1

Address:0x1F011

Pattern matching configuration register for eqz_offs and eqz_agc control Note, if mask is set to 0, all bits are "matching" and taken into account for parameter control.

Table 264 • **APC EQZ Pattern Matching Cfg 1**

Bit	Name	Access	Description	Default
31:24	EQZ_OFFS_PAT_MASK	R/W	EQZ-Offset-control pattern mask (only those bits are used for pattern matching whose mask bit is set)	0x00
23:16	EQZ_OFFS_PAT_MATCH	R/W	EQZ-Offset-control pattern used for pattern matching (corresponding mask bits must be set)	0x00
15:8	EQZ_AGC_PAT_MASK	R/W	EQZ-AGC-control pattern mask (only those bits are used for pattern matching whose mask bit is set)	0x00
7:0	EQZ_AGC_PAT_MATCH	R/W	EQZ-AGC-control pattern used for pattern matching (corresponding mask bits must be set)	0x00

2.5.1.19 APC EQZ_OFFS Control

Short Name:APC_EQZ_OFFS_CTRL

Address:0x1F012

General behavior control for EQZ_OFFS parameter control.

Table 265 • **APC EQZ_OFFS Control**

Bit	Name	Access	Description	Default
29:27	EQZ_OFFS_RECOVER_MODE	R/W	EQZ_OFFS recovery behavior 0: No auto-recovery 1: Freeze EQZ_OFFS on weak (eqz_gain > eqz_gain_freeze_thres) or missing input signal 2: Freeze EQZ_OFFS on weak signal and restart on missing input signal 3: Freeze EQZ_OFFS on missing input signal 4: Freeze EQZ_OFFS on missing input signal and auto-restart after Restart-Delay-Timer has expired 5: Auto-restart EQZ_OFFS on missing input signal 6-7: Reserved	0x0

Table 265 • **APC EQZ_OFFS Control**

Bit	Name	Access	Description	Default
26	EQZ_OFFS_CTRL_DONE	R/O	Parameter control state in one-time mode 1: Finished	0x0
25:16	EQZ_OFFS_ACTVAL	R/O	Parameter value (controlled/computed value)	0x000
15:14	EQZ_OFFS_SYNC_MODE	R/W	Synchronization mode 0: Independent 1: Attached to parctrl FSM 1 2: Attached to parctrl FSM 2 3: Attached to both parctrl FSMs	0x0
13:12	EQZ_OFFS_READ_CNT_SEL	R/W	Select counter to be read 0: eqz_offs_value 1: Hit counter 2: Error counter	0x0
10	EQZ_OFFS_CTRL_MODE	R/W	Parameter control mode for EQZ_OFFS parameter 0: Discrete 1: Continuous	0x1
9:4	EQZ_OFFS_CTRL_THRES	R/W	Alternative threshold for EQZ_OFFS parameter (controller goal: err_cnt = 0.5*EQZ_OFFS_THRES)	0x28
3	EQZ_OFFS_CTRL_THRES_ENA	R/W	Enable use of alternative threshold for EQZ_OFFS parameter 0: Use default threshold 1: Use alternative threshold	0x0
2	EQZ_OFFS_START_CTRL	R/W	Start operation (parameter update). Should be cleared afterwards in One-time mode and stay set in Non-stop and Paused mode	0x0
1:0	EQZ_OFFS_OP_MODE	R/W	Operation mode 0: Off 1: One-time 2: Non-stop 3: Paused	0x0

2.5.1.20 APC EQZ_OFFS Timer Config

Short Name:APC_EQZ_OFFS_TIMER_CFG

Address:0x1F013

Configuration registers for EQZ_OFFS controller timing.

Table 266 • **APC EQZ_OFFS Timer Config**

Bit	Name	Access	Description	Default
31:16	EQZ_OFFS_PS_TIME	R/W	Pause time (in number of rx_clk cycles)	0x0064
15:0	EQZ_OFFS_OP_TIME	R/W	Operation time (in number of rx_clk cycles)	0x03E8

2.5.1.21 APC EQZ_OFFS Parameter Control

Short Name:APC_EQZ_OFFS_PAR_CFG

Address:0x1F014

Configuration register for controlled EQZ_OFFS parameter. Note, for parameters larger than 8 bits, ini/min/max values are shifted to the left. For parameters smaller than 8 bits only the lower bits of ini/min/max are used.

Table 267 • **APC EQZ_OFFS Parameter Control**

Bit	Name	Access	Description	Default
31	EQZ_OFFS_DIR_SEL	R/W	Select parameter update direction 0: Normal 1: Inverted	0x0
30:26	EQZ_OFFS_RANGE_SEL	R/W	Parameter range selection (only when CTRL_MODE = continuous). Value complies to number of left-shifts	0x00
25:24	EQZ_OFFS_CHG_MODE	R/W	Parameter change mode 0: Automatic update 1: Preset (use EQZ_OFFS_INI as fix value internal processing continues) 2: Freeze (internal processing stops parameter stays at current value) 3: No update (internal processing continues but parameter is not updated)	0x0
23:16	EQZ_OFFS_MAX	R/W	Maximum value of parameter	0x00
15:8	EQZ_OFFS_MIN	R/W	Minimum value of parameter	0x00
7:0	EQZ_OFFS_INI	R/W	Parameter initial value	0x00

2.5.1.22 APC EQZ_C Control

Short Name:APC_EQZ_C_CTRL

Address:0x1F015

General behavior control for EQZ_C parameter control.

Table 268 • **APC EQZ_C Control**

Bit	Name	Access	Description	Default
29:27	EQZ_C_RECOVER_MODE	R/W	EQZ_C recovery behavior 0: No auto-recovery 1: Freeze EQZ_C on weak (eqz_gain > eqz_gain_freeze_thres) or missing input signal 2: Freeze EQZ_C on weak signal and restart on missing input signal 3: Freeze EQZ_C on missing input signal 4: Freeze EQZ_C on missing input signal and auto-restart after Restart-Delay-Timer has expired 5: Auto-restart EQZ_C on missing input signal 6-7: Reserved	0x0
26	EQZ_C_CTRL_DONE	R/O	Parameter control state in one-time mode 1: Finished	0x0
25:16	EQZ_C_ACTVAL	R/O	Parameter value (controlled/computed value)	0x000

Table 268 • **APC EQZ_C Control**

Bit	Name	Access	Description	Default
15:14	EQZ_C_SYNC_MODE	R/W	Synchronization mode 0: Independent 1: Attached to parctrl FSM 1 2: Attached to parctrl FSM 2 3: Attached to both parctrl FSMs	0x0
13:12	EQZ_C_READ_CNT_SEL	R/W	Select counter to be read 0: eqz_c_value 1: Hit counter 2: Error counter	0x0
10	EQZ_C_CTRL_MODE	R/W	Parameter control mode for EQZ_C parameter 0: Discrete 1: Continuous	0x1
9:4	EQZ_C_CTRL_THRES	R/W	Alternative threshold for EQZ_C parameter (controller goal: err_cnt = 0.5*EQZ_C_THRES)	0x28
3	EQZ_C_CTRL_THRES_ENA	R/W	Enable use of alternative threshold for EQZ_C parameter 0: Use default threshold 1: Use alternative threshold	0x0
2	EQZ_C_START_CTRL	R/W	Start operation (parameter update). Should be cleared afterwards in One-time mode and stay set in Non-stop and Paused mode	0x0
1:0	EQZ_C_OP_MODE	R/W	Operation mode 0: Off 1: One-time 2: Non-stop 3: Paused	0x0

2.5.1.23 APC EQZ_C Timer Config

Short Name:APC_EQZ_C_TIMER_CFG

Address:0x1F016

Configuration registers for EQZ_C controller timing.

Table 269 • **APC EQZ_C Timer Config**

Bit	Name	Access	Description	Default
31:16	EQZ_C_PS_TIME	R/W	Pause time (in number of rx_clk cycles)	0x0064
15:0	EQZ_C_OP_TIME	R/W	Operation time (in number of rx_clk cycles)	0x03E8

2.5.1.24 APC EQZ_C Parameter Control

Short Name:APC_EQZ_C_PAR_CFG

Address:0x1F017

Configuration register for controlled EQZ_C parameter. Note, for parameters larger than 8 bits, ini/min/max values are shifted to the left. For parameters smaller than 8 bits only the lower bits of ini/min/max are used.

Table 270 • **APC EQZ_C Parameter Control**

Bit	Name	Access	Description	Default
31	EQZ_C_DIR_SEL	R/W	Select parameter update direction 0: Normal 1: Inverted	0x0
30:26	EQZ_C_RANGE_SEL	R/W	Parameter range selection (only when CTRL_MODE = continuous). Value complies to number of left-shifts	0x00
25:24	EQZ_C_CHG_MODE	R/W	Parameter change mode 0: Automatic update 1: Preset (use EQZ_C_INI as fix value internal processing continues) 2: Freeze (internal processing stops parameter stays at current value) 3: No update (internal processing continues but parameter is not updated)	0x0
23:16	EQZ_C_MAX	R/W	Maximum value of parameter	0x00
15:8	EQZ_C_MIN	R/W	Minimum value of parameter	0x00
7:0	EQZ_C_INI	R/W	Parameter initial value	0x00

2.5.1.25 APC EQZ_L Control

Short Name:APC_EQZ_L_CTRL

Address:0x1F018

General behavior control for EQZ_L parameter control.

Table 271 • **APC EQZ_L Control**

Bit	Name	Access	Description	Default
29:27	EQZ_L_RECOVER_MODE	R/W	EQZ_L recovery behavior 0: No auto-recovery 1: Freeze EQZ_L on weak (eqz_gain > eqz_gain_freeze_thres) or missing input signal 2: Freeze EQZ_L on weak signal and restart on missing input signal 3: Freeze EQZ_L on missing input signal 4: Freeze EQZ_L on missing input signal and auto-restart after Restart-Delay-Timer has expired 5: Auto-restart EQZ_L on missing input signal 6-7: Reserved	0x0
26	EQZ_L_CTRL_DONE	R/O	Parameter control state in one-time mode 1: Finished	0x0
25:16	EQZ_L_ACTVAL	R/O	Parameter value (controlled/computed value)	0x000

Table 271 • **APC EQZ_L Control**

Bit	Name	Access	Description	Default
15:14	EQZ_L_SYNC_MODE	R/W	Synchronization mode 0: Independent 1: Attached to parctrl FSM 1 2: Attached to parctrl FSM 2 3: Attached to both parctrl FSMs	0x0
13:12	EQZ_L_READ_CNT_SEL	R/W	Select counter to be read 0: eqz_l_value 1: Hit counter 2: Error counter	0x0
10	EQZ_L_CTRL_MODE	R/W	Parameter control mode for EQZ_L parameter 0: Discrete 1: Continuous	0x1
9:4	EQZ_L_CTRL_THRES	R/W	Alternative threshold for EQZ_L parameter (controller goal: err_cnt = 0.5*EQZ_L_THRES)	0x28
3	EQZ_L_CTRL_THRES_ENA	R/W	Enable use of alternative threshold for EQZ_L parameter 0: Use default threshold 1: Use alternative threshold	0x0
2	EQZ_L_START_CTRL	R/W	Start operation (parameter update). Should be cleared afterwards in One-time mode and stay set in Non-stop and Paused mode	0x0
1:0	EQZ_L_OP_MODE	R/W	Operation mode 0: Off 1: One-time 2: Non-stop 3: Paused	0x0

2.5.1.26 APC EQZ_L Timer Config

Short Name:APC_EQZ_L_TIMER_CFG

Address:0x1F019

Configuration registers for EQZ_L controller timing.

Table 272 • **APC EQZ_L Timer Config**

Bit	Name	Access	Description	Default
31:16	EQZ_L_PS_TIME	R/W	Pause time (in number of rx_clk cycles)	0x0064
15:0	EQZ_L_OP_TIME	R/W	Operation time (in number of rx_clk cycles)	0x03E8

2.5.1.27 APC EQZ_L Parameter Control

Short Name:APC_EQZ_L_PAR_CFG

Address:0x1F01A

Configuration register for controlled EQZ_L parameter. Note, for parameters larger than 8 bits, ini/min/max values are shifted to the left. For parameters smaller than 8 bits only the lower bits of ini/min/max are used.

Table 273 • **APC EQZ_L Parameter Control**

Bit	Name	Access	Description	Default
31	EQZ_L_DIR_SEL	R/W	Select parameter update direction 0: Normal 1: Inverted	0x0
30:26	EQZ_L_RANGE_SEL	R/W	Parameter range selection (only when CTRL_MODE = continuous). Value complies to number of left-shifts	0x00
25:24	EQZ_L_CHG_MODE	R/W	Parameter change mode 0: Automatic update 1: Preset (use EQZ_L_INI as fix value internal processing continues) 2: Freeze (internal processing stops parameter stays at current value) 3: No update (internal processing continues but parameter is not updated)	0x0
23:16	EQZ_L_MAX	R/W	Maximum value of parameter	0x00
15:8	EQZ_L_MIN	R/W	Minimum value of parameter	0x00
7:0	EQZ_L_INI	R/W	Parameter initial value	0x00

2.5.1.28 APC EQZ_AGC Control

Short Name:APC_EQZ_AGC_CTRL

Address:0x1F01B

General behavior control for EQZ_AGC parameter control.

Table 274 • **APC EQZ_AGC Control**

Bit	Name	Access	Description	Default
29:27	EQZ_AGC_RECOVER_MODE	R/W	EQZ_AGC recovery behavior 0: No auto-recovery 1: Freeze EQZ_AGC on weak (eqz_gain > eqz_gain_freeze_thres) or missing input signal 2: Freeze EQZ_AGC on weak signal and restart on missing input signal 3: Freeze EQZ_AGC on missing input signal 4: Freeze EQZ_AGC on missing input signal and auto-restart after Restart-Delay-Timer has expired 5: Auto-restart EQZ_AGC on missing input signal 6-7: Reserved	0x0
26	EQZ_AGC_CTRL_DONE	R/O	Parameter control state in one-time mode 1: Finished	0x0
25:16	EQZ_AGC_ACTVAL	R/O	Parameter value (controlled/computed value)	0x000

Table 274 • **APC EQZ_AGC Control**

Bit	Name	Access	Description	Default
15:14	EQZ_AGC_SYNC_MODE	R/W	Synchronization mode 0: Independent 1: Attached to parctrl FSM 1 2: Attached to parctrl FSM 2 3: Attached to both parctrl FSMs	0x0
13:12	EQZ_AGC_READ_CNT_SEL	R/W	Select counter to be read 0: eqz_agc_value 1: Hit counter 2: Error counter	0x0
10	EQZ_AGC_CTRL_MODE	R/W	Parameter control mode for EQZ_AGC parameter 0: Discrete 1: Continuous	0x1
9:4	EQZ_AGC_CTRL_THRES	R/W	Alternative threshold for EQZ_AGC parameter (controller goal: err_cnt = 0.5*EQZ_AGC_THRES)	0x28
3	EQZ_AGC_CTRL_THRES_ENA	R/W	Enable use of alternative threshold for EQZ_AGC parameter 0: Use default threshold 1: Use alternative threshold	0x0
2	EQZ_AGC_START_CTRL	R/W	Start operation (parameter update). Should be cleared afterwards in One-time mode and stay set in Non-stop and Paused mode	0x0
1:0	EQZ_AGC_OP_MODE	R/W	Operation mode 0: Off 1: One-time 2: Non-stop 3: Paused	0x0

2.5.1.29 APC EQZ_AGC Timer Config

Short Name:APC_EQZ_AGC_TIMER_CFG

Address:0x1F01C

Configuration registers for EQZ_AGC controller timing.

Table 275 • **APC EQZ_AGC Timer Config**

Bit	Name	Access	Description	Default
31:16	EQZ_AGC_PS_TIME	R/W	Pause time (in number of rx_clk cycles)	0x0064
15:0	EQZ_AGC_OP_TIME	R/W	Operation time (in number of rx_clk cycles)	0x03E8

2.5.1.30 APC EQZ_AGC Parameter Control

Short Name:APC_EQZ_AGC_PAR_CFG

Address:0x1F01D

Configuration register for controlled EQZ_AGC parameter. Note, for parameters larger than 8 bits, ini/min/max values are shifted to the left. For parameters smaller than 8 bits only the lower bits of ini/min/max are used.

Table 276 • **APC EQZ_AGC Parameter Control**

Bit	Name	Access	Description	Default
31	EQZ_AGC_DIR_SEL	R/W	Select parameter update direction 0: Normal 1: Inverted	0x0
30:26	EQZ_AGC_RANGE_SEL	R/W	Parameter range selection (only when CTRL_MODE = continuous). Value complies to number of left-shifts	0x00
25:24	EQZ_AGC_CHG_MODE	R/W	Parameter change mode 0: Automatic update 1: Preset (use EQZ_AGC_INI as fix value internal processing continues) 2: Freeze (internal processing stops parameter stays at current value) 3: No update (internal processing continues but parameter is not updated)	0x0
23:16	EQZ_AGC_MAX	R/W	Maximum value of parameter	0x00
15:8	EQZ_AGC_MIN	R/W	Minimum value of parameter	0x00
7:0	EQZ_AGC_INI	R/W	Parameter initial value	0x00

2.5.1.31 APC DFE1 Control

Short Name:APC_DFE1_CTRL

Address:0x1F01E

General behavior control for DFE1 parameter control.

Table 277 • **APC DFE1 Control**

Bit	Name	Access	Description	Default
29:27	DFE1_RECOVER_MODE	R/W	DFE1 recovery behavior 0: No auto-recovery 1: Freeze DFE1 on weak (eqz_gain > eqz_gain_freeze_thres) or missing input signal 2: Freeze DFE1 on weak signal and restart on missing input signal 3: Freeze DFE1 on missing input signal 4: Freeze DFE1 on missing input signal and auto-restart after Restart-Delay-Timer has expired 5: Auto-restart DFE1 on missing input signal 6-7: Reserved	0x0
26	DFE1_CTRL_DONE	R/O	Parameter control state in one-time mode 1: Finished	0x0
25:16	DFE1_ACTVAL	R/O	Parameter value (controlled/computed value)	0x000

Table 277 • **APC DFE1 Control**

Bit	Name	Access	Description	Default
15:14	DFE1_SYNC_MODE	R/W	Synchronization mode 0: Independent 1: Attached to parctrl FSM 1 2: Attached to parctrl FSM 2 3: Attached to both parctrl FSMs	0x0
13:12	DFE1_READ_CNT_SEL	R/W	Select counter to be read 0: dfe1_value 1: Hit counter 2: Error counter	0x0
10	DFE1_CTRL_MODE	R/W	Parameter control mode for DFE1 parameter 0: Discrete 1: Continuous	0x1
9:4	DFE1_CTRL_THRES	R/W	Alternative threshold for DFE1 parameter (controller goal: err_cnt = 0.5*DFE1_THRES)	0x28
3	DFE1_CTRL_THRES_ENA	R/W	Enable use of alternative threshold for DFE1 parameter 0: Use default threshold 1: Use alternative threshold	0x0
2	DFE1_START_CTRL	R/W	Start operation (parameter update). Should be cleared afterwards in One-time mode and stay set in Non-stop and Paused mode	0x0
1:0	DFE1_OP_MODE	R/W	Operation mode 0: Off 1: One-time 2: Non-stop 3: Paused	0x0

2.5.1.32 APC DFE1 Timer Config

Short Name:APC_DFE1_TIMER_CFG

Address:0x1F01F

Configuration registers for DFE1 controller timing.

Table 278 • **APC DFE1 Timer Config**

Bit	Name	Access	Description	Default
31:16	DFE1_PS_TIME	R/W	Pause time (in number of rx_clk cycles)	0x0064
15:0	DFE1_OP_TIME	R/W	Operation time (in number of rx_clk cycles)	0x03E8

2.5.1.33 APC DFE1 Parameter Control

Short Name:APC_DFE1_PAR_CFG

Address:0x1F020

Configuration register for controlled DFE1 parameter. Note, for parameters larger than 8 bits, ini/min/max values are shifted to the left. For parameters smaller than 8 bits only the lower bits of ini/min/max are used.

Table 279 • **APC DFE1 Parameter Control**

Bit	Name	Access	Description	Default
31	DFE1_DIR_SEL	R/W	Select parameter update direction 0: Normal 1: Inverted	0x0
30:26	DFE1_RANGE_SEL	R/W	Parameter range selection (only when CTRL_MODE = continuous). Value complies to number of left-shifts	0x00
25:24	DFE1_CHG_MODE	R/W	Parameter change mode 0: Automatic update 1: Preset (use DFE1_INI as fix value internal processing continues) 2: Freeze (internal processing stops parameter stays at current value) 3: No update (internal processing continues but parameter is not updated)	0x0
23:16	DFE1_MAX	R/W	Maximum value of parameter	0x00
15:8	DFE1_MIN	R/W	Minimum value of parameter	0x00
7:0	DFE1_INI	R/W	Parameter initial value	0x00

2.5.1.34 APC DFE2 Control

Short Name:APC_DFE2_CTRL

Address:0x1F021

General behavior control for DFE2 parameter control.

Table 280 • **APC DFE2 Control**

Bit	Name	Access	Description	Default
29:27	DFE2_RECOVER_MODE	R/W	DFE2 recovery behavior 0: No auto-recovery 1: Freeze DFE2 on weak (eqz_gain > eqz_gain_freeze_thres) or missing input signal 2: Freeze DFE2 on weak signal and restart on missing input signal 3: Freeze DFE2 on missing input signal 4: Freeze DFE2 on missing input signal and auto-restart after Restart-Delay-Timer has expired 5: Auto-restart DFE2 on missing input signal 6-7: Reserved	0x0
26	DFE2_CTRL_DONE	R/O	Parameter control state in one-time mode 1: Finished	0x0
25:16	DFE2_ACTVAL	R/O	Parameter value (controlled/computed value)	0x000

Table 280 • **APC DFE2 Control**

Bit	Name	Access	Description	Default
15:14	DFE2_SYNC_MODE	R/W	Synchronization mode 0: Independent 1: Attached to parctrl FSM 1 2: Attached to parctrl FSM 2 3: Attached to both parctrl FSMs	0x0
13:12	DFE2_READ_CNT_SEL	R/W	Select counter to be read 0: dfe2_value 1: Hit counter 2: Error counter	0x0
10	DFE2_CTRL_MODE	R/W	Parameter control mode for DFE2 parameter 0: Discrete 1: Continuous	0x1
9:4	DFE2_CTRL_THRES	R/W	Alternative threshold for DFE2 parameter (controller goal: err_cnt = 0.5*DFE2_THRES)	0x28
3	DFE2_CTRL_THRES_ENA	R/W	Enable use of alternative threshold for DFE2 parameter 0: Use default threshold 1: Use alternative threshold	0x0
2	DFE2_START_CTRL	R/W	Start operation (parameter update). Should be cleared afterwards in One-time mode and stay set in Non-stop and Paused mode	0x0
1:0	DFE2_OP_MODE	R/W	Operation mode 0: Off 1: One-time 2: Non-stop 3: Paused	0x0

2.5.1.35 APC DFE2 Timer Config

Short Name:APC_DFE2_TIMER_CFG

Address:0x1F022

Configuration registers for DFE2 controller timing.

Table 281 • **APC DFE2 Timer Config**

Bit	Name	Access	Description	Default
31:16	DFE2_PS_TIME	R/W	Pause time (in number of rx_clk cycles)	0x0064
15:0	DFE2_OP_TIME	R/W	Operation time (in number of rx_clk cycles)	0x03E8

2.5.1.36 APC DFE2 Parameter Control

Short Name:APC_DFE2_PAR_CFG

Address:0x1F023

Configuration register for controlled DFE2 parameter. Note, for parameters larger than 8 bits, ini/min/max values are shifted to the left. For parameters smaller than 8 bits only the lower bits of ini/min/max are used.

Table 282 • **APC DFE2 Parameter Control**

Bit	Name	Access	Description	Default
31	DFE2_DIR_SEL	R/W	Select parameter update direction 0: Normal 1: Inverted	0x0
30:26	DFE2_RANGE_SEL	R/W	Parameter range selection (only when CTRL_MODE = continuous). Value complies to number of left-shifts	0x00
25:24	DFE2_CHG_MODE	R/W	Parameter change mode 0: Automatic update 1: Preset (use DFE2_INI as fix value internal processing continues) 2: Freeze (internal processing stops parameter stays at current value) 3: No update (internal processing continues but parameter is not updated)	0x0
23:16	DFE2_MAX	R/W	Maximum value of parameter	0x00
15:8	DFE2_MIN	R/W	Minimum value of parameter	0x00
7:0	DFE2_INI	R/W	Parameter initial value	0x00

2.5.1.37 APC DFE3 Control

Short Name:APC_DFE3_CTRL

Address:0x1F024

General behavior control for DFE3 parameter control.

Table 283 • **APC DFE3 Control**

Bit	Name	Access	Description	Default
29:27	DFE3_RECOVER_MODE	R/W	DFE3 recovery behavior 0: No auto-recovery 1: Freeze DFE3 on weak (eqz_gain > eqz_gain_freeze_thres) or missing input signal 2: Freeze DFE3 on weak signal and restart on missing input signal 3: Freeze DFE3 on missing input signal 4: Freeze DFE3 on missing input signal and auto-restart after Restart-Delay-Timer has expired 5: Auto-restart DFE3 on missing input signal 6-7: Reserved	0x0
26	DFE3_CTRL_DONE	R/O	Parameter control state in one-time mode 1: Finished	0x0
25:16	DFE3_ACTVAL	R/O	Parameter value (controlled/computed value)	0x000

Table 283 • **APC DFE3 Control**

Bit	Name	Access	Description	Default
15:14	DFE3_SYNC_MODE	R/W	Synchronization mode 0: Independent 1: Attached to parctrl FSM 1 2: Attached to parctrl FSM 2 3: Attached to both parctrl FSMs	0x0
13:12	DFE3_READ_CNT_SEL	R/W	Select counter to be read 0: dfe3_value 1: Hit counter 2: Error counter	0x0
10	DFE3_CTRL_MODE	R/W	Parameter control mode for DFE3 parameter 0: Discrete 1: Continuous	0x1
9:4	DFE3_CTRL_THRES	R/W	Alternative threshold for DFE3 parameter (controller goal: err_cnt = 0.5*DFE3_THRES)	0x28
3	DFE3_CTRL_THRES_ENA	R/W	Enable use of alternative threshold for DFE3 parameter 0: Use default threshold 1: Use alternative threshold	0x0
2	DFE3_START_CTRL	R/W	Start operation (parameter update). Should be cleared afterwards in One-time mode and stay set in Non-stop and Paused mode	0x0
1:0	DFE3_OP_MODE	R/W	Operation mode 0: Off 1: One-time 2: Non-stop 3: Paused	0x0

2.5.1.38 APC DFE3 Timer Config

Short Name:APC_DFE3_TIMER_CFG

Address:0x1F025

Configuration registers for DFE3 controller timing.

Table 284 • **APC DFE3 Timer Config**

Bit	Name	Access	Description	Default
31:16	DFE3_PS_TIME	R/W	Pause time (in number of rx_clk cycles)	0x0064
15:0	DFE3_OP_TIME	R/W	Operation time (in number of rx_clk cycles)	0x03E8

2.5.1.39 APC DFE3 Parameter Control

Short Name:APC_DFE3_PAR_CFG

Address:0x1F026

Configuration register for controlled DFE3 parameter. Note, for parameters larger than 8 bits, ini/min/max values are shifted to the left. For parameters smaller than 8 bits only the lower bits of ini/min/max are used.

Table 285 • **APC DFE3 Parameter Control**

Bit	Name	Access	Description	Default
31	DFE3_DIR_SEL	R/W	Select parameter update direction 0: Normal 1: Inverted	0x0
30:26	DFE3_RANGE_SEL	R/W	Parameter range selection (only when CTRL_MODE = continuous). Value complies to number of left-shifts	0x00
25:24	DFE3_CHG_MODE	R/W	Parameter change mode 0: Automatic update 1: Preset (use DFE3_INI as fix value internal processing continues) 2: Freeze (internal processing stops parameter stays at current value) 3: No update (internal processing continues but parameter is not updated)	0x0
23:16	DFE3_MAX	R/W	Maximum value of parameter	0x00
15:8	DFE3_MIN	R/W	Minimum value of parameter	0x00
7:0	DFE3_INI	R/W	Parameter initial value	0x00

2.5.1.40 APC DFE4 Control

Short Name:APC_DFE4_CTRL

Address:0x1F027

General behavior control for DFE4 parameter control.

Table 286 • **APC DFE4 Control**

Bit	Name	Access	Description	Default
29:27	DFE4_RECOVER_MODE	R/W	DFE4 recovery behavior 0: No auto-recovery 1: Freeze DFE4 on weak (eqz_gain > eqz_gain_freeze_thres) or missing input signal 2: Freeze DFE4 on weak signal and restart on missing input signal 3: Freeze DFE4 on missing input signal 4: Freeze DFE4 on missing input signal and auto-restart after Restart-Delay-Timer has expired 5: Auto-restart DFE4 on missing input signal 6-7: Reserved	0x0
26	DFE4_CTRL_DONE	R/O	Parameter control state in one-time mode 1: Finished	0x0
25:16	DFE4_ACTVAL	R/O	Parameter value (controlled/computed value)	0x000

Table 286 • **APC DFE4 Control**

Bit	Name	Access	Description	Default
15:14	DFE4_SYNC_MODE	R/W	Synchronization mode 0: Independent 1: Attached to parctrl FSM 1 2: Attached to parctrl FSM 2 3: Attached to both parctrl FSMs	0x0
13:12	DFE4_READ_CNT_SEL	R/W	Select counter to be read 0: dfe4_value 1: Hit counter 2: Error counter	0x0
10	DFE4_CTRL_MODE	R/W	Parameter control mode for DFE4 parameter 0: Discrete 1: Continuous	0x1
9:4	DFE4_CTRL_THRES	R/W	Alternative threshold for DFE4 parameter (controller goal: err_cnt = 0.5*DFE4_THRES)	0x28
3	DFE4_CTRL_THRES_ENA	R/W	Enable use of alternative threshold for DFE4 parameter 0: Use default threshold 1: Use alternative threshold	0x0
2	DFE4_START_CTRL	R/W	Start operation (parameter update). Should be cleared afterwards in One-time mode and stay set in Non-stop and Paused mode	0x0
1:0	DFE4_OP_MODE	R/W	Operation mode 0: Off 1: One-time 2: Non-stop 3: Paused	0x0

2.5.1.41 APC DFE4 Timer Config

Short Name:APC_DFE4_TIMER_CFG

Address:0x1F028

Configuration registers for DFE4 controller timing.

Table 287 • **APC DFE4 Timer Config**

Bit	Name	Access	Description	Default
31:16	DFE4_PS_TIME	R/W	Pause time (in number of rx_clk cycles)	0x0064
15:0	DFE4_OP_TIME	R/W	Operation time (in number of rx_clk cycles)	0x03E8

2.5.1.42 APC DFE4 Parameter Control

Short Name:APC_DFE4_PAR_CFG

Address:0x1F029

Configuration register for controlled DFE4 parameter. Note, for parameters larger than 8 bits, ini/min/max values are shifted to the left. For parameters smaller than 8 bits only the lower bits of ini/min/max are used.

Table 288 • **APC DFE4 Parameter Control**

Bit	Name	Access	Description	Default
31	DFE4_DIR_SEL	R/W	Select parameter update direction 0: Normal 1: Inverted	0x0
30:26	DFE4_RANGE_SEL	R/W	Parameter range selection (only when CTRL_MODE = continuous). Value complies to number of left-shifts	0x00
25:24	DFE4_CHG_MODE	R/W	Parameter change mode 0: Automatic update 1: Preset (use DFE4_INI as fix value internal processing continues) 2: Freeze (internal processing stops parameter stays at current value) 3: No update (internal processing continues but parameter is not updated)	0x0
23:16	DFE4_MAX	R/W	Maximum value of parameter	0x00
15:8	DFE4_MIN	R/W	Minimum value of parameter	0x00
7:0	DFE4_INI	R/W	Parameter initial value	0x00

2.5.1.43 APC LC softcontrol Configuration

Short Name:APC_LC_SOFTCTRL_CFG

Address:0x1F02A

Configuration register for the LC-Softcontrol logic block. The L and C parameters can be controlled depending on DFE1 and DFE2 and EQZ_AGC parameters instead of pattern matching.

Table 289 • **APC LC softcontrol Configuration**

Bit	Name	Access	Description	Default
31:28	LC_SC_TIMER	R/W	Operation timer configuration: L/C-control operates in every 2^(2*LC_SC_TIMER)-th clock cycle. 0: Operate every clock cycle 1: Operate every 4th clock cycle 2: Operate every 16th clock cycle ...	0x0
27:24	LC_SC_AVGSHFT	R/W	DFE1/2 and EQZ_AGC averaging behavior. DFE/AGC parameters are averaged over 2^(8+LC_SC_AVGSHFT) input values. 0: Average over 256 values 1: Average over 512 values ...	0x8
23:20	LC_SC_DFE1_THRESHOLD	R/W	DFE1 comparison threshold for L-control used in mode 2. EQZ_L is increased/decreased if DFE1 differs from neutral value by more than LC_SC_DFE1_THRESHOLD.	0x8

Table 289 • **APC LC softcontrol Configuration**

Bit	Name	Access	Description	Default
19:16	LC_SC_DFE2_THRESHOLD	R/W	DFE2 comparison threshold for C-control used in mode 2. EQZ_C is increased/decreased if DFE1 differs from neutral value by more than LC_SC_DFE2_THRESHOLD.	0x4
15:9	LC_SC_AGC_THRESHOLD	R/W	EQZ_AGC threshold for mandatory increase of L and C. If EQZ_AGC > (128+LC_SC_AGC_THRESHOLD) then L and C control values are increased. 0: 128 1: 129 ... 127: 255	0x7D
8	LC_SC_DIV_C_SEL	R/W	Define DFE2 comparison parameter for EQZ_C control in mode 1 0: EQZ_L 1: EQZ_C	0x0
7:5	LC_SC_DIV_L	R/W	Select divider for L-control used in mode 1 (Divider = 4+LC_SC_DIV_L) 0: Divide by 4 1: Divide by 5 ... 7: Divide by 11	0x4
4:2	LC_SC_DIV_C	R/W	Select divider for C-control used in mode 1 (Divider = 4+LC_SC_DIV_C) 0: Divide by 4 1: Divide by 5 ... 7: Divide by 11	0x4
1:0	LC_SC_MODE	R/W	Select LC soft-control mode. LC soft-control modes must be enabled first after INI/MIN/MAX values of all parameters have been programmed. 0: Disabled 1: Mode 1 2: Mode 2 3: Reserved	0x0

2.5.2 SD10G65 DES Configuration and Status

Configuration and status register set for SD10G65 DES

2.5.2.1 SD10G65 DES Configuration 0

Short Name:SD10G65_DES_CFG0

Address:0x1F100

Configuration register 0 for SD10G65 DES.

Table 290 • **SD10G65 DES Configuration 0**

Bit	Name	Access	Description	Default
7	DES_INV_H	R/W	Invert output of high auxiliary deserializer	0x0
6	DES_INV_L	R/W	Invert output of low auxiliary deserializer	0x0

Table 290 • **SD10G65 DES Configuration 0 *(continued)***

Bit	Name	Access	Description	Default
5	DES_INV_M	R/W	Invert output of main deserializer	0x0
4:2	DES_IF_MODE_SEL	R/W	Interface width 0: 8 1: 10 2: 16 (energy efficient) 3: 20 (energy efficient) 4: 32 5: 40 6: 16 bit (fast) 7: 20 bit (fast)	0x4
1	DES_VSC_DIS	R/W	Auxiliary deserializer channels disable.	0x1
0	DES_DIS	R/W	Deserializer disable.	0x0

2.5.2.2 SD10G65 MOEBDIV Configuration 0

Short Name:SD10G65_MOEBDIV_CFG0

Address:0x1F101

Configuration register 0 for SD10G65 MoebiusDivider

Table 291 • **SD10G65 MOEBDIV Configuration 0**

Bit	Name	Access	Description	Default
11:9	MOEBDIV_BW_CDR_SEL_A	R/W	Bandwidth selection for cp/md of cdr loop when core NOT flags valid data detected	0x3
8:6	MOEBDIV_BW_CDR_SEL_B	R/W	Bandwidth selection for cp/md of cdr loop when core flags valid data detected	0x3
5:3	MOEBDIV_BW_CORE_SEL	R/W	Bandwidth selection for cp/md signals towards core	0x0
2	MOEBDIV_CPMD_SWAP	R/W	CP/MD swapping	0x0
1	MOEBDIV_DIV32_ENA	R/W	MD divider enable	0x0
0	MOEBDIV_DIS	R/W	Divider disable	0x0

2.5.3 SD10G65 OB Configuration and Status

Configuration and status register set for SD10G65 OB

2.5.3.1 SD10G65 OB Configuration 0

Short Name:SD10G65_OB_CFG0

Address:0x1F110

Configuration register 0 for SD10G65 OB.

Table 292 • **SD10G65 OB Configuration 0**

Bit	Name	Access	Description	Default
23	SER_INV	R/W	Invert input to serializer	0x0
22:21	CLK_BUF_CMV	R/W	Control of common mode voltage of clock buffer between synthesizer and OB.	0x0
17	RST	R/W	Set digital part into pseudo reset	0x0

Table 292 • **SD10G65 OB Configuration 0 *(continued)***

Bit	Name	Access	Description	Default
16	EN_PAD_LOOP	R/W	Enable pad loop	0x0
15	EN_INP_LOOP	R/W	Enable input loop	0x0
14	EN_DIRECT	R/W	Enable direct path	0x0
13	EN_OB	R/W	Enable output buffer and serializer	0x0
8	INCR_LEVN	R/W	Selects amplitude range controlled via levn. See description of levn.	0x1
7:5	SEL_IFW	R/W	Interface width 0: 8 1: 10 2: 16 3: 20 4: 32 5: 40 6-7: Reserved	0x4
4:0	LEVN	R/W	Amplitude control value. Step size is 25 mVpp, decreasing amplitude with increasing control value. Range depends on incr_levn. Coding for incr_levn=0: 31: 500mVpp 30: 525mVpp 29: 550mVpp ... 0: 1275mVpp. Coding for incr_levn=1: 31: 300mVpp 30: 325mVpp 29: 350mVpp ... 0: 1075mVpp. (Note: maximum achievable amplitude depends on the supply voltage)	0x07

2.5.3.2 SD10G65 OB Configuration 1

Short Name:SD10G65_OB_CFG1

Address:0x1F111

Configuration register 1 for SD10G65 OB.

Table 293 • **SD10G65 OB Configuration 1**

Bit	Name	Access	Description	Default
26	AB_COMP_EN	R/W	Enable amplitude compensation of AB bleed current	0x1
25:23	DIODE_CUR	R/W	Bleed current for class AB operation of driver 0: 1% 1: 0.5% 2: 2% 3: reserved	0x0

Table 293 • **SD10G65 OB Configuration 1 *(continued)***

Bit	Name	Access	Description	Default
22:21	LEV_SHFT	R/W	Level shift ctrl of class AB bias generator 0: 50mV 1: 100mV 2:150mV 3: 200mV	0x1
19:18	PREDRV_R_CTRL	R/W	Slew rate ctrl of OB (R), encoding see PREDRV_C_CTRL	0x3
17:16	PREDRV_C_CTRL	R/W	Slew rate ctrl of OB (C) C=3 R=3: 25ps C=3 R=0: 35ps C=0 R=3: 55ps C=1 R=0: 70ps C=0 R=0: 120 ps	0x3
15:10	VTAIL	R/W	Tail voltage driver settings 0: reserved 1: 75mV 2: 100mV 4: 125mV 8: 150mV 16: 175mV 32: 200mV Intermediate values possible when setting two bits	0x02
9:5	VCAS	R/W	Ctrl of cascade volt in drv stage 0: reserved 1: 0 2: 1/12 4: 2/12 8: 3/12 16: 4/12 Intermediate values possible when setting two bits	0x01
4	R_COR	R/W	Additional resistor calibration trim	0x0
3:0	R_I	R/W	Offset resistance adjustment for CML cells (two-complement) 1000: -8 1111: -1 0000: 0 0111: 7	0x0

2.5.3.3 SD10G65 OB Configuration 2

Short Name:SD10G65_OB_CFG2

Address:0x1F112

Configuration register 2 for SD10G65 OB. D_filter contains four 6-bit precalculated DA input values. Please note the differences in programming for various interface (IF) bit widths. For calculation details see documentation of OB10G.

Table 294 • **SD10G65 OB Configuration 2**

Bit	Name	Access	Description	Default
23:0	D_FILTER	R/W	Transmit filter coefficients for FIR taps. Suggested start value (no emphasis, max amplitude) 0x820820: for I/F width 8/10 bits 0x7DF820: for I/F width 16/20/32/40 bits	0x7DF820

2.5.3.4 SD10G65 OB Configuration 3

Access to receiver detect functionality

Short Name:SD10G65_OB_CFG3

Address:0x1F113

Configuration register 3 for SD10G65 OB.

Table 295 • **SD10G65 OB Configuration 3**

Bit	Name	Access	Description	Default
18	REC_DET_DONE	R/O	Indicates a completed receiver detect measurement. Should be one few us after rec_det_start is set.	0x0
17	REC_DET_START	R/W	Rising edge starts receiver detect measurement. Has to be keept set until rec_det_value has been read.	0x0
16	REC_DET_ENABLE	R/W	Enable receiver detect function. MUST be disabled for normal operation!	0x0
15:12	RESERVED	R/W	Must be set to its default.	0x2
11:0	REC_DET_VALUE	R/O	Holds the time between the start and the flag of the receiver detect measurement. Time [ns +/- 4 ns] = 8 * value - 12	0x000

2.5.4 SD10G65 IB Configuration and Status

Configuration and status register set for SD10G65 IB

2.5.4.1 SD10G65 IB Configuration 0

Short Name:SD10G65_IB_CFG0

Address:0x1F120

Configuration register 0 for SD10G65 IB. Note: Configuration bit-grp IB_CLKDIV_ENA was named IB_VSCOPE_CLK_ENA in an early revision of the input buffer.

Table 296 • **SD10G65 IB Configuration 0**

Bit	Name	Access	Description	Default
30:27	IB_RCML_ADJ	R/W	Offset resistance adjustment for CML cells (two-complement) 1000: -8 1111: -1 0000: 0 0111: 7	0x0
26:23	IB_TERM_V_SEL	R/W	Select termination voltage	0x8
22	IB_TERM_VDD_ENA	R/W	Enable common mode termination 0: no common mode termination (only AC-common mode termination) 1: termination to VDDI	0x0
21	IB_RIB_SHIFT	R/W	Shifts resistance adjustment value ib_rib_adj by +1	0x0
20:17	IB_RIB_ADJ	R/W	Offset resistance adjustment for termination (two-complement) 1000: -8 1111: -1 0000: 0 0111: 7	0x0
14	IB_DFE_ENA	R/W	Enable DFE stage (gates IB_ISEL_DFE) 0: Disable 1: Enable	0x0
13:12	IB_SIG_SEL	R/W	Select input buffer input signal 0: normal operation 1: -6dB input 2: OB->IB data loop or test signal 3: RESERVED	0x0
11	IB_VBULK_SEL	R/W	Controls Bulk Voltage of High Speed Cells 0: High 1: Low (mission mode)	0x1
10	IB_IA_ENA	R/W	Enable for IA including ACJtag 0: Disable 1: Enable	0x1
9	IB_IA_SDET_ENA	R/W	Enable for IA signal detect circuit (IB_SDET_SEL = 0 required) 0: Disable 1: Enable	0x0
8	IB_IE_SDET_ENA	R/W	Enable for IA signal detect circuit (IB_SDET_SEL = 1 required) 0: Disable 1: Enable	0x0
7	IB_LD_ENA	R/W	Enable for level detect circuit 0: Disable 1: Enable	0x0
6	IB_1V_ENA	R/W	Enable for 1V mode 0: VDDI=1.2V 1: VDDI=1.0V	0x0

Table 296 • **SD10G65 IB Configuration 0 *(continued)***

Bit	Name	Access	Description	Default
5	IB_CLKDIV_ENA	R/W	Enable clock dividers in sampling stag 0: Disable (use in double rate mode) 1: Enable (use in full rate mode)	0x0
3	IB_VSCOPE_ENA	R/W	Enable VScope Path of Sampling-Stage 0: Disable 1: Enable	0x0
2	IB_SAM_ENA	R/W	Enable SAMpling stage 0: Disable 1: Enable (mission mode)	0x0
1	IB_EQZ_ENA	R/W	Enable EQualiZation stage 0: Disable 1: Enable (mission mode)	0x0

2.5.4.2 SD10G65 IB Configuration 1

Short Name:SD10G65_IB_CFG1

Address:0x1F121

Configuration register 1 for SD10G65 IB.

Table 297 • **SD10G65 IB Configuration 1**

Bit	Name	Access	Description	Default
31:28	IB_AMP_L	R/W	Inductor peaking of 1. stage Input buffer 0: no peaking 15: max. peaking max. peaking > 3db at 8GHz	0x8
27:24	IB_EQZ_L0	R/W	Inductor peaking of EQ-Buffer0 (over all 2. stage) 0: no peaking 15: max. peaking max. peaking > 3db at 8GHz	0x8
23:20	IB_EQZ_L1	R/W	Inductor peaking of EQ-Buffer1 (over all 3. stage) 0: no peaking 15: max. peaking max. peaking > 3dB at 8GHz	0x8
19:16	IB_EQZ_L2	R/W	Inductor peaking of EQ-Buffer2 (over all 4. stage) 0: no peaking 15: max. peaking max. peaking > 3dB at 8GHz	0x8
15:12	IB_AGC_L	R/W	Inductor peaking of EQ-Buffer3 (over all 5. stage) 0: no peaking 15: max. peaking max. peaking > 3dB at 8GHz	0x8
11:9	IB_AMP_C	R/W	C-gain peaking for IB-stage 0: no peaking 7: max. peaking corner frequency adjustment with ib_eqz_c_adj_ib	0x4

Table 297 • **SD10G65 IB Configuration 1 *(continued)***

Bit	Name	Access	Description	Default
8:6	IB_EQZ_C0	R/W	C-gain peaking for EQ-stage0 0: no peaking 7: max. peaking corner frequency adjustment with ib_eqz_c_adj_es0	0x4
5:3	IB_EQZ_C1	R/W	C-gain peaking for EQ-stage1 0: no peaking 7: max. peaking corner frequency adjustment with ib_eqz_c_adj_es1	0x4
2:0	IB_EQZ_C2	R/W	C-gain peaking for EQ-stage2 0: no peaking 7: max. peaking corner frequency adjustment with ib_eqz_c_adj_es2	0x4

2.5.4.3 SD10G65 IB Configuration 2

Short Name:SD10G65_IB_CFG2

Address:0x1F122

Configuration register 2 for SD10G65 IB.

Table 298 • **SD10G65 IB Configuration 2**

Bit	Name	Access	Description	Default
27:18	IB_EQZ_GAIN	R/W	Gain of Input Buffer 0-511 gain adjustment only in first stage > 511 gain in first stage at max. 512-639 gain in 2.stage increased from 1 to 2 > 639 gain = 2 640-767 gain in 3.stage increased from 1 to 2 > 767 gain = 2 768-895 gain in 4.stage increased from 1 to 2 >895 gain at max.	0x040
17:10	IB_EQZ_AGC	R/W	Amplification (gain) of AGC in Input Buffer (normal operation) after gain calibration 0: gain = 0.3 255: gain = 1.5 if disp/disn is active dac function for dfe gain calibration	0x80
9:0	IB_EQZ_OFFSET	R/W	Offset value for IB-stage of Input Buffer 512: neutral > 512: positive < 512: negative range +/- 600mV (low gain) to +/-30mV (high gain) gain dependent offset sensitivity required for Base line wander compensation not supported in test chip	0x200

2.5.4.4 SD10G65 IB Configuration 3

Short Name:SD10G65_IB_CFG3

Address:0x1F123

Configuration register 1 for SD10G65 IB. Note: the behavior of IB_EQ_LD1_OFFSET changes when APC is disabled. In this case IB_EQ_LD1_OFFSET directly controls the level for Level-Detect circuitry 1. Coding: 0: 20mV, 1: 25mV, ... 63: 340mV.

Table 299 • **SD10G65 IB Configuration 3**

Bit	Name	Access	Description	Default
31:30	IB_LDSD_DIVSEL	R/W	Dividing factor for SDET and LD circuits of IE. 0: 128 1: 32 2: 8 3: 4	0x1
29:27	IB_SDET_CLK_DIV	R/W	Clock dividing factor for Signal Detect circuit of IA 0: 2 ... 7: 256	0x5
26	IB_SET_SDET	R/W	Force Signal-Detect output to high level 0: Normal operation 1: Force sigdet high	0x0
24	IB_SDET_SEL	R/W	Selects source of signal detect (ib_X_sdet_ena must be enabled accordingly) 0: IA 1: IE	0x0
23	IB_DIRECT_SEL	R/W	Selects source of direct data path to core 0: IE 1: IA	0x0
22:17	IB_EQ_LD1_OFFSET	R/W	With APC enabled level offset (6bit-signed) compared to IB_EQ_LD0_LEVEL for Level-Detect circuitry 1. Saturating between 20mV and 340mV. See also note in register description. 0: no offset 1: +5mV 31: +155mV 63(= -1): -5mV 32(= -32): -160mV.	0x00
16:11	IB_EQ_LD0_LEVEL	R/W	Level for Level-Detect circuitry 0. 0: 20mV 1: 25mV ... 40: 220mV ... 63: 340mV	0x28
10:5	IB_IE_SDET_LEVEL	R/W	Threshold value for IE Signal-Detect. 0: 20mV 1: 25mV 2: 30mV ... 63: 340mV	0x02

Table 299 • **SD10G65 IB Configuration 3 *(continued)***

Bit	Name	Access	Description	Default
4:0	IB_IA_SDET_LEVEL	R/W	Threshold value for IA Signal-Detect. 0: 0mV ... 8: 80mV ... 31: 310mV	0x08

2.5.4.5 SD10G65 IB Configuration 4

Short Name:SD10G65_IB_CFG4

Address:0x1F124

Configuration register 4 for SD10G65 IB.

Table 300 • **SD10G65 IB Configuration 4**

Bit	Name	Access	Description	Default
31:30	IB_EQZ_C_ADJ_IB	R/W	corner frequency selection for c-gain peaking 1.stage 0: lowest corner frequency 3: highest corner frequency	0x2
29:28	IB_EQZ_C_ADJ_ES2	R/W	corner frequency selection for c-gain peaking 2.stage 0: lowest corner frequency 3: highest corner frequency	0x2
27:26	IB_EQZ_C_ADJ_ES1	R/W	corner frequency selection for c-gain peaking 3.stage 0: lowest corner frequency 3: highest corner frequency	0x2
25:24	IB_EQZ_C_ADJ_ES0	R/W	corner frequency selection for c-gain peaking 4.stage 0: lowest corner frequency 3: highest corner frequency	0x2
23:21	IB_EQZ_L_MODE	R/W	Coder mode: APC L value to IE inductance 0: equ. distributed (double step 3->4) 1: equ. distributed (no change 6+7) 2: 1st buffer max - 2nd buffer max - ...	0x0
20:18	IB_EQZ_C_MODE	R/W	Coder mode: APC C value to IE capacitance 0: equ. distributed 2: 1st buffer max - 2nd buffer max - ...	0x0
17:12	IB_VSCOPE_H_THRES	R/W	Threshold value (offset) for vscope-high sampling path 0: -max 31: -0 32: +0 63: +max (depending on calibration)	0x30
11:6	IB_VSCOPE_L_THRES	R/W	Threshold value (offset) for vscope-low sampling path 0: -max 31: -0 32: +0 63: +max (depending on calibration)	0x0F

Table 300 • **SD10G65 IB Configuration 4 *(continued)***

Bit	Name	Access	Description	Default
5:0	IB_MAIN_THRES	R/W	Threshold value (offset) for main sampling path 0: -max 31: -0 32: +0 63: +max (depending on calibration)	0x20

2.5.4.6 SD10G65 IB Configuration 5

Short Name:SD10G65_IB_CFG5

Address:0x1F125

Configuration register 5 for SD10G65 IB.

Table 301 • **SD10G65 IB Configuration 5**

Bit	Name	Access	Description	Default
31:28	IB_TSTGEN_AMPL	R/W	Test generator amplitude setting 0: 0mV ... 15: 150mV	0x0
27	IB_TSTGEN_ENA	R/W	Test generator enable but data path selected with 'ib_sig_sel' (disable input loop if test generator is used) 0: inactive 1: active	0x0
26	IB_TSTGEN_DATA	R/W	Test generator data 0: low 1: high	0x0
25	IB_TSTGEN_TOGGLE_ENA	R/W	Test generator data toggle enable 0: inactive 1: active	0x0
22	IB_JUMPH_ENA	R/W	Enable jump to opposite half of h-channel 0: Post main sampler 1: Pre main sampler	0x0
21	IB_JUMPL_ENA	R/W	Enable jump to opposite half of l-channel 0: Post main sampler 1: Pre main sampler	0x0
20:19	IB_DFE_DIS	R/W	DFE output disable required to calibrate IS 0: mission mode 3: Vout = 0V 1: Vout= xx*ampldfe/64 2: Vout=-xx*ampldfe/64 ampldfe=196mV if ena1V = '1' (1V mode) ampldfe=260mV if ena1V = '0' (1.2V mode) xx= TBD	0x0

Table 301 • **SD10G65 IB Configuration 5 *(continued)***

Bit	Name	Access	Description	Default
18:17	IB_AGC_DIS	R/W	AGC output disable required to calibrate DFE-gain 0: mission mode 3: Vout = 0V 1: Vout= xx*ampldfe/64 2: Vout=-xx*ampldfe/64 ampldfe=270mV if ena1V = '1' (1V mode) ampldfe=360mV if ena1V = '0' (1.2V mode) xx=	0x0
16	IB_EQ_LD_CAL_ENA	R/W	Selects EQ Level Detect for calibration	0x0
15	IB_THRES_CAL_ENA	R/W	Selects IS threshold circuit for calibration	0x0
14	IB_IS_OFFS_CAL_ENA	R/W	Selects IS offset circuit for calibration	0x0
13	IB_IA_OFFS_CAL_ENA	R/W	Selects IA offset circuit for calibration	0x0
12	IB_IE_SDET_CAL_ENA	R/W	Selects IE Signal Detect for calibration	0x0
11	IB_HYS_CAL_ENA	R/W	Enable calibration in order to eliminate hysteresis 1: Enable 0: Disable	0x0
10	IB_CALMUX_ENA	R/W	Enables IS MUX in detblk1	0x1
9:6	IB_OFFS_BLKSEL	R/W	Selects calibration target (sample stage threshold, sample stage offset, aux.-stage offset), dependent on calibration group, see encoding. When ib_thres_cal_ena = 1 0: MD0 threshold 1: MD1 threshold 2: CP0 threshold 3: CP1 threshold 4: VH0 threshold 5: VH1 threshold 6: VL0 threshold 7: VL1 threshold When ib_is_offs_cal_ena = 1 0: MD0 offset 1: MD1 offset 2: CP0 offset 3: CP1 offset 4: VH0 offset 5: VH1 offset 6: VL0 offset 7: VL1 offset When ib_ia_offs_cal_ena = 1 0: Observe0 offset 1: Observe1 offset 2: Observe0 threshold 3: Observe1 threshold (MSB not used)	0x0

Table 301 • **SD10G65 IB Configuration 5 *(continued)***

Bit	Name	Access	Description	Default
5:0	IB_OFFS_VALUE	R/W	Calibration value for IA/IS. Values for threshold calibration get inverted for negative threshold voltages (ib_vscope_h_thres, ib_vscope_l_thres or ib_main_thres). For offset calibration 0: -max_offset * 32/32 31: -max_offset * 1/32 32: +max_offset * 1/32 63: +max_offset * 32/32 For threshold calibration 0: min_threshold 63: max_threshold	0x1F

2.5.4.7 SD10G65 IB Configuration 6

Short Name:SD10G65_IB_CFG6

Address:0x1F126

Configuration register 6 for SD10G65 IB.

Table 302 • **SD10G65 IB Configuration 6**

Bit	Name	Access	Description	Default
22:16	IB_EQZ_GAIN_ADJ	R/W	0dB Gain adjustment for EQZ-stages of Input Buffer level at LD0 = LD1 -> 0dB level range 160mV-220mV	0x2A
12	IB_AUTO_AGC_ADJ	R/W	Enable automatic AGC adjustment 1: AGC is adjusted automatically (IB_EQZ_AGC_ADJ value is not used) 0: AGC is adjusted with value stored in IB_EQZ_AGC_ADJ	0x0
11:5	IB_EQZ_AGC_ADJ	R/W	Gain adjustment of AGC-amplifier Bitgroup should be set to 2*IB_DFE_GAIN_ADJ	0x3E
4:0	IB_SAM_OFFS_ADJ	R/W	Range for offset calibration of all sampling paths 0: 0mV 32: 80mV	0x10

2.5.4.8 SD10G65 IB Configuration 7

Short Name:SD10G65_IB_CFG7

Address:0x1F127

Configuration register 7 for SD10G65 IB.

Table 303 • **SD10G65 IB Configuration 7**

Bit	Name	Access	Description	Default
28:23	IB_MAIN_THRES_CAL	R/W	Initial value for calibration of main sampling path	0x30
22	IB_DFE_OFFSET_H_L	R/W	Selects higher or lower DFE offset for IS calibration 0: ib_dfe_offset_l 1: ib_dfe_offset_h	0x0

Table 303 • **SD10G65 IB Configuration 7 *(continued)***

Bit	Name	Access	Description	Default
21:16	IB_DFE_GAIN_ADJ	R/W	Gain adjustment of DFE amplifier DFE Gain 1 Volt mode = 0dB 1.2 Volt mode 1dB measurement with int. DAC and VScope Channels	0x24
11:6	IB_DFE_OFFSET_H	R/W	Higher threshold offset of DFE buffer for IS calibration 0: 0mv 63: 200mV	0x17
5:0	IB_DFE_OFFSET_L	R/W	Lower sample offset of DFE buffer for IS calibration 0: 0mv 63: 200mV	0x06

2.5.4.9 SD10G65 IB Configuration 8

Short Name:SD10G65_IB_CFG8

Address:0x1F128

Configuration register 8 for SD10G65 IB.

Table 304 • **SD10G65 IB Configuration 8**

Bit	Name	Access	Description	Default
20	IB_SEL_VCLK	R/W	Use separate vscope clock for vscope-channels	0x0
19	IB_BIAS_MODE	R/W	Bias regulation mode 0: constant resistor 1: constant current	0x1
18	IB_LAT_NEUTRAL	R/W	Enables neutral setting of latches 1: Reset to mid values 0: Normal operation	0x0
14	RESERVED	R/W	Must be set to its default.	0x1
12:10	IB_CML_AMPL	R/W	Amplitude of cml stages inside IS 0: 200mVppd 7: 240mVppd	0x4
9:4	IB_BIAS_ADJ	R/W	Gain of cml stages inside IS 0: 3dB 31: 6dB 63: 9dB	0x1F
3:0	IB_CML_CURR	R/W	Current through CML Cells 0: 150% 5: 100% 15: 50%	0x5

2.5.4.10 SD10G65 IB Configuration 9

Automatically Adapted DFE Coefficients

Short Name:SD10G65_IB_CFG9

Address:0x1F129

Configuration register 9 for SD10G65 IB.

Table 305 • **SD10G65 IB Configuration 9**

Bit	Name	Access	Description	Default
28:24	IB_DFE_COEF4	R/W	Weighting for fourth DFE coefficient	0x10
20:16	IB_DFE_COEF3	R/W	Weighting for third DFE coefficient	0x10
13:8	IB_DFE_COEF2	R/W	Weighting for second DFE coefficient	0x20
6:0	IB_DFE_COEF1	R/W	Weighting for first DFE coefficient	0x40

2.5.4.11 SD10G65 IB Configuration register 10 JTAG related setting

Short Name:SD10G65_IB_CFG10

Address:0x1F12A

Configuration register 10 for SD10G65 IB.

Table 306 • **SD10G65 IB Configuration register 10 JTAG related setting**

Bit	Name	Access	Description	Default
31	IB_IA_DOFFS_CAL	R/O	Data offset calibration result IA stage	0x0
30	IB_IS_DOFFS_CAL	R/O	Data offset calibration result IS stage	0x0
29	IB_IE_SDET_PEDGE	R/O	Detection of toggling signal at PADP and PADN	0x0
28	IB_IE_SDET_NEDGE	R/O	Detection of toggling signal at PADP and PADN	0x0
27	IB_IE_SDET	R/O	Result signal detect of IE stage	0x0
26	IB_IA_SDET	R/O	Result signal detect of IA stage	0x0
25	IB_EQZ_LD1_PEDGE	R/O	Result of Level-Detect1 (after ES2-stage of EQZ) circuitry 1: Input level above threshold defined by IB_EQ_LD_LEV	0x0
24	IB_EQZ_LD1_NEDGE	R/O	Result of Level-Detect1 (after ES2-stage of EQZ) circuitry 1: Input level above threshold defined by IB_EQ_LD_LEV	0x0
23	IB_EQZ_LD0_PEDGE	R/O	Result of Level-Detect0 (after IB-stage of EQZ) circuitry 1: Input level above threshold defined by IB_EQ_LD_LEV	0x0
22	IB_EQZ_LD0_NEDGE	R/O	Result of Level-Detect0 (after IB-stage of EQZ) circuitry 1: Input level above threshold defined by IB_EQ_LD_LEV	0x0
21	IB_IE_DIRECT_DATA	R/O	Direct Data output from IE block	0x0
20	IB_IA_DIRECT_DATA	R/O	Direct Data output from IA block	0x0
17	IB_LOOP_REC	R/W	Receive enable for BiDi loop (a.k.a. PAD loop o. Tx->Rx loop). Is or'ed with primary input: ib_pad_loop_ena_i. Disable test generator 'ib_tstgen_ena' if input loop is used	0x0
16	IB_LOOP_DRV	R/W	Drive enable for BiDi loop (a.k.a. Input loop o. Rx->Tx loop). Is or'ed with primary input: ib_inp_loop_ena_i. Is overruled by PAD loop.	0x0

Table 306 • **SD10G65 IB Configuration register 10 JTAG related setting *(continued)***

Bit	Name	Access	Description	Default
10	IB_JTAG_OUT_P	R/O	JTAG debug p-output	0x0
9	IB_JTAG_OUT_N	R/O	JTAG debug n-output	0x0
8:4	IB_JTAG_THRES	R/W	JTAG debug threshold 0: 0mV 1: 10mV 31: 310mV	0x08
3	IB_JTAG_IN_P	R/W	JTAG debug p-input	0x0
2	IB_JTAG_IN_N	R/W	JTAG debug n-input	0x0
1	IB_JTAG_CLK	R/W	JTAG debug clk	0x0
0	IB_JTAG_ENA	R/W	JTAG debug enable	0x0

2.5.4.12 SD10G65 IB Configuration 11 JTAG Related Setting

Short Name:SD10G65_IB_CFG11

Address:0x1F12B

Configuration register 11 for SD10G65 IB.

Table 307 • **SD10G65 IB Configuration 11 JTAG Related Setting**

Bit	Name	Access	Description	Default
15:12	IB_DFE_ISEL	R/W	DFE Bias current settings (bit-group is gated with IB_DFE_ENA) 0: DFE disabled 1: Minimum current 15: Maximum current	0x7
11	IB_ENA_400_INP	R/W	Increase current in first stage (only available in 1.2 Volt mode)	0x0
10:6	IB_TC_DFE	R/W	Gain temperature coefficient for DFE stage	0x0C
5:1	IB_TC_EQ	R/W	Gain temperature coefficient for AGC stage	0x0C

2.5.4.13 SD10G65 SBUS Rx CFG Service-Bus Related Setting

Short Name:SD10G65_SBUS_RX_CFG

Address:0x1F12C

Configuration register for Service-Bus related setting. Note: SBUS configuration applies for Rx/Tx aggregates only, any configuration applied to SBUS_TX_CFG (output buffer cfg space) will be ignored.

Table 308 • **SD10G65 SBUS Rx CFG Service-Bus Related Setting**

Bit	Name	Access	Description	Default
12	SBUS_LOOPDRV_ENA	R/W	Enable BiDi loop driver for F2DF testing	0x0

Table 308 • **SD10G65 SBUS Rx CFG Service-Bus Related Setting *(continued)***

Bit	Name	Access	Description	Default
11:8	SBUS_ANAOUT_SEL	R/W	Analog test output 0: I0_ctrlspeed[0] 1: vbulk 2: nref 3: vref820m 4: vddfilt 5: vddfilt 6: ie_aout 7: ib_aout 8: ob_aout2 9: pll_frange 10: pll_srange 11: pll_vreg820m_tx 12: pll_vreg820m_rx 13: ob_aout_n 14: ob_aout_p 15: vddfilt	0x0
7	SBUS_ANAOUT_EN	R/W	Enable analog test output multiplexer	0x0
6:3	SBUS_RCOMP	R/W	Offset value for BIAS resistor calibration (2-complement) 1000: -8 1111: -1 0000: 0 0111: 7	0x0
2:1	SBUS_BIAS_SPEED_SEL	R/W	Bias speed selection 0: Below 4Gbps 1: 4Gbps to 6Gbps 2: 6Gbps to 9Gbps 3: Above 9Gbps	0x3
0	SBUS_BIAS_EN	R/W	Bias enable 1: Enable 0: Disable	0x0

2.5.5 SD10G65 Rx RCPLL Configuration and Status

Configuration and status register set for SD10G65 Rx RCPLL

2.5.5.1 SD10G65 Rx RCPLL Configuration 0

Short Name:SD10G65_RX_RCPLL_CFG0

Address:0x1F130

Configuration register 0 for SD10G65 Rx RCPLL.

Table 309 • **SD10G65 Rx RCPLL Configuration 0**

Bit	Name	Access	Description	Default
25:16	PLLF_START_CNT	R/W	Preload value of the ramp up counter, reduces ramp up time for higher frequencies	0x002

Table 309 • **SD10G65 Rx RCPLL Configuration 0 *(continued)***

Bit	Name	Access	Description	Default
9:7	PLLF_RAMP_MODE_SEL	R/W	Sets the ramp characteristic of the FSM, higher values give faster ramp up but less accuracy, 0: normal (default) ramping 1: faster ramping 2: fastest ramping 3: slow ramping uses all possible values of r_ctrl	0x0
5	RESERVED	R/W	Must be set to its default.	0x1
4	RESERVED	R/W	Must be set to its default.	0x1
0	PLLF_ENA	R/W	Enable RCPLL FSM	0x0

2.5.5.2 SD10G65 Rx RCPLL Configuration 1

Short Name:SD10G65_RX_RCPLL_CFG1

Address:0x1F131

Configuration register 1 for SD10G65 Rx RCPLL.

Table 310 • **SD10G65 Rx RCPLL Configuration 1**

Bit	Name	Access	Description	Default
31:16	PLLF_REF_CNT_END	R/W	Target value: 1/vco_frq * par.bit.width * 512 * ref_clk_frq	0x00C6
13:4	RESERVED	R/W	Must be set to its default.	0x002
1:0	RESERVED	R/W	Must be set to its default.	0x1

2.5.5.3 SD10G65 Rx RCPLL Configuration 2

Short Name:SD10G65_RX_RCPLL_CFG2

Address:0x1F132

Configuration register 2 for SD10G65 Rx RCPLL.

Table 311 • **SD10G65 Rx RCPLL Configuration 2**

Bit	Name	Access	Description	Default
23:20	RESERVED	R/W	Must be set to its default.	0x3
16	RESERVED	R/W	Must be set to its default.	0x1
15	RESERVED	R/W	Must be set to its default.	0x1
14	RESERVED	R/W	Must be set to its default.	0x1
13	RESERVED	R/W	Must be set to its default.	0x1
12:11	PLL_LPF_CUR	R/W	Select charge pump current, 0: 50uA 1: 100uA 2: 150uA 3: 200uA	0x3

Table 311 • **SD10G65 Rx RCPLL Configuration 2 *(continued)***

Bit	Name	Access	Description	Default
10:7	PLL_LPF_RES	R/W	Select loop filter resistor value, 0: not allowed 1: 2400 2: 1600 3: 960 4: 1200 5: 800 6: 685 7: 533 8: 800 9: 600 10: 533 11: 436 12: 480 13: 400 14: 369 15: 320	0xA
6:2	RESERVED	R/W	Must be set to its default.	0x1F
0	PLL_ENA	R/W	Enable analog RCPLL part	0x0

2.5.5.4 SD10G65 Rx RCPLL Status 0

Short Name:SD10G65_RX_RCPLL_STAT0

Address:0x1F133

Status register 0 for SD10G65 Rx RCPLL.

Table 312 • **SD10G65 Rx RCPLL Status 0**

Bit	Name	Access	Description	Default
31	PLLF_LOCK_STAT	R/O	PLL lock status, 0: not locked 1: locked	0x0

2.5.6 SD10G65 Rx SYNTH Configuration and Status

Configuration and status register set for SD10G65 Rx SYNTH

2.5.6.1 SD10G65 Rx Synthesizer Configuration 0

Short Name:SD10G65_RX_SYNTH_CFG0

Address:0x1F140

Configuration register 0 for SD10G65 Rx SYNTH.

Table 313 • **SD10G65 Rx Synthesizer Configuration 0**

Bit	Name	Access	Description	Default
21:18	RESERVED	R/W	Must be set to its default.	0xF
17:16	SYNTH_FBDIV_SEL	R/W	selects feedback divider setting. 0: divide by 1 1: divide by 2 2: divide by 4 3: reserved	0x1

Table 313 • **SD10G65 Rx Synthesizer Configuration 0 *(continued)***

Bit	Name	Access	Description	Default
15:14	SYNTH_FB_STEP	R/W	selects step width for sync output	0x0
12:11	SYNTH_I2_STEP	R/W	selects step width for integrator2	0x0
9	SYNTH_I2_ENA	R/W	enable contribution of integral2 part	0x1
8	SYNTH_I1_STEP	R/W	selects step width for integrator1	0x0
6	SYNTH_P_STEP	R/W	selects step width for proportional	0x0
4	SYNTH_SPEED_SEL	R/W	Selects circuit speed. 0: for settings with synth_fbdiv_sel = 2 1: for setting with synth_fbdiv_sel less than 2	0x1
3	SYNTH_HRATE_ENA	R/W	enables half rate mode	0x0
1	RESERVED	R/W	Must be set to its default.	0x1
0	SYNTH_ENA	R/W	synthesizer enable	0x0

2.5.6.2 SD10G65 Rx Synthesizer Configuration 1

Short Name:SD10G65_RX_SYNTH_CFG1

Address:0x1F141

Configuration register 1 for SD10G65 Rx SYNTH.

Table 314 • **SD10G65 Rx Synthesizer Configuration 1**

Bit	Name	Access	Description	Default
25:22	RESERVED	R/W	Must be set to its default.	0x4
21:8	SYNTH_FREQ_MULT	R/W	frequency multiplier	0x2100
7:4	SYNTH_FREQM_1	R/W	frequency m setting bits 35:32	0x0
3:0	SYNTH_FREQN_1	R/W	frequency n setting bits 35:32	0x8

2.5.6.3 SD10G65 Rx Synthesizer Configuration 2

Short Name:SD10G65_RX_SYNTH_CFG2

Address:0x1F142

Configuration register 2 for SD10G65 Rx SYNTH.

Table 315 • **SD10G65 Rx Synthesizer Configuration 2**

Bit	Name	Access	Description	Default
31	SYNTH_SKIP_BIT_FWD	R/W	Rising edge triggers bit skip forward in serial data stream. Used to align data to parallel interface boundaries.	0x0
30	SYNTH_SKIP_BIT_REV	R/W	Rising edge triggers bit skip reverse in serial data stream. Used to align data to parallel interface boundaries.	0x0
27:26	SYNTH_DV_CTRL_I2E	R/W	Controls the data valid behavior for the CDRLF I2 enable function: b0 = 0 => external signal controls, 1 => b1 controls	0x0

Table 315 • **SD10G65 Rx Synthesizer Configuration 2 *(continued)***

Bit	Name	Access	Description	Default
25:24	SYNTH_DV_CTRL_I1M	R/W	Controls the data valid behavior for the CDRLF I1 max function: b0 = 0 => external signal controls, 1 => b1 controls	0x0
23:22	SYNTH_DV_CTRL_I1E	R/W	Controls the data valid behavior for the CDRLF I1 enable function: b0 = 0 => external signal controls, 1 => b1 controls	0x0
21:20	SYNTH_DV_CTRL_MD	R/W	Controls the data valid behavior for the moebdiv select function: b0 = 0 => external signal controls, 1 => b1 controls	0x0
18	SYNTH_CPMD_DIG_SEL	R/W	Cp/md dig select. Coding 0: select Bit 0/5 as cp/md (FX100 mode); 1: use cp/md from core	0x0
17	SYNTH_CPMD_DIG_ENA	R/W	uses cp/md selected via synth_cpmd_dig_sel instead of cp/md from sample stage	0x0
16	SYNTH_AUX_ENA	R/W	enables clock for VScope / APC auxiliary data channels	0x1
14:8	SYNTH_PHASE_DATA	R/W	relationship phase center/edge	0x08
6:0	SYNTH_PHASE_AUX	R/W	relationship phase center/aux	0x08

2.5.6.4 SD10G65 Rx Synthesizer Configuration 3

Short Name:SD10G65_RX_SYNTH_CFG3

Address:0x1F143

Configuration register 3 for SD10G65 Rx SYNTH.

Table 316 • **SD10G65 Rx Synthesizer Configuration 3**

Bit	Name	Access	Description	Default
31:0	SYNTH_FREQM_0	R/W	frequency m setting bits 31:0	0x00000000

2.5.6.5 SD10G65 Rx Synthesizer Configuration 4

Short Name:SD10G65_RX_SYNTH_CFG4

Address:0x1F144

Configuration register 4 for SD10G65 Rx SYNTH.

Table 317 • **SD10G65 Rx Synthesizer Configuration 4**

Bit	Name	Access	Description	Default
31:0	SYNTH_FREQN_0	R/W	frequency n setting bits 31:0	0x00000000

2.5.6.6 SD10G65 Rx Synthesizer Register CDR loopfilter Control

Short Name:SD10G65_RX_SYNTH_CDRLF

Address:0x1F145

Register for CDR loopfilter control for SD10G65 Rx SYNTH.

Table 318 • **SD10G65 Rx Synthesizer Register CDR loopfilter Control**

Bit	Name	Access	Description	Default
31	SYNTH_INTEG3_ENA	R/W	Enables integrator 3	0x0
30:26	SYNTH_INTEG3_DSEL	R/W	Select filter damping / gain peaking when integrator 3 is enabled. The control value is interpreted as signed value. Positive values increase the damping, i.e. lowering the gain peaking; negative values decease the damping, i.e. raising the gain peaking. The allowed programming range depends on the SYNTH_INTEG2_FSEL setting: 0 <= (SYNTH_INTEG2_FSEL - SYNTH_INTEG3_DSEL) <= 53. SYNTH_INTEG2_FSEL - SYNTH_INTEG3_DSEL = 0 and SYNTH_INTEG2_FSEL - SYNTH_INTEG3_DSEL = 1 gives the same damping.	0x00
25:21	SYNTH_INTEG1_MAX1	R/W	max value of integrator 1 during normal operation	0x02
20:16	SYNTH_INTEG1_MAX0	R/W	max value of integrator 1 during init phase	0x00
15:11	SYNTH_INTEG1_LIM	R/W	limit of integrator 1	0x02
10:6	SYNTH_INTEG1_FSEL	R/W	frequency select of integrator 1	0x02
5:0	SYNTH_INTEG2_FSEL	R/W	frequency select of integrator 2	0x31

2.5.6.7 SD10G65 Rx Synthesizer 0 for Qualifier Access

Short Name:SD10G65_RX_SYNTH_QUALIFIER0

Address:0x1F146

Register 0 for qualifier access for SD10G65 Rx SYNTH.

Table 319 • **SD10G65 Rx Synthesizer 0 for Qualifier Access**

Bit	Name	Access	Description	Default
20	SYNTH_CAPTURE_QUAL	R/W	Rising edge captures qualifier for readback	0x0
19:16	SYNTH_QUAL_I2_MSB	R/O	MS Bits of captured integrator 2	0x0
15:0	SYNTH_QUAL_I1	R/O	Captured integrator 1 value	0x0000

2.5.6.8 SD10G65 Rx Synthesizer 1 for Qualifier Access

Short Name:SD10G65_RX_SYNTH_QUALIFIER1

Address:0x1F147

Register 1 for qualifier access for SD10G65 Rx SYNTH.

Table 320 • **SD10G65 Rx Synthesizer 1 for Qualifier Access**

Bit	Name	Access	Description	Default
31:0	SYNTH_QUAL_I2_LSB	R/O	LS Bits of captured integrator 2	0x00000000

2.5.6.9 SD10G65 Rx Synthesizer for Sync Control Data

Short Name:SD10G65_RX_SYNTH_SYNC_CTRL

Address:0x1F148

Register 0 for sync control data for SD10G65 Rx SYNTH.

Table 321 • **SD10G65 Rx Synthesizer for Sync Control Data**

Bit	Name	Access	Description	Default
3:0	SYNTH_SC_SYNC_TIMER_SEL	R/W	Selects the synchronization period for the I2 value via sync control bus. Must be disabled (0) when sync control test generator is used. Coding in 312.5MHz clock cycles: 0: disabled, 1: 2^6, 2: 2^7, .., 15: 2^20.	0xF

2.5.6.10 F2DF Configuration / Status

Short Name:F2DF_CFG_STAT

Address:0x1F149

Configuration / status register for the F2DF control logic.

Table 322 • **F2DF Configuration / Status**

Bit	Name	Access	Description	Default
27:25	F2DF_SAMPLE_DIV	R/W	Sampling divider: sample every 2^f2df_sample_div parallel data word.	0x0
21:17	F2DF_SIDE_DET_BIT_SEL	R/W	Select bit from input data used for side detection. Debug feature: '31' select constant zero, '30' select constant one.	0x00
16:14	F2DF_SIDE_DET_ONES_WEIGHT	R/W	Sample '1' => increment 8bit filter saturating counter by 2**n. Cnt >= 0xC0 => ProperSide detected.	0x0
13:11	F2DF_SIDE_DET_ZEROS_WEIGHT	R/W	Sample '0' => decrement 8bit filter saturating counter by 2**n. Cnt < 0x40 => WrongSide detected.	0x0
9:4	F2DF_TOG_DET_CNT	R/W	Determines the number of samples that have to show at least one toggle.	0x00
3	F2DF_DATA_VALID_PROPPER_SIDE	R/W	Data valid value in "ProperSide" state. '0': data valid flagged only in "Lock" state; '1' data valid also flagged in "ProperSide" state.	0x0
0	F2DF_ENABLE	R/W	F2df enable. Enabling the f2df circuit automatically switches the input of the CDR-loop to the f2df control block (overrules synth_cpmd_dig_sel and synth_cpmd_dig_ena) and replaces the data valid signal from the core logic by the data valid signal generated by the f2df control logic.	0x0

2.5.7 SD10G65 Tx SYNTH Configuration and Status

Configuration and status register set for SD10G65 Tx SYNTH

2.5.7.1 SD10G65 Tx Synthesizer Configuration 0

Short Name:SD10G65_TX_SYNTH_CFG0

Address:0x1F150

Configuration register 0 for SD10G65 Tx SYNTH.

Table 323 • **SD10G65 Tx Synthesizer Configuration 0**

Bit	Name	Access	Description	Default
25:23	RESERVED	R/W	Must be set to its default.	0x3
22:18	RESERVED	R/W	Must be set to its default.	0x17
17:16	SYNTH_FBDIV_SEL	R/W	selects feedback divider setting	0x2
13:11	SYNTH_CS_SPEED	R/W	comon sync speed	0x0
10	SYNTH_LS_SPEED	R/W	lane sync speed	0x0
8	SYNTH_LS_ENA	R/W	lane sync enable	0x1
7	SYNTH_DS_SPEED	R/W	dig. sync speed	0x0
5	SYNTH_DS_ENA	R/W	dig. sync enable	0x0
4	SYNTH_SPEED_SEL	R/W	Selects circuit speed. Coding: 0 for settings with synth_fbdiv_sel = 2; 1 for setting with synth_fbdiv_sel smaller than 2.	0x0
3	SYNTH_HRATE_ENA	R/W	half rate enable	0x0
2	RESERVED	R/W	Must be set to its default.	0x1
1	RESERVED	R/W	Must be set to its default.	0x1
0	SYNTH_ENA	R/W	synthesizer enable	0x0

2.5.7.2 SD10G65 Tx Synthesizer Configuration 1

Short Name:SD10G65_TX_SYNTH_CFG1

Address:0x1F151

Configuration register 1 for SD10G65 Tx SYNTH.

Table 324 • **SD10G65 Tx Synthesizer Configuration 1**

Bit	Name	Access	Description	Default
25:22	RESERVED	R/W	Must be set to its default.	0x4
21:8	SYNTH_FREQ_MULT	R/W	frequency multiplier	0x2100
7:4	SYNTH_FREQM_1	R/W	frequency m setting bits 35:32	0x0
3:0	SYNTH_FREQN_1	R/W	frequency n setting bits 35:32	0x8

2.5.7.3 SD10G65 Tx Synthesizer Configuration 3

Short Name:SD10G65_TX_SYNTH_CFG3

Address:0x1F152

Configuration register 3 for SD10G65 Tx SYNTH.

Table 325 • **SD10G65 Tx Synthesizer Configuration 3**

Bit	Name	Access	Description	Default
31:0	SYNTH_FREQM_0	R/W	frequency m setting bits 31:0	0x00000000

2.5.7.4 SD10G65 Tx Synthesizer Configuration 4

Short Name:SD10G65_TX_SYNTH_CFG4

Address:0x1F153

Configuration register 4 for SD10G65 Tx SYNTH.

Table 326 • **SD10G65 Tx Synthesizer Configuration 4**

Bit	Name	Access	Description	Default
31:0	SYNTH_FREQN_0	R/W	frequency n setting bits 31:0	0x00000000

2.5.7.5 SD10G65 SSC Generator Configuration 0

Short Name:SD10G65_SSC_CFG0

Address:0x1F154

Configuration register 0 for SD10G65 SSC generator.

Table 327 • **SD10G65 SSC Generator Configuration 0**

Bit	Name	Access	Description	Default
31:19	SSC_MOD_LIM	R/W	SSC modulation amplitude limiter	0x0000
18:7	SSC_MOD_PERIOD	R/W	SSC modulation period / amplitude.	0x000
6:1	SSC_MOD_FREQ	R/W	SSC modulation frequency fine tuning control	0x00
0	SSC_ENA	R/W	SSC generator enable.	0x0

2.5.7.6 SD10G65 SSC Generator Configuration 1

Short Name:SD10G65_SSC_CFG1

Address:0x1F155

Configuration register 1 for SD10G65 SSC generator.

Table 328 • **SD10G65 SSC Generator Configuration 1**

Bit	Name	Access	Description	Default
29	MLD_SYNC_SRC_SEL	R/W	Select between the internal and external MLD phase detector: 0: internal; 1: external	0x0
28:25	MLD_SYNC_CTRL	R/W	Control of the internal MLD phase detector: b0: enable; b1: enable hyst. b2: enable window function; b3: select window size	0x0
24:23	MLD_SYNC_CLK_SEL	R/W	Select the MLD clock source for the internal MLD phase detector	0x0
22	SYNC_CTRL_WRAP_INHIBIT	R/W	Controls integrator 2 replica behavior: '0': wrapping; '1': saturating.	0x0
21:16	SYNC_CTRL_FSEL	R/W	Frequency select of integrator 2 replica used for lane sync.	0x31

Table 328 • **SD10G65 SSC Generator Configuration 1 *(continued)***

Bit	Name	Access	Description	Default
10	SMOOTH_ENA	R/W	Enables Smooth generator	0x0
9:5	SSC_SD_GAIN	R/W	SSC sigma delta gain.	0x00
4:3	SSC_SYNC_POS	R/W	SSC modulation start position on synchronization trigger	0x0
2:0	SSC_MOD_MUL	R/W	SSC modulation period multiplier encoded 2**n: 0 => 1; 1 => 2; 2 => 4, 3 => 8 ...	0x0

2.5.8 SD10G65 Tx RCPLL Configuration and Status

Configuration and status register set for SD10G65 Tx RCPLL

2.5.8.1 SD10G65 Tx RCPLL Configuration 0

Short Name:SD10G65_TX_RCPLL_CFG0

Address:0x1F160

Configuration register 0 for SD10G65 Tx RCPLL.

Table 329 • **SD10G65 Tx RCPLL Configuration 0**

Bit	Name	Access	Description	Default
25:16	PLLF_START_CNT	R/W	Preload value of the ramp up counter, reduces ramp up time for higher frequencies	0x002
9:7	PLLF_RAMP_MODE_SEL	R/W	Sets the ramp characteristic of the FSM, higher values give faster ramp up but less accuracy, 0: normal (default) ramping 1: faster ramping 2: fastest ramping 3: slow ramping uses all possible values of r_ctrl	0x0
5	RESERVED	R/W	Must be set to its default.	0x1
4	RESERVED	R/W	Must be set to its default.	0x1
0	PLLF_ENA	R/W	Enable RCPLL FSM	0x0

2.5.8.2 SD10G65 Tx RCPLL Configuration 1

Short Name:SD10G65_TX_RCPLL_CFG1

Address:0x1F161

Configuration register 1 for SD10G65 Tx RCPLL.

Table 330 • **SD10G65 Tx RCPLL Configuration 1**

Bit	Name	Access	Description	Default
31:16	PLLF_REF_CNT_END	R/W	Target value: 1/vco_frq * par.bit.width * 512 * ref_clk_frq	0x00C6
13:4	RESERVED	R/W	Must be set to its default.	0x002
1:0	RESERVED	R/W	Must be set to its default.	0x1

2.5.8.3 SD10G65 Tx RCPLL Configuration 2

Short Name:SD10G65_TX_RCPLL_CFG2

Address:0x1F162

Configuration register 2 for SD10G65 Tx RCPLL.

Table 331 • **SD10G65 Tx RCPLL Configuration 2**

Bit	Name	Access	Description	Default
23:20	RESERVED	R/W	Must be set to its default.	0x3
16	RESERVED	R/W	Must be set to its default.	0x1
15	RESERVED	R/W	Must be set to its default.	0x1
14	RESERVED	R/W	Must be set to its default.	0x1
13	RESERVED	R/W	Must be set to its default.	0x1
12:11	PLL_LPF_CUR	R/W	Select charge pump current, 0: 50uA 1: 100uA 2: 150uA 3: 200uA	0x3
10:7	PLL_LPF_RES	R/W	Select loop filter resistor value, 0: not allowed 1: 2400 2: 1600 3: 960 4: 1200 5: 800 6: 685 7: 533 8: 800 9: 600 10: 533 11: 436 12: 480 13: 400 14: 369 15: 320	0xA
6:2	RESERVED	R/W	Must be set to its default.	0x1F
0	PLL_ENA	R/W	Enable analog RCPLL part	0x0

2.5.8.4 SD10G65 Tx RCPLL Status 0

Short Name:SD10G65_TX_RCPLL_STAT0

Address:0x1F163

Status register 0 for SD10G65 Tx RCPLL.

Table 332 • **SD10G65 Tx RCPLL Status 0**

Bit	Name	Access	Description	Default
31	PLLF_LOCK_STAT	R/O	PLL lock status, 0: not locked 1: locked	0x0

2.6 HOST_PMA (Device 0x9)

Table 333 • **DEV1_IEEE_PMA_CONTROL**

Address	Short Description	Register Name	Details
0x90000	PMA Control 1	PMA_CONTROL_1	Page 151

Table 334 • **DEV1_IEEE_PMA_STATUS**

Address	Short Description	Register Name	Details
0x90001	PMA Status 1	PMA_STATUS_1	Page 151

Table 335 • **DEV1_IEEE_PMA_PMD_STATUS**

Address	Short Description	Register Name	Details
0x90008	PMA Status 2	PMA_STATUS_2	Page 151

Table 336 • **DEV1_IEEE_PMD_CONTROL_AND_STATUS**

Address	Short Description	Register Name	Details
0x9000A	PMA Status 3	PMA_STATUS_3	Page 152

Table 337 • **KR_FEC_ABILITY**

Address	Short Description	Register Name	Details
0x900AA	KR FEC Ability	KR_FEC_ABILITY	Page 152

Table 338 • **KR_FEC_CONTROL_1**

Address	Short Description	Register Name	Details
0x900AB	KR FEC Control 1	KR_FEC_CONTROL_1	Page 152

Table 339 • **KR_FEC_STATUS**

Address	Short Description	Register Name	Details
0x900AC	KR FEC Corrected Lower	KR_FEC_CORRECTED_LOWER	Page 153
0x900AD	KR FEC Corrected Upper	KR_FEC_CORRECTED_UPPER	Page 153
0x900AE	KR FEC Uncorrected Lower	KR_FEC_UNCORRECTED_LOWER	Page 154
0x900AF	KR FEC Uncorrected Upper	KR_FEC_UNCORRECTED_UPPER	Page 154

Table 340 • **KR_FEC_CONTROL_2**

Address	Short Description	Register Name	Details
0x98300	KR FEC Control 2	KR_FEC_Control_2	Page 155

Table 341 • **LOOPBACK_CONTROL**

Address	Short Description	Register Name	Details
0x9A003	Datapath Loopback Control	PMA_LOOPBACK_CTRL	Page 155

Table 342 • **BYPASS_CONFIG_STAT**

Address	Short Description	Register Name	Details
0x9A020	Repeater Mode Configuration	BYPASS_CFG1	Page 156
0x9A021	Bypass Status	BYPASS_STATUS	Page 156
0x9A022	Bypass Interrupt Enable	BYPASS_INTR_EN	Page 156
0x9A023	Bypass Interrupt	BYPASS_INTR	Page 156

Table 343 • **Vendor_Specific_PMA_Control_2**

Address	Short Description	Register Name	Details
0x9A100	Vendor Specific PMA Control 2	Vendor_Specific_PMA_Control_2	Page 157

Table 344 • **SPARE_RW_REGISTERS**

Address	Short Description	Register Name	Details
0x9AEF0	Device1 Spare R/W 0	DEV1_SPARE_RW0	Page 158
0x9AEF1	Device1 Spare R/W 1	DEV1_SPARE_RW1	Page 159
0x9AEF2	Device1 Spare R/W 2	DEV1_SPARE_RW2	Page 159
0x9AEF3	Device1 Spare R/W 3	DEV1_SPARE_RW3	Page 159
0x9AEF4	Device1 Spare R/W 4	DEV1_SPARE_RW4	Page 159
0x9AEF5	Device1 Spare R/W 5	DEV1_SPARE_RW5	Page 159
0x9AEF6	Device1 Spare R/W 6	DEV1_SPARE_RW6	Page 159
0x9AEF7	Device1 Spare R/W 7	DEV1_SPARE_RW7	Page 160
0x9AEF8	Device1 Spare R/W 8	DEV1_SPARE_RW8	Page 160
0x9AEF9	Device1 Spare R/W 9	DEV1_SPARE_RW9	Page 160
0x9AEFA	Device1 Spare R/W 10	DEV1_SPARE_RW10	Page 160
0x9AEFB	Device1 Spare R/W 11	DEV1_SPARE_RW11	Page 160
0x9AEFC	Device1 Spare R/W 12	DEV1_SPARE_RW12	Page 161
0x9AEFD	Device1 Spare R/W 13	DEV1_SPARE_RW13	Page 161
0x9AEFE	Device1 Spare R/W 14	DEV1_SPARE_RW14	Page 161
0x9AEFF	Device1 Spare R/W 15	DEV1_SPARE_RW15	Page 161

Table 345 • **SD10G65_VScope2**

Address	Short Description	Register Name	Details
0x9B000	VScope Main Config A	VSCOPE_MAIN_CFG_A	Page 161
0x9B001	VScope Main Config B	VSCOPE_MAIN_CFG_B	Page 162
0x9B002	VScope Main Config C	VSCOPE_MAIN_CFG_C	Page 163
0x9B003	VScope Pattern Lock Config A	VSCOPE_PAT_LOCK_CFG_A	Page 163
0x9B004	VScope Pattern Lock Config B	VSCOPE_PAT_LOCK_CFG_B	Page 163
0x9B005	VScope HW Scan Config 1A	VSCOPE_HW_SCAN_CFG_1A	Page 164
0x9B006	VScope HW Scan Config 1B	VSCOPE_HW_SCAN_CFG_1B	Page 164
0x9B007	VScope HW Config 2A	VSCOPE_HW_SCAN_CFG_2A	Page 164
0x9B008	VScope HW Config 2B	VSCOPE_HW_SCAN_CFG_2B	Page 165
0x9B009	VScope Status	VSCOPE_STAT	Page 165
0x9B00A	VScope Counter A	VSCOPE_CNT_A	Page 165
0x9B00B	VScope Counter B	VSCOPE_CNT_B	Page 166
0x9B00C	VScope General Purpose A	VSCOPE_DBG_LSB_A	Page 166
0x9B00D	VScope General Purpose B	VSCOPE_DBG_LSB_B	Page 166

Table 346 • **SD10G65_DFT**

Address	Short Description	Register Name	Details
0x9B100	SD10G65 DFT Main Configuration 1	DFT_RX_CFG_1	Page 166
0x9B101	SD10G65 DFT Main Configuration 2	DFT_RX_CFG_2	Page 167
0x9B102	SD10G65 DFT Pattern Mask Configuration 1	DFT_RX_MASK_CFG_1	Page 168
0x9B103	SD10G65 DFT Pattern Mask Configuration 2	DFT_RX_MASK_CFG_2	Page 168
0x9B104	SD10G65 DFT Pattern Checker Configuration 1	DFT_RX_PAT_CFG_1	Page 169
0x9B105	SD10G65 DFT Pattern Checker Configuration 2	DFT_RX_PAT_CFG_2	Page 169
0x9B106	SD10G65 DFT BIST Configuration 0A	DFT_BIST_CFG0A	Page 169
0x9B107	SD10G65 DFT BIST Configuration 0B	DFT_BIST_CFG0B	Page 169
0x9B108	SD10G65 DFT BIST Configuration 1A	DFT_BIST_CFG1A	Page 170
0x9B109	SD10G65 DFT BIST Configuration 1B	DFT_BIST_CFG1B	Page 170
0x9B10A	SD10G65 DFT BIST Configuration 2A	DFT_BIST_CFG2A	Page 170
0x9B10B	SD10G65 DFT BIST Configuration 2B	DFT_BIST_CFG2B	Page 170
0x9B10C	SD10G65 DFT BIST Configuration 3A	DFT_BIST_CFG3A	Page 171
0x9B10D	SD10G65 DFT BIST Configuration 3B	DFT_BIST_CFG3B	Page 171
0x9B10E	SD10G65 DFT Error Status 1	DFT_ERR_STAT_1	Page 171
0x9B10F	SD10G65 DFT Error Status 2	DFT_ERR_STAT_2	Page 171
0x9B110	SD10G65 DFT PRBS Status 1	DFT_PRBS_STAT_1	Page 171
0x9B111	SD10G65 DFT PRBS Status 2	DFT_PRBS_STAT_2	Page 172
0x9B112	SD10G65 DFT Miscellaneous Status 1	DFT_MAIN_STAT_1	Page 172
0x9B113	SD10G65 DFT Miscellaneous Status 2	DFT_MAIN_STAT_2	Page 172

Table 346 • **SD10G65_DFT *(continued)***

Address	Short Description	Register Name	Details
0x9B114	SD10G65 DFT Main Configuration	DFT_TX_CFG	Page 173
0x9B115	SD10G65 DFT Tx Constant Pattern Configuration 1	DFT_TX_PAT_CFG_1	Page 173
0x9B116	SD10G65 DFT Tx Constant Pattern Configuration 2	DFT_TX_PAT_CFG_2	Page 174
0x9B117	SD10G65 DFT Tx Constant Pattern Status	DFT_TX_CMP_DAT_STAT	Page 174
0x9B118	DFT Clock Compare Config	DFT_CLK_CMP_CFG	Page 174
0x9B119	DFT Clock Compare Timer A	DFT_CLK_CMP_TIMERA	Page 175
0x9B11A	DFT Clock Compare Timer B	DFT_CLK_CMP_TIMERB	Page 175
0x9B11B	DFT Clock Comparison Value A	DFT_CLK_CMP_VALUEA	Page 175
0x9B11C	DFT Clock Comparison Value B	DFT_CLK_CMP_VALUEB	Page 176
0x9B11D	DFT Clock Comparison Maximum Value A	DFT_CLK_CMP_MAXVALA	Page 176
0x9B11E	DFT Clock Comparison Maximum Value B	DFT_CLK_CMP_MAXVALB	Page 176
0x9B11F	DFT Tx Error Insertion Configuration 1	DFT_TX_ERR_INSERT_CFG_1	Page 177
0x9B120	DFT Tx Error Insertion Configuration 2	DFT_TX_ERR_INSERT_CFG_2	Page 177
0x9B121	DFT Clock Generator Configuration 1	DFT_CLK_GEN_CFG_1	Page 177
0x9B122	DFT Clock Generator Configuration 2	DFT_CLK_GEN_CFG_2	Page 178
0x9B123	DFT Clock Generator Configuration 3	DFT_CLK_GEN_CFG_3	Page 178

Table 347 • **ROMENG_1**

Address	Short Description	Register Name	Details
0x9B200 - 0x9B286	SPI Address Field of ROM Table Entry (x135)	spi_adr	Page 178
0x9B300 - 0x9B386	Lower 16 bits of SPI Data Field of ROM Table Entry (x135)	data_lsw	Page 179
0x9B400 - 0x9B486	Upper 16 bits of SPI Data Field of ROM Table Entry (x135)	data_msw	Page 179

Table 348 • **ROMENG_2**

Address	Short Description	Register Name	Details
0x9B600	ROM Table Start/End Addresses of Tx 10G Setting Routine	adr_tx10g	Page 179
0x9B601	ROM Table Start/End Addresses of Rx 10G setting Routine	adr_rx10g	Page 179
0x9B602	ROM Table Start/End Addresses of Tx 1G Setting Routine	adr_tx1g	Page 179
0x9B603	ROM Table Start/End Addresses of Rx 1G Setting Routine	adr_rx1g	Page 180
0x9B604	ROM Table Start/End Addresses of WAN Setting Routine	adr_wan	Page 180

Table 349 • **ROMENG_STATUS**

Address	Short Description	Register Name	Details
0x9B6FF	ROM Engine Status	ROMENG_STATUS	Page 180

2.6.1 PMA IEEE Configuration and Status

2.6.1.1 PMA Control 1

Short Name:PMA_CONTROL_1

Address:0x90000

Table 350 • **PMA Control 1**

Bit	Name	Access	Description	Default
15	RST	One-shot	MDIO Manageable Device (MMD) software reset. This register resets functions associated exclusively with the host side PMA. Data path logic and configuration registers are reset. This register is self-clearing. 0: Normal operation 1: Reset	0x0
0	EN_PAD_LOOP	R/W	Enable PMA Pad Loopback L0 0: Disable 1: Enable	0x0

2.6.1.2 PMA Status 1

Short Name:PMA_STATUS_1

Address:0x90001

Table 351 • **PMA Status 1**

Bit	Name	Access	Description	Default
7	FAULT	R/O	Indicates a fault condition for this interface in either the transmit or the receive paths. 0: Fault condition not detected. Latch-high alarm status bits TRANSMIT_FAULT=0 AND RECEIVE_FAULT=0. 1: Fault condition detected. Latch-high alarm status bits TRANSMIT_FAULT=1 OR RECEIVE_FAULT=1.	0x0
2	RECEIVE_LINK_STATUS	R/O	Indicates the receive link status for this interface. This is a sticky bit that latches the low state. The latch-low bit is cleared when the register is read. 0: PMA/PMD receive link down 1: PMA/PMD receive link up	0x1

2.6.1.3 PMA Status 2

Short Name:PMA_STATUS_2

Address:0x90008

Table 352 • **PMA Status 2**

Bit	Name	Access	Description	Default
11	TRANSMIT_FAULT	R/O	Indicates a fault condition on this interface's transmit path. This is a sticky bit that latches the high state. The latch-high bit is cleared when the register is read. 0: No fault condition on transmit path 1: Fault condition on transmit path	0x0
10	RECEIVE_FAULT	R/O	Indicates a fault condition on this interface's receive path.This is a sticky bit that latches the high state. The latch-high bit is cleared when the register is read. 0: No fault condition on receive path 1: Fault condition on receive path	0x0

2.6.1.4 PMA Status 3

Short Name:PMA_STATUS_3

Address:0x9000A

Table 353 • **PMA Status 3**

Bit	Name	Access	Description	Default
0	GLOBAL_PMD_RECEIVE_SIGNAL_DETECT	R/O	Host PMA receiver signal detect 0: Signal not detected by receiver 1: Signal detected by receiver	0x0

2.6.2 KR FEC IEEE Configuration and Status

2.6.2.1 KR FEC Ability

Short Name:KR_FEC_ABILITY

Address:0x900AA

Table 354 • **KR FEC Ability**

Bit	Name	Access	Description	Default
1	FEC_error_indication_ability	R/O	FEC error reporting ability 0: This PHY device is not able to report FEC decoding errors to the PCS layer. 1: This PHY device is able to report FEC decoding errors to the PCS layer.	0x1
0	FEC_ability	R/O	FEC ability 0: This PHY device does not support FEC. 1: This PHY device supports FEC.	0x1

2.6.2.2 KR FEC Control 1

Short Name:KR_FEC_CONTROL_1

Address:0x900AB

Table 355 • **KR FEC Control 1**

Bit	Name	Access	Description	Default
1	FEC_enable_error_indication	R/W	0: Decoding errors have no effect on PCS sync bits 1: Enable decoder to indicate errors to PCS sync bits	0x0
0	FEC_enable	R/W	FEC enable 0: Disable FEC 1: Enable FEC	0x0

2.6.2.3 KR FEC Corrected Lower

Short Name:KR_FEC_CORRECTED_LOWER

Address:0x900AC

Table 356 • **KR FEC Corrected Lower**

Bit	Name	Access	Description	Default
15:0	FEC_CORRECTED_BLOCKS_LOWER	R/O	The FEC corrected block count is split across two registers, KR_FEC_corrected_lower and KR_FEC_corrected_upper. KR_FEC_corrected_lower contains the least significant 16 bits of the count. KR_FEC_corrected_upper contains the most significant 16 bits of the count. Reading address KR_FEC_corrected_lower latches the 16 most significant bits of the counter in KR_FEC_corrected_upper for future read out. The block count register is cleared when KR_FEC_corrected_lower is read.	0x0000

2.6.2.4 KR FEC Corrected Upper

Short Name:KR_FEC_CORRECTED_UPPER

Address:0x900AD

Table 357 • **KR FEC Corrected Upper**

Bit	Name	Access	Description	Default
15:0	FEC_CORRECTED_BLOCKS_UPPER	R/O	The FEC corrected block count is split across two registers, KR_FEC_corrected_lower and KR_FEC_corrected_upper. KR_FEC_corrected_lower contains the least significant 16 bits of the count. KR_FEC_corrected_upper contains the most significant 16 bits of the count. Reading address KR_FEC_corrected_lower latches the 16 most significant bits of the counter in KR_FEC_corrected_upper for future read out. The block count register is cleared when KR_FEC_corrected_lower is read.	0x0000

2.6.2.5 KR FEC Uncorrected Lower

Short Name:KR_FEC_UNCORRECTED_LOWER

Address:0x900AE

Table 358 • **KR FEC Uncorrected Lower**

Bit	Name	Access	Description	Default
15:0	FEC_UNCORRECTED_BLOCKS_LOWER	R/O	The FEC uncorrectable block count is split across two registers, KR_FEC_uncorrected_lower and KR_FEC_uncorrected_upper. KR_FEC_uncorrected_lower contains the least significant 16 bits of the count. KR_FEC_uncorrected_upper contains the most significant 16 bits of the count. Reading address KR_FEC_uncorrected_lower latches the 16 most significant bits of the counter in KR_FEC_uncorrected_upper for future read out. The block count register is cleared when KR_FEC_uncorrected_lower is read.	0x0000

2.6.2.6 KR FEC Uncorrected Upper

Short Name:KR_FEC_UNCORRECTED_UPPER

Address:0x900AF

Table 359 • **KR FEC Uncorrected Upper**

Bit	Name	Access	Description	Default
15:0	FEC_UNCORRECTED_BLOCKS_UPPER	R/O	The FEC uncorrectable block count is split across two registers, KR_FEC_uncorrected_lower and KR_FEC_uncorrected_upper. KR_FEC_uncorrected_lower contains the least significant 16 bits of the count. KR_FEC_uncorrected_upper contains the most significant 16 bits of the count. Reading address KR_FEC_uncorrected_lower latches the 16 most significant bits of the counter in KR_FEC_uncorrected_upper for future read out. The block count register is cleared when KR_FEC_uncorrected_lower is read.	0x0000

2.6.3 KR FEC Vendor Specific Configuration and Status

Vendor specific configuration and status register set for KR FEC Block

2.6.3.1 KR FEC Control 2

Short Name:KR_FEC_Control_2

Address:0x98300

Table 360 • **KR_FEC_Control_2**

Bit	Name	Access	Description	Default
1	fec_inframe	R/O	FEC in frame lock indication. This is a sticky bit that latches the low state. The latch-low bit is cleared when the register is read. 0: FEC has not achieved lock 1: FEC has achieved lock	0x1
0	fec_rstmon	R/W	FEC counters reset 0: no effect 1: reset FEC counters	0x0

2.6.4 Data Path Controls

2.6.4.1 Datapath Loopback Control

Short Name:PMA_LOOPBACK_CTRL

Address:0x9A003

Datapath Loopback Control

Table 361 • **Datapath Loopback Control**

Bit	Name	Access	Description	Default
0	L3_CONTROL	R/W	Loopback L3 Enable 0 = Normal Operation 1 = Enable L3 Loopback	0x0

2.6.5 Repeater Mode Configuration

2.6.5.1 Repeater Mode Configuration

Short Name:BYPASS_CFG1

Address:0x9A020

Table 362 • **Repeater Mode Configuration**

Bit	Name	Access	Description	Default
8	FIFO_RESET	One-shot	Reset the bypass FIFO 0 = Normal operation 1 = RESET	0x0
7:4	RESERVED	R/W	Must be set to its default.	0x4
2	RESERVED	R/W	Must be set to its default.	0x1
1	REPEATER_FIFO_EN	R/W	Enable bypass FIFO 0 = FIFO Disabled 1 = FIFO Enabled	0x0
0	REPEATER_MODE_EN	R/W	Enable repeater mode. This causes the transmit multiplexor to select bypass data rather than data from the processing core 0 = Standard mode 1 = Repeater Mode	0x0

2.6.5.2 Byass Status

Short Name:BYPASS_STATUS

Address:0x9A021

Table 363 •

Bit	Name	Access	Description	Default
1	FIFO_UNDERFLOW_STAT	R/O	FIFO Underflow state	0x0
0	FIFO_OVERFLOW_STAT	R/O	FIFO Overflow state	0x0

2.6.5.3 Bypass Interrupt Enable

Short Name:BYPASS_INTR_EN

Address:0x9A022

Table 364 •

Bit	Name	Access	Description	Default
1	FIFO_UNDERFLOW_INTR_EN	R/W	Allow FIFO_UNDERFLOW_STICKY to propagate to interrupt	0x0
0	FIFO_OVERFLOW_INTR_EN	R/W	Enable FIFO_OVERFLOW_STICKY to propagate to interrupt	0x0

2.6.5.4 Bypass Interrupt

Short Name:BYPASS_INTR

Address:0x9A023

Table 365 •

Bit	Name	Access	Description	Default
1	FIFO_UNDERFLOW_STICKY	Sticky		0x0
0	FIFO_OVERFLOW_STICKY	Sticky	FIFO overflow occurred	0x0

2.6.6 Vendor Specific PMA Controls

2.6.6.1 Vendor Specific PMA Control 2

Short Name: Vendor_Specific_PMA_Control_2

Address:0x9A100

Table 366 • **Vendor Specific PMA Control 2**

Bit	Name	Access	Description	Default
10	Suppress_LOS_detection	R/W	LOS circuitry is driven by a signal detection status signal in the line-side input buffer. The signal detection alarm driving the LOS circuitry can be squelched with this register bit. LOS detection is 0: Allowed 1: Suppressed	0x0
9	Suppress_LOL_detection	R/W	LOL circuitry is driven by a status signal in the line-side CRU. The status signal driving the LOL circuitry can be squelched with this register bit. LOL detection is 0: Allowed 1: Suppressed	0x0

2.6.7 PMA Status and Interrupts

2.6.7.1 PMA_STAT

Short Name:PMA_STAT

Address:0x9A202

Table 367 • **PMA Status**

Bit	Name	Access	Description	Default
2	TX_LOL_STAT	R/O	Current state of Tx LOL from SerDes 0 = Tx PLL Locked 1 = Tx PLL Not locked	0x0
1	RX_LOL_STAT	R/O	Current state of Rx LOL from SerDes 0 = Rx PLL Locked 1 = Rx PLL Not locked	0x0
0	RX_LOS_STAT	R/O	LOS detected at Serdes 0 = Signal detected at input receiver 1 = No signal detected at input receiver	0x0

2.6.7.2 PMA Interrupt Mask

Short Name:PMA_INTR_MASK

Address:0x9A203

Table 368 • **PMA Interrupt Mask**

Bit	Name	Access	Description	Default
2	TX_LOL_INTR_EN	R/W	Enable interrupt when Tx LOL detected 0 = Detected Tx LOL condition not propagated to interrupt 1 = Detected Tx LOL condition is propagated to interrupt	0x0
1	RX_LOL_INTR_EN	R/W	Enable interrupt when Rx LOL detected 0 = Detected Rx LOL condition not propagated to interrupt 1 = Detected Rx LOL condition is propagated to interrupt	0x0
0	RX_LOS_INTR_EN	R/W	Enable interrupt when Rx LOS detected 0 = Detected LOS condition not propagated to interrupt 1 = Detected LOS condition is propagated to interrupt	0x0

2.6.7.3 PMA Interrupt Status

Short Name:PMA_INTR_STAT

Address:0x9A204

Table 369 • **PMA Interrupt Status**

Bit	Name	Access	Description	Default
2	TX_LOL_STICKY	Sticky	Tx LOL Detected 0 = No Tx LOL detected since last cleared 1 = Tx LOL Detected since last cleared	0x0
1	RX_LOL_STICKY	Sticky	Rx LOL Detected 0 = No Rx LOL detected since last cleared 1 = Rx LOL Detected since last cleared	0x0
0	RX_LOS_STICKY	Sticky	Rx LOS Detected 0 = No Rx LOS detected since last cleared 1 = Rx LOS Detected since last cleared	0x0

2.6.8 Spare R/W Registers

Spare R/W registers intended to be used by firmware.

2.6.8.1 Device1 Spare R/W 0

Short Name:DEV1_SPARE_RW0

Address:0x9AEF0

Table 370 • **Device1 Spare R/W 0**

Bit	Name	Access	Description	Default
15:0	dev1_spare_rw0	R/W	Spare	0x0000

2.6.8.2 Device1 Spare R/W 1

Short Name:DEV1_SPARE_RW1

Address:0x9AEF1

Table 371 • **Device1 Spare R/W 1**

Bit	Name	Access	Description	Default
15:0	dev1_spare_rw1	R/W	Spare	0x0000

2.6.8.3 Device1 Spare R/W 2

Short Name:DEV1_SPARE_RW2

Address:0x9AEF2

Table 372 • **Device1 Spare R/W 2**

Bit	Name	Access	Description	Default
15:0	dev1_spare_rw2	R/W	Spare	0x0000

2.6.8.4 Device1 Spare R/W 3

Short Name:DEV1_SPARE_RW3

Address:0x9AEF3

Table 373 • **Device1 Spare R/W 3**

Bit	Name	Access	Description	Default
15:0	dev1_spare_rw3	R/W	Spare	0x0000

2.6.8.5 Device1 Spare R/W 4

Short Name:DEV1_SPARE_RW4

Address:0x9AEF4

Table 374 • **Device1 Spare R/W 4**

Bit	Name	Access	Description	Default
15:0	dev1_spare_rw4	R/W	Spare	0x0000

2.6.8.6 Device1 Spare R/W 5

Short Name:DEV1_SPARE_RW5

Address:0x9AEF5

Table 375 • **Device1 Spare R/W 5**

Bit	Name	Access	Description	Default
15:0	dev1_spare_rw5	R/W	Spare	0x0000

2.6.8.7 Device1 Spare R/W 6

Short Name:DEV1_SPARE_RW6

Address:0x9AEF6

Table 376 • **Device1 Spare R/W 6**

Bit	Name	Access	Description	Default
15:0	dev1_spare_rw6	R/W	Spare	0x0000

2.6.8.8 Device1 Spare R/W 7

Short Name:DEV1_SPARE_RW7

Address:0x9AEF7

Table 377 • **Device1 Spare R/W 7**

Bit	Name	Access	Description	Default
15:0	dev1_spare_rw7	R/W	Spare	0x0000

2.6.8.9 Device1 Spare R/W 8

Short Name:DEV1_SPARE_RW8

Address:0x9AEF8

Table 378 • **Device1 Spare R/W 8**

Bit	Name	Access	Description	Default
15:0	dev1_spare_rw8	R/W	Spare	0x0000

2.6.8.10 Device1 Spare R/W 9

Short Name:DEV1_SPARE_RW9

Address:0x9AEF9

Table 379 • **Device1 Spare R/W 9**

Bit	Name	Access	Description	Default
15:0	dev1_spare_rw9	R/W	Spare	0x0000

2.6.8.11 Device1 Spare R/W 10

Short Name:DEV1_SPARE_RW10

Address:0x9AEFA

Table 380 • **Device1 Spare R/W 10**

Bit	Name	Access	Description	Default
15:0	dev1_spare_rw10	R/W	Spare	0x0000

2.6.8.12 Device1 Spare R/W 11

Short Name:DEV1_SPARE_RW11

Address:0x9AEFB

Table 381 • **Device1 Spare R/W 11**

Bit	Name	Access	Description	Default
15:0	dev1_spare_rw11	R/W	Spare	0x0000

2.6.8.13 Device1 Spare R/W 12

Short Name:DEV1_SPARE_RW12

Address:0x9AEFC

Table 382 • **Device1 Spare R/W 12**

Bit	Name	Access	Description	Default
15:0	dev1_spare_rw12	R/W	Spare	0x0000

2.6.8.14 Device1 Spare R/W 13

Short Name:DEV1_SPARE_RW13

Address:0x9AEFD

Table 383 • **Device1 Spare R/W 13**

Bit	Name	Access	Description	Default
15:0	dev1_spare_rw13	R/W	Spare	0x0000

2.6.8.15 Device1 Spare R/W 14

Short Name:DEV1_SPARE_RW14

Address:0x9AEFE

Table 384 • **Device1 Spare R/W 14**

Bit	Name	Access	Description	Default
15:0	dev1_spare_rw14	R/W	Spare	0x0000

2.6.8.16 Device1 Spare R/W 15

Short Name:DEV1_SPARE_RW15

Address:0x9AEFF

Table 385 • **Device1 Spare R/W 15**

Bit	Name	Access	Description	Default
15:0	dev1_spare_rw15	R/W	Spare	0x0000

2.6.9 SD10G65 VScope Configuration and Status

Configuration and status register set for SD10G65 VScope

2.6.9.1 VScope Main Config A

Short Name:VSCOPE_MAIN_CFG_A

Address:0x9B000

VScope main configuration register A

Table 386 • **VScope Main Config A**

Bit	Name	Access	Description	Default
8	SYN_PHASE_WR_DIS	R/W	Disables writing of synth_phase_aux in synthesizer	0x0
7	IB_AUX_OFFS_WR_DIS	R/W	Disables writing of ib_auxl_offset and ib_auxh_offset in IB	0x0
6	IB_JUMP_ENA_WR_DIS	R/W	Disables writing of ib_jumpl_ena and ib_jumph_ena in IB	0x0
5:3	CNT_OUT_SEL	R/W	Counter output selection 0-3: error counter 0-3 4: hit counter 5: clock counter 6: 8 LSBs of error counter 3-1 and hit counter 7: 8 LSBs of error counter 3-0	0x0
2:0	COMP_SEL	R/W	Comparator input selection [REF] 0 1: auxL 4 5: auxH 2 7: main; [SUB] 5 7: auxL 0 2: auxH 1 4: main (3 6: reserved)	0x0

2.6.9.2 VScope Main Config B

Short Name:VSCOPE_MAIN_CFG_B

Address:0x9B001

VScope main configuration register B

Table 387 • **VScope Main Config B**

Bit	Name	Access	Description	Default
9:8	GP_SELECT	R/W	Select GP reg input 0: rx (main)	0x0
7	GP_REG_FREEZE	R/W	Allows to freeze the GP register value to assure valid reading	0x0
6:5	SCAN_LIM	R/W	Scan limit, selects which counter saturation limits the other counters 0: clock counter 1: hit counter 2: error counters 3: no limit	0x0
4:0	PRELOAD_VAL	R/W	Preload value for error counter	0x00

2.6.9.3 VScope Main Config C

Short Name:VSCOPE_MAIN_CFG_C

Address:0x9B002

VScope main configuration register C

Table 388 • **VScope Main Config C**

Bit	Name	Access	Description	Default
12	INTR_DIS	R/W	Disable interrupt output	0x0
11	TRIG_ENA	R/W	Enable trigger	0x0
10	QUICK_SCAN	R/W	Counter enable (bit 4) implicitly done by reading the counter; unused in hw-scan mode	0x0
9:5	COUNT_PER	R/W	Counter period: preload value for clock counter	0x00
4	CNT_ENA	R/W	Enable Counting; unused in hw-scan mode	0x0
3:1	IF_MODE	R/W	Interface Width 0: 8 bit 1: 10 bit 2: 16 bit 3: 20 bit 4: 32 bit 5: 40 bit others: reserved	0x0
0	VSCOPE_ENA	R/W	Enable VScope	0x0

2.6.9.4 VScope pattern lock Config A

Short Name:VSCOPE_PAT_LOCK_CFG_A

Address:0x9B003

VScope pattern lock configuration register A

Table 389 • **VScope pattern lock Config A**

Bit	Name	Access	Description	Default
14:10	PRELOAD_HIT_CNT	R/W	Preload value for hit counter	0x00
9:0	DC_MASK	R/W	Don't Care mask: Enable history mask usage. 0: enable history mask bit 1: history mask bit is "don't care"	0x3FF

2.6.9.5 VScope pattern lock Config B

Short Name:VSCOPE_PAT_LOCK_CFG_B

Address:0x9B004

VScope pattern lock configuration register B

Table 390 • **VScope pattern lock Config B**

Bit	Name	Access	Description	Default
9:0	HIST_MASK	R/W	History mask: Respective sequence is expected in reference input (comp_sel); if enabled (dc_mask) before hit and error counting is enabled	0x000

2.6.9.6 VScope HW Scan Config 1A

Short Name:VSCOPE_HW_SCAN_CFG_1A

Address:0x9B005

VScope HW scan configuration register 1A

Table 391 • **VScope HW Scan Config 1A**

Bit	Name	Access	Description	Default
13	PHASE_JUMP_INV	R/W	Invert the jumph_ena and jumpl_ena bit in HW scan mode	0x0
12:8	AMPL_OFFS_VAL	R/W	Offset between AuxL amplitude (reference) and AuxH amplitude, signed (2s-complement), +- 1/4 amplitude max.	0x00
7:0	MAX_PHASE_INCR_VAL	R/W	Maximum phase increment value before wrapping	0xFF

2.6.9.7 VScope HW Scan Config 1B

Short Name:VSCOPE_HW_SCAN_CFG_1B

Address:0x9B006

VScope HW scan configuration register 1B

Table 392 • **VScope HW Scan Config 1B**

Bit	Name	Access	Description	Default
15:10	MAX_AMPL_INCR_VAL	R/W	Maximum amplitude increment value before wrapping	0x3F
9:7	PHASE_INCR	R/W	Phase increment per scan step Increment = phase_incr + 1	0x0
6:4	AMPL_INCR	R/W	Amplitude increment per scan step Increment = ampl_incr + 1	0x0
3:2	NUM_SCANS_PER_ITR	R/W	Number of scans per iteration in N-point-scan mode 0: 1 1: 2 2: 4 3: 8	0x2
1:0	HW_SCAN_ENA	R/W	Enables HW scan with N results per scan or fast-scan 0: off 1: N-point scan 2: fast-scan (sq) 3: fast-scan (diag)	0x0

2.6.9.8 VScope HW Config 2A

Short Name:VSCOPE_HW_SCAN_CFG_2A

Address:0x9B007

VScope HW scan configuration register 2A

Table 393 • **VScope HW Config 2A**

Bit	Name	Access	Description	Default
15:13	FAST_SCAN_THRES	R/W	Threshold for error_counter in fast-scan modeN+1	0x0
12:8	FS_THRES_SHIFT	R/W	Left shift for threshold of error_counter in fast-scan mode threshold = (fast_scan_thres+1) shift_left fs_thres_shift	0x00
7:0	PHASE_JUMP_VAL	R/W	Value at which jumpl_ena and jumph_ena in IB must be toggled	0x00

2.6.9.9 VScope HW Config 2B

Short Name:VSCOPE_HW_SCAN_CFG_2B

Address:0x9B008

VScope HW scan configuration register 2B

Table 394 • **VScope HW Config 2B**

Bit	Name	Access	Description	Default
15	AUX_AMPL_SYM_DIS	R/W	Disable IB amplitude symmetry compensation for AuxH and AuxL	0x0
13:8	AMPL_START_VAL	R/W	Start value for VScope amplitude in N-point-scan mode and fast-scan mode (before IB amplitude symmetry compensation)	0x00
7:0	PHASE_START_VAL	R/W	Start value for VScope phase in N-point-scan mode and fast-scan mode	0x00

2.6.9.10 VScope Status

Short Name:VSCOPE_STAT

Address:0x9B009

VScope status register

Table 395 • **VScope Status**

Bit	Name	Access	Description	Default
15:8	GP_REG_MSB	R/O	8 MSBs of general purpose register	0x00
7:4	FAST_SCAN_HIT	R/O	Fast scan mode: Indicator per cursor position whether threshold was reached	0x0
0	DONE_STICKY	R/O	Done sticky	0x0

2.6.9.11 VScope Counter A

Short Name:VSCOPE_CNT_A

Address:0x9B00A

VScope counter register A

Table 396 • **VScope Counter A**

Bit	Name	Access	Description	Default
15:0	COUNTER_MSB	R/O	Counter value higher 16-bit MSB [31:16]	0x0000

2.6.9.12 VScope Counter B

Short Name:VSCOPE_CNT_B

Address:0x9B00B

VScope counter register B

Table 397 • **VScope Counter B**

Bit	Name	Access	Description	Default
15:0	COUNTER_LSB	R/O	Counter value lower 16-bit LSB [15:0]	0x0000

2.6.9.13 VScope General Purpose A

Short Name:VSCOPE_DBG_LSB_A

Address:0x9B00C

VScope general purpose register A

Table 398 • **VScope General Purpose A**

Bit	Name	Access	Description	Default
15:0	GP_REG_LSB_A	R/O	16 bit MSB of a 32 bit general purpose register [31:16]	0x0000

2.6.9.14 VScope General Purpose A

Short Name:VSCOPE_DBG_LSB_B

Address:0x9B00D

VScope general purpose register B

Table 399 • **VScope General Purpose A**

Bit	Name	Access	Description	Default
15:0	GP_REG_LSB_B	R/O	16 bit LSB of a 32 bit general purpose register [15:0]	0x0000

2.6.10 SD10G65 DFT Configuration and Status

Configuration and status register set for SD10G65 DFT

2.6.10.1 SD10G65 DFT Main Configuration 1

Short Name:DFT_RX_CFG_1

Address:0x9B100

Main configuration register 1 for SD10G65 DFT.

Table 400 • **SD10G65 DFT Main Configuration 1**

Bit	Name	Access	Description	Default
12	STUCK_AT_PAR_MASK_CFG	R/W	Disables error generation based on stuck_at_par errors, 0: stuck_at_par error generates 63 errors per clock cycle (in PRBS mode only) 1: stuck_at_par error does not generate errors	0x1
11	STUCK_AT_01_MASK_CFG	R/W	Disables error generation based on stuck_at_01 errors, 0: stuck_at_01 error generates 63 errors per clock cycle (in PRBS mode only) 1: stuck_at_01 error does not generate errors	0x0
10	DIRECT_THROUGH_ENA_CFG	R/W	Enables data through from gearbox to gearbox	0x0
9	ERR_CNT_CAPT_CFG	R/W	Captures data from error counter to allow reading of stable data	0x0
8:7	RX_DATA_SRC_SEL	R/W	Data source selection 0: main path 1: vscope high path 2: vscope low path	0x0
6:5	BIST_CNT_CFG	R/W	States in which error counting is enabled 3:all but IDLE; 2:check 1:stable+check 0:wait_stable+stable+check	0x0
4	FREEZE_PATTERN_CFG	R/W	Disable change of stored patterns (e.g. to avoid changes during read-out)	0x0
3	CHK_MODE_CFG	R/W	Selects pattern to check 0: PRBS pattern 1: constant pattern	0x0
2:0	RX_WID_SEL_CFG	R/W	Selects DES interface width 0:8 1:10 2:16 3:20 4:32 5:40 (default)	0x4

2.6.10.2 SD10G65 DFT Main Configuration 2

Short Name:DFT_RX_CFG_2

Address:0x9B101

Main configuration register 2 for SD10G65 DFT.

Table 401 • **SD10G65 DFT Main Configuration 2**

Bit	Name	Access	Description	Default
14	RX_WORD_MODE_CFG	R/W	Pattern generator: 0:bytes mode; 1:10-bits word mode	0x0

Table 401 • **SD10G65 DFT Main Configuration 2 *(continued)***

Bit	Name	Access	Description	Default
13:11	RX_PRBS_SEL_CFG	R/W	Selects PRBS check 0: prbs7 1: prbs15 2: prbs23 3: prbs11 4: prbs31 (default) 5: prbs9	0x4
10	INV_ENA_CFG	R/W	Enables PRBS checker input inversion	0x0
9	CMP_MODE_CFG	R/W	Selects compare mode 0: compare mode possible 1 learn mode is forced	0x0
8:6	LRN_CNT_CFG	R/W	Number of consecutive errors/non-errors before transitioning to respective state value = num-40-bits-words + 1	0x0
5	CNT_RST	R/W	SW reset of error counter; rising edge activates reset	0x0
4:3	CNT_CFG	R/W	Selects modes in which error counter is active 0:learn and compare mode 1:transition between modes 2:learn mode 3:compare mode	0x0
2:1	BIST_MODE_CFG	R/W	BIST mode 0: off 1: BIST 2: BER 3:CONT (infinite mode)	0x3
0	DFT_RX_ENA	R/W	Enable Rx DFT capability 0: Disable DFT 1: Enable DFT	0x0

2.6.10.3 SD10G65 DFT Pattern Mask Configuration 1

Short Name:DFT_RX_MASK_CFG_1

Address:0x9B102

Configuration register 1 for SD10G65 DFT to mask data bits preventing error counting for these bits.

Table 402 • **SD10G65 DFT Pattern Mask Configuration 1**

Bit	Name	Access	Description	Default
15:0	LSB_MASK_CFG_1	R/W	Mask out (active high) errors in 16 bit MSB data bits [31:16]	0x0000

2.6.10.4 SD10G65 DFT pattern mask Configuration 2

Short Name:DFT_RX_MASK_CFG_2

Address:0x9B103

Configuration register 2 for SD10G65 DFT to mask data bits preventing error counting for these bits.

Table 403 • **SD10G65 DFT Pattern Mask Configuration 2**

Bit	Name	Access	Description	Default
15:0	LSB_MASK_CFG_2	R/W	Mask out (active high) errors in 16 LSB data bits [15:0]	0x0000

2.6.10.5 SD10G65 DFT Pattern Checker Configuration 1

Short Name:DFT_RX_PAT_CFG_1

Address:0x9B104

Pattern checker configuration register 1 for SD10G65 DFT.

Table 404 • **SD10G65 DFT Pattern Checker Configuration 1**

Bit	Name	Access	Description	Default
15:8	MSB_MASK_CFG	R/W	Mask out (active high) errors in 8 MSB data bits	0x00
0	PAT_READ_CFG	R/W	Pattern read enable	0x0

2.6.10.6 SD10G65 DFT Pattern Checker Configuration 2

Short Name:DFT_RX_PAT_CFG_2

Address:0x9B105

Pattern checker configuration register 2 for SD10G65 DFT.

Table 405 • **SD10G65 DFT Pattern Checker Configuration 2**

Bit	Name	Access	Description	Default
11:8	MAX_ADDR_CHK_CFG	R/W	Maximum address in Checker (before continuing with address 0)	0x0
3:0	READ_ADDR_CFG	R/W	Address to read patterns from used by SW	0x0

2.6.10.7 SD10G65 DFT BIST Configuration A

Short Name:DFT_BIST_CFG0A

Address:0x9B106

BIST configuration register A for SD10G65 DFT controlling 'check and wait-stable' mode.

Table 406 • **SD10G65 DFT BIST Configuration A**

Bit	Name	Access	Description	Default
15:0	WAKEUP_DLY_CFG	R/W	BIST FSM: threshold to leave DOZE state	0x0000

2.6.10.8 SD10G65 DFT BIST Configuration B

Short Name:DFT_BIST_CFG0B

Address:0x9B107

BIST configuration register B for SD10G65 DFT controlling 'check and wait-stable' mode.

Table 407 • **SD10G65 DFT BIST Configuration B**

Bit	Name	Access	Description	Default
15:0	MAX_BIST_FRAMES_CFG	R/W	BIST FSM: threshold to enter FINISHED state	0x0000

2.6.10.9 SD10G65 DFT BIST Configuration A

Short Name:DFT_BIST_CFG1A

Address:0x9B108

BIST configuration register A for SD10G65 DFT controlling 'stable' mode.

Table 408 • **SD10G65 DFT BIST Configuration A**

Bit	Name	Access	Description	Default
15:0	MAX_UNSTABLE_CYC_CFG	R/W	BIST FSM: threshold to iterate counter for max_stable_attempts	0x0000

2.6.10.10 SD10G65 DFT BIST Configuration B

Short Name:DFT_BIST_CFG1B

Address:0x9B109

BIST configuration register B for SD10G65 DFT controlling 'stable' mode.

Table 409 • **SD10G65 DFT BIST Configuration B**

Bit	Name	Access	Description	Default
15:0	STABLE_THRES_CFG	R/W	BIST FSM: threshold to enter CHECK state	0x0000

2.6.10.11 SD10G65 DFT BIST Configuration A

Short Name:DFT_BIST_CFG2A

Address:0x9B10A

BIST configuration register B for SD10G65 DFT controlling frame length in 'check' mode.

Table 410 • **SD10G65 DFT BIST Configuration A**

Bit	Name	Access	Description	Default
15:0	FRAME_LEN_CFG_MSB	R/W	BIST FSM: threshold to iterate counter for max_bist_frames [31:16]	0x0000

2.6.10.12 SD10G65 DFT BIST Configuration B

Short Name:DFT_BIST_CFG2B

Address:0x9B10B

BIST configuration register B for SD10G65 DFT controlling frame length in 'check' mode.

Table 411 • **SD10G65 DFT BIST Configuration B**

Bit	Name	Access	Description	Default
15:0	FRAME_LEN_CFG_LSB	R/W	BIST FSM: threshold to iterate counter for max_bist_frames [15:0]	0x0000

2.6.10.13 SD10G65 DFT BIST Configuration A

Short Name:DFT_BIST_CFG3A

Address:0x9B10C

BIST configuration register A for SD10G65 DFT controlling stable attempts in ' wait-stable' mode.

Table 412 • **SD10G65 DFT BIST Configuration A**

Bit	Name	Access	Description	Default
15:0	MAX_STABLE_ATTEMPTS_CFG_MSB	R/W	BIST FSM: threshold to enter SYNC_ERR state [31:16]	0x0000

2.6.10.14 SD10G65 DFT BIST Configuration B

Short Name:DFT_BIST_CFG3B

Address:0x9B10D

BIST configuration register B for SD10G65 DFT controlling stable attempts in ' wait-stable' mode.

Table 413 • **SD10G65 DFT BIST Configuration B**

Bit	Name	Access	Description	Default
15:0	MAX_STABLE_ATTEMPTS_CFG_LSB	R/W	BIST FSM: threshold to enter SYNC_ERR state [15:0]	0x0000

2.6.10.15 SD10G65 DFT Error Status 1

Short Name:DFT_ERR_STAT_1

Address:0x9B10E

Status register 1 for SD10G65 DFT containing the error counter value

Table 414 • **SD10G65 DFT Error Status 1**

Bit	Name	Access	Description	Default
15:0	ERR_CNT_MSB	R/O	Counter output depending on cnt_cfg [31:16]	0x0000

2.6.10.16 SD10G65 DFT Error Status 2

Short Name:DFT_ERR_STAT_2

Address:0x9B10F

Status register B2 for SD10G65 DFT containing the error counter value

Table 415 • **SD10G65 DFT Error Status 2**

Bit	Name	Access	Description	Default
15:0	ERR_CNT_LSB	R/O	Counter output depending on cnt_cfg [15:0]	0x0000

2.6.10.17 SD10G65 DFT PRBS Status 1

Short Name:DFT_PRBS_STAT_1

Address:0x9B110

Status register 1 for SD10G65 DFT containing the PRBS data related to 1st sync lost event

Table 416 • **SD10G65 DFT PRBS Status 1**

Bit	Name	Access	Description	Default
15:0	PRBS_DATA_STAT_MSB	R/O	PRBS data after first sync lost [31:16]	0x0000

2.6.10.18 SD10G65 DFT PRBS Status 2

Short Name:DFT_PRBS_STAT_2

Address:0x9B111

Status register 2 for SD10G65 DFT containing the PRBS data related to 1st sync lost event

Table 417 • **SD10G65 DFT PRBS Status 2**

Bit	Name	Access	Description	Default
15:0	PRBS_DATA_STAT_LSB	R/O	PRBS data after first sync lost [15:0]	0x0000

2.6.10.19 SD10G65 DFT Miscellaneous Status 1

Short Name:DFT_MAIN_STAT_1

Address:0x9B112

Status register 1 for SD10G65 DFT

Table 418 • **SD10G65 DFT Miscellaneous Status 1**

Bit	Name	Access	Description	Default
9:0	CMP_DATA_STAT	R/O	10 bits data word at address 'read_addr_cfg' used for further observation by SW	0x000

2.6.10.20 SD10G65 DFT Miscellaneous Status 2

Short Name:DFT_MAIN_STAT_2

Address:0x9B113

Status register 2 for SD10G65 DFT

Table 419 • **SD10G65 DFT Miscellaneous Status 2**

Bit	Name	Access	Description	Default
5	STUCK_AT_PAR	R/O	Data input is unchanged for all 40 parallel bits for at least 7 clock cycles (defined by c_STCK_CNT_THRES)	0x0
4	STUCK_AT_01	R/O	Data input is constantly 0 or constantly 1 for all 40 parallel bits for at least 7 clock cycles (defined by c_STCK_CNT_THRES)	0x0
3	NO_SYNC	R/O	BIST: no sync found since BIST enabled	0x0
2	INSTABLE	R/O	BIST: input data not stable	0x0
1	INCOMPLETE	R/O	BIST not complete (i.e. not reached stable state or following)	0x0
0	ACTIVE	R/O	BIST is active (i.e. left DOZE but did not enter a final state)	0x0

2.6.10.21 SD10G65 DFT Main Configuration

Short Name:DFT_TX_CFG

Address:0x9B114

Main configuration register for SD10G65 DFT.

Table 420 • **SD10G65 DFT Main Configuration**

Bit	Name	Access	Description	Default
12	RST_ON_STUCK_AT_CFG	R/W	Enables (1) reset of PRBS generator in case of unchanged data ('stuck-at') for at least 511 clock cycles. Can be disabled (0) e.g. in scrambler mode to avoid the very rare case that input patterns allow to keep the generator's shift register filled with a constant value.	0x1
11:9	TX_WID_SEL_CFG	R/W	Selects SER interface width 0:8 1:10 2:16 3:20 4:32 5:40 (default)	0x4
8:6	TX_PRBS_SEL_CFG	R/W	Selects PRBS generator 0: prbs7 1: prbs15 2: prbs23 3: prbs11 4: prbs31 (default) 5: prbs9	0x4
5	SCRAM_INV_CFG	R/W	Inverts the scrambler output	0x0
4	IPATH_CFG	R/W	Selects PRBS generator input 0:pat-gen 1:core	0x0
3:2	OPATH_CFG	R/W	Selects DFT-Tx output 0:PRBS/scrambler (default) 1:bypass	0x0
1	TX_WORD_MODE_CFG	R/W	Word width of constant pattern generator 0:bytes mode 1:10-bits word mode	0x0
0	DFT_TX_ENA	R/W	Enable Tx DFT capability 0: Disable DFT 1: Enable DFT	0x0

2.6.10.22 SD10G65 DFT Tx Constant Pattern Configuration 1

Short Name:DFT_TX_PAT_CFG_1

Address:0x9B115

Tx Constant MSB pattern configuration register 1 for SD10G65 DFT.

Table 421 • **SD10G65 DFT Tx Constant Pattern Configuration 1**

Bit	Name	Access	Description	Default
4	PAT_VLD_CFG	R/W	Constant patterns are valid to store	0x0

Table 421 • **SD10G65 DFT Tx Constant Pattern Configuration 1 *(continued)***

Bit	Name	Access	Description	Default
3:0	MAX_ADDR_GEN_CFG	R/W	Maximum address in generator (before continuing with address 0)	0x0

2.6.10.23 SD10G65 DFT Tx Constant Pattern Configuration 2

Short Name:DFT_TX_PAT_CFG_2

Address:0x9B116

Tx Constant MSB pattern configuration register 2 for SD10G65 DFT.

Table 422 • **SD10G65 DFT Tx Constant Pattern Configuration 2**

Bit	Name	Access	Description	Default
13:10	STORE_ADDR_CFG	R/W	Current storage address for patterns in generator	0x0
9:0	PATTERN_CFG	R/W	10 bits word of constant patterns for transmission	0x000

2.6.10.24 SD10G65 DFT Tx Constant Pattern Status

Short Name:DFT_TX_CMP_DAT_STAT

Address:0x9B117

Status register for SD10G65 DFT containing the constant patterns used for comparison (last in LEARN mode)

Table 423 • **SD10G65 DFT Tx Constant Pattern Status**

Bit	Name	Access	Description	Default
12	TX_STUCK_AT_STICKY	Sticky	Scrambler/PRBS generator output unchanged for at least 511 clock cycles. The high state is cleared by writing a 1 to the bit.	0x0
9:0	PAT_STAT	R/O	10 bits data word at address 'store_addr_cfg' used for further observation by SW	0x000

2.6.10.25 DFT Clock Compare Config

Short Name:DFT_CLK_CMP_CFG

Address:0x9B118

Configuration register for Clock Compare logic. Compared clocks are always divided by 4 before any further processing. A clock edge on tx_clk increments the counter, a clock edge on rx_clk decrements the counter. If only one clock is selected for clock comparison, the number of clock cycles within a given time can be measured.

Table 424 • **DFT Clock Compare Config**

Bit	Name	Access	Description	Default
12	CLK_CMP_UPDTOG	R/O	Clock compare value updated toggle bit. Toggles on each update of CLK_CMP_VALUE	0x0
8	CLK_CMP_WRAP_ENA	R/W	Enable clock comparison counter wrap 0: counter saturates 1: counter wraps	0x0

Table 424 • **DFT Clock Compare Config *(continued)***

Bit	Name	Access	Description	Default
7:6	CLK_CMP_DIV_TX	R/W	Clock compare divider for Tx clock 0: tx clk 1: tx_clk/2 2: tx_clk/4 3: tx_clk/8	0x3
5:4	CLK_CMP_DIV_RX	R/W	Clock compare divider for Rx clock 0: rx clk 1: rx_clk/2 2: rx_clk/4 3: rx_clk/8	0x3
3:2	CLK_CMP_SEL	R/W	Clock compare selection 0: rx_clk vs. tx_clk 1: rx_clk 2: tx_clk 3: Reserved	0x0
1	CLK_CMP_MODE	R/W	Clock comparison mode 0: single shot 1: continuous	0x0
0	CLK_CMP_ENA	R/W	Enable clock comparison (enabling automatically clears comparison counter)	0x0

2.6.10.26 DFT Clock Compare Timer A

Short Name:DFT_CLK_CMP_TIMERA

Address:0x9B119

Upper half of clock comparison timer. After timer has expired, current clock comparison value is stored. The timer is clocked at 156.25 MHz.

Table 425 • **DFT Clock Compare Timer A**

Bit	Name	Access	Description	Default
15:0	CLK_CMP_TIMER_MSB	R/W	Clock comparison timer, bits [31:16]. Counter interval is N + 1 clock cycles where the clock frequency is 156.25 MHz.	0x0950

2.6.10.27 DFT Clock Compare Timer B

Short Name:DFT_CLK_CMP_TIMERB

Address:0x9B11A

Lower half of clock comparison timer. After timer has expired, current clock comparison value is stored. The timer is clocked at 156.25 MHz.

Table 426 • **DFT Clock Compare Timer B**

Bit	Name	Access	Description	Default
15:0	CLK_CMP_TIMER_LSB	R/W	Clock comparison timer, bits [15:0]. Counter interval is N + 1 clock cycles where the clock frequency is 156.25 MHz.	0x2F8F

2.6.10.28 DFT Clock Comparison Value A

Short Name:DFT_CLK_CMP_VALUEA

Address:0x9B11B

Upper half of clock comparison result. This register is updated after clock comparison timer has expired. In continuous mode this register is periodically updated.

Table 427 • **DFT Clock Comparison Value A**

Bit	Name	Access	Description	Default
15:0	CLK_CMP_VALUE_MSB	R/O	Clock comparison value (difference between clk0 and clk1), bits [31:16]	0x0000

2.6.10.29 DFT Clock Comparison Value B

Short Name:DFT_CLK_CMP_VALUEB

Address:0x9B11C

Lower half of clock comparison result. This register is updated after clock comparison timer has expired. In continuous mode this register is periodically updated.

Table 428 • **DFT Clock Comparison Value B**

Bit	Name	Access	Description	Default
15:0	CLK_CMP_VALUE_LSB	R/O	Clock comparison value (difference between clk0 and clk1), bits [15:0]	0x0000

2.6.10.30 DFT Clock Comparison Maximum Value A

Short Name:DFT_CLK_CMP_MAXVALA

Address:0x9B11D

Upper half of clock comparison max result. Can be used to judge e.g. SSC clock deviation. This register is updated after clock comparison timer has expired. In continuous mode this register is periodically updated.

Table 429 • **DFT Clock Comparison Maximum Value A**

Bit	Name	Access	Description	Default
15:0	CLK_CMP_MAXVAL_MSB	R/O	Clock comparison max value (maximum measured difference between clk0 and clk1), bits [31:16]	0x0000

2.6.10.31 DFT Clock Comparison Maximum Value B

Short Name:DFT_CLK_CMP_MAXVALB

Address:0x9B11E

Lower half of clock comparison max result. Can be used to judge e.g. SSC clock deviation. This register is updated after clock comparison timer has expired. In continuous mode this register is periodically updated.

Table 430 • **DFT Clock Comparison Maximum Value B**

Bit	Name	Access	Description	Default
15:0	CLK_CMP_MAXVAL_LSB	R/O	Clock comparison max value (maximum measured difference between clk0 and clk1), bits [15:0]	0x0000

2.6.10.32 DFT Tx Error Insertion Configuration 1

Short Name:DFT_TX_ERR_INSERT_CFG_1

Address:0x9B11F

Configuration register for explicit error insertion into DFT driven data stream. Allows to insert expected errors to check e.g. Tx/Rx connectivity

Table 431 • **DFT Tx Error Insertion Configuration 1**

Bit	Name	Access	Description	Default
15:6	CG_TIMER_CFG	R/W	Preload value for clock generator timer	0x000
4	ERR_TRIG_ONESHOT_CFG	R/W	Trigger a single error or a burst of errors (refer to num_err_cfg) 0 to 1 (edge) activates this function	0x0
3:0	ERR_FREQ_CFG	R/W	Frequency of continuous/limited error insertion in steps of 40 bits 0: disable continuous insertion 1-15: step between 2 errors = 2^(err_freq_cfg + 5) 40 bit words (refer also to err_posit_offs_cfg)	0x0

2.6.10.33 DFT Tx Error Insertion Configuration 2

Short Name:DFT_TX_ERR_INSERT_CFG_2

Address:0x9B120

Configuration register for explicit error insertion into DFT driven data stream. Allows to insert expected errors to check e.g. Tx/Rx connectivity

Table 432 • **DFT Tx Error Insertion Configuration 2**

Bit	Name	Access	Description	Default
15:10	ERR_POSIT_CFG	R/W	Position within 40 bit word where an error is inserted by inverting the bit value 0: LSB 39: MSB 40-63: reserved	0x00
9:4	ERR_POSIT_OFFS_CFG	R/W	Offset of bit position increased per inserted error; allows 'walking' error. Offset is reset when continuous/limited error insertion is disabled or burst mode is enabled and burst insertion is finished or err_posit_offs_cfg = 0 0: disabled 1: move 1 bit (from LSB to MSB) ... 39: move 39 bit (from LSB to MSB) 40-63: reserved	0x00
3:0	NUM_ERR_CFG	R/W	limited error insertion: burst mode (err_freq_cfg must be > 0) 0: burst mode is disabled 1-15: number of errors after each error triggering = 2^(num_err_cfg + 5)	0x0

2.6.10.34 DFT Clock Generator Configuration 1

Short Name:DFT_CLK_GEN_CFG_1

Address:0x9B121

Configuration register for clock generator to build a low speed clock signal of variable length and variable duty cycle provided on all data bits simultaneously

Table 433 • **DFT Clock Generator Configuration 1**

Bit	Name	Access	Description	Default
9:0	CG_PER_CFG	R/W	(Half) clock period cfg in normal mode: high period = cg_per_cfg + cg_dcd_cfg, low period = cg_per_cfg - cg_dcd_cfg	0x000

2.6.10.35 DFT Clock Generator Configuration 2

Short Name:DFT_CLK_GEN_CFG_2

Address:0x9B122

Configuration register for clock generator to build a low speed clock signal of variable length and variable duty cycle provided on all data bits simultaneously

Table 434 • **DFT Clock Generator Configuration 2**

Bit	Name	Access	Description	Default
9:0	CG_PER_JUMP_CFG	R/W	(Half) clock period cfg in jump mode: high period = cg_per_cfg + cg_dcd_cfg, low period = cg_per_cfg - cg_dcd_cfg	0x000

2.6.10.36 DFT Clock Generator Configuration 3

Short Name:DFT_CLK_GEN_CFG_3

Address:0x9B123

Configuration register for clock generator to build a low speed clock signal of variable length and variable duty cycle provided on all data bits simultaneously

Table 435 • **DFT Clock Generator Configuration 3**

Bit	Name	Access	Description	Default
11:2	CG_DCD_CFG	R/W	Duty cycle distortion: high period = cg_per_cfg + cg_dcd_cfg, low period = cg_per_cfg - cg_dcd_cfg	0x000
1:0	CG_MODE_CFG	R/W	clock generator mode 0: normal operation cg_per_cfg controls period; 0->1 transition: after current period has finished (only) the next period is controlled by cg_per_jump_cfg afterwards normal operation 2: every N'th period the high value is replaced by a low value N is defined by cg_timer_cfg 3: every N'th period the low value is replaced by a high value N is defined by cg_timer_cfg	0x0

2.6.11 ROM Engine

2.6.11.1 SPI Address Field of ROM Table Entry ... replication_count=135

Short Name:spi_adr

Addresses:0x9B200 - 0x9B286

Table 436 • **SPI Address Field of ROM Table Entry ... replication_count=135**

Bit	Name	Access	Description	Default
6:0	spi_adr	R/W	SPI address to write	0x00

2.6.11.2 Lower 16 bits of SPI Data Field of ROM Table Entry ... replication_count=135

Short Name:data_lsw

Addresses:0x9B300 - 0x9B386

Table 437 • **Lower 16 bits of SPI Data Field of ROM Table Entry ... replication_count=135**

Bit	Name	Access	Description	Default
15:0	spi_dat_lsw	R/W	SPI data lsw	0x0000

2.6.11.3 Upper 16 bits of SPI Data Field of ROM Table Entry ... replication_count=135

Short Name:data_msw

Addresses:0x9B400 - 0x9B486

Table 438 • **Upper 16 bits of SPI Data Field of ROM Table Entry ... replication_count=135**

Bit	Name	Access	Description	Default
15:0	spi_dat_msw	R/W	SPI data msw	0x0000

2.6.11.4 ROM Table Start/End Addresses of Tx 10G Setting Routine

Short Name:adr_tx10g

Address:0x9B600

Table 439 • **ROM Table Start/End Addresses of Tx 10G Setting Routine**

Bit	Name	Access	Description	Default
15:8	adr_tx10g_start	R/W	Starting ROM address of Tx 10G routine	0x00
7:0	adr_tx10g_end	R/W	Ending ROM address of Tx 10G routine	0x10

2.6.11.5 ROM Table Start/End Addresses of Rx 10G Setting Routine

Short Name:adr_rx10g

Address:0x9B601

Table 440 • **ROM Table Start/End Addresses of Rx 10G Setting Routine**

Bit	Name	Access	Description	Default
15:8	adr_rx10g_start	R/W	Starting ROM address of Rx 10G routine	0x11
7:0	adr_rx10g_end	R/W	Ending ROM address of Rx 10G routine	0x2C

2.6.11.6 ROM Table Start/End Addresses of Tx 1G Setting Routine

Short Name:adr_tx1g

Address:0x9B602

Table 441 • **ROM Table Start/End Addresses of Tx 1G Setting Routine**

Bit	Name	Access	Description	Default
15:8	adr_tx1g_start	R/W	Starting ROM address of Tx 1G routine	0x2D
7:0	adr_tx1g_end	R/W	Ending ROM address of Tx 1G routine	0x3D

2.6.11.7 ROM table start/end addresses of Rx 1G setting routine

Short Name:adr_rx1g

Address:0x9B603

Table 442 • **ROM table start/end addresses of Rx 1G setting routine**

Bit	Name	Access	Description	Default
15:8	adr_rx1g_start	R/W	Starting ROM address of Rx 1G routine	0x3E
7:0	adr_rx1g_end	R/W	Ending ROM address of Rx 1G routine	0x59

2.6.11.8 ROM table start/end addresses of WAN setting routine

Short Name:adr_wan

Address:0x9B604

Table 443 • **ROM table start/end addresses of WAN setting routine**

Bit	Name	Access	Description	Default
15:8	adr_wan_start	R/W	Starting ROM address of WAN routine	0x5A
7:0	adr_wan_end	R/W	Ending ROM address of WAN routine	0x86

2.6.11.9 ROM Engine Status

Short Name:ROMENG_STATUS

Address:0x9B6FF

Rom Engine Status

Table 444 • **Rom Engine Status**

Bit	Name	Access	Description	Default
5:1	exe_last	R/O	Rom Engine last routine executed 00000: 10G - configured for 10G mode 00001: TX10G - Tx configured for 10G mode 00010: RX10G - Rx configured for 10G mode 00011: 1G - configured for 1G mode 00100: TX1G - Rx configured for 1G mode 00101: RX1G - Rx configured for 1G mode 00110: 3G - configured for 3G mode 00111: TX3G - Rx configured for 3G mode 01000: RX3G - Rx configured for 3G mode 01001: WAN - configured for WAN mode 01010: RST - configured to Reset condition 01011: LBON - configured for Loopback enabled 01100: LBOFF - configured for Loopback disabled 01101: LPON - LowPower mode enabled 01110: LPOFF - LowPower mode disabled 01111: RC - RCOMP routine 10000: LRON - Lock2Ref enabled 10001: LROFF - Lock2Ref disabled others: invalid	0x00
0	exe_done	R/O	Rom Engine status This is a sticky bit that latches the high state. The latch-high bit is cleared when the register is read. 0: Rom Engine has not executed a new routine since the last time this bit is read 1: Rom Engine has executed a new routine since the last time this bit is read	0x0

2.7 HOST_KR_DEV1 (Device 0x9)

Table 445 • **KR_1x0096**

Address	Short Description	Register Name	Details
0x90096	KR PMD Control	KR_1x0096	Page 185

Table 446 • **KR_1x0097**

Address	Short Description	Register Name	Details
0x90097	KR PMD Status	KR_1x0097	Page 186

Table 447 • **KR_1x0098**

Address	Short Description	Register Name	Details
0x90098	KR LP Coefficient Update	KR_1x0098	Page 186

Table 448 • **KR_1x0099**

Address	Short Description	Register Name	Details
0x90099	KR LP Status Report	KR_1x0099	Page 186

Table 449 • **KR_1x009A**

Address	Short Description	Register Name	Details
0x9009A	KR LD Coefficient Update	KR_1x009A	Page 187

Table 450 • **KR_1x009B**

Address	Short Description	Register Name	Details
0x9009B	KR LD Status Report	KR_1x009B	Page 187

Table 451 • **tr_cfg0**

Address	Short Description	Register Name	Details
0x98200	VS Training Config 0	tr_cfg0	Page 187

Table 452 • **tr_cfg1**

Address	Short Description	Register Name	Details
0x98201	VS Training Config 1	tr_cfg1	Page 187

Table 453 • **tr_cfg2**

Address	Short Description	Register Name	Details
0x98202	VS Training Config 2	tr_cfg2	Page 188

Table 454 • **tr_cfg3**

Address	Short Description	Register Name	Details
0x98203	VS Training Config 3	tr_cfg3	Page 188

Table 455 • **tr_cfg4**

Address	Short Description	Register Name	Details
0x98204	VS Training Config 4	tr_cfg4	Page 188

Table 456 • **tr_cfg5**

Address	Short Description	Register Name	Details
0x98205	VS Training Config 5	tr_cfg5	Page 188

Table 457 • **tr_cfg6**

Address	Short Description	Register Name	Details
0x98206	VS Training Config 6	tr_cfg6	Page 189

Table 458 • **tr_cfg7**

Address	Short Description	Register Name	Details
0x98207	VS Training Config 7	tr_cfg7	Page 189

Table 459 • **tr_cfg8**

Address	Short Description	Register Name	Details
0x98208	VS Training Config 8	tr_cfg8	Page 189

Table 460 • **tr_cfg9**

Address	Short Description	Register Name	Details
0x98209	VS Training Config 9	tr_cfg9	Page 189

Table 461 • **tr_gain**

Address	Short Description	Register Name	Details
0x9820A	VS Training Gain Target And Margin Values	tr_gain	Page 190

Table 462 • **tr_coef_ovrd**

Address	Short Description	Register Name	Details
0x9820B	VS Training Coefficient Update Override	tr_coef_ovrd	Page 190

Table 463 • **tr_stat_ovrd**

Address	Short Description	Register Name	Details
0x9820C	VS Training Status Report Override	tr_stat_ovrd	Page 190

Table 464 • **tr_ovrd**

Address	Short Description	Register Name	Details
0x9820D	VS Training Override	tr_ovrd	Page 190

Table 465 • **tr_step**

Address	Short Description	Register Name	Details
0x9820E	VS Training State Step	tr_step	Page 191

Table 466 • **tr_mthd**

Address	Short Description	Register Name	Details
0x9820F	VS Training Method	tr_mthd	Page 191

Table 467 • **tr_ber_thr**

Address	Short Description	Register Name	Details
0x98210	VS Training BER Threshold Settings	tr_ber_thr	Page 191

Table 468 • **tr_ber_ofs**

Address	Short Description	Register Name	Details
0x98211	VS Training BER Offset Setting	tr_ber_ofs	Page 191

Table 469 • **tr_lutsel**

Address	Short Description	Register Name	Details
0x98212	VS Training LUT Selection	tr_lutsel	Page 192

Table 470 • **tr_brkmask**

Address	Short Description	Register Name	Details
0x98213	VS Training break_mask LSW	brkmask_lsw	Page 192
0x98214	VS Training break_mask MSW	brkmask_msw	Page 192

Table 471 • **obcfg_addr**

Address	Short Description	Register Name	Details
0x98230	VS Training ROM Address for End and obcfg	obcfg_addr	Page 192

Table 472 • **apc_tmr**

Address	Short Description	Register Name	Details
0x98240	VS Training apc_timer	apc_tmr	Page 193

Table 473 • **wt_tmr**

Address	Short Description	Register Name	Details
0x98241	VS Training wait_timer	wt_tmr	Page 193

Table 474 • **mw_tmr**

Address	Short Description	Register Name	Details
0x98242	VS Training maxwait_timer LSW	mw_tmr_lsw	Page 193
0x98243	VS Training maxwait_timer MSW	mw_tmr_msw	Page 193

Table 475 • **tr_sts1**

Address	Short Description	Register Name	Details
0x98250	VS Training Status 1	tr_sts1	Page 193

Table 476 • **tr_sts2**

Address	Short Description	Register Name	Details
0x98251	VS Training Status 2	tr_sts2	Page 194

Table 477 • **tr_tapval**

Address	Short Description	Register Name	Details
0x98254	VS Tap CM Value	tr_cmval	Page 194
0x98255	VS Tap C0 Value	tr_c0val	Page 194
0x98256	VS Tap CP Value	tr_cpval	Page 194

Table 478 • **tr_frames_sent**

Address	Short Description	Register Name	Details
0x98260	VS Training frames_sent LSW	frsent_lsw	Page 195
0x98261	VS Training frames_sent MSW	frsent_msw	Page 195

Table 479 • **tr_lut**

Address	Short Description	Register Name	Details
0x98270	VS Training lut_read LSW	lut_lsw	Page 195
0x98271	VS Training lut_read MSW	lut_msw	Page 195

Table 480 • **tr_errcnt**

Address	Short Description	Register Name	Details
0x98272	VS Training PRBS11 error_count	tr_errcnt	Page 195

2.7.1 KR PMD Control and Status

2.7.1.1 KR PMD Control

Short Name:KR_1x0096

Address:0x90096

Table 481 • **KR PMD Control**

Bit	Name	Access	Description	Default
1	tr_enable	R/W	Training enable 1: Enable KR start-up protocol 0: Disable KR start-up protocol	0x0
0	tr_restart	R/W	Restart training (SC) 1: Reset KR start-up protocol 0: Normal operation	0x0

2.7.1.2 KR PMD Status

Short Name:KR_1x0097

Address:0x90097

Table 482 • **KR PMD Status**

Bit	Name	Access	Description	Default
3	tr_fail	R/O	Training failure 1: Training failure has been detected 0: Training failure has not been detected	0x0
2	stprot	R/O	Startup protocol status 1: Start-up protocol in progress 0: Start-up protocol complete	0x0
1	frlock	R/O	Frame lock 1: Training frame delineation detected, 0: Training frame delineation not detected	0x0
0	rcvr_rdy	R/O	Receiver status 1: Receiver trained and ready to receive data 0: Receiver training	0x0

2.7.1.3 KR LP Coefficient Update

Short Name:KR_1x0098

Address:0x90098

Table 483 • **KR LP coefficient update**

Bit	Name	Access	Description	Default
15:0	lpcoef	R/O	Received coefficient update field	N/A

2.7.1.4 KR LP Status Report

Short Name:KR_1x0099

Address:0x90099

Table 484 • **KR LP Status Report**

Bit	Name	Access	Description	Default
15:0	lpstat	R/O	Received status report field	N/A

2.7.1.5 KR LD Coefficient Update

Short Name:KR_1x009A

Address:0x9009A

Table 485 • **KR LD Coefficient Update**

Bit	Name	Access	Description	Default
15:0	ldcoef	R/O	Transmitted coefficient update field	N/A

2.7.1.6 KR LD Status Report

Short Name:KR_1x009B

Address:0x9009B

Table 486 • **KR LD Status Report**

Bit	Name	Access	Description	Default
15:0	ldstat	R/O	Transmitted status report field	N/A

2.7.2 Vendor Specific Training

2.7.2.1 VS Training Config 0

Short Name:tr_cfg0

Address:0x98200

Table 487 • **VS Training Config 0**

Bit	Name	Access	Description	Default
15:12	tmr_dvdr	R/W	Clock divider value for timer clocks.	0x4
10	rx_inv	R/W	Invert received prbs11 within training frame	0x0
9	tx_inv	R/W	Invert transmitted prbs11 within training frame	0x0
4	ld_pre_init	R/W	Set local taps starting point 0: Set to INITIALIZE 1: Set to PRESET	0x1
3	lp_pre_init	R/W	Send first LP request 0: Send INITIALIZE 1: Send PRESET	0x1
2	nosum	R/W	Update taps regardless of v2,vp sum.	0x0
1	part_cfg_en	R/W	Enable partial OB tap configuration.	0x1
0	tapctl_en	R/W	Allow LP to to control tap settings.	0x1

2.7.2.2 VS Training Config 1

Short Name:tr_cfg1

Address:0x98201

Table 488 • **VS Training Config 1**

Bit	Name	Access	Description	Default
10:0	tmr_hold	R/W	Freeze timers. Bit set... 0: wait 1: max_wait 2: 1g 3: 3g 4: 10g 5: training 6: pgdet 7: link_pass 8: link_fail 9: an_wait 10: break_link	0x000

2.7.2.3 VS Training Config 2

Short Name:tr_cfg2

Address:0x98202

Table 489 • **VS Training Config 2**

Bit	Name	Access	Description	Default
11:6	vp_max	R/W	max settings for vp sum.	0x1F
5:0	v2_min	R/W	min settings for v2 sum.	0x01

2.7.2.4 VS Training Config 3

Short Name:tr_cfg3

Address:0x98203

Table 490 • **VS Training Config 3**

Bit	Name	Access	Description	Default
11:6	cp_max	R/W	max settings for local transmitter.	0x00
5:0	cp_min	R/W	min settings for local transmitter.	0x34

2.7.2.5 VS Training Config 4

Short Name:tr_cfg4

Address:0x98204

Table 491 • **VS Training Config 4**

Bit	Name	Access	Description	Default
11:6	c0_max	R/W	max settings for local transmitter.	0x1F
5:0	c0_min	R/W	min settings for local transmitter.	0x11

2.7.2.6 VS Training Config 5

Short Name:tr_cfg5

Address:0x98205

Table 492 • **VS Training Config 5**

Bit	Name	Access	Description	Default
11:6	cm_max	R/W	max settings for local transmitter.	0x00
5:0	cm_min	R/W	min settings for local transmitter.	0x3A

2.7.2.7 VS Training Config 6

Short Name:tr_cfg6

Address:0x98206

Table 493 • **VS Training Config 6**

Bit	Name	Access	Description	Default
11:6	cp_init	R/W	initialize settings for local transmitter.	0x38
5:0	c0_init	R/W	initialize settings for local transmitter.	0x14

2.7.2.8 VS Training Config 7

Short Name:tr_cfg7

Address:0x98207

Table 494 • **VS Training Config 7**

Bit	Name	Access	Description	Default
11:6	cm_init	R/W	initialize settings for local transmitter.	0x3E
5:0	dfe_ofs	R/W	Signed value to adjust final LP C(+1) tap position from calculated optimal setting.	0x00

2.7.2.9 VS Training Config 8

Short Name:tr_cfg8

Address:0x98208

Table 495 • **VS Training Config 8**

Bit	Name	Access	Description	Default
7:6	wt1	R/W	Weighted average calculation of DFE tap 1	0x1
5:4	wt2	R/W	Weighted average calculation of DFE tap 2	0x1
3:2	wt3	R/W	Weighted average calculation of DFE tap 3	0x1
1:0	wt4	R/W	Weighted average calculation of DFE tap 4	0x1

2.7.2.10 VS Training Config 9

Short Name:tr_cfg9

Address:0x98209

Table 496 • **VS Training Config 9**

Bit	Name	Access	Description	Default
15:0	frcnt_ber	R/W	Number of training frames used for BER calculation.	0x0014

2.7.2.11 VS Training Gain Target And Margin Values

Short Name:tr_gain

Address:0x9820A

Table 497 • **VS Training Gain Target And Margin Values**

Bit	Name	Access	Description	Default
15:10	gain_marg	R/W	LP C(0) optimized when GAIN is gain_targ +/- 2*gain_marg	0x28
9:0	gain_targ	R/W	Target value of GAIN setting during LP C(0) optimization.	0x000

2.7.2.12 VS Training Coefficient Update Override

Short Name:tr_coef_ovrd

Address:0x9820B

Table 498 • **VS Training Coefficient Update Override**

Bit	Name	Access	Description	Default
15:0	coef_ovrd	R/W	Override Coef_update field to transmit	0x0000

2.7.2.13 VS Training Status Report Override

Short Name:tr_stat_ovrd

Address:0x9820C

Table 499 • **VS TrAining Status Report Override**

Bit	Name	Access	Description	Default
15:0	stat_ovrd	R/W	Override Stat_report field to transmit	0x0000

2.7.2.14 VS Training Override

Short Name:tr_ovrd

Address:0x9820D

Table 500 • **VS Training Override**

Bit	Name	Access	Description	Default
4	ovrd_en	R/W	Enable manual training	0x0
3	rxtrained_ovrd	R/W	Control of rx_trained variable for training SM	0x0
2	ber_en_ovrd	R/W	Generate BER enable pulse (SC)	0x0
1	coef_ovrd_vld	R/W	Generate Coef_update_valid pulse (SC)	0x0
0	stat_ovrd_vld	R/W	Generate Stat_report_valid pulse (SC)	0x0

2.7.2.15 VS Training State Step

Short Name:tr_step

Address:0x9820E

Table 501 • **VS Training State Step**

Bit	Name	Access	Description	Default
0	step	R/W	Step to next lptrain state (if at breakpoint) (SC)	0x0

2.7.2.16 VS Training Method

Short Name:tr_mthd

Address:0x9820F

Table 502 • **VS Training Method**

Bit	Name	Access	Description	Default
11:10	mthd_cp	R/W	Training method for remote C(+1) 0: BER method 1: Gain method 2: DFE method	0x2
9:8	mthd_c0	R/W	Training method for remote C(0)	0x1
7:6	mthd_cm	R/W	Training method for remote C(-1)	0x0
5:4	ord1	R/W	remote tap to optimize first 0: C(-1) 1: C(0) 2: C(+1)	0x1
3:2	ord2	R/W	remote tap to optimize second	0x2
1:0	ord3	R/W	remote tap to optimize third	0x0

2.7.2.17 VS Training BER Threshold Settings

Short Name:tr_ber_thr

Address:0x98210

Table 503 • **VS Training BER Threshold Settings**

Bit	Name	Access	Description	Default
15:8	ber_err_th	R/W	Only consider error count > ber_err_th	0x00
7:0	ber_wid_th	R/W	Only consider errored range > ber_wid_th	0x00

2.7.2.18 VS Training BER Offset Setting

Short Name:tr_ber_ofs

Address:0x98211

Table 504 • **VS Training BER Offset Setting**

Bit	Name	Access	Description	Default
14:10	cp_ber_ofs	R/W	Signed value to adjust final cp tap position from calculated optimal setting.	0x00

Table 504 • **VS Training BER Offset Setting *(continued)***

Bit	Name	Access	Description	Default
9:5	c0_ber_ofs	R/W	Signed value to adjust final c0 tap position from calculated optimal setting.	0x00
4:0	cm_ber_ofs	R/W	Signed value to adjust final cm tap position from calculated optimal setting.	0x00

2.7.2.19 VS Training LUT Selection

Short Name:tr_lutsel

Address:0x98212

Table 505 • **VS Training LUT Selection**

Bit	Name	Access	Description	Default
8:3	lut_row	R/W	Selects LUT table entry (0 to 63).	0x00
2:0	lut_sel	R/W	Selects LUT for lut_o 0: Gain 1: DFE_1 2: DFE_2 3: DFE_avg_1 4: DFE_avg_2 5: BER_1 6: BER_2 7: BER_3	0x0

2.7.2.20 VS Training Break_mask LSW

Short Name:brkmask_lsw

Address:0x98213

Table 506 • **VS Training Break_mask LSW**

Bit	Name	Access	Description	Default
15:0	brkmask_lsw	R/W	Select lptrain state machine breakpoints. Each bit corresponds to a state (see design doc)	0x0000

2.7.2.21 VS Training Break_mask MSW

Short Name:brkmask_msw

Address:0x98214

Table 507 • **VS Training Break_mask MSW**

Bit	Name	Access	Description	Default
15:0	brkmask_msw	R/W	Select lptrain state machine breakpoints. Each bit corresponds to a state (see design doc)	0x0000

2.7.2.22 VS Training ROM Address for End and OBCfg

Short Name:obcfg_addr

Address:0x98230

Table 508 • **VS Training ROM Address for End and OBCfg**

Bit	Name	Access	Description	Default
6:0	obcfg_addr	R/W	Address of OB tap configuration settings	0x00

2.7.2.23 VS Training apc_timer

Short Name:apc_tmr

Address:0x98240

Table 509 • **VS Training apc_timer**

Bit	Name	Access	Description	Default
15:0	apc_tmr	R/W	Delay between LP tap update, and capture of direct-connect apc values	0x0000

2.7.2.24 VS Training wait_timer

Short Name:wt_tmr

Address:0x98241

Table 510 • **VS Training wait_timer**

Bit	Name	Access	Description	Default
15:0	wt_tmr	R/W	wait_timer for training state machine to allow extra training frames to be exchanged	0x0A08

2.7.2.25 VS Training maxwait_timer LSW

Short Name:mw_tmr_lsw

Address:0x98242

Table 511 • **VS Training maxwait_timer LSW**

Bit	Name	Access	Description	Default
15:0	mw_tmr_lsw	R/W	maxwait_timer, when training expires and failure declared. 500ms	0xA30A

2.7.2.26 VS Training maxwait_timer MSW

Short Name:mw_tmr_msw

Address:0x98243

Table 512 • **VS Training maxwait_timer MSW**

Bit	Name	Access	Description	Default
15:0	mw_tmr_msw	R/W	maxwait_timer, when training expires and failure declared. 500ms	0x0133

2.7.2.27 VS Training Status 1

Short Name:tr_sts1

Address:0x98250

Table 513 • **VS Training Status 1**

Bit	Name	Access	Description	Default
12	ber_busy	R/O	Indicates prbs11 checker is active	N/A
11:9	tr_sm	R/O	Training state machine	N/A
8:4	lptrain_sm	R/O	LP training state machine	N/A
3	gain_fail	R/O	Indicates gain_target was not reached during LP training	N/A
2	training	R/O	training variable from training state machine	N/A
1	dme_viol	R/O	Indicates a DME violation has occurred (LH)	N/A
0	tr_done	R/O	Indicates that local and remote training has completed	N/A

2.7.2.28 VS Training Status 2

Short Name:tr_sts2

Address:0x98251

Table 514 • **VS Training Status 2**

Bit	Name	Access	Description	Default
2	cp_range_err	R/O	CP range error (LH)	N/A
1	c0_range_err	R/O	C0 range error (LH)	N/A
0	cm_range_err	R/O	CM range error (LH)	N/A

2.7.3 Vendor Specific Tap Values

2.7.3.1 VS Tap CM Value

Short Name:tr_cmval

Address:0x98254

Table 515 • **VS Tap CM Value**

Bit	Name	Access	Description	Default
6:0	cm_val	R/O	CM value	0x00

2.7.3.2 VS Tap C0 Value

Short Name:tr_c0val

Address:0x98255

Table 516 • **VS Tap C0 Value**

Bit	Name	Access	Description	Default
6:0	c0_val	R/O	C0 value	0x00

2.7.3.3 VS Tap CP Value

Short Name:tr_cpval

Address:0x98256

Table 517 • **VS Tap CP Value**

Bit	Name	Access	Description	Default
6:0	cp_val	R/O	CP value	0x00

2.7.4 Vendor Specific Counters

2.7.4.1 VS Training frames_sent LSW

Short Name:frsent_lsw

Address:0x98260

Table 518 • **VS Training frames_sent LSW**

Bit	Name	Access	Description	Default
15:0	frsent_lsw	R/O	Number of training frames sent to complete training.	N/A

2.7.4.2 VS Training frames_sent MSW

Short Name:frsent_msw

Address:0x98261

Table 519 • **VS Training frames_sent LSW**

Bit	Name	Access	Description	Default
15:0	frsent_msw	R/O	Number of training frames sent to complete training.	N/A

2.7.4.3 VS Training lut_read LSW

Short Name:lut_lsw

Address:0x98270

Table 520 • **VS Training lut_read LSW**

Bit	Name	Access	Description	Default
15:0	lut_lsw	R/O	Measured value of selected LUT.	0x0000

2.7.4.4 VS Training lut_read MSW

Short Name:lut_msw

Address:0x98271

Table 521 • **VS Training lut_read MSW**

Bit	Name	Access	Description	Default
15:0	lut_msw	R/O	Measured value of selected LUT.	0x0000

2.7.4.5 VS Training prbs11 error_count

Short Name:tr_errcnt

Address:0x98272

Table 522 • **VS Training prbs11 error_count**

Bit	Name	Access	Description	Default
15:0	errcnt	R/O	bit error count of prbs11 checker	0x0000

2.8 HOST_PMA_32BIT (Device 0x9)

Table 523 • **SD10G65_APC**

Address	Short Description	Register Name	Details
0x9F000	APC Top Control Configuration	APC_TOP_CTRL_CFG	Page 199
0x9F001	APC Common Configuration 0	APC_COMMON_CFG0	Page 199
0x9F002	APC Parameter Control Synchronization	APC_PARCTRL_SYNC_CFG	Page 201
0x9F003	APC parctrl FSM1 Timer Config	APC_PARCTRL_FSM1_TIMER_CFG	Page 203
0x9F004	APC parctrl FSM2 Timer Config	APC_PARCTRL_FSM2_TIMER_CFG	Page 203
0x9F005	APC FLEXCTRL Read Counter	APC_FLEXCTRL_CNT_STATUS	Page 203
0x9F006	APC Level Detect Calibration Configuration	APC_LD_CAL_CFG	Page 203
0x9F007	APC Sampling Stage Calibration Configuration 0	APC_IS_CAL_CFG0	Page 204
0x9F008	APC Sampling Stage Calibration Configuration 1	APC_IS_CAL_CFG1	Page 205
0x9F009	APC EQZ CTRL Config	APC_EQZ_COMMON_CFG	Page 205
0x9F00A	APC EQZ CTRL Configuration	APC_EQZ_GAIN_CTRL_CFG	Page 206
0x9F00B	APC EQZ ADJ CTRL Configuration	APC_EQZ_GAIN_ADJ_CTRL_CFG	Page 206
0x9F00C	APC EQZ CTRL Status	APC_EQZ_CTRL_STATUS	Page 207
0x9F00D	APC EQZ LD Control	APC_EQZ_LD_CTRL	Page 207
0x9F00E	APC EQZ LD CTRL Config0	APC_EQZ_LD_CTRL_CFG0	Page 208
0x9F00F	APC EQZ LD CTRL Config1	APC_EQZ_LD_CTRL_CFG1	Page 208
0x9F010	APC EQZ Pattern Matching cfg	APC_EQZ_PAT_MATCH_CFG0	Page 208
0x9F011	APC EQZ Pattern Matching cfg	APC_EQZ_PAT_MATCH_CFG1	Page 209
0x9F012	APC EQZ_OFFS Control	APC_EQZ_OFFS_CTRL	Page 209
0x9F013	APC EQZ_OFFS Timer Config	APC_EQZ_OFFS_TIMER_CFG	Page 210
0x9F014	APC EQZ_OFFS Parameter Control	APC_EQZ_OFFS_PAR_CFG	Page 210
0x9F015	APC EQZ_C Control	APC_EQZ_C_CTRL	Page 211
0x9F016	APC EQZ_C Timer Config	APC_EQZ_C_TIMER_CFG	Page 212
0x9F017	APC EQZ_C Parameter control	APC_EQZ_C_PAR_CFG	Page 212
0x9F018	APC EQZ_L Control	APC_EQZ_L_CTRL	Page 213
0x9F019	APC EQZ_L Timer Config	APC_EQZ_L_TIMER_CFG	Page 214
0x9F01A	APC EQZ_L Parameter Control	APC_EQZ_L_PAR_CFG	Page 214
0x9F01B	APC EQZ_AGC Control	APC_EQZ_AGC_CTRL	Page 215

Table 523 • **SD10G65_APC *(continued)***

Address	Short Description	Register Name	Details
0x9F01C	APC EQZ_AGC Timer Config	APC_EQZ_AGC_TIMER_CFG	Page 216
0x9F01D	APC EQZ_AGC Parameter Control	APC_EQZ_AGC_PAR_CFG	Page 216
0x9F01E	APC DFE1 Control	APC_DFE1_CTRL	Page 217
0x9F01F	APC DFE1 Timer Config	APC_DFE1_TIMER_CFG	Page 218
0x9F020	APC DFE1 Parameter Control	APC_DFE1_PAR_CFG	Page 218
0x9F021	APC DFE2 Control	APC_DFE2_CTRL	Page 219
0x9F022	APC DFE2 Timer Config	APC_DFE2_TIMER_CFG	Page 220
0x9F023	APC DFE2 Parameter Control	APC_DFE2_PAR_CFG	Page 220
0x9F024	APC DFE3 Control	APC_DFE3_CTRL	Page 221
0x9F025	APC DFE3 Timer Config	APC_DFE3_TIMER_CFG	Page 222
0x9F026	APC DFE3 Parameter Control	APC_DFE3_PAR_CFG	Page 222
0x9F027	APC DFE4 Control	APC_DFE4_CTRL	Page 223
0x9F028	APC DFE4 Timer Config	APC_DFE4_TIMER_CFG	Page 224
0x9F029	APC DFE4 Parameter Control	APC_DFE4_PAR_CFG	Page 224
0x9F02A	APC LC softcontrol Configuration	APC_LC_SOFTCTRL_CFG	Page 225

Table 524 • **SD10G65_DES**

Address	Short Description	Register Name	Details
0x9F100	SD10G65 DES Configuration 0	SD10G65_DES_CFG0	Page 226
0x9F101	SD10G65 MOEBDIV Configuration 0	SD10G65_MOEBDIV_CFG0	Page 227

Table 525 • **SD10G65_OB**

Address	Short Description	Register Name	Details
0x9F110	SD10G65 OB Configuration 0	SD10G65_OB_CFG0	Page 227
0x9F111	SD10G65 OB Configuration 1	SD10G65_OB_CFG1	Page 228
0x9F112	SD10G65 OB Configuration 2	SD10G65_OB_CFG2	Page 229
0x9F113	SD10G65 OB Configuration 3	SD10G65_OB_CFG3	Page 230

Table 526 • **SD10G65_IB**

Address	Short Description	Register Name	Details
0x9F120	SD10G65 IB Configuration 0	SD10G65_IB_CFG0	Page 230
0x9F121	SD10G65 IB Configuration 1	SD10G65_IB_CFG1	Page 232
0x9F122	SD10G65 IB Configuration 2	SD10G65_IB_CFG2	Page 233
0x9F123	SD10G65 IB Configuration 3	SD10G65_IB_CFG3	Page 233
0x9F124	SD10G65 IB Configuration 4	SD10G65_IB_CFG4	Page 235
0x9F125	SD10G65 IB Configuration 5	SD10G65_IB_CFG5	Page 235

Table 526 • **SD10G65_IB *(continued)***

Address	Short Description	Register Name	Details
0x9F126	SD10G65 IB Configuration 6	SD10G65_IB_CFG6	Page 237
0x9F127	SD10G65 IB Configuration 7	SD10G65_IB_CFG7	Page 238
0x9F128	SD10G65 IB Configuration 8	SD10G65_IB_CFG8	Page 238
0x9F129	SD10G65 IB Configuration 9	SD10G65_IB_CFG9	Page 239
0x9F12A	SD10G65 IB Configuration 10	SD10G65_IB_CFG10	Page 239
0x9F12B	SD10G65 IB Configuration 11	SD10G65_IB_CFG11	Page 240
0x9F12C	SD10G65 SBUS Rx CFG Service-Bus Related Setting	SD10G65_SBUS_RX_CFG	Page 241

Table 527 • **SD10G65_RX_RCPLL**

Address	Short Description	Register Name	Details
0x9F130	SD10G65 Rx RCPLL Configuration 0	SD10G65_RX_RCPLL_CFG0	Page 242
0x9F131	SD10G65 Rx RCPLL Configuration 1	SD10G65_RX_RCPLL_CFG1	Page 242
0x9F132	SD10G65 Rx RCPLL Configuration 2	SD10G65_RX_RCPLL_CFG2	Page 243
0x9F133	SD10G65 Rx RCPLL Status register 0	SD10G65_RX_RCPLL_STAT0	Page 243

Table 528 • **SD10G65_RX_SYNTH**

Address	Short Description	Register Name	Details
0x9F140	SD10G65 Rx Synthesizer Configuration 0	SD10G65_RX_SYNTH_CFG0	Page 244
0x9F141	SD10G65 Rx Synthesizer Configuration 1	SD10G65_RX_SYNTH_CFG1	Page 244
0x9F142	SD10G65 Rx Synthesizer Configuration 2	SD10G65_RX_SYNTH_CFG2	Page 244
0x9F143	SD10G65 Rx Synthesizer Configuration 3	SD10G65_RX_SYNTH_CFG3	Page 245
0x9F144	SD10G65 Rx Synthesizer Configuration 4	SD10G65_RX_SYNTH_CFG4	Page 245
0x9F145	SD10G65 Rx Synthesizer CDR loopfilter Control	SD10G65_RX_SYNTH_CDRLF	Page 246
0x9F146	SD10G65 Rx Synthesizer 0 for Qualifier Access	SD10G65_RX_SYNTH_QUALIFIER0	Page 246
0x9F147	SD10G65 Rx Synthesizer 1 for Qualifier Access	SD10G65_RX_SYNTH_QUALIFIER1	Page 247
0x9F148	SD10G65 Rx Synthesizer for Sync Control Data	SD10G65_RX_SYNTH_SYNC_CTRL	Page 247
0x9F149	F2DF Configuration / Status	F2DF_CFG_STAT	Page 247

Table 529 • **SD10G65_TX_SYNTH**

Address	Short Description	Register Name	Details
0x9F150	SD10G65 Tx Synthesizer Configuration 0	SD10G65_TX_SYNTH_CFG0	Page 248
0x9F151	SD10G65 Tx Synthesizer Configuration 1	SD10G65_TX_SYNTH_CFG1	Page 248
0x9F152	SD10G65 Tx Synthesizer Configuration 3	SD10G65_TX_SYNTH_CFG3	Page 249
0x9F153	SD10G65 Tx Synthesizer Configuration 4	SD10G65_TX_SYNTH_CFG4	Page 249

Table 529 • **SD10G65_TX_SYNTH *(continued)***

Address	Short Description	Register Name	Details
0x9F154	SD10G65 SSC Generator Configuration 0	SD10G65_SSC_CFG0	Page 249
0x9F155	SD10G65 SSC Generator Configuration 1	SD10G65_SSC_CFG1	Page 249

Table 530 • **SD10G65_TX_RCPLL**

Address	Short Description	Register Name	Details
0x9F160	SD10G65 Tx RCPLL Configuration 0	SD10G65_TX_RCPLL_CFG0	Page 250
0x9F161	SD10G65 Tx RCPLL Configuration 1	SD10G65_TX_RCPLL_CFG1	Page 251
0x9F162	SD10G65 Tx RCPLL Configuration 2	SD10G65_TX_RCPLL_CFG2	Page 251
0x9F163	SD10G65 Tx RCPLL Status 0	SD10G65_TX_RCPLL_STAT0	Page 252

2.8.1 SD10G65 APC Configuration and Status

Configuration and status register set for SD10G65 APC

2.8.1.1 APC Top Control Configuration

Short Name:APC_TOP_CTRL_CFG

Address:0x9F000

Configuration register for top control logic

Table 531 • **APC Top Control Configuration**

Bit	Name	Access	Description	Default
31:24	PWR_UP_TIME	R/W	Delay time required to power up auxiliary channels	0x0F
23:16	PWR_DN_TIME	R/W	Delay time required to power down auxiliary channels	0x05
15:0	SLEEP_TIME	R/W	APC top-control sleep-time (power-down). Given in number of clock cycles (typically 2.5 ... 5 ns)	0xC350

2.8.1.2 APC Common Configuration 0

Short Name:APC_COMMON_CFG0

Address:0x9F001

Common configurations 0 for APC logic. Note: For HML error correction logic HML=000/001/011/111 are considered valid, 010 and 101 are considered correctable (010 correctable to 011; 101 correctable to 001) and 100 and 110 are considered uncorrectable.

Table 532 • **APC Common Configuration 0**

Bit	Name	Access	Description	Default
31	HML_CLR_CNT	R/W	Clear HML sampling error counter 1: Clear counter	0x0

Table 532 • **APC Common Configuration 0** ***(continued)***

Bit	Name	Access	Description	Default
30	HML_ERRCORR_MODE	R/W	HML sampling error correction mode. Correctable sampling errors can be automatically corrected. 0: Disable auto-correction 1: Enable auto-correction	0x1
29	HML_ERRCORR_ENA	R/W	HML sampling error correction enable. Invalid samples are not used for parameter control (smart sampling). 0: Disable smart sampling 1: Enable smart sampling	0x0
28	HML_SWAP_HL	R/W	H/L swapping in HML sampling error correction logic 0: No H/L swapping 1: H/L swapped	0x1
27:26	APC_FSM_RECOVER_MODE	R/W	Top-ctrl FSM recovery behavior 0: No auto-recovery 1: Auto-restart on missing input signal after Restart-Delay-Timer has expired 2: Auto-restart on missing input signal	0x0
25	SIG_DET_VALID_CFG	R/W	Signal detect valid configuration (Offs/AGC/L/C/DFE) 0: Signal_detect input directly used 1: Signal_detect input gated with gain_ctrl ramp-up done (EQZ_GAIN_CTRL_DONE)	0x0
24:20	SIG_LOST_DELAY_TIME	R/W	Signal lost delay timer configuration used for APC recovery. The signal lost delay time specifies the time when a missing input signal is considered a lost input signal on sig_det = 0. The delay time is T = (2^sig_lost_delay_time) * T_rx_clk_per	0x14
19:16	TOP_CTRL_STATE	R/O	Current state of APC top control state machine 0: Off 1: Power-up 2: Power-down 3: Manual mode 4: Calibrate IS 5: Calibrate LD 6: Not used 7: Gain-control ramp-up 8: Mission mode (FSM1 controlled) 9: Mission mode (FSM2 controlled) 10-12: Debug states 13: Snooze 14-15: Not used	0x0

Table 532 • **APC Common Configuration 0** ***(continued)***

Bit	Name	Access	Description	Default
15:12	BLOCK_READ_SEL	R/W	Select flexctrl block in order to read internal counters. Counter values readable from APC_FLEXCTRL_CNT_STATUS. 0: Offset-ctrl 1: L-ctrl 2: C-ctrl 3: AGC-ctrl 4: DFE1-ctrl 5: DFE2-ctrl 6: DFE3-ctrl 7: DFE4-ctrl 8: SAM_Offset-cal 9: Level-cal 10: HML sampling errors	0x0
11	RESET_APC	R/W	Reset APC core logic (configuration registers are not reset) 1: Reset APC 0: Normal operation (mission mode)	0x0
10	FREEZE_APC	R/W	Freeze current state 0: Normal operation 1: Freeze APC	0x0
8:6	IF_WIDTH	R/W	Interface bit-width 0: 8-bit 1: 10-bit 2: 16-bit 3: 20-bit 4: 32-bit 5: 40-bit	0x4
5	RESERVED	R/W	Must be set to its default.	0x1
4	THROTTLE_MODE	R/W	APC throttling mode 0: Disable - no power reduction (continuous operation) 1: Enable - power reduced operation (pulsed operation)	0x0
3	APC_DIRECT_ENA	R/W	Enable APC direct connections instead of local IB configuration registers.	0x0
2:0	APC_MODE	R/W	APC operation mode 0: Off 1: Manual mode 2: Perform calibration and run FSM1 3: Perform calibration and run FSM2 4: Perform calibration and run FSM1 and FSM2 in ping-pong operation 5: Perform calibration and then enter manual mode	0x0

2.8.1.3 APC Parameter Control Synchronization

Short Name:APC_PARCTRL_SYNC_CFG

Address:0x9F002

Configuration register for common flexible parameter control FSMs

Table 533 • **APC Parameter Control Synchronization**

Bit	Name	Access	Description	Default
31:28	RESERVED	R/W	Must be set to its default.	0x3
15	FSM2_CTRL_MODE	R/W	Parameter control mode for FSM2 0: Discrete 1: Continuous	0x1
14	FSM1_CTRL_MODE	R/W	Parameter control mode for FSM1 0: Discrete 1: Continuous	0x1
13:11	FSM2_RECOVER_MODE	R/W	FSM2 recovery behavior 0: No auto-recovery 1: Freeze FSM2 on weak (eqz_gain > eqz_gain_freeze_thres) or missing input signal 2: Freeze FSM2 on weak signal and restart on missing input signal 3: Freeze FSM2 on missing input signal 4: Freeze FSM2 on missing input signal and auto-restart after Restart-Delay-Timer has expired 5: Auto-restart FSM2 on missing input signal 6-7: Reserved	0x0
10:8	FSM1_RECOVER_MODE	R/W	FSM1 recovery behavior 0: No auto-recovery 1: Freeze FSM1 on weak (eqz_gain > eqz_gain_freeze_thres) or missing input signal 2: Freeze FSM1 on weak signal and restart on missing input signal 3: Freeze FSM1 on missing input signal 4: Freeze FSM1 on missing input signal and auto-restart after Restart-Delay-Timer has expired 5: Auto-restart FSM1 on missing input signal 6-7: Reserved	0x0
7	FSM2_CTRL_DONE	R/O	Parameter control state of FSM2 in one-time mode 1: finished	0x0
6	FSM2_START_CTRL	R/W	Start operation of FSM2 (parameter update). Should be cleared afterwards in One-time mode and stay set in Non-stop and Paused mode	0x0
5:4	FSM2_OP_MODE	R/W	Operation mode of FSM2 0: Off 1: One-time 2: Non-stop 3: Paused	0x0
3	FSM1_CTRL_DONE	R/O	Parameter control state of FSM1 in one-time mode 1: finished	0x0
2	FSM1_START_CTRL	R/W	Start operation of FSM1 (parameter update). Should be cleared afterwards in One-time mode and stay set in Non-stop and Paused mode	0x0

Table 533 • **APC Parameter Control Synchronization**

Bit	Name	Access	Description	Default
1:0	FSM1_OP_MODE	R/W	Operation mode of FSM1 0: Off 1: One-time 2: Non-stop 3: Paused	0x0

2.8.1.4 APC parctrl FSM1 Timer Config

Short Name:APC_PARCTRL_FSM1_TIMER_CFG

Address:0x9F003

Timing configuration register for common flexible parameter control FSM1

Table 534 • **APC parctrl FSM1 Timer Config**

Bit	Name	Access	Description	Default
31:16	FSM1_PS_TIME	R/W	FSM1 Pause time (in number of rx_clk cycles)	0x0064
15:0	FSM1_OP_TIME	R/W	FSM1 Operation time (in number of rx_clk cycles)	0x03E8

2.8.1.5 APC parctrl FSM2 Timer Config

Short Name:APC_PARCTRL_FSM2_TIMER_CFG

Address:0x9F004

Timing configuration register for common flexible parameter control FSM2

Table 535 • **APC parctrl FSM2 Timer Config**

Bit	Name	Access	Description	Default
31:16	FSM2_PS_TIME	R/W	FSM2 Pause time (in number of rx_clk cycles)	0x0064
15:0	FSM2_OP_TIME	R/W	FSM2 Operation time (in number of rx_clk cycles)	0x03E8

2.8.1.6 APC FLEXCTRL Read Counter

Short Name:APC_FLEXCTRL_CNT_STATUS

Address:0x9F005

Observation register for multiple counters. The selection is done via APC_COMMON_CFG.BLOCK_READ_SEL (select flexctrl block to be read) and APC_XXX_CTRL.XXX_READ_CNT_SEL (counter within flexctrl block XXX) or APC_COMMON_CFG.OFFSCAL_READ_CNT_SEL. Note that the EQZ and DFE counters hit_cnt and err_cnt make only sense in DISCRETE control mode.

Table 536 • **APC FLEXCTRL Read Counter**

Bit	Name	Access	Description	Default
31:0	APC_CTRL_CNTVAL	R/O	Current counter value	0x00000000

2.8.1.7 APC Level Detect Calibration Configuration

Short Name:APC_LD_CAL_CFG

Address:0x9F006

Configuration register for APC level detect calibrations logic

Table 537 • **APC Level Detect Calibration Configuration**

Bit	Name	Access	Description	Default
30:28	CAL_CLK_DIV	R/W	Calibration clock divider. Clock used in calibration blocks is divided by 2^(2*CAL_CLK_DIV) 0: No clock division 1: Clock is divided by 4 2: Clock is divided by 16 ... 7: Clock is divided by 16384	0x2
19	DETLEV_CAL_DONE	R/O	Detect level calibration state 1: finished	0x0
12	SKIP_SDET_CAL	R/W	Skip signal detect calibration	0x0
11	SKIP_LD_CAL	R/W	Skip level detect calibration	0x0
10:5	IE_SDET_LEVEL	R/W	Level for IE signal detect (when controlled by APC) 0: 20mV	0x02
4:1	DETLVL_TIMER	R/W	Timer for calibration process 14: Use for 400MHz rx_clk	0xE
0	START_DETLVL_CAL	R/W	Start signal and level detect calibration process (sampling stage; only in manual mode, see apc_mode)	0x0

2.8.1.8 APC Sampling Stage Calibration Configuration 0

Short Name:APC_IS_CAL_CFG0

Address:0x9F007

Configuration register 0 for APC sampling stage calibrations logic

Table 538 • **APC Sampling Stage Calibration Configuration 0**

Bit	Name	Access	Description	Default
25:20	IB_DFE_GAIN_ADJ	R/W	Gain adjustment for DFE amplifier	0x24
19:14	CPMD_THRES_INIT	R/W	Initial value for CP/MD FF threshold calibration.	0x00
13:8	VSC_THRES_INIT	R/W	Initial value for VScope FF threshold calibration.	0x00
7	SKIP_OBSERVE_INIT	R/W	Skip observe block initialization	0x0
6	SKIP_OFFSET_INIT	R/W	Skip sample FF offset initialization	0x0
5	SKIP_THRESHOLD_INIT	R/W	Skip sample FF threshold initialization	0x0
4	SKIP_DFE_BUFFER_INIT	R/W	Skip DFE buffer 0db initialization	0x0
3	SKIP_OBSERVE_CAL	R/W	Skip observe block calibration	0x0
2	SKIP_OFFSET_CAL	R/W	Skip sample FF offset calibration	0x0
1	SKIP_THRESHOLD_CAL	R/W	Skip sample FF threshold calibration	0x0
0	SKIP_DFE_BUFFER_CAL	R/W	Skip DFE buffer 0db calibration	0x0

2.8.1.9 APC Sampling Stage Calibration Configuration 1

Short Name:APC_IS_CAL_CFG1

Address:0x9F008

Configuration register 1 for APC sampling stage calibrations logic

Table 539 • **APC Sampling Stage Calibration Configuration 1**

Bit	Name	Access	Description	Default
31:24	EQZ_AGC_DAC_VAL	R/W	AGC-DAC value used for DFE 0dB calibration during IB-calibration process	0x58
23	USE_AGC_DAC_VAL	R/W	Enable use of EQZ_AGC_DAC_VAL instead of EQZ_AGC_INI during DFE 0dB IB calibration	0x0
19:16	CAL_NUM_ITERATIONS	R/W	Controls number of calibrations iterations to settle values that depend on each other (offset vs threshold). Coding number of iterations = cal_num_iterations + 1.	0xF
13:9	PAR_DATA_NUM_ONES_THRES	R/W	Selects the number of ones threshold when using parallel data. Value for rising ramp from zero to one. The value for the falling ramp (one -> zero) is half the interface width minus par_data_num_ones_thres.	0x10
8	PAR_DATA_SEL	R/W	Controls whether the parallel data from the deserializer or the signal from the observe multiplexer in the sample stage is used. Coding: 0: observe multiplexer, 1: parallel data.	0x1
7:3	OFFSCAL_READ_CNT_SEL	R/W	Select offset calibration result to be read (BLOCK_READ_SEL = 8 required)	0x00
2	OFFSCAL_DIS_SWAP	R/W	Swaps disp with disn used during calibration	0x0
1	OFFSCAL_DONE	R/O	Offset calibration state 1: finished	0x0
0	START_OFFSCAL	R/W	Start offset calibration process (sampling stage; only in manual mode, see apc_mode)	0x0

2.8.1.10 APC EQZ CTRL Config

Short Name:APC_EQZ_COMMON_CFG

Address:0x9F009

Configuration register for gain control logic

Table 540 • **APC EQZ CTRL Config**

Bit	Name	Access	Description	Default
22:13	EQZ_GAIN_FREEZE_THRES	R/W	Gain freeze threshold, used in APC recovery mode for low input signals	0x37A
12:11	EQZ_GAIN_RECOVER_MODE	R/W	Gain recovery behavior 0: No auto-recovery 1: Freeze gain on missing input signal and auto-restart after Restart-Delay-Timer has expired 2: Auto-restart Gain control on missing input signal 3: Reserved	0x0

Table 540 • **APC EQZ CTRL Config *(continued)***

Bit	Name	Access	Description	Default
10	EQZ_GAIN_ADJ_HALT	R/W	Stop update of gain_adj	0x0
9	EQZ_GAIN_CAL_MODE	R/W	Gain calibration mode 0: Use successive approximation to find required gain 1: use max gain and reduce linearly to find required gain	0x0
8	EQZ_GAIN_ADJ_START_UPDATE	R/W	Start (initiate) gain_adj update process (on rising edge of cfg bit)	0x0
7	EQZ_GAIN_START_UPDATE	R/W	Start (initiate) gain update process (on rising edge of cfg bit)	0x0
6	EQZ_GAIN_START_CTRL	R/W	(Re-)start (initiate) main gain/gain_adj calibration process (on rising edge of cfg bit)	0x0
5:4	EQZ_GAIN_OP_MODE	R/W	Operation mode (only when EQZ_GAIN_STOP_CTRL = 1) 0: Idle 1: Calibrate and work 2: Work	0x0
3	EQZ_GAIN_STOP_CTRL	R/W	Stop main gain control machine immediately	0x0
2	EQZ_GAIN_AUTO_RESTART	R/W	Restart gain/gain_adj calibration automatically on rising edge of signal_detect	0x1
1:0	EQZ_GAIN_CHG_MODE	R/W	Parameter change mode 0: Automatic update 1: Preset (use PAR_INI as fix value internal processing continues) 2: Freeze (internal processing stops parameter stays at current value) 3: No update (internal processing continues but parameter is not updated)	0x0

2.8.1.11 APC EQZ CTRL Configuration

Short Name:APC_EQZ_GAIN_CTRL_CFG

Address:0x9F00A

Configuration register for gain

Table 541 • **APC EQZ CTRL Configuration**

Bit	Name	Access	Description	Default
29:20	EQZ_GAIN_MAX	R/W	Maximum gain in normal operation (should be not greater then 895 (512+3*128-1)	0x37F
19:10	EQZ_GAIN_MIN	R/W	Minimum gain in normal operation	0x000
9:0	EQZ_GAIN_INI	R/W	Gain initial value (used if EQZ_GAIN_CHG_MODE = 1)	0x000

2.8.1.12 APC EQZ ADJ CTRL Configuration

Short Name:APC_EQZ_GAIN_ADJ_CTRL_CFG

Address:0x9F00B

Configuration register for gain_adj

Table 542 • **APC EQZ ADJ CTRL Configuration**

Bit	Name	Access	Description	Default
26:20	EQZ_GAIN_ADJ_MAX	R/W	Maximum gain_adj in normal operation	0x7F
16:10	EQZ_GAIN_ADJ_MIN	R/W	Minimum gain_adj in normal operation	0x00
6:0	EQZ_GAIN_ADJ_INI	R/W	Gain_adj initial value (used if EQZ_GAIN_CHG_MODE = 1)	0x00

2.8.1.13 APC EQZ CTRL Status

Short Name:APC_EQZ_CTRL_STATUS

Address:0x9F00C

Observation register for controlled settings

Table 543 • **APC EQZ CTRL Status**

Bit	Name	Access	Description	Default
23	EQZ_GAIN_CTRL_DONE	R/O	Status flag indicating main gain/gain_adj ramp-up process has finished	0x0
22:16	EQZ_GAIN_ADJ_ACTVAL	R/O	Parameter value (controlled/computed gain adjustment value)	0x00
15:6	EQZ_GAIN_ACTVAL	R/O	Parameter value (controlled/computed gain value)	0x000
5:0	LD_LEV_ACTVAL	R/O	Parameter value (controlled/computed level for level-detect logic)	0x00

2.8.1.14 APC EQZ LD Control

Short Name:APC_EQZ_LD_CTRL

Address:0x9F00D

Configuration register for level-detect (LD) control, timing and behavior (timing: number of rx_clk cycles, used for LD toggling)

Table 544 • **APC EQZ LD Control**

Bit	Name	Access	Description	Default
31	LD_EQ_TOGGLE	R/O	Captured toggling of LD-EQ	0x0
30	LD_IB_TOGGLE	R/O	Captured toggling of LD-IB	0x0
29	LD_CATCH_BYPASS	R/W	Bypass LD catch circuitry (allows capturing pulses shorter then one rx_clk cycle)	0x1
28:26	LD_WD_CNT_MAX	R/W	Max value for LD updates in gain_adjust (watch-dog; prevent endless loop of LD adjustment; max is 2^value - 1)	0x3
25:22	LD_TOG_THRESHOLD	R/W	Number of required toggles before toggling is considered valid	0x2
21:14	LD_T_TOGGLE_DEADTIME	R/W	Sensitivity deadtime between two toggles (value is multiplied by 2)	0x02
8	LD_LEV_UPDATE	R/W	Update internal LD_lev value with LD_LEV_INI	0x0

Table 544 • **APC EQZ LD Control *(continued)***

Bit	Name	Access	Description	Default
7	LD_EQ_START_TOG_CHK	R/W	Start (initiate) a LD-EQ toggle check (for present LD-level)	0x0
6	LD_IB_START_TOG_CHK	R/W	Start (initiate) a LD-IB toggle check (for present LD-level)	0x0
5:0	LD_LEV_INI	R/W	LD_lev initial value (used as preset value if EQZ_GAIN_CHG_MODE = 1)	0x28

2.8.1.15 APC EQZ LD CTRL Config0

Short Name:APC_EQZ_LD_CTRL_CFG0

Address:0x9F00E

Configuration register 0 for level-detect (LD) controller timing (number of rx_clk cycles, used for operation timing). Important note: For small ld_t_* values it might be necessary to change IB configuration bit-group IB_LDSD_DIVSEL to higher values!

Table 545 • **APC EQZ LD CTRL Config0**

Bit	Name	Access	Description	Default
31:16	LD_T_DEADTIME_WRK	R/W	Minimum activity for LD in work mode (value is multiplied by 8)	0x0064
15:0	LD_T_TIMEOUT_WRK	R/W	Activity timeout threshold for LD in work mode (value is multiplied by 8)	0x03E8

2.8.1.16 APC EQZ LD CTRL Config1

Short Name:APC_EQZ_LD_CTRL_CFG1

Address:0x9F00F

Configuration register 1 for level-detect (LD) controller timing (number of rx_clk cycles, used for calibration timing). Important note: For small ld_t_* values it might be necessary to change IB configuration bit-group IB_LDSD_DIVSEL to higher values!

Table 546 • **APC EQZ LD CTRL Config1**

Bit	Name	Access	Description	Default
31:16	LD_T_DEADTIME_CAL	R/W	Minimum activity for LD in calibration mode (value is multiplied by 8)	0x0064
15:0	LD_T_TIMEOUT_CAL	R/W	Activity timeout threshold for LD in calibration mode (value is multiplied by 8)	0x03E8

2.8.1.17 APC EQZ Pattern Matching Cfg 0

Short Name:APC_EQZ_PAT_MATCH_CFG0

Address:0x9F010

Pattern matching Configuration register for eqz_c and eqz_l control

Table 547 • **APC EQZ Pattern Matching Cfg 0**

Bit	Name	Access	Description	Default
31:24	EQZ_C_PAT_MASK	R/W	EQZ-C-control pattern mask (only those bits are used for pattern matching whose mask bit is set)	0x00

Table 547 • **APC EQZ Pattern Matching Cfg 0 *(continued)***

Bit	Name	Access	Description	Default
23:16	EQZ_C_PAT_MATCH	R/W	EQZ-C-control pattern used for pattern matching (corresponding mask bits must be set)	0x00
15:8	EQZ_L_PAT_MASK	R/W	EQZ-L-control pattern mask (only those bits are used for pattern matching whose mask bit is set)	0x00
7:0	EQZ_L_PAT_MATCH	R/W	EQZ-L-control pattern used for pattern matching (corresponding mask bits must be set)	0x00

2.8.1.18 APC EQZ Pattern Matching Cfg 1

Short Name:APC_EQZ_PAT_MATCH_CFG1

Address:0x9F011

Pattern matching configuration register for eqz_offs and eqz_agc control Note, if mask is set to 0, all bits are "matching" and taken into account for parameter control.

Table 548 • **APC EQZ Pattern Matching Cfg 1**

Bit	Name	Access	Description	Default
31:24	EQZ_OFFS_PAT_MASK	R/W	EQZ-Offset-control pattern mask (only those bits are used for pattern matching whose mask bit is set)	0x00
23:16	EQZ_OFFS_PAT_MATCH	R/W	EQZ-Offset-control pattern used for pattern matching (corresponding mask bits must be set)	0x00
15:8	EQZ_AGC_PAT_MASK	R/W	EQZ-AGC-control pattern mask (only those bits are used for pattern matching whose mask bit is set)	0x00
7:0	EQZ_AGC_PAT_MATCH	R/W	EQZ-AGC-control pattern used for pattern matching (corresponding mask bits must be set)	0x00

2.8.1.19 APC EQZ_OFFS Control

Short Name:APC_EQZ_OFFS_CTRL

Address:0x9F012

General behavior control for EQZ_OFFS parameter control.

Table 549 • **APC EQZ_OFFS Control**

Bit	Name	Access	Description	Default
29:27	EQZ_OFFS_RECOVER_MODE	R/W	EQZ_OFFS recovery behavior 0: No auto-recovery 1: Freeze EQZ_OFFS on weak (eqz_gain > eqz_gain_freeze_thres) or missing input signal 2: Freeze EQZ_OFFS on weak signal and restart on missing input signal 3: Freeze EQZ_OFFS on missing input signal 4: Freeze EQZ_OFFS on missing input signal and auto-restart after Restart-Delay-Timer has expired 5: Auto-restart EQZ_OFFS on missing input signal 6-7: Reserved	0x0

Table 549 • **APC EQZ_OFFS Control** ***(continued)***

Bit	Name	Access	Description	Default
26	EQZ_OFFS_CTRL_DONE	R/O	Parameter control state in one-time mode 1: Finished	0x0
25:16	EQZ_OFFS_ACTVAL	R/O	Parameter value (controlled/computed value)	0x000
15:14	EQZ_OFFS_SYNC_MODE	R/W	Synchronization mode 0: Independent 1: Attached to parctrl FSM 1 2: Attached to parctrl FSM 2 3: Attached to both parctrl FSMs	0x0
13:12	EQZ_OFFS_READ_CNT_SEL	R/W	Select counter to be read 0: eqz_offs_value 1: Hit counter 2: Error counter	0x0
10	EQZ_OFFS_CTRL_MODE	R/W	Parameter control mode for EQZ_OFFS parameter 0: Discrete 1: Continuous	0x1
9:4	EQZ_OFFS_CTRL_THRES	R/W	Alternative threshold for EQZ_OFFS parameter (controller goal: err_cnt = 0.5*EQZ_OFFS_THRES)	0x28
3	EQZ_OFFS_CTRL_THRES_ENA	R/W	Enable use of alternative threshold for EQZ_OFFS parameter 0: Use default threshold 1: Use alternative threshold	0x0
2	EQZ_OFFS_START_CTRL	R/W	Start operation (parameter update). Should be cleared afterwards in One-time mode and stay set in Non-stop and Paused mode	0x0
1:0	EQZ_OFFS_OP_MODE	R/W	Operation mode 0: Off 1: One-time 2: Non-stop 3: Paused	0x0

2.8.1.20 APC EQZ_OFFS Timer Config

Short Name:APC_EQZ_OFFS_TIMER_CFG

Address:0x9F013

Configuration registers for EQZ_OFFS controller timing.

Table 550 • **APC EQZ_OFFS Timer Config**

Bit	Name	Access	Description	Default
31:16	EQZ_OFFS_PS_TIME	R/W	Pause time (in number of rx_clk cycles)	0x0064
15:0	EQZ_OFFS_OP_TIME	R/W	Operation time (in number of rx_clk cycles)	0x03E8

2.8.1.21 APC EQZ_OFFS Parameter Control

Short Name:APC_EQZ_OFFS_PAR_CFG

Address:0x9F014

Configuration register for controlled EQZ_OFFS parameter. Note, for parameters larger than 8 bits, ini/min/max values are shifted to the left. For parameters smaller than 8 bits only the lower bits of ini/min/max are used.

Table 551 • **APC EQZ_OFFS Parameter Control**

Bit	Name	Access	Description	Default
31	EQZ_OFFS_DIR_SEL	R/W	Select parameter update direction 0: Normal 1: Inverted	0x0
30:26	EQZ_OFFS_RANGE_SEL	R/W	Parameter range selection (only when CTRL_MODE = continuous). Value complies to number of left-shifts	0x00
25:24	EQZ_OFFS_CHG_MODE	R/W	Parameter change mode 0: Automatic update 1: Preset (use EQZ_OFFS_INI as fix value internal processing continues) 2: Freeze (internal processing stops parameter stays at current value) 3: No update (internal processing continues but parameter is not updated)	0x0
23:16	EQZ_OFFS_MAX	R/W	Maximum value of parameter	0x00
15:8	EQZ_OFFS_MIN	R/W	Minimum value of parameter	0x00
7:0	EQZ_OFFS_INI	R/W	Parameter initial value	0x00

2.8.1.22 APC EQZ_C Control

Short Name:APC_EQZ_C_CTRL

Address:0x9F015

General behavior control for EQZ_C parameter control.

Table 552 • **APC EQZ_C Control**

Bit	Name	Access	Description	Default
29:27	EQZ_C_RECOVER_MODE	R/W	EQZ_C recovery behavior 0: No auto-recovery 1: Freeze EQZ_C on weak (eqz_gain > eqz_gain_freeze_thres) or missing input signal 2: Freeze EQZ_C on weak signal and restart on missing input signal 3: Freeze EQZ_C on missing input signal 4: Freeze EQZ_C on missing input signal and auto-restart after Restart-Delay-Timer has expired 5: Auto-restart EQZ_C on missing input signal 6-7: Reserved	0x0
26	EQZ_C_CTRL_DONE	R/O	Parameter control state in one-time mode 1: Finished	0x0
25:16	EQZ_C_ACTVAL	R/O	Parameter value (controlled/computed value)	0x000

Table 552 • **APC EQZ_C Control *(continued)***

Bit	Name	Access	Description	Default
15:14	EQZ_C_SYNC_MODE	R/W	Synchronization mode 0: Independent 1: Attached to parctrl FSM 1 2: Attached to parctrl FSM 2 3: Attached to both parctrl FSMs	0x0
13:12	EQZ_C_READ_CNT_SEL	R/W	Select counter to be read 0: eqz_c_value 1: Hit counter 2: Error counter	0x0
10	EQZ_C_CTRL_MODE	R/W	Parameter control mode for EQZ_C parameter 0: Discrete 1: Continuous	0x1
9:4	EQZ_C_CTRL_THRES	R/W	Alternative threshold for EQZ_C parameter (controller goal: err_cnt = 0.5*EQZ_C_THRES)	0x28
3	EQZ_C_CTRL_THRES_ENA	R/W	Enable use of alternative threshold for EQZ_C parameter 0: Use default threshold 1: Use alternative threshold	0x0
2	EQZ_C_START_CTRL	R/W	Start operation (parameter update). Should be cleared afterwards in One-time mode and stay set in Non-stop and Paused mode	0x0
1:0	EQZ_C_OP_MODE	R/W	Operation mode 0: Off 1: One-time 2: Non-stop 3: Paused	0x0

2.8.1.23 APC EQZ_C Timer Config

Short Name:APC_EQZ_C_TIMER_CFG

Address:0x9F016

Configuration registers for EQZ_C controller timing.

Table 553 • **APC EQZ_C Timer Config**

Bit	Name	Access	Description	Default
31:16	EQZ_C_PS_TIME	R/W	Pause time (in number of rx_clk cycles)	0x0064
15:0	EQZ_C_OP_TIME	R/W	Operation time (in number of rx_clk cycles)	0x03E8

2.8.1.24 APC EQZ_C Parameter Control

Short Name:APC_EQZ_C_PAR_CFG

Address:0x9F017

Configuration register for controlled EQZ_C parameter. Note, for parameters larger than 8 bits, ini/min/max values are shifted to the left. For parameters smaller than 8 bits only the lower bits of ini/min/max are used.

Table 554 • **APC EQZ_C Parameter Control**

Bit	Name	Access	Description	Default
31	EQZ_C_DIR_SEL	R/W	Select parameter update direction 0: Normal 1: Inverted	0x0
30:26	EQZ_C_RANGE_SEL	R/W	Parameter range selection (only when CTRL_MODE = continuous). Value complies to number of left-shifts	0x00
25:24	EQZ_C_CHG_MODE	R/W	Parameter change mode 0: Automatic update 1: Preset (use EQZ_C_INI as fix value internal processing continues) 2: Freeze (internal processing stops parameter stays at current value) 3: No update (internal processing continues but parameter is not updated)	0x0
23:16	EQZ_C_MAX	R/W	Maximum value of parameter	0x00
15:8	EQZ_C_MIN	R/W	Minimum value of parameter	0x00
7:0	EQZ_C_INI	R/W	Parameter initial value	0x00

2.8.1.25 APC EQZ_L Control

Short Name:APC_EQZ_L_CTRL

Address:0x9F018

General behavior control for EQZ_L parameter control.

Table 555 • **APC EQZ_L Control**

Bit	Name	Access	Description	Default
29:27	EQZ_L_RECOVER_MODE	R/W	EQZ_L recovery behavior 0: No auto-recovery 1: Freeze EQZ_L on weak (eqz_gain > eqz_gain_freeze_thres) or missing input signal 2: Freeze EQZ_L on weak signal and restart on missing input signal 3: Freeze EQZ_L on missing input signal 4: Freeze EQZ_L on missing input signal and auto-restart after Restart-Delay-Timer has expired 5: Auto-restart EQZ_L on missing input signal 6-7: Reserved	0x0
26	EQZ_L_CTRL_DONE	R/O	Parameter control state in one-time mode 1: Finished	0x0
25:16	EQZ_L_ACTVAL	R/O	Parameter value (controlled/computed value)	0x000

Table 555 • **APC EQZ_L Control *(continued)***

Bit	Name	Access	Description	Default
15:14	EQZ_L_SYNC_MODE	R/W	Synchronization mode 0: Independent 1: Attached to parctrl FSM 1 2: Attached to parctrl FSM 2 3: Attached to both parctrl FSMs	0x0
13:12	EQZ_L_READ_CNT_SEL	R/W	Select counter to be read 0: eqz_l_value 1: Hit counter 2: Error counter	0x0
10	EQZ_L_CTRL_MODE	R/W	Parameter control mode for EQZ_L parameter 0: Discrete 1: Continuous	0x1
9:4	EQZ_L_CTRL_THRES	R/W	Alternative threshold for EQZ_L parameter (controller goal: err_cnt = 0.5*EQZ_L_THRES)	0x28
3	EQZ_L_CTRL_THRES_ENA	R/W	Enable use of alternative threshold for EQZ_L parameter 0: Use default threshold 1: Use alternative threshold	0x0
2	EQZ_L_START_CTRL	R/W	Start operation (parameter update). Should be cleared afterwards in One-time mode and stay set in Non-stop and Paused mode	0x0
1:0	EQZ_L_OP_MODE	R/W	Operation mode 0: Off 1: One-time 2: Non-stop 3: Paused	0x0

2.8.1.26 APC EQZ_L Timer Config

Short Name:APC_EQZ_L_TIMER_CFG

Address:0x9F019

Configuration registers for EQZ_L controller timing.

Table 556 • **APC EQZ_L Timer Config**

Bit	Name	Access	Description	Default
31:16	EQZ_L_PS_TIME	R/W	Pause time (in number of rx_clk cycles)	0x0064
15:0	EQZ_L_OP_TIME	R/W	Operation time (in number of rx_clk cycles)	0x03E8

2.8.1.27 APC EQZ_L Parameter Control

Short Name:APC_EQZ_L_PAR_CFG

Address:0x9F01A

Configuration register for controlled EQZ_L parameter. Note, for parameters larger than 8 bits, ini/min/max values are shifted to the left. For parameters smaller than 8 bits only the lower bits of ini/min/max are used.

Table 557 • **APC EQZ_L Parameter Control**

Bit	Name	Access	Description	Default
31	EQZ_L_DIR_SEL	R/W	Select parameter update direction 0: Normal 1: Inverted	0x0
30:26	EQZ_L_RANGE_SEL	R/W	Parameter range selection (only when CTRL_MODE = continuous). Value complies to number of left-shifts	0x00
25:24	EQZ_L_CHG_MODE	R/W	Parameter change mode 0: Automatic update 1: Preset (use EQZ_L_INI as fix value internal processing continues) 2: Freeze (internal processing stops parameter stays at current value) 3: No update (internal processing continues but parameter is not updated)	0x0
23:16	EQZ_L_MAX	R/W	Maximum value of parameter	0x00
15:8	EQZ_L_MIN	R/W	Minimum value of parameter	0x00
7:0	EQZ_L_INI	R/W	Parameter initial value	0x00

2.8.1.28 APC EQZ_AGC Control

Short Name:APC_EQZ_AGC_CTRL

Address:0x9F01B

General behavior control for EQZ_AGC parameter control.

Table 558 • **APC EQZ_AGC Control**

Bit	Name	Access	Description	Default
29:27	EQZ_AGC_RECOVER_MODE	R/W	EQZ_AGC recovery behavior 0: No auto-recovery 1: Freeze EQZ_AGC on weak (eqz_gain > eqz_gain_freeze_thres) or missing input signal 2: Freeze EQZ_AGC on weak signal and restart on missing input signal 3: Freeze EQZ_AGC on missing input signal 4: Freeze EQZ_AGC on missing input signal and auto-restart after Restart-Delay-Timer has expired 5: Auto-restart EQZ_AGC on missing input signal 6-7: Reserved	0x0
26	EQZ_AGC_CTRL_DONE	R/O	Parameter control state in one-time mode 1: Finished	0x0
25:16	EQZ_AGC_ACTVAL	R/O	Parameter value (controlled/computed value)	0x000

Table 558 • **APC EQZ_AGC Control *(continued)***

Bit	Name	Access	Description	Default
15:14	EQZ_AGC_SYNC_MODE	R/W	Synchronization mode 0: Independent 1: Attached to parctrl FSM 1 2: Attached to parctrl FSM 2 3: Attached to both parctrl FSMs	0x0
13:12	EQZ_AGC_READ_CNT_SEL	R/W	Select counter to be read 0: eqz_agc_value 1: Hit counter 2: Error counter	0x0
10	EQZ_AGC_CTRL_MODE	R/W	Parameter control mode for EQZ_AGC parameter 0: Discrete 1: Continuous	0x1
9:4	EQZ_AGC_CTRL_THRES	R/W	Alternative threshold for EQZ_AGC parameter (controller goal: err_cnt = 0.5*EQZ_AGC_THRES)	0x28
3	EQZ_AGC_CTRL_THRES_ENA	R/W	Enable use of alternative threshold for EQZ_AGC parameter 0: Use default threshold 1: Use alternative threshold	0x0
2	EQZ_AGC_START_CTRL	R/W	Start operation (parameter update). Should be cleared afterwards in One-time mode and stay set in Non-stop and Paused mode	0x0
1:0	EQZ_AGC_OP_MODE	R/W	Operation mode 0: Off 1: One-time 2: Non-stop 3: Paused	0x0

2.8.1.29 APC EQZ_AGC Timer Config

Short Name:APC_EQZ_AGC_TIMER_CFG

Address:0x9F01C

Configuration registers for EQZ_AGC controller timing.

Table 559 • **APC EQZ_AGC Timer Config**

Bit	Name	Access	Description	Default
31:16	EQZ_AGC_PS_TIME	R/W	Pause time (in number of rx_clk cycles)	0x0064
15:0	EQZ_AGC_OP_TIME	R/W	Operation time (in number of rx_clk cycles)	0x03E8

2.8.1.30 APC EQZ_AGC Parameter Control

Short Name:APC_EQZ_AGC_PAR_CFG

Address:0x9F01D

Configuration register for controlled EQZ_AGC parameter. Note, for parameters larger than 8 bits, ini/min/max values are shifted to the left. For parameters smaller than 8 bits only the lower bits of ini/min/max are used.

Table 560 • **APC EQZ_AGC Parameter Control**

Bit	Name	Access	Description	Default
31	EQZ_AGC_DIR_SEL	R/W	Select parameter update direction 0: Normal 1: Inverted	0x0
30:26	EQZ_AGC_RANGE_SEL	R/W	Parameter range selection (only when CTRL_MODE = continuous). Value complies to number of left-shifts	0x00
25:24	EQZ_AGC_CHG_MODE	R/W	Parameter change mode 0: Automatic update 1: Preset (use EQZ_AGC_INI as fix value internal processing continues) 2: Freeze (internal processing stops parameter stays at current value) 3: No update (internal processing continues but parameter is not updated)	0x0
23:16	EQZ_AGC_MAX	R/W	Maximum value of parameter	0x00
15:8	EQZ_AGC_MIN	R/W	Minimum value of parameter	0x00
7:0	EQZ_AGC_INI	R/W	Parameter initial value	0x00

2.8.1.31 APC DFE1 Control

Short Name:APC_DFE1_CTRL

Address:0x9F01E

General behavior control for DFE1 parameter control.

Table 561 • **APC DFE1 Control**

Bit	Name	Access	Description	Default
29:27	DFE1_RECOVER_MODE	R/W	DFE1 recovery behavior 0: No auto-recovery 1: Freeze DFE1 on weak (eqz_gain > eqz_gain_freeze_thres) or missing input signal 2: Freeze DFE1 on weak signal and restart on missing input signal 3: Freeze DFE1 on missing input signal 4: Freeze DFE1 on missing input signal and auto-restart after Restart-Delay-Timer has expired 5: Auto-restart DFE1 on missing input signal 6-7: Reserved	0x0
26	DFE1_CTRL_DONE	R/O	Parameter control state in one-time mode 1: Finished	0x0
25:16	DFE1_ACTVAL	R/O	Parameter value (controlled/computed value)	0x000

Table 561 • **APC DFE1 Control** ***(continued)***

Bit	Name	Access	Description	Default
15:14	DFE1_SYNC_MODE	R/W	Synchronization mode 0: Independent 1: Attached to parctrl FSM 1 2: Attached to parctrl FSM 2 3: Attached to both parctrl FSMs	0x0
13:12	DFE1_READ_CNT_SEL	R/W	Select counter to be read 0: dfe1_value 1: Hit counter 2: Error counter	0x0
10	DFE1_CTRL_MODE	R/W	Parameter control mode for DFE1 parameter 0: Discrete 1: Continuous	0x1
9:4	DFE1_CTRL_THRES	R/W	Alternative threshold for DFE1 parameter (controller goal: err_cnt = 0.5*DFE1_THRES)	0x28
3	DFE1_CTRL_THRES_ENA	R/W	Enable use of alternative threshold for DFE1 parameter 0: Use default threshold 1: Use alternative threshold	0x0
2	DFE1_START_CTRL	R/W	Start operation (parameter update). Should be cleared afterwards in One-time mode and stay set in Non-stop and Paused mode	0x0
1:0	DFE1_OP_MODE	R/W	Operation mode 0: Off 1: One-time 2: Non-stop 3: Paused	0x0

2.8.1.32 APC DFE1 Timer Config

Short Name:APC_DFE1_TIMER_CFG

Address:0x9F01F

Configuration registers for DFE1 controller timing.

Table 562 • **APC DFE1 Timer Config**

Bit	Name	Access	Description	Default
31:16	DFE1_PS_TIME	R/W	Pause time (in number of rx_clk cycles)	0x0064
15:0	DFE1_OP_TIME	R/W	Operation time (in number of rx_clk cycles)	0x03E8

2.8.1.33 APC DFE1 Parameter Control

Short Name:APC_DFE1_PAR_CFG

Address:0x9F020

Configuration register for controlled DFE1 parameter. Note, for parameters larger than 8 bits, ini/min/max values are shifted to the left. For parameters smaller than 8 bits only the lower bits of ini/min/max are used.

Table 563 • **APC DFE1 Parameter Control**

Bit	Name	Access	Description	Default
31	DFE1_DIR_SEL	R/W	Select parameter update direction 0: Normal 1: Inverted	0x0
30:26	DFE1_RANGE_SEL	R/W	Parameter range selection (only when CTRL_MODE = continuous). Value complies to number of left-shifts	0x00
25:24	DFE1_CHG_MODE	R/W	Parameter change mode 0: Automatic update 1: Preset (use DFE1_INI as fix value internal processing continues) 2: Freeze (internal processing stops parameter stays at current value) 3: No update (internal processing continues but parameter is not updated)	0x0
23:16	DFE1_MAX	R/W	Maximum value of parameter	0x00
15:8	DFE1_MIN	R/W	Minimum value of parameter	0x00
7:0	DFE1_INI	R/W	Parameter initial value	0x00

2.8.1.34 APC DFE2 Control

Short Name:APC_DFE2_CTRL

Address:0x9F021

General behavior control for DFE2 parameter control.

Table 564 • **APC DFE2 Control**

Bit	Name	Access	Description	Default
29:27	DFE2_RECOVER_MODE	R/W	DFE2 recovery behavior 0: No auto-recovery 1: Freeze DFE2 on weak (eqz_gain > eqz_gain_freeze_thres) or missing input signal 2: Freeze DFE2 on weak signal and restart on missing input signal 3: Freeze DFE2 on missing input signal 4: Freeze DFE2 on missing input signal and auto-restart after Restart-Delay-Timer has expired 5: Auto-restart DFE2 on missing input signal 6-7: Reserved	0x0
26	DFE2_CTRL_DONE	R/O	Parameter control state in one-time mode 1: Finished	0x0
25:16	DFE2_ACTVAL	R/O	Parameter value (controlled/computed value)	0x000

Table 564 • **APC DFE2 Control** ***(continued)***

Bit	Name	Access	Description	Default
15:14	DFE2_SYNC_MODE	R/W	Synchronization mode 0: Independent 1: Attached to parctrl FSM 1 2: Attached to parctrl FSM 2 3: Attached to both parctrl FSMs	0x0
13:12	DFE2_READ_CNT_SEL	R/W	Select counter to be read 0: dfe2_value 1: Hit counter 2: Error counter	0x0
10	DFE2_CTRL_MODE	R/W	Parameter control mode for DFE2 parameter 0: Discrete 1: Continuous	0x1
9:4	DFE2_CTRL_THRES	R/W	Alternative threshold for DFE2 parameter (controller goal: err_cnt = 0.5*DFE2_THRES)	0x28
3	DFE2_CTRL_THRES_ENA	R/W	Enable use of alternative threshold for DFE2 parameter 0: Use default threshold 1: Use alternative threshold	0x0
2	DFE2_START_CTRL	R/W	Start operation (parameter update). Should be cleared afterwards in One-time mode and stay set in Non-stop and Paused mode	0x0
1:0	DFE2_OP_MODE	R/W	Operation mode 0: Off 1: One-time 2: Non-stop 3: Paused	0x0

2.8.1.35 APC DFE2 Timer Config

Short Name:APC_DFE2_TIMER_CFG

Address:0x9F022

Configuration registers for DFE2 controller timing.

Table 565 • **APC DFE2 Timer Config**

Bit	Name	Access	Description	Default
31:16	DFE2_PS_TIME	R/W	Pause time (in number of rx_clk cycles)	0x0064
15:0	DFE2_OP_TIME	R/W	Operation time (in number of rx_clk cycles)	0x03E8

2.8.1.36 APC DFE2 Parameter Control

Short Name:APC_DFE2_PAR_CFG

Address:0x9F023

Configuration register for controlled DFE2 parameter. Note, for parameters larger than 8 bits, ini/min/max values are shifted to the left. For parameters smaller than 8 bits only the lower bits of ini/min/max are used.

Table 566 • **APC DFE2 Parameter Control**

Bit	Name	Access	Description	Default
31	DFE2_DIR_SEL	R/W	Select parameter update direction 0: Normal 1: Inverted	0x0
30:26	DFE2_RANGE_SEL	R/W	Parameter range selection (only when CTRL_MODE = continuous). Value complies to number of left-shifts	0x00
25:24	DFE2_CHG_MODE	R/W	Parameter change mode 0: Automatic update 1: Preset (use DFE2_INI as fix value internal processing continues) 2: Freeze (internal processing stops parameter stays at current value) 3: No update (internal processing continues but parameter is not updated)	0x0
23:16	DFE2_MAX	R/W	Maximum value of parameter	0x00
15:8	DFE2_MIN	R/W	Minimum value of parameter	0x00
7:0	DFE2_INI	R/W	Parameter initial value	0x00

2.8.1.37 APC DFE3 Control

Short Name:APC_DFE3_CTRL

Address:0x9F024

General behavior control for DFE3 parameter control.

Table 567 • **APC DFE3 Control**

Bit	Name	Access	Description	Default
29:27	DFE3_RECOVER_MODE	R/W	DFE3 recovery behavior 0: No auto-recovery 1: Freeze DFE3 on weak (eqz_gain > eqz_gain_freeze_thres) or missing input signal 2: Freeze DFE3 on weak signal and restart on missing input signal 3: Freeze DFE3 on missing input signal 4: Freeze DFE3 on missing input signal and auto-restart after Restart-Delay-Timer has expired 5: Auto-restart DFE3 on missing input signal 6-7: Reserved	0x0
26	DFE3_CTRL_DONE	R/O	Parameter control state in one-time mode 1: Finished	0x0
25:16	DFE3_ACTVAL	R/O	Parameter value (controlled/computed value)	0x000

Table 567 • **APC DFE3 Control** ***(continued)***

Bit	Name	Access	Description	Default
15:14	DFE3_SYNC_MODE	R/W	Synchronization mode 0: Independent 1: Attached to parctrl FSM 1 2: Attached to parctrl FSM 2 3: Attached to both parctrl FSMs	0x0
13:12	DFE3_READ_CNT_SEL	R/W	Select counter to be read 0: dfe3_value 1: Hit counter 2: Error counter	0x0
10	DFE3_CTRL_MODE	R/W	Parameter control mode for DFE3 parameter 0: Discrete 1: Continuous	0x1
9:4	DFE3_CTRL_THRES	R/W	Alternative threshold for DFE3 parameter (controller goal: err_cnt = 0.5*DFE3_THRES)	0x28
3	DFE3_CTRL_THRES_ENA	R/W	Enable use of alternative threshold for DFE3 parameter 0: Use default threshold 1: Use alternative threshold	0x0
2	DFE3_START_CTRL	R/W	Start operation (parameter update). Should be cleared afterwards in One-time mode and stay set in Non-stop and Paused mode	0x0
1:0	DFE3_OP_MODE	R/W	Operation mode 0: Off 1: One-time 2: Non-stop 3: Paused	0x0

2.8.1.38 APC DFE3 Timer Config

Short Name:APC_DFE3_TIMER_CFG

Address:0x9F025

Configuration registers for DFE3 controller timing.

Table 568 • **APC DFE3 Timer Config**

Bit	Name	Access	Description	Default
31:16	DFE3_PS_TIME	R/W	Pause time (in number of rx_clk cycles)	0x0064
15:0	DFE3_OP_TIME	R/W	Operation time (in number of rx_clk cycles)	0x03E8

2.8.1.39 APC DFE3 Parameter Control

Short Name:APC_DFE3_PAR_CFG

Address:0x9F026

Configuration register for controlled DFE3 parameter. Note, for parameters larger than 8 bits, ini/min/max values are shifted to the left. For parameters smaller than 8 bits only the lower bits of ini/min/max are used.

Table 569 • **APC DFE3 Parameter Control**

Bit	Name	Access	Description	Default
31	DFE3_DIR_SEL	R/W	Select parameter update direction 0: Normal 1: Inverted	0x0
30:26	DFE3_RANGE_SEL	R/W	Parameter range selection (only when CTRL_MODE = continuous). Value complies to number of left-shifts	0x00
25:24	DFE3_CHG_MODE	R/W	Parameter change mode 0: Automatic update 1: Preset (use DFE3_INI as fix value internal processing continues) 2: Freeze (internal processing stops parameter stays at current value) 3: No update (internal processing continues but parameter is not updated)	0x0
23:16	DFE3_MAX	R/W	Maximum value of parameter	0x00
15:8	DFE3_MIN	R/W	Minimum value of parameter	0x00
7:0	DFE3_INI	R/W	Parameter initial value	0x00

2.8.1.40 APC DFE4 Control

Short Name:APC_DFE4_CTRL

Address:0x9F027

General behavior control for DFE4 parameter control.

Table 570 • **APC DFE4 Control**

Bit	Name	Access	Description	Default
29:27	DFE4_RECOVER_MODE	R/W	DFE4 recovery behavior 0: No auto-recovery 1: Freeze DFE4 on weak (eqz_gain > eqz_gain_freeze_thres) or missing input signal 2: Freeze DFE4 on weak signal and restart on missing input signal 3: Freeze DFE4 on missing input signal 4: Freeze DFE4 on missing input signal and auto-restart after Restart-Delay-Timer has expired 5: Auto-restart DFE4 on missing input signal 6-7: Reserved	0x0
26	DFE4_CTRL_DONE	R/O	Parameter control state in one-time mode 1: Finished	0x0
25:16	DFE4_ACTVAL	R/O	Parameter value (controlled/computed value)	0x000

Table 570 • **APC DFE4 Control *(continued)***

Bit	Name	Access	Description	Default
15:14	DFE4_SYNC_MODE	R/W	Synchronization mode 0: Independent 1: Attached to parctrl FSM 1 2: Attached to parctrl FSM 2 3: Attached to both parctrl FSMs	0x0
13:12	DFE4_READ_CNT_SEL	R/W	Select counter to be read 0: dfe4_value 1: Hit counter 2: Error counter	0x0
10	DFE4_CTRL_MODE	R/W	Parameter control mode for DFE4 parameter 0: Discrete 1: Continuous	0x1
9:4	DFE4_CTRL_THRES	R/W	Alternative threshold for DFE4 parameter (controller goal: err_cnt = 0.5*DFE4_THRES)	0x28
3	DFE4_CTRL_THRES_ENA	R/W	Enable use of alternative threshold for DFE4 parameter 0: Use default threshold 1: Use alternative threshold	0x0
2	DFE4_START_CTRL	R/W	Start operation (parameter update). Should be cleared afterwards in One-time mode and stay set in Non-stop and Paused mode	0x0
1:0	DFE4_OP_MODE	R/W	Operation mode 0: Off 1: One-time 2: Non-stop 3: Paused	0x0

2.8.1.41 APC DFE4 Timer Config

Short Name:APC_DFE4_TIMER_CFG

Address:0x9F028

Configuration registers for DFE4 controller timing.

Table 571 • **APC DFE4 Timer Config**

Bit	Name	Access	Description	Default
31:16	DFE4_PS_TIME	R/W	Pause time (in number of rx_clk cycles)	0x0064
15:0	DFE4_OP_TIME	R/W	Operation time (in number of rx_clk cycles)	0x03E8

2.8.1.42 APC DFE4 Parameter Control

Short Name:APC_DFE4_PAR_CFG

Address:0x9F029

Configuration register for controlled DFE4 parameter. Note, for parameters larger than 8 bits, ini/min/max values are shifted to the left. For parameters smaller than 8 bits only the lower bits of ini/min/max are used.

Table 572 • **APC DFE4 Parameter Control**

Bit	Name	Access	Description	Default
31	DFE4_DIR_SEL	R/W	Select parameter update direction 0: Normal 1: Inverted	0x0
30:26	DFE4_RANGE_SEL	R/W	Parameter range selection (only when CTRL_MODE = continuous). Value complies to number of left-shifts	0x00
25:24	DFE4_CHG_MODE	R/W	Parameter change mode 0: Automatic update 1: Preset (use DFE4_INI as fix value internal processing continues) 2: Freeze (internal processing stops parameter stays at current value) 3: No update (internal processing continues but parameter is not updated)	0x0
23:16	DFE4_MAX	R/W	Maximum value of parameter	0x00
15:8	DFE4_MIN	R/W	Minimum value of parameter	0x00
7:0	DFE4_INI	R/W	Parameter initial value	0x00

2.8.1.43 APC LC softcontrol Configuration

Short Name:APC_LC_SOFTCTRL_CFG

Address:0x9F02A

Configuration register for the LC-Softcontrol logic block. The L and C parameters can be controlled depending on DFE1 and DFE2 and EQZ_AGC parameters instead of pattern matching.

Table 573 • **APC LC softcontrol Configuration**

Bit	Name	Access	Description	Default
31:28	LC_SC_TIMER	R/W	Operation timer configuration: L/C-control operates in every 2^(2*LC_SC_TIMER)-th clock cycle. 0: Operate every clock cycle 1: Operate every 4th clock cycle 2: Operate every 16th clock cycle ...	0x0
27:24	LC_SC_AVGSHFT	R/W	DFE1/2 and EQZ_AGC averaging behavior. DFE/AGC parameters are averaged over 2^(8+LC_SC_AVGSHFT) input values. 0: Average over 256 values 1: Average over 512 values ...	0x8
23:20	LC_SC_DFE1_THRESHOLD	R/W	DFE1 comparison threshold for L-control used in mode 2. EQZ_L is increased/decreased if DFE1 differs from neutral value by more than LC_SC_DFE1_THRESHOLD.	0x8

Table 573 • **APC LC softcontrol Configuration**

Bit	Name	Access	Description	Default
19:16	LC_SC_DFE2_THRESHOLD	R/W	DFE2 comparison threshold for C-control used in mode 2. EQZ_C is increased/decreased if DFE1 differs from neutral value by more than LC_SC_DFE2_THRESHOLD.	0x4
15:9	LC_SC_AGC_THRESHOLD	R/W	EQZ_AGC threshold for mandatory increase of L and C. If EQZ_AGC > (128+LC_SC_AGC_THRESHOLD) then L and C control values are increased. 0: 128 1: 129 ... 127: 255	0x7D
8	LC_SC_DIV_C_SEL	R/W	Define DFE2 comparison parameter for EQZ_C control in mode 1 0: EQZ_L 1: EQZ_C	0x0
7:5	LC_SC_DIV_L	R/W	Select divider for L-control used in mode 1 (Divider = 4+LC_SC_DIV_L) 0: Divide by 4 1: Divide by 5 ... 7: Divide by 11	0x4
4:2	LC_SC_DIV_C	R/W	Select divider for C-control used in mode 1 (Divider = 4+LC_SC_DIV_C) 0: Divide by 4 1: Divide by 5 ... 7: Divide by 11	0x4
1:0	LC_SC_MODE	R/W	Select LC soft-control mode. LC soft-control modes must be enabled first after INI/MIN/MAX values of all parameters have been programmed. 0: Disabled 1: Mode 1 2: Mode 2 3: Reserved	0x0

2.8.2 SD10G65 DES Configuration and Status

Configuration and status register set for SD10G65 DES

2.8.2.1 SD10G65 DES Configuration 0

Short Name:SD10G65_DES_CFG0

Address:0x9F100

Configuration register 0 for SD10G65 DES.

Table 574 • **SD10G65 DES Configuration 0**

Bit	Name	Access	Description	Default
7	DES_INV_H	R/W	Invert output of high auxiliary deserializer	0x0
6	DES_INV_L	R/W	Invert output of low auxiliary deserializer	0x0

Table 574 • **SD10G65 DES Configuration 0 *(continued)***

Bit	Name	Access	Description	Default
5	DES_INV_M	R/W	Invert output of main deserializer	0x0
4:2	DES_IF_MODE_SEL	R/W	Interface width 0: 8 1: 10 2: 16 (energy efficient) 3: 20 (energy efficient) 4: 32 5: 40 6: 16 bit (fast) 7: 20 bit (fast)	0x4
1	DES_VSC_DIS	R/W	Auxiliary deserializer channels disable.	0x1
0	DES_DIS	R/W	Deserializer disable.	0x0

2.8.2.2 SD10G65 MOEBDIV Configuration 0

Short Name:SD10G65_MOEBDIV_CFG0

Address:0x9F101

Configuration register 0 for SD10G65 MoebiusDivider

Table 575 • **SD10G65 MOEBDIV Configuration 0**

Bit	Name	Access	Description	Default
11:9	MOEBDIV_BW_CDR_SEL_A	R/W	Bandwidth selection for cp/md of cdr loop when core NOT flags valid data detected	0x3
8:6	MOEBDIV_BW_CDR_SEL_B	R/W	Bandwidth selection for cp/md of cdr loop when core flags valid data detected	0x3
5:3	MOEBDIV_BW_CORE_SEL	R/W	Bandwidth selection for cp/md signals towards core	0x0
2	MOEBDIV_CPMD_SWAP	R/W	CP/MD swapping	0x0
1	MOEBDIV_DIV32_ENA	R/W	MD divider enable	0x0
0	MOEBDIV_DIS	R/W	Divider disable	0x0

2.8.3 SD10G65 OB Configuration and Status

Configuration and status register set for SD10G65 OB

2.8.3.1 SD10G65 OB Configuration 0

Short Name:SD10G65_OB_CFG0

Address:0x9F110

Configuration register 0 for SD10G65 OB.

Table 576 • **SD10G65 OB Configuration 0**

Bit	Name	Access	Description	Default
23	SER_INV	R/W	Invert input to serializer	0x0
22:21	CLK_BUF_CMV	R/W	Control of common mode voltage of clock buffer between synthesizer and OB.	0x0
17	RST	R/W	Set digital part into pseudo reset	0x0

Table 576 • **SD10G65 OB Configuration 0 *(continued)***

Bit	Name	Access	Description	Default
16	EN_PAD_LOOP	R/W	Enable pad loop	0x0
15	EN_INP_LOOP	R/W	Enable input loop	0x0
14	EN_DIRECT	R/W	Enable direct path	0x0
13	EN_OB	R/W	Enable output buffer and serializer	0x0
8	INCR_LEVN	R/W	Selects amplitude range controlled via levn. See description of levn.	0x1
7:5	SEL_IFW	R/W	Interface width 0: 8 1: 10 2: 16 3: 20 4: 32 5: 40 6-7: Reserved	0x4
4:0	LEVN	R/W	Amplitude control value. Step size is 25 mVpp, decreasing amplitude with increasing control value. Range depends on incr_levn. Coding for incr_levn=0: 31: 500mVpp 30: 525mVpp 29: 550mVpp ... 0: 1275mVpp. Coding for incr_levn=1: 31: 300mVpp 30: 325mVpp 29: 350mVpp ... 0: 1075mVpp. (Note: maximum achievable amplitude depends on the supply voltage)	0x07

2.8.3.2 SD10G65 OB Configuration 1

Short Name:SD10G65_OB_CFG1

Address:0x9F111

Configuration register 1 for SD10G65 OB.

Table 577 • **SD10G65 OB Configuration 1**

Bit	Name	Access	Description	Default
26	AB_COMP_EN	R/W	Enable amplitude compensation of AB bleed current	0x1
25:23	DIODE_CUR	R/W	Bleed current for class AB operation of driver 0: 1% 1: 0.5% 2: 2% 3: reserved	0x0

Table 577 • **SD10G65 OB Configuration 1 *(continued)***

Bit	Name	Access	Description	Default
22:21	LEV_SHFT	R/W	Level shift ctrl of class AB bias generator 0: 50mV 1: 100mV 2:150mV 3: 200mV	0x1
19:18	PREDRV_R_CTRL	R/W	Slew rate ctrl of OB (R), encoding see PREDRV_C_CTRL	0x3
17:16	PREDRV_C_CTRL	R/W	Slew rate ctrl of OB (C) C=3 R=3: 25ps C=3 R=0: 35ps C=0 R=3: 55ps C=1 R=0: 70ps C=0 R=0: 120 ps	0x3
15:10	VTAIL	R/W	Tail voltage driver settings 0: reserved 1: 75mV 2: 100mV 4: 125mV 8: 150mV 16: 175mV 32: 200mV Intermediate values possible when setting two bits	0x02
9:5	VCAS	R/W	Ctrl of cascade volt in drv stage 0: reserved 1: 0 2: 1/12 4: 2/12 8: 3/12 16: 4/12 Intermediate values possible when setting two bits	0x01
4	R_COR	R/W	Additional resistor calibration trim	0x0
3:0	R_I	R/W	Offset resistance adjustment for CML cells (two-complement) 1000: -8 1111: -1 0000: 0 0111: 7	0x0

2.8.3.3 SD10G65 OB Configuration 2

Short Name:SD10G65_OB_CFG2

Address:0x9F112

Configuration register 2 for SD10G65 OB. D_filter contains four 6-bit precalculated DA input values. Please note the differences in programming for various interface (IF) bit widths. For calculation details see documentation of OB10G.

Table 578 • **SD10G65 OB Configuration 2**

Bit	Name	Access	Description	Default
23:0	D_FILTER	R/W	Transmit filter coefficients for FIR taps. Suggested start value (no emphasis, max amplitude) 0x820820: for I/F width 8/10 bits 0x7DF820: for I/F width 16/20/32/40 bits	0x7DF820

2.8.3.4 SD10G65 OB Configuration 3

Short Name:SD10G65_OB_CFG3

Address:0x9F113

Configuration register 3 for SD10G65 OB access to receiver detect functionality.

Table 579 • **SD10G65 OB Configuration 3**

Bit	Name	Access	Description	Default
18	REC_DET_DONE	R/O	Indicates a completed receiver detect measurement. Should be one few us after rec_det_start is set.	0x0
17	REC_DET_START	R/W	Rising edge starts receiver detect measurement. Has to be kept set until rec_det_value has been read.	0x0
16	REC_DET_ENABLE	R/W	Enable receiver detect function. MUST be disabled for normal operation!	0x0
15:12	RESERVED	R/W	Must be set to its default.	0x2
11:0	REC_DET_VALUE	R/O	Holds the time between the start and the flag of the receiver detect measurement. Time [ns +/- 4 ns] = 8 * value - 12	0x000

2.8.4 SD10G65 IB Configuration and Status

Configuration and status register set for SD10G65 IB

2.8.4.1 SD10G65 IB Configuration 0

Short Name:SD10G65_IB_CFG0

Address:0x9F120

Configuration register 0 for SD10G65 IB. Note: Configuration bit-grp IB_CLKDIV_ENA was named IB_VSCOPE_CLK_ENA in an early revision of the input buffer.

Table 580 • **SD10G65 IB Configuration 0**

Bit	Name	Access	Description	Default
30:27	IB_RCML_ADJ	R/W	Offset resistance adjustment for CML cells (two-complement) 1000: -8 1111: -1 0000: 0 0111: 7	0x0

Table 580 • **SD10G65 IB Configuration 0** ***(continued)***

Bit	Name	Access	Description	Default
26:23	IB_TERM_V_SEL	R/W	Select termination voltage	0x8
22	IB_TERM_VDD_ENA	R/W	Enable common mode termination 0: no common mode termination (only AC-common mode termination) 1: termination to VDDI	0x0
21	IB_RIB_SHIFT	R/W	Shifts resistance adjustment value ib_rib_adj by +1	0x0
20:17	IB_RIB_ADJ	R/W	Offset resistance adjustment for termination (two-complement) 1000: -8 1111: -1 0000: 0 0111: 7	0x0
14	IB_DFE_ENA	R/W	Enable DFE stage (gates IB_ISEL_DFE) 0: Disable 1: Enable	0x0
13:12	IB_SIG_SEL	R/W	Select input buffer input signal 0: normal operation 1: -6dB input 2: OB->IB data loop or test signal 3: RESERVED	0x0
11	IB_VBULK_SEL	R/W	Controls Bulk Voltage of High Speed Cells 0: High 1: Low (mission mode)	0x1
10	IB_IA_ENA	R/W	Enable for IA including ACJtag 0: Disable 1: Enable	0x1
9	IB_IA_SDET_ENA	R/W	Enable for IA signal detect circuit (IB_SDET_SEL = 0 required) 0: Disable 1: Enable	0x0
8	IB_IE_SDET_ENA	R/W	Enable for IA signal detect circuit (IB_SDET_SEL = 1 required) 0: Disable 1: Enable	0x0
7	IB_LD_ENA	R/W	Enable for level detect circuit 0: Disable 1: Enable	0x0
6	IB_1V_ENA	R/W	Enable for 1V mode 0: VDDI=1.2V 1: VDDI=1.0V	0x0
5	IB_CLKDIV_ENA	R/W	Enable clock dividers in sampling stag 0: Disable (use in double rate mode) 1: Enable (use in full rate mode)	0x0
3	IB_VSCOPE_ENA	R/W	Enable VScope Path of Sampling-Stage 0: Disable 1: Enable	0x0

Table 580 • **SD10G65 IB Configuration 0 *(continued)***

Bit	Name	Access	Description	Default
2	IB_SAM_ENA	R/W	Enable SAMpling stage 0: Disable 1: Enable (mission mode)	0x0
1	IB_EQZ_ENA	R/W	Enable EQualiZation stage 0: Disable 1: Enable (mission mode)	0x0

2.8.4.2 SD10G65 IB Configuration 1

Short Name:SD10G65_IB_CFG1

Address:0x9F121

Configuration register 1 for SD10G65 IB.

Table 581 • **SD10G65 IB Configuration 1**

Bit	Name	Access	Description	Default
31:28	IB_AMP_L	R/W	Inductor peaking of 1. stage Input buffer 0: no peaking 15: max. peaking max. peaking > 3db at 8GHz	0x8
27:24	IB_EQZ_L0	R/W	Inductor peaking of EQ-Buffer0 (over all 2. stage) 0: no peaking 15: max. peaking max. peaking > 3db at 8GHz	0x8
23:20	IB_EQZ_L1	R/W	Inductor peaking of EQ-Buffer1 (over all 3. stage) 0: no peaking 15: max. peaking max. peaking > 3dB at 8GHz	0x8
19:16	IB_EQZ_L2	R/W	Inductor peaking of EQ-Buffer2 (over all 4. stage) 0: no peaking 15: max. peaking max. peaking > 3dB at 8GHz	0x8
15:12	IB_AGC_L	R/W	Inductor peaking of EQ-Buffer3 (over all 5. stage) 0: no peaking 15: max. peaking max. peaking > 3dB at 8GHz	0x8
11:9	IB_AMP_C	R/W	C-gain peaking for IB-stage 0: no peaking 7: max. peaking corner frequency adjustment with ib_eqz_c_adj_ib	0x4
8:6	IB_EQZ_C0	R/W	C-gain peaking for EQ-stage0 0: no peaking 7: max. peaking corner frequency adjustment with ib_eqz_c_adj_es0	0x4

Table 581 • **SD10G65 IB Configuration 1 *(continued)***

Bit	Name	Access	Description	Default
5:3	IB_EQZ_C1	R/W	C-gain peaking for EQ-stage1 0: no peaking 7: max. peaking corner frequency adjustment with ib_eqz_c_adj_es1	0x4
2:0	IB_EQZ_C2	R/W	C-gain peaking for EQ-stage2 0: no peaking 7: max. peaking corner frequency adjustment with ib_eqz_c_adj_es2	0x4

2.8.4.3 SD10G65 IB Configuration 2

Short Name:SD10G65_IB_CFG2

Address:0x9F122

Configuration register 2 for SD10G65 IB.

Table 582 • **SD10G65 IB Configuration 2**

Bit	Name	Access	Description	Default
27:18	IB_EQZ_GAIN	R/W	Gain of Input Buffer 0-511 gain adjustment only in first stage > 511 gain in first stage at max. 512-639 gain in 2.stage increased from 1 to 2 > 639 gain = 2 640-767 gain in 3.stage increased from 1 to 2 > 767 gain = 2 768-895 gain in 4.stage increased from 1 to 2 >895 gain at max.	0x040
17:10	IB_EQZ_AGC	R/W	Amplification (gain) of AGC in Input Buffer (normal operation) after gain calibration 0: gain = 0.3 255: gain = 1.5 if disp/disn is active dac function for dfe gain calibration	0x80
9:0	IB_EQZ_OFFSET	R/W	Offset value for IB-stage of Input Buffer 512: neutral > 512: positive < 512: negative range +/- 600mV (low gain) to +/-30mV (high gain) gain dependent offset sensitivity required for Base line wander compensation not supported in test chip	0x200

2.8.4.4 SD10G65 IB Configuration 3

Short Name:SD10G65_IB_CFG3

Address:0x9F123

Configuration register 1 for SD10G65 IB. Note: the behavior of IB_EQ_LD1_OFFSET changes when APC is disabled. In this case IB_EQ_LD1_OFFSET directly controls the level for Level-Detect circuitry 1. Coding: 0: 20mV, 1: 25mV, ... 63: 340mV.

Table 583 • **SD10G65 IB Configuration 3**

Bit	Name	Access	Description	Default
31:30	IB_LDSD_DIVSEL	R/W	Dividing factor for SDET and LD circuits of IE. 0: 128 1: 32 2: 8 3: 4	0x1
29:27	IB_SDET_CLK_DIV	R/W	Clock dividing factor for Signal Detect circuit of IA 0: 2 ... 7: 256	0x5
26	IB_SET_SDET	R/W	Force Signal-Detect output to high level 0: Normal operation 1: Force sigdet high	0x0
24	IB_SDET_SEL	R/W	Selects source of signal detect (ib_X_sdet_ena must be enabled accordingly) 0: IA 1: IE	0x0
23	IB_DIRECT_SEL	R/W	Selects source of direct data path to core 0: IE 1: IA	0x0
22:17	IB_EQ_LD1_OFFSET	R/W	With APC enabled level offset (6bit-signed) compared to IB_EQ_LD0_LEVEL for Level-Detect circuitry 1. Saturating between 20mV and 340mV. See also note in register description. 0: no offset 1: +5mV 31: +155mV 63(= -1): -5mV 32(= -32): -160mV.	0x00
16:11	IB_EQ_LD0_LEVEL	R/W	Level for Level-Detect circuitry 0. 0: 20mV 1: 25mV ... 40: 220mV ... 63: 340mV	0x28
10:5	IB_IE_SDET_LEVEL	R/W	Threshold value for IE Signal-Detect. 0: 20mV 1: 25mV 2: 30mV ... 63: 340mV	0x02
4:0	IB_IA_SDET_LEVEL	R/W	Threshold value for IA Signal-Detect. 0: 0mV ... 8: 80mV ... 31: 310mV	0x08

2.8.4.5 SD10G65 IB Configuration 4

Short Name:SD10G65_IB_CFG4

Address:0x9F124

Configuration register 4 for SD10G65 IB.

Table 584 • **SD10G65 IB Configuration 4**

Bit	Name	Access	Description	Default
31:30	IB_EQZ_C_ADJ_IB	R/W	corner frequency selection for c-gain peaking 1.stage 0: lowest corner frequency 3: highest corner frequency	0x2
29:28	IB_EQZ_C_ADJ_ES2	R/W	corner frequency selection for c-gain peaking 2.stage 0: lowest corner frequency 3: highest corner frequency	0x2
27:26	IB_EQZ_C_ADJ_ES1	R/W	corner frequency selection for c-gain peaking 3.stage 0: lowest corner frequency 3: highest corner frequency	0x2
25:24	IB_EQZ_C_ADJ_ES0	R/W	corner frequency selection for c-gain peaking 4.stage 0: lowest corner frequency 3: highest corner frequency	0x2
23:21	IB_EQZ_L_MODE	R/W	Coder mode: APC L value to IE inductance 0: equ. distributed (double step 3->4) 1: equ. distributed (no change 6+7) 2: 1st buffer max - 2nd buffer max - ...	0x0
20:18	IB_EQZ_C_MODE	R/W	Coder mode: APC C value to IE capacitance 0: equ. distributed 2: 1st buffer max - 2nd buffer max - ...	0x0
17:12	IB_VSCOPE_H_THRES	R/W	Threshold value (offset) for vscope-high sampling path 0: -max 31: -0 32: +0 63: +max (depending on calibration)	0x30
11:6	IB_VSCOPE_L_THRES	R/W	Threshold value (offset) for vscope-low sampling path 0: -max 31: -0 32: +0 63: +max (depending on calibration)	0x0F
5:0	IB_MAIN_THRES	R/W	Threshold value (offset) for main sampling path 0: -max 31: -0 32: +0 63: +max (depending on calibration)	0x20

2.8.4.6 SD10G65 IB Configuration 5

Short Name:SD10G65_IB_CFG5

Address:0x9F125

Configuration register 5 for SD10G65 IB.

Table 585 • **SD10G65 IB Configuration 5**

Bit	Name	Access	Description	Default
31:28	IB_TSTGEN_AMPL	R/W	Test generator amplitude setting 0: 0mV ... 15: 150mV	0x0
27	IB_TSTGEN_ENA	R/W	Test generator enable but data path selected with 'ib_sig_sel' (disable input loop if test generator is used) 0: inactive 1: active	0x0
26	IB_TSTGEN_DATA	R/W	Test generator data 0: low 1: high	0x0
25	IB_TSTGEN_TOGGLE_ENA	R/W	Test generator data toggle enable 0: inactive 1: active	0x0
22	IB_JUMPH_ENA	R/W	Enable jump to opposite half of h-channel 0: Post main sampler 1: Pre main sampler	0x0
21	IB_JUMPL_ENA	R/W	Enable jump to opposite half of l-channel 0: Post main sampler 1: Pre main sampler	0x0
20:19	IB_DFE_DIS	R/W	DFE output disable required to calibrate IS 0: mission mode 3: Vout = 0V 1: Vout= xx*ampldfe/64 2: Vout=-xx*ampldfe/64 ampldfe=196mV if ena1V = '1' (1V mode) ampldfe=260mV if ena1V = '0' (1.2V mode) xx= TBD	0x0
18:17	IB_AGC_DIS	R/W	AGC output disable required to calibrate DFE-gain 0: mission mode 3: Vout = 0V 1: Vout= xx*ampldfe/64 2: Vout=-xx*ampldfe/64 ampldfe=270mV if ena1V = '1' (1V mode) ampldfe=360mV if ena1V = '0' (1.2V mode) xx=	0x0
16	IB_EQ_LD_CAL_ENA	R/W	Selects EQ Level Detect for calibration	0x0
15	IB_THRES_CAL_ENA	R/W	Selects IS threshold circuit for calibration	0x0
14	IB_IS_OFFS_CAL_ENA	R/W	Selects IS offset circuit for calibration	0x0
13	IB_IA_OFFS_CAL_ENA	R/W	Selects IA offset circuit for calibration	0x0
12	IB_IE_SDET_CAL_ENA	R/W	Selects IE Signal Detect for calibration	0x0

Table 585 • **SD10G65 IB Configuration 5** ***(continued)***

Bit	Name	Access	Description	Default
11	IB_HYS_CAL_ENA	R/W	Enable calibration in order to eliminate hysteresis 1: Enable 0: Disable	0x0
10	IB_CALMUX_ENA	R/W	Enables IS MUX in detblk1	0x1
9:6	IB_OFFS_BLKSEL	R/W	Selects calibration target (sample stage threshold, sample stage offset, aux.-stage offset), dependent on calibration group, see encoding. When ib_thres_cal_ena = 1 0: MD0 threshold 1: MD1 threshold 2: CP0 threshold 3: CP1 threshold 4: VH0 threshold 5: VH1 threshold 6: VL0 threshold 7: VL1 threshold When ib_is_offs_cal_ena = 1 0: MD0 offset 1: MD1 offset 2: CP0 offset 3: CP1 offset 4: VH0 offset 5: VH1 offset 6: VL0 offset 7: VL1 offset When ib_ia_offs_cal_ena = 1 0: Observe0 offset 1: Observe1 offset 2: Observe0 threshold 3: Observe1 threshold (MSB not used)	0x0
5:0	IB_OFFS_VALUE	R/W	Calibration value for IA/IS. Values for threshold calibration get inverted for negative threshold voltages (ib_vscope_h_thres, ib_vscope_l_thres or ib_main_thres). For offset calibration 0: -max_offset * 32/32 31: -max_offset * 1/32 32: +max_offset * 1/32 63: +max_offset * 32/32 For threshold calibration 0: min_threshold 63: max_threshold	0x1F

2.8.4.7 SD10G65 IB Configuration 6

Short Name:SD10G65_IB_CFG6

Address:0x9F126

Configuration register 6 for SD10G65 IB.

Table 586 • **SD10G65 IB Configuration 6**

Bit	Name	Access	Description	Default
22:16	IB_EQZ_GAIN_ADJ	R/W	0dB Gain adjustment for EQZ-stages of Input Buffer level at LD0 = LD1 -> 0dB level range 160mV-220mV	0x2A
12	IB_AUTO_AGC_ADJ	R/W	Enable automatic AGC adjustment 1: AGC is adjusted automatically (IB_EQZ_AGC_ADJ value is not used) 0: AGC is adjusted with value stored in IB_EQZ_AGC_ADJ	0x0
11:5	IB_EQZ_AGC_ADJ	R/W	Gain adjustment of AGC-amplifier Bitgroup should be set to 2*IB_DFE_GAIN_ADJ	0x3E
4:0	IB_SAM_OFFS_ADJ	R/W	Range for offset calibration of all sampling paths 0: 0mV 32: 80mV	0x10

2.8.4.8 SD10G65 IB Configuration 7

Short Name:SD10G65_IB_CFG7

Address:0x9F127

Configuration register 7 for SD10G65 IB.

Table 587 • **SD10G65 IB Configuration 7**

Bit	Name	Access	Description	Default
28:23	IB_MAIN_THRES_CAL	R/W	Initial value for calibration of main sampling path	0x30
22	IB_DFE_OFFSET_H_L	R/W	Selects higher or lower DFE offset for IS calibration 0: ib_dfe_offset_l 1: ib_dfe_offset_h	0x0
21:16	IB_DFE_GAIN_ADJ	R/W	Gain adjustment of DFEamplifier DFE Gain 1 Volt mode = 0dB 1.2 Volt mode 1dB measurement with int. DAC and VScope Channels	0x24
11:6	IB_DFE_OFFSET_H	R/W	Higher threshold offset of DFE buffer for IS calibration 0: 0mv 63: 200mV	0x17
5:0	IB_DFE_OFFSET_L	R/W	Lower sample offset of DFE buffer for IS calibration 0: 0mv 63: 200mV	0x06

2.8.4.9 SD10G65 IB Configuration 8

Short Name:SD10G65_IB_CFG8

Address:0x9F128

Configuration register 8 for SD10G65 IB.

Table 588 • **SD10G65 IB Configuration 8**

Bit	Name	Access	Description	Default
20	IB_SEL_VCLK	R/W	Use separate vscope clock for vscope-channels	0x0
19	IB_BIAS_MODE	R/W	Bias regulation mode 0: constant resistor 1: constant current	0x1
18	IB_LAT_NEUTRAL	R/W	Enables neutral setting of latches 1: Reset to mid values 0: Normal operation	0x0
14	RESERVED	R/W	Must be set to its default.	0x1
12:10	IB_CML_AMPL	R/W	Amplitude of cml stages inside IS 0: 200mVppd 7: 240mVppd	0x4
9:4	IB_BIAS_ADJ	R/W	Gain of cml stages inside IS 0: 3dB 31: 6dB 63: 9dB	0x1F
3:0	IB_CML_CURR	R/W	Current through CML Cells 0: 150% 5: 100% 15: 50%	0x5

2.8.4.10 SD10G65 IB Configuration 9

Short Name:SD10G65_IB_CFG9

Address:0x9F129

Configuration register 9 for SD10G65 IB automatically adapted DFE coefficients.

Table 589 • **SD10G65 IB Configuration 9**

Bit	Name	Access	Description	Default
28:24	IB_DFE_COEF4	R/W	Weighting for fourth DFE coefficient	0x10
20:16	IB_DFE_COEF3	R/W	Weighting for third DFE coefficient	0x10
13:8	IB_DFE_COEF2	R/W	Weighting for second DFE coefficient	0x20
6:0	IB_DFE_COEF1	R/W	Weighting for first DFE coefficient	0x40

2.8.4.11 SD10G65 IB Configuration 10

Short Name:SD10G65_IB_CFG10

Address:0x9F12A

Configuration register 10 for SD10G65 IB.

Table 590 • **SD10G65 IB Configuration 10**

Bit	Name	Access	Description	Default
31	IB_IA_DOFFS_CAL	R/O	Data offset calibration result IA stage	0x0
30	IB_IS_DOFFS_CAL	R/O	Data offset calibration result IS stage	0x0
29	IB_IE_SDET_PEDGE	R/O	Detection of toggling signal at PADP and PADN	0x0

Table 590 • **SD10G65 IB Configuration 10** ***(continued)***

Bit	Name	Access	Description	Default
28	IB_IE_SDET_NEDGE	R/O	Detection of toggling signal at PADP and PADN	0x0
27	IB_IE_SDET	R/O	Result signal detect of IE stage	0x0
26	IB_IA_SDET	R/O	Result signal detect of IA stage	0x0
25	IB_EQZ_LD1_PEDGE	R/O	Result of Level-Detect1 (after ES2-stage of EQZ) circuitry 1: Input level above threshold defined by IB_EQ_LD_LEV	0x0
24	IB_EQZ_LD1_NEDGE	R/O	Result of Level-Detect1 (after ES2-stage of EQZ) circuitry 1: Input level above threshold defined by IB_EQ_LD_LEV	0x0
23	IB_EQZ_LD0_PEDGE	R/O	Result of Level-Detect0 (after IB-stage of EQZ) circuitry 1: Input level above threshold defined by IB_EQ_LD_LEV	0x0
22	IB_EQZ_LD0_NEDGE	R/O	Result of Level-Detect0 (after IB-stage of EQZ) circuitry 1: Input level above threshold defined by IB_EQ_LD_LEV	0x0
21	IB_IE_DIRECT_DATA	R/O	Direct Data output from IE block	0x0
20	IB_IA_DIRECT_DATA	R/O	Direct Data output from IA block	0x0
17	IB_LOOP_REC	R/W	Receive enable for BiDi loop (a.k.a. PAD loop o. Tx->Rx loop). Is or'ed with primary input: ib_pad_loop_ena_i. Disable test generator 'ib_tstgen_ena' if input loop is used	0x0
16	IB_LOOP_DRV	R/W	Drive enable for BiDi loop (a.k.a. Input loop o. Rx->Tx loop). Is or'ed with primary input: ib_inp_loop_ena_i. Is overruled by PAD loop.	0x0
10	IB_JTAG_OUT_P	R/O	JTAG debug p-output	0x0
9	IB_JTAG_OUT_N	R/O	JTAG debug n-output	0x0
8:4	IB_JTAG_THRES	R/W	JTAG debug threshold 0: 0mV 1: 10mV 31: 310mV	0x08
3	IB_JTAG_IN_P	R/W	JTAG debug p-input	0x0
2	IB_JTAG_IN_N	R/W	JTAG debug n-input	0x0
1	IB_JTAG_CLK	R/W	JTAG debug clk	0x0
0	IB_JTAG_ENA	R/W	JTAG debug enable	0x0

2.8.4.12 SD10G65 IB Configuration 11

Short Name:SD10G65_IB_CFG11

Address:0x9F12B

Configuration register 11 for SD10G65 IB.

Table 591 • **SD10G65 IB Configuration 11 JTAG Related Setting**

Bit	Name	Access	Description	Default
15:12	IB_DFE_ISEL	R/W	DFE Bias current settings (bit-group is gated with IB_DFE_ENA) 0: DFE disabled 1: Minimum current 15: Maximum current	0x7
11	IB_ENA_400_INP	R/W	Increase current in first stage (only available in 1.2 Volt mode)	0x0
10:6	IB_TC_DFE	R/W	Gain temperature coefficient for DFE stage	0x0C
5:1	IB_TC_EQ	R/W	Gain temperature coefficient for AGC stage	0x0C

2.8.4.13 SD10G65 SBUS Rx CFG Service-Bus Related Setting

Short Name:SD10G65_SBUS_RX_CFG

Address:0x9F12C

Configuration register for Service-Bus related setting. Note: SBUS configuration applies for Rx/Tx aggregates only, any configuration applied to SBUS_TX_CFG (output buffer cfg space) will be ignored.

Table 592 • **SD10G65 SBUS Rx CFG Service-Bus Related Setting**

Bit	Name	Access	Description	Default
12	SBUS_LOOPDRV_ENA	R/W	Enable BiDi loop driver for F2DF testing	0x0
11:8	SBUS_ANAOUT_SEL	R/W	Analog test output 0: l0_ctrlspeed[0] 1: vbulk 2: nref 3: vref820m 4: vddfilt 5: vddfilt 6: ie_aout 7: ib_aout 8: ob_aout2 9: pll_frange 10: pll_srange 11: pll_vreg820m_tx 12: pll_vreg820m_rx 13: ob_aout_n 14: ob_aout_p 15: vddfilt	0x0
7	SBUS_ANAOUT_EN	R/W	Enable analog test output multiplexer	0x0
6:3	SBUS_RCOMP	R/W	Offset value for BIAS resistor calibration (2-complement) 1000: -8 1111: -1 0000: 0 0111: 7	0x0

Table 592 • **SD10G65 SBUS Rx CFG Service-Bus Related Setting *(continued)***

Bit	Name	Access	Description	Default
2:1	SBUS_BIAS_SPEED_SEL	R/W	Bias speed selection 0: Below 4Gbps 1: 4Gbps to 6Gbps 2: 6Gbps to 9Gbps 3: Above 9Gbps	0x3
0	SBUS_BIAS_EN	R/W	Bias enable 1: Enable 0: Disable	0x0

2.8.5 SD10G65 Rx RCPLL Configuration and Status

Configuration and status register set for SD10G65 Rx RCPLL

2.8.5.1 SD10G65 Rx RCPLL Configuration 0

Short Name:SD10G65_RX_RCPLL_CFG0

Address:0x9F130

Configuration register 0 for SD10G65 Rx RCPLL.

Table 593 • **SD10G65 Rx RCPLL Configuration 0**

Bit	Name	Access	Description	Default
25:16	PLLF_START_CNT	R/W	Preload value of the ramp up counter, reduces ramp up time for higher frequencies	0x002
9:7	PLLF_RAMP_MODE_SEL	R/W	Sets the ramp characteristic of the FSM, higher values give faster ramp up but less accuracy, 0: normal (default) ramping 1: faster ramping 2: fastest ramping 3: slow ramping uses all possible values of r_ctrl	0x0
5	RESERVED	R/W	Must be set to its default.	0x1
4	RESERVED	R/W	Must be set to its default.	0x1
0	PLLF_ENA	R/W	Enable RCPLL FSM	0x0

2.8.5.2 SD10G65 Rx RCPLL Configuration 1

Short Name:SD10G65_RX_RCPLL_CFG1

Address:0x9F131

Configuration register 1 for SD10G65 Rx RCPLL.

Table 594 • **SD10G65 Rx RCPLL Configuration 1**

Bit	Name	Access	Description	Default
31:16	PLLF_REF_CNT_END	R/W	Target value: 1/vco_frq * par.bit.width * 512 * ref_clk_frq	0x00C6
13:4	RESERVED	R/W	Must be set to its default.	0x002
1:0	RESERVED	R/W	Must be set to its default.	0x1

2.8.5.3 SD10G65 Rx RCPLL Configuration 2

Short Name:SD10G65_RX_RCPLL_CFG2

Address:0x9F132

Configuration register 2 for SD10G65 Rx RCPLL.

Table 595 • **SD10G65 Rx RCPLL Configuration 2**

Bit	Name	Access	Description	Default
23:20	RESERVED	R/W	Must be set to its default.	0x3
16	RESERVED	R/W	Must be set to its default.	0x1
15	RESERVED	R/W	Must be set to its default.	0x1
14	RESERVED	R/W	Must be set to its default.	0x1
13	RESERVED	R/W	Must be set to its default.	0x1
12:11	PLL_LPF_CUR	R/W	Select charge pump current, 0: 50uA 1: 100uA 2: 150uA 3: 200uA	0x3
10:7	PLL_LPF_RES	R/W	Select loop filter resistor value, 0: not allowed 1: 2400 2: 1600 3: 960 4: 1200 5: 800 6: 685 7: 533 8: 800 9: 600 10: 533 11: 436 12: 480 13: 400 14: 369 15: 320	0xA
6:2	RESERVED	R/W	Must be set to its default.	0x1F
0	PLL_ENA	R/W	Enable analog RCPLL part	0x0

2.8.5.4 SD10G65 Rx RCPLL Status 0

Short Name:SD10G65_RX_RCPLL_STAT0

Address:0x9F133

Status register 0 for SD10G65 Rx RCPLL.

Table 596 • **SD10G65 Rx RCPLL Status 0**

Bit	Name	Access	Description	Default
31	PLLF_LOCK_STAT	R/O	PLL lock status, 0: not locked 1: locked	0x0

2.8.6 SD10G65 Rx SYNTH Configuration and Status

Configuration and status register set for SD10G65 Rx SYNTH

2.8.6.1 SD10G65 Rx Synthesizer Configuration 0

Short Name:SD10G65_RX_SYNTH_CFG0

Address:0x9F140

Configuration register 0 for SD10G65 Rx SYNTH.

Table 597 • **SD10G65 Rx Synthesizer Configuration 0**

Bit	Name	Access	Description	Default
21:18	RESERVED	R/W	Must be set to its default.	0xF
17:16	SYNTH_FBDIV_SEL	R/W	selects feedback divider setting. 0: divide by 1 1: divide by 2 2: divide by 4 3: reserved	0x1
15:14	SYNTH_FB_STEP	R/W	selects step width for sync output	0x0
12:11	SYNTH_I2_STEP	R/W	selects step width for integrator2	0x0
9	SYNTH_I2_ENA	R/W	enable contribution of integral2 part	0x1
8	SYNTH_I1_STEP	R/W	selects step width for integrator1	0x0
6	SYNTH_P_STEP	R/W	selects step width for proportional	0x0
4	SYNTH_SPEED_SEL	R/W	Selects circuit speed. 0: for settings with synth_fbdiv_sel = 2 1: for setting with synth_fbdiv_sel less than 2	0x1
3	SYNTH_HRATE_ENA	R/W	enables half rate mode	0x0
1	RESERVED	R/W	Must be set to its default.	0x1
0	SYNTH_ENA	R/W	synthesizer enable	0x0

2.8.6.2 SD10G65 Rx Synthesizer Configuration 1

Short Name:SD10G65_RX_SYNTH_CFG1

Address:0x9F141

Configuration register 1 for SD10G65 Rx SYNTH.

Table 598 • **SD10G65 Rx Synthesizer Configuration 1**

Bit	Name	Access	Description	Default
25:22	RESERVED	R/W	Must be set to its default.	0x4
21:8	SYNTH_FREQ_MULT	R/W	frequency multiplier	0x2100
7:4	SYNTH_FREQM_1	R/W	frequency m setting bits 35:32	0x0
3:0	SYNTH_FREQN_1	R/W	frequency n setting bits 35:32	0x8

2.8.6.3 SD10G65 Rx Synthesizer Configuration 2

Short Name:SD10G65_RX_SYNTH_CFG2

Address:0x9F142

Configuration register 2 for SD10G65 Rx SYNTH.

Table 599 • **SD10G65 Rx Synthesizer Configuration 2**

Bit	Name	Access	Description	Default
31	SYNTH_SKIP_BIT_FWD	R/W	Rising edge triggers bit skip forward in serial data stream. Used to align data to parallel interface boundaries.	0x0
30	SYNTH_SKIP_BIT_REV	R/W	Rising edge triggers bit skip reverse in serial data stream. Used to align data to parallel interface boundaries.	0x0
27:26	SYNTH_DV_CTRL_I2E	R/W	Controls the data valid behavior for the CDRLF I2 enable function: b0 = 0 => external signal controls, 1 => b1 controls	0x0
25:24	SYNTH_DV_CTRL_I1M	R/W	Controls the data valid behavior for the CDRLF I1 max function: b0 = 0 => external signal controls, 1 => b1 controls	0x0
23:22	SYNTH_DV_CTRL_I1E	R/W	Controls the data valid behavior for the CDRLF I1 enable function: b0 = 0 => external signal controls, 1 => b1 controls	0x0
21:20	SYNTH_DV_CTRL_MD	R/W	Controls the data valid behavior for the moebdiv select function: b0 = 0 => external signal controls, 1 => b1 controls	0x0
18	SYNTH_CPMD_DIG_SEL	R/W	Cp/md dig select. Coding 0: select Bit 0/5 as cp/md (FX100 mode); 1: use cp/md from core	0x0
17	SYNTH_CPMD_DIG_ENA	R/W	uses cp/md selected via synth_cpmd_dig_sel instead of cp/md from sample stage	0x0
16	SYNTH_AUX_ENA	R/W	enables clock for VScope / APC auxiliary data channels	0x1
14:8	SYNTH_PHASE_DATA	R/W	relationship phase center/edge	0x08
6:0	SYNTH_PHASE_AUX	R/W	relationship phase center/aux	0x08

2.8.6.4 SD10G65 Rx Synthesizer Configuration 3

Short Name:SD10G65_RX_SYNTH_CFG3

Address:0x9F143

Configuration register 3 for SD10G65 Rx SYNTH.

Table 600 • **SD10G65 Rx Synthesizer Configuration 3**

Bit	Name	Access	Description	Default
31:0	SYNTH_FREQM_0	R/W	frequency m setting bits 31:0	0x00000000

2.8.6.5 SD10G65 Rx Synthesizer Configuration 4

Short Name:SD10G65_RX_SYNTH_CFG4

Address:0x9F144

Configuration register 4 for SD10G65 Rx SYNTH.

Table 601 • **SD10G65 Rx Synthesizer Configuration 4**

Bit	Name	Access	Description	Default
31:0	SYNTH_FREQN_0	R/W	frequency n setting bits 31:0	0x00000000

2.8.6.6 SD10G65 Rx Synthesizer CDR loopfilter control

Short Name:SD10G65_RX_SYNTH_CDRLF

Address:0x9F145

Register for CDR loopfilter control for SD10G65 Rx SYNTH.

Table 602 • **SD10G65 Rx Synthesizer CDR loopfilter control**

Bit	Name	Access	Description	Default
31	SYNTH_INTEG3_ENA	R/W	Enables integrator 3	0x0
30:26	SYNTH_INTEG3_DSEL	R/W	Select filter damping / gain peaking when integrator 3 is enabled. The control value is interpreted as signed value. Positive values increase the damping, i.e. lowering the gain peaking; negative values decease the damping, i.e. raising the gain peaking. The allowed programming range depends on the SYNTH_INTEG2_FSEL setting: 0 <= (SYNTH_INTEG2_FSEL - SYNTH_INTEG3_DSEL) <= 53. SYNTH_INTEG2_FSEL - SYNTH_INTEG3_DSEL = 0 and SYNTH_INTEG2_FSEL - SYNTH_INTEG3_DSEL = 1 gives the same damping.	0x00
25:21	SYNTH_INTEG1_MAX1	R/W	max value of integrator 1 during normal operation	0x02
20:16	SYNTH_INTEG1_MAX0	R/W	max value of integrator 1 during init phase	0x00
15:11	SYNTH_INTEG1_LIM	R/W	limit of integrator 1	0x02
10:6	SYNTH_INTEG1_FSEL	R/W	frequency select of integrator 1	0x02
5:0	SYNTH_INTEG2_FSEL	R/W	frequency select of integrator 2	0x31

2.8.6.7 SD10G65 Rx Synthesizer 0 for Qualifier Access

Short Name:SD10G65_RX_SYNTH_QUALIFIER0

Address:0x9F146

Register 0 for qualifier access for SD10G65 Rx SYNTH.

Table 603 • **SD10G65 Rx Synthesizer 0 for Qualifier Access**

Bit	Name	Access	Description	Default
20	SYNTH_CAPTURE_QUAL	R/W	Rising edge captures qualifier for readback	0x0
19:16	SYNTH_QUAL_I2_MSB	R/O	MS Bits of captured integrator 2	0x0
15:0	SYNTH_QUAL_I1	R/O	Captured integrator 1 value	0x0000

2.8.6.8 SD10G65 Rx Synthesizer 1 for Qualifier Access

Short Name:SD10G65_RX_SYNTH_QUALIFIER1

Address:0x9F147

Register 1 for qualifier access for SD10G65 Rx SYNTH.

Table 604 • **SD10G65 Rx Synthesizer 1 for Qualifier Access**

Bit	Name	Access	Description	Default
31:0	SYNTH_QUAL_I2_LSB	R/O	LS Bits of captured integrator 2	0x00000000

2.8.6.9 SD10G65 Rx Synthesizer for Sync Control Data

Short Name:SD10G65_RX_SYNTH_SYNC_CTRL

Address:0x9F148

Register 0 for sync control data for SD10G65 Rx SYNTH.

Table 605 • **SD10G65 Rx Synthesizer for Sync Control Data**

Bit	Name	Access	Description	Default
3:0	SYNTH_SC_SYNC_TIMER_SEL	R/W	Selects the synchronization period for the I2 value via sync control bus. Must be disabled (0) when sync control test generator is used. Coding in 312.5MHz clock cycles: 0: disabled, 1: 2^6, 2: 2^7, .., 15: 2^20.	0xF

2.8.6.10 F2DF Configuration / Status

Short Name:F2DF_CFG_STAT

Address:0x9F149

Configuration / status register for the F2DF control logic.

Table 606 • **F2DF Configuration / Status**

Bit	Name	Access	Description	Default
27:25	F2DF_SAMPLE_DIV	R/W	Sampling divider: sample every 2^f2df_sample_div parallel data word.	0x0
21:17	F2DF_SIDE_DET_BIT_SEL	R/W	Select bit from input data used for side detection. Debug feature: '31' select constant zero, '30' select constant one.	0x00
16:14	F2DF_SIDE_DET_ONES_WEIGHT	R/W	Sample '1' => increment 8bit filter saturating counter by 2**n. Cnt >= 0xC0 => ProperSide detected.	0x0
13:11	F2DF_SIDE_DET_ZEROS_WEIGHT	R/W	Sample '0' => decrement 8bit filter saturating counter by 2**n. Cnt < 0x40 => WrongSide detected.	0x0
9:4	F2DF_TOG_DET_CNT	R/W	Determines the number of samples that have to show at least one toggle.	0x00
3	F2DF_DATA_VALID_PROPPER_SIDE	R/W	Data valid value in "ProperSide" state. '0': data valid flagged only in "Lock" state; '1' data valid also flagged in "ProperSide" state.	0x0

Table 606 • **F2DF Configuration / Status**

Bit	Name	Access	Description	Default
0	F2DF_ENABLE	R/W	F2df enable. Enabling the f2df circuit automatically switches the input of the CDR-loop to the f2df control block (overrules synth_cpmd_dig_sel and synth_cpmd_dig_ena) and replaces the data valid signal from the core logic by the data valid signal generated by the f2df control logic.	0x0

2.8.7 SD10G65 Tx SYNTH Configuration and Status

Configuration and status register set for SD10G65 Tx SYNTH

2.8.7.1 SD10G65 Tx Synthesizer Configuration 0

Short Name:SD10G65_TX_SYNTH_CFG0

Address:0x9F150

Configuration register 0 for SD10G65 Tx SYNTH.

Table 607 • **SD10G65 Tx Synthesizer Configuration 0**

Bit	Name	Access	Description	Default
25:23	RESERVED	R/W	Must be set to its default.	0x3
22:18	RESERVED	R/W	Must be set to its default.	0x17
17:16	SYNTH_FBDIV_SEL	R/W	selects feedback divider setting	0x2
13:11	SYNTH_CS_SPEED	R/W	common sync speed	0x0
10	SYNTH_LS_SPEED	R/W	lane sync speed	0x0
8	SYNTH_LS_ENA	R/W	lane sync enable	0x1
7	SYNTH_DS_SPEED	R/W	dig. sync speed	0x0
5	SYNTH_DS_ENA	R/W	dig. sync enable	0x0
4	SYNTH_SPEED_SEL	R/W	Selects circuit speed. Coding: 0 for settings with synth_fbdiv_sel = 2; 1 for setting with synth_fbdiv_sel smaller than 2.	0x0
3	SYNTH_HRATE_ENA	R/W	half rate enable	0x0
2	RESERVED	R/W	Must be set to its default.	0x1
1	RESERVED	R/W	Must be set to its default.	0x1
0	SYNTH_ENA	R/W	synthesizer enable	0x0

2.8.7.2 SD10G65 Tx Synthesizer Configuration 1

Short Name:SD10G65_TX_SYNTH_CFG1

Address:0x9F151

Configuration register 1 for SD10G65 Tx SYNTH.

Table 608 • **SD10G65 Tx Synthesizer Configuration 1**

Bit	Name	Access	Description	Default
25:22	RESERVED	R/W	Must be set to its default.	0x4
21:8	SYNTH_FREQ_MULT	R/W	frequency multiplier	0x2100

Table 608 • **SD10G65 Tx Synthesizer Configuration 1 *(continued)***

Bit	Name	Access	Description	Default
7:4	SYNTH_FREQM_1	R/W	frequency m setting bits 35:32	0x0
3:0	SYNTH_FREQN_1	R/W	frequency n setting bits 35:32	0x8

2.8.7.3 SD10G65 Tx Synthesizer Configuration 3

Short Name:SD10G65_TX_SYNTH_CFG3

Address:0x9F152

Configuration register 3 for SD10G65 Tx SYNTH.

Table 609 • **SD10G65 Tx Synthesizer Configuration 3**

Bit	Name	Access	Description	Default
31:0	SYNTH_FREQM_0	R/W	frequency m setting bits 31:0	0x00000000

2.8.7.4 SD10G65 Tx Synthesizer Configuration 4

Short Name:SD10G65_TX_SYNTH_CFG4

Address:0x9F153

Configuration register 4 for SD10G65 Tx SYNTH.

Table 610 • **SD10G65 Tx Synthesizer Configuration 4**

Bit	Name	Access	Description	Default
31:0	SYNTH_FREQN_0	R/W	frequency n setting bits 31:0	0x00000000

2.8.7.5 SD10G65 SSC generator Configuration 0

Short Name:SD10G65_SSC_CFG0

Address:0x9F154

Configuration register 0 for SD10G65 SSC generator.

Table 611 • **SD10G65 SSC Generator Configuration 0**

Bit	Name	Access	Description	Default
31:19	SSC_MOD_LIM	R/W	SSC modulation amplitude limiter	0x0000
18:7	SSC_MOD_PERIOD	R/W	SSC modulation period / amplitude.	0x000
6:1	SSC_MOD_FREQ	R/W	SSC modulation frequency fine tuning control	0x00
0	SSC_ENA	R/W	SSC generator enable.	0x0

2.8.7.6 SD10G65 SSC Generator Configuration 1

Short Name:SD10G65_SSC_CFG1

Address:0x9F155

Configuration register 1 for SD10G65 SSC generator.

Table 612 • **SD10G65 SSC Generator Configuration 1**

Bit	Name	Access	Description	Default
29	MLD_SYNC_SRC_SEL	R/W	Select between the internal and external MLD phase detector: 0: internal 1: external	0x0
28:25	MLD_SYNC_CTRL	R/W	Control of the internal MLD phase detector: b0: enable; b1: enable hyst. b2: enable window function; b3: select window size	0x0
24:23	MLD_SYNC_CLK_SEL	R/W	Select the MLD clock source for the internal MLD phase detector	0x0
22	SYNC_CTRL_WRAP_INHIBIT	R/W	Controls integrator 2 replica behavior: '0': wrapping; '1': saturating.	0x0
21:16	SYNC_CTRL_FSEL	R/W	Frequency select of integrator 2 replica used for lane sync.	0x31
10	SMOOTH_ENA	R/W	Enables Smooth generator	0x0
9:5	SSC_SD_GAIN	R/W	SSC sigma delta gain.	0x00
4:3	SSC_SYNC_POS	R/W	SSC modulation start position on synchronization trigger	0x0
2:0	SSC_MOD_MUL	R/W	SSC modulation period multiplier encoded 2**n: 0 => 1; 1 => 2; 2 => 4, 3 => 8 ...	0x0

2.8.8 SD10G65 Tx RCPLL Configuration and Status

Configuration and status register set for SD10G65 Tx RCPLL

2.8.8.1 SD10G65 Tx RCPLL Configuration 0

Short Name:SD10G65_TX_RCPLL_CFG0

Address:0x9F160

Configuration register 0 for SD10G65 Tx RCPLL.

Table 613 • **SD10G65 Tx RCPLL Configuration 0**

Bit	Name	Access	Description	Default
25:16	PLLF_START_CNT	R/W	Preload value of the ramp up counter, reduces ramp up time for higher frequencies	0x002
9:7	PLLF_RAMP_MODE_SEL	R/W	Sets the ramp characteristic of the FSM, higher values give faster ramp up but less accuracy, 0: normal (default) ramping 1: faster ramping 2: fastest ramping 3: slow ramping uses all possible values of r_ctrl	0x0
5	RESERVED	R/W	Must be set to its default.	0x1
4	RESERVED	R/W	Must be set to its default.	0x1
0	PLLF_ENA	R/W	Enable RCPLL FSM	0x0

2.8.8.2 SD10G65 Tx RCPLL Configuration 1

Short Name:SD10G65_TX_RCPLL_CFG1

Address:0x9F161

Configuration register 1 for SD10G65 Tx RCPLL.

Table 614 • **SD10G65 Tx RCPLL Configuration 1**

Bit	Name	Access	Description	Default
31:16	PLLF_REF_CNT_END	R/W	Target value: 1/vco_frq * par.bit.width * 512 * ref_clk_frq	0x00C6
13:4	RESERVED	R/W	Must be set to its default.	0x002
1:0	RESERVED	R/W	Must be set to its default.	0x1

2.8.8.3 SD10G65 Tx RCPLL Configuration 2

Short Name:SD10G65_TX_RCPLL_CFG2

Address:0x9F162

Configuration register 2 for SD10G65 Tx RCPLL.

Table 615 • **SD10G65 Tx RCPLL Configuration 2**

Bit	Name	Access	Description	Default
23:20	RESERVED	R/W	Must be set to its default.	0x3
16	RESERVED	R/W	Must be set to its default.	0x1
15	RESERVED	R/W	Must be set to its default.	0x1
14	RESERVED	R/W	Must be set to its default.	0x1
13	RESERVED	R/W	Must be set to its default.	0x1
12:11	PLL_LPF_CUR	R/W	Select charge pump current, 0: 50uA 1: 100uA 2: 150uA 3: 200uA	0x3
10:7	PLL_LPF_RES	R/W	Select loop filter resistor value, 0: not allowed 1: 2400 2: 1600 3: 960 4: 1200 5: 800 6: 685 7: 533 8: 800 9: 600 10: 533 11: 436 12: 480 13: 400 14: 369 15: 320	0xA
6:2	RESERVED	R/W	Must be set to its default.	0x1F
0	PLL_ENA	R/W	Enable analog RCPLL part	0x0

2.8.8.4 SD10G65 Tx RCPLL Status 0

Short Name:SD10G65_TX_RCPLL_STAT0

Address:0x9F163

Status register 0 for SD10G65 Tx RCPLL.

Table 616 • **SD10G65 Tx RCPLL Status 0**

Bit	Name	Access	Description	Default
31	PLLF_LOCK_STAT	R/O	PLL lock status, 0: not locked 1: locked	0x0

2.9 WIS (Device 0x2)

Table 617 • **WIS_Control_1**

Address	Short Description	Register Name	Details
0x20000	WIS Control 1	WIS_CTRL1	Page 262

Table 618 • **WIS_Status_1**

Address	Short Description	Register Name	Details
0x20001	WIS Status 1	WIS_STAT1	Page 263

Table 619 • **WIS_Device_Identifier**

Address	Short Description	Register Name	Details
0x20002	WIS Device Identifier 1	WIS_DEVID1	Page 263
0x20003	WIS Device Identifier 2	WIS_DEVID2	Page 263

Table 620 • **WIS_Speed_Capability**

Address	Short Description	Register Name	Details
0x20004	WIS Speed Capability	WIS_SPEED	Page 264

Table 621 • **WIS_Devices_in_Package**

Address	Short Description	Register Name	Details
0x20005	WIS Devices in Package 1	WIS_DEVPKG1	Page 264
0x20006	WIS Devices in Package 2	WIS_DEVPKG2	Page 264

Table 622 • **WIS_Control_2**

Address	Short Description	Register Name	Details
0x20007	WIS Control 2	WIS_CTRL2	Page 265

Table 623 • **WIS_Status_2**

Address	Short Description	Register Name	Details
0x20008	WIS Status 2	WIS_STAT2	Page 265

Table 624 • **WIS_Test_Pattern_Error_Counter**

Address	Short Description	Register Name	Details
0x20009	WIS Test Pattern Error Counter	WIS_TSTPAT_CNT	Page 266

Table 625 • **WIS_Package_Identifier**

Address	Short Description	Register Name	Details
0x2000E	WIS Package Identifier 1	WIS_PKGID1	Page 266
0x2000F	WIS Package Identifier 2	WIS_PKGID2	Page 266

Table 626 • **WIS_Status_3**

Address	Short Description	Register Name	Details
0x20021	WIS Status 3	WIS_STAT3	Page 267

Table 627 • **WIS_Far_End_Path_Block_Error_Count**

Address	Short Description	Register Name	Details
0x20025	WIS Far-End Path Block Error Count	WIS_REIP_CNT	Page 268

Table 628 • **WIS_Tx_J1_Octets_0_15**

Address	Short Description	Register Name	Details
0x20027	WIS Tx J1 Octets 1-0	WIS_Tx_J1_Octets_1_0	Page 268
0x20028	WIS Tx J1 Octets 3-2	WIS_Tx_J1_Octets_3_2	Page 269
0x20029	WIS Tx J1 Octets 5-4	WIS_Tx_J1_Octets_5_4	Page 269
0x2002A	WIS Tx J1 Octets 7-6	WIS_Tx_J1_Octets_7_6	Page 269
0x2002B	WIS Tx J1 Octets 9-8	WIS_Tx_J1_Octets_9_8	Page 269
0x2002C	WIS Tx J1 Octets 11-10	WIS_Tx_J1_Octets_11_10	Page 269
0x2002D	WIS Tx J1 Octets 13-12	WIS_Tx_J1_Octets_13_12	Page 270
0x2002E	WIS Tx J1 Octets 15-14	WIS_Tx_J1_Octets_15_14	Page 270

Table 629 • **WIS_Rx_J1_Octets_0_15**

Address	Short Description	Register Name	Details
0x2002F	WIS Rx J1 Octets 1-0	WIS_Rx_J1_Octets_1_0	Page 270
0x20030	WIS Rx J1 Octets 3-2	WIS_Rx_J1_Octets_3_2	Page 271
0x20031	WIS Rx J1 Octets 5-4	WIS_Rx_J1_Octets_5_4	Page 271
0x20032	WIS Rx J1 Octets 7-6	WIS_Rx_J1_Octets_7_6	Page 271
0x20033	WIS Rx J1 Octets 9-8	WIS_Rx_J1_Octets_9_8	Page 271
0x20034	WIS Rx J1 Octets 11-10	WIS_Rx_J1_Octets_11_10	Page 272
0x20035	WIS Rx J1 Octets 13-12	WIS_Rx_J1_Octets_13_12	Page 272
0x20036	WIS Rx J1 Octets 15-14	WIS_Rx_J1_Octets_15_14	Page 272

Table 630 • **WIS_IEEE_Error_Counters**

Address	Short Description	Register Name	Details
0x20037	WIS Far-End Line BIP Errors 1	WIS_REIL_CNT1	Page 272
0x20038	WIS Far-End Line BIP Errors 0	WIS_REIL_CNT0	Page 273
0x20039	WIS L-BIP Error Count 1	WIS_B2_CNT1	Page 273
0x2003A	WIS L-BIP Error Count 0	WIS_B2_CNT0	Page 274
0x2003B	WIS P-BIP Block Error Count	WIS_B3_CNT	Page 274
0x2003C	WIS S-BIP Error Count	WIS_B1_CNT	Page 274

Table 631 • **WIS_Tx_J0_Octets_0_15**

Address	Short Description	Register Name	Details
0x20040	WIS Tx J0 Octets 1-0	WIS_Tx_J0_Octets_1_0	Page 275
0x20041	WIS Tx J0 Octets 3-2	WIS_Tx_J0_Octets_3_2	Page 275
0x20042	WIS Tx J0 Octets 5-4	WIS_Tx_J0_Octets_5_4	Page 275
0x20043	WIS Tx J0 Octets 7-6	WIS_Tx_J0_Octets_7_6	Page 276
0x20044	WIS Tx J0 Octets 9-8	WIS_Tx_J0_Octets_9_8	Page 276
0x20045	WIS Tx J0 Octets 11-10	WIS_Tx_J0_Octets_11_10	Page 276
0x20046	WIS Tx J0 Octets 13-12	WIS_Tx_J0_Octets_13_12	Page 276
0x20047	WIS Tx J0 Octets 15-14	WIS_Tx_J0_Octets_15_14	Page 277

Table 632 • **WIS_Rx_J0_Octets_0_15**

Address	Short Description	Register Name	Details
0x20048	WIS Rx J0 Octets 1-0	WIS_Rx_J0_Octets_1_0	Page 277
0x20049	WIS Rx J0 Octets 3-2	WIS_Rx_J0_Octets_3_2	Page 277
0x2004A	WIS Rx J0 Octets 5-4	WIS_Rx_J0_Octets_5_4	Page 277
0x2004B	WIS Rx J0 Octets 7-6	WIS_Rx_J0_Octets_7_6	Page 278
0x2004C	WIS Rx J0 Octets 9-8	WIS_Rx_J0_Octets_9_8	Page 278

Table 632 • **WIS_Rx_J0_Octets_0_15 *(continued)***

Address	Short Description	Register Name	Details
0x2004D	WIS Rx J0 Octets 11-10	WIS_Rx_J0_Octets_11_10	Page 278
0x2004E	WIS Rx J0 Octets 13-12	WIS_Rx_J0_Octets_13_12	Page 278
0x2004F	WIS Rx J0 Octets 15-14	WIS_Rx_J0_Octets_15_14	Page 279

Table 633 • **WIS_Tx_Control**

Address	Short Description	Register Name	Details
0x2E5FF	WIS Tx Control 1	EWIS_TXCTRL1	Page 279
0x2E600	WIS Tx Control 2	EWIS_TXCTRL2	Page 279

Table 634 • **LOOP_H4_FIFO_STAT**

Address	Short Description	Register Name	Details
0x2E606	LOOP_H4_FIFO_STAT	LOOP_H4_FIFO_STAT	Page 280

Table 635 • **EWIS_Tx_Overhead_Octets**

Address	Short Description	Register Name	Details
0x2E611	E-WIS Tx A1/A2 Octets	EWIS_TX_A1_A2	Page 281
0x2E612	E-WIS Tx Z0/E1 Octets	EWIS_TX_Z0_E1	Page 281
0x2E613	E-WIS Tx F1/D1 Octets	EWIS_TX_F1_D1	Page 281
0x2E614	E-WIS Tx D2/D3 Octets	EWIS_TX_D2_D3	Page 282
0x2E615	E-WIS Tx C2/H1 Octets	EWIS_TX_C2_H1	Page 282
0x2E616	E-WIS Tx H2/H3 Octets	EWIS_TX_H2_H3	Page 282
0x2E617	E-WIS Tx G1/K1 Octets	EWIS_TX_G1_K1	Page 282
0x2E618	E-WIS Tx K2/F2 Octets	EWIS_TX_K2_F2	Page 282
0x2E619	E-WIS Tx D4/D5 Octets	EWIS_TX_D4_D5	Page 283
0x2E61A	E-WIS Tx D6/H4 Octets	EWIS_TX_D6_H4	Page 283
0x2E61B	E-WIS Tx D7/D8 Octets	EWIS_TX_D7_D8	Page 283
0x2E61C	E-WIS Tx D9/Z3 Octets	EWIS_TX_D9_Z3	Page 283
0x2E61D	E-WIS Tx D10/D11 Octets	EWIS_TX_D10_D11	Page 284
0x2E61E	E-WIS Tx D12/Z4 Octets	EWIS_TX_D12_Z4	Page 284
0x2E61F	E-WIS Tx S1/Z1 Octets	EWIS_TX_S1_Z1	Page 284
0x2E620	E-WIS Tx Z2/E2 Octets	EWIS_TX_Z2_E2	Page 284
0x2E621	E-WIS Tx N1 Octet	EWIS_TX_N1	Page 285

Table 636 • **EWIS_Tx_Trace_Message_Length_Control**

Address	Short Description	Register Name	Details
0x2E700	E-WIS Tx Trace Message Length Control	EWIS_TX_MSGLEN	Page 285

Table 637 • **EWIS_Tx_J0_Octets_16_63**

Address	Short Description	Register Name	Details
0x2E800	E-WIS Tx J0 Octets 17-16	EWIS_Tx_J0_Octets_17_16	Page 285
0x2E801	E-WIS Tx J0 Octets 19-18	EWIS_Tx_J0_Octets_19_18	Page 286
0x2E802	E-WIS Tx J0 Octets 21-20	EWIS_Tx_J0_Octets_21_20	Page 286
0x2E803	E-WIS Tx J0 Octets 23-22	EWIS_Tx_J0_Octets_23_22	Page 286
0x2E804	E-WIS Tx J0 Octets 25-24	EWIS_Tx_J0_Octets_25_24	Page 286
0x2E805	E-WIS Tx J0 Octets 27-26	EWIS_Tx_J0_Octets_27_26	Page 287
0x2E806	E-WIS Tx J0 Octets 29-28	EWIS_Tx_J0_Octets_29_28	Page 287
0x2E807	E-WIS Tx J0 Octets 31-30	EWIS_Tx_J0_Octets_31_30	Page 287
0x2E808	E-WIS Tx J0 Octets 33-32	EWIS_Tx_J0_Octets_33_32	Page 287
0x2E809	E-WIS Tx J0 Octets 35-34	EWIS_Tx_J0_Octets_35_34	Page 288
0x2E80A	E-WIS Tx J0 Octets 37-36	EWIS_Tx_J0_Octets_37_36	Page 288
0x2E80B	E-WIS Tx J0 Octets 39-38	EWIS_Tx_J0_Octets_39_38	Page 288
0x2E80C	E-WIS Tx J0 Octets 41-40	EWIS_Tx_J0_Octets_41_40	Page 288
0x2E80D	E-WIS Tx J0 Octets 43-42	EWIS_Tx_J0_Octets_43_42	Page 289
0x2E80E	E-WIS Tx J0 Octets 45-44	EWIS_Tx_J0_Octets_45_44	Page 289
0x2E80F	E-WIS Tx J0 Octets 47-46	EWIS_Tx_J0_Octets_47_46	Page 289
0x2E810	E-WIS Tx J0 Octets 49-48	EWIS_Tx_J0_Octets_49_48	Page 289
0x2E811	E-WIS Tx J0 Octets 51-50	EWIS_Tx_J0_Octets_51_50	Page 290
0x2E812	E-WIS Tx J0 Octets 53-52	EWIS_Tx_J0_Octets_53_52	Page 290
0x2E813	E-WIS Tx J0 Octets 55-54	EWIS_Tx_J0_Octets_55_54	Page 290
0x2E814	E-WIS Tx J0 Octets 57-56	EWIS_Tx_J0_Octets_57_56	Page 290
0x2E815	E-WIS Tx J0 Octets 59-58	EWIS_Tx_J0_Octets_59_58	Page 291
0x2E816	E-WIS Tx J0 Octets 61-60	EWIS_Tx_J0_Octets_61_60	Page 291
0x2E817	E-WIS Tx J0 Octets 63-62	EWIS_Tx_J0_Octets_63_62	Page 291

Table 638 • **EWIS_Rx_J0_Octets_16_63**

Address	Short Description	Register Name	Details
0x2E900	E-WIS Rx J0 Octets 17-16	EWIS_Rx_J0_Octets_17_16	Page 292
0x2E901	E-WIS Rx J0 Octets 19-18	EWIS_Rx_J0_Octets_19_18	Page 292
0x2E902	E-WIS Rx J0 Octets 21-20	EWIS_Rx_J0_Octets_21_20	Page 292
0x2E903	E-WIS Rx J0 Octets 23-22	EWIS_Rx_J0_Octets_23_22	Page 292
0x2E904	E-WIS Rx J0 Octets 25-24	EWIS_Rx_J0_Octets_25_24	Page 292
0x2E905	E-WIS Rx J0 Octets 27-26	EWIS_Rx_J0_Octets_27_26	Page 293
0x2E906	E-WIS Rx J0 Octets 29-28	EWIS_Rx_J0_Octets_29_28	Page 293
0x2E907	E-WIS Rx J0 Octets 31-30	EWIS_Rx_J0_Octets_31_30	Page 293
0x2E908	E-WIS Rx J0 Octets 33-32	EWIS_Rx_J0_Octets_33_32	Page 293
0x2E909	E-WIS Rx J0 Octets 35-34	EWIS_Rx_J0_Octets_35_34	Page 294

Table 638 • **EWIS_Rx_J0_Octets_16_63** ***(continued)***

Address	Short Description	Register Name	Details
0x2E90A	E-WIS Rx J0 Octets 37-36	EWIS_Rx_J0_Octets_37_36	Page 294
0x2E90B	E-WIS Rx J0 Octets 39-38	EWIS_Rx_J0_Octets_39_38	Page 294
0x2E90C	E-WIS Rx J0 Octets 41-40	EWIS_Rx_J0_Octets_41_40	Page 294
0x2E90D	E-WIS Rx J0 Octets 43-42	EWIS_Rx_J0_Octets_43_42	Page 295
0x2E90E	E-WIS Rx J0 Octets 45-44	EWIS_Rx_J0_Octets_45_44	Page 295
0x2E90F	E-WIS Rx J0 Octets 47-46	EWIS_Rx_J0_Octets_47_46	Page 295
0x2E910	E-WIS Rx J0 Octets 49-48	EWIS_Rx_J0_Octets_49_48	Page 295
0x2E911	E-WIS Rx J0 Octets 51-50	EWIS_Rx_J0_Octets_51_50	Page 296
0x2E912	E-WIS Rx J0 Octets 53-52	EWIS_Rx_J0_Octets_53_52	Page 296
0x2E913	E-WIS Rx J0 Octets 55-54	EWIS_Rx_J0_Octets_55_54	Page 296
0x2E914	E-WIS Rx J0 Octets 57-56	EWIS_Rx_J0_Octets_57_56	Page 296
0x2E915	E-WIS Rx J0 Octets 59-58	EWIS_Rx_J0_Octets_59_58	Page 297
0x2E916	E-WIS Rx J0 Octets 61-60	EWIS_Rx_J0_Octets_61_60	Page 297
0x2E917	E-WIS Rx J0 Octets 63-62	EWIS_Rx_J0_Octets_63_62	Page 297

Table 639 • **EWIS_Tx_J1_Octets_16_63**

Address	Short Description	Register Name	Details
0x2EA00	E-WIS Tx J1 Octets 17-16	EWIS_Tx_J1_Octets_17_16	Page 298
0x2EA01	E-WIS Tx J1 Octets 19-18	EWIS_Tx_J1_Octets_19_18	Page 298
0x2EA02	E-WIS Tx J1 Octets 21-20	EWIS_Tx_J1_Octets_21_20	Page 298
0x2EA03	E-WIS Tx J1 Octets 23-22	EWIS_Tx_J1_Octets_23_22	Page 298
0x2EA04	E-WIS Tx J1 Octets 25-24	EWIS_Tx_J1_Octets_25_24	Page 298
0x2EA05	E-WIS Tx J1 Octets 27-26	EWIS_Tx_J1_Octets_27_26	Page 299
0x2EA06	E-WIS Tx J1 Octets 29-28	EWIS_Tx_J1_Octets_29_28	Page 299
0x2EA07	E-WIS Tx J1 Octets 31-30	EWIS_Tx_J1_Octets_31_30	Page 299
0x2EA08	E-WIS Tx J1 Octets 33-32	EWIS_Tx_J1_Octets_33_32	Page 299
0x2EA09	E-WIS Tx J1 Octets 35-34	EWIS_Tx_J1_Octets_35_34	Page 300
0x2EA0A	E-WIS Tx J1 Octets 37-36	EWIS_Tx_J1_Octets_37_36	Page 300
0x2EA0B	E-WIS Tx J1 Octets 39-38	EWIS_Tx_J1_Octets_39_38	Page 300
0x2EA0C	E-WIS Tx J1 Octets 41-40	EWIS_Tx_J1_Octets_41_40	Page 300
0x2EA0D	E-WIS Tx J1 Octets 43-42	EWIS_Tx_J1_Octets_43_42	Page 301
0x2EA0E	E-WIS Tx J1 Octets 45-44	EWIS_Tx_J1_Octets_45_44	Page 301
0x2EA0F	E-WIS Tx J1 Octets 47-46	EWIS_Tx_J1_Octets_47_46	Page 301
0x2EA10	E-WIS Tx J1 Octets 49-48	EWIS_Tx_J1_Octets_49_48	Page 301
0x2EA11	E-WIS Tx J1 Octets 51-50	EWIS_Tx_J1_Octets_51_50	Page 302
0x2EA12	E-WIS Tx J1 Octets 53-52	EWIS_Tx_J1_Octets_53_52	Page 302
0x2EA13	E-WIS Tx J1 Octets 55-54	EWIS_Tx_J1_Octets_55_54	Page 302
0x2EA14	E-WIS Tx J1 Octets 57-56	EWIS_Tx_J1_Octets_57_56	Page 302

Table 639 • **EWIS_Tx_J1_Octets_16_63 *(continued)***

Address	Short Description	Register Name	Details
0x2EA15	E-WIS Tx J1 Octets 59-58	EWIS_Tx_J1_Octets_59_58	Page 303
0x2EA16	E-WIS Tx J1 Octets 61-60	EWIS_Tx_J1_Octets_61_60	Page 303
0x2EA17	E-WIS Tx J1 Octets 63-62	EWIS_Tx_J1_Octets_63_62	Page 303

Table 640 • **EWIS_Rx_J1_Octets_16_63**

Address	Short Description	Register Name	Details
0x2EB00	E-WIS Rx J1 Octets 17-16	EWIS_Rx_J1_Octets_17_16	Page 304
0x2EB01	E-WIS Rx J1 Octets 19-18	EWIS_Rx_J1_Octets_19_18	Page 304
0x2EB02	E-WIS Rx J1 Octets 21-20	EWIS_Rx_J1_Octets_21_20	Page 304
0x2EB03	E-WIS Rx J1 Octets 23-22	EWIS_Rx_J1_Octets_23_22	Page 304
0x2EB04	E-WIS Rx J1 Octets 25-24	EWIS_Rx_J1_Octets_25_24	Page 304
0x2EB05	E-WIS Rx J1 Octets 27-26	EWIS_Rx_J1_Octets_27_26	Page 305
0x2EB06	E-WIS Rx J1 Octets 29-28	EWIS_Rx_J1_Octets_29_28	Page 305
0x2EB07	E-WIS Rx J1 Octets 31-30	EWIS_Rx_J1_Octets_31_30	Page 305
0x2EB08	E-WIS Rx J1 Octets 33-32	EWIS_Rx_J1_Octets_33_32	Page 305
0x2EB09	E-WIS Rx J1 Octets 35-34	EWIS_Rx_J1_Octets_35_34	Page 306
0x2EB0A	E-WIS Rx J1 Octets 37-36	EWIS_Rx_J1_Octets_37_36	Page 306
0x2EB0B	E-WIS Rx J1 Octets 39-38	EWIS_Rx_J1_Octets_39_38	Page 306
0x2EB0C	E-WIS Rx J1 Octets 41-40	EWIS_Rx_J1_Octets_41_40	Page 306
0x2EB0D	E-WIS Rx J1 Octets 43-42	EWIS_Rx_J1_Octets_43_42	Page 307
0x2EB0E	E-WIS Rx J1 Octets 45-44	EWIS_Rx_J1_Octets_45_44	Page 307
0x2EB0F	E-WIS Rx J1 Octets 47-46	EWIS_Rx_J1_Octets_47_46	Page 307
0x2EB10	E-WIS Rx J1 Octets 49-48	EWIS_Rx_J1_Octets_49_48	Page 307
0x2EB11	E-WIS Rx J1 Octets 51-50	EWIS_Rx_J1_Octets_51_50	Page 308
0x2EB12	E-WIS Rx J1 Octets 53-52	EWIS_Rx_J1_Octets_53_52	Page 308
0x2EB13	E-WIS Rx J1 Octets 55-54	EWIS_Rx_J1_Octets_55_54	Page 308
0x2EB14	E-WIS Rx J1 Octets 57-56	EWIS_Rx_J1_Octets_57_56	Page 308
0x2EB15	E-WIS Rx J1 Octets 59-58	EWIS_Rx_J1_Octets_59_58	Page 309
0x2EB16	E-WIS Rx J1 Octets 61-60	EWIS_Rx_J1_Octets_61_60	Page 309
0x2EB17	E-WIS Rx J1 Octets 63-62	EWIS_Rx_J1_Octets_63_62	Page 309

Table 641 • **EWIS_RX_FRMR_CFG**

Address	Short Description	Register Name	Details
0x2EC00	E-WIS Rx Framer Control 1	EWIS_RX_FRM_CTRL1	Page 309
0x2EC01	E-WIS Rx Framer Control 2	EWIS_RX_FRM_CTRL2	Page 310
0x2EC02	E-WIS Loss of Frame Control 1	EWIS_LOF_CTRL1	Page 310
0x2EC03	E-WIS Loss of Frame Control 2	EWIS_LOF_CTRL2	Page 311

Table 642 • **EWIS_Rx_Control_1**

Address	Short Description	Register Name	Details
0x2EC10	E-WIS Rx Control 1	EWIS_RX_CTRL1	Page 311

Table 643 • **EWIS_Rx_Trace_Message_Length_Control**

Address	Short Description	Register Name	Details
0x2EC20	E-WIS Rx Trace Message Length Control	EWIS_RX_MSGLEN	Page 312

Table 644 • **EWIS_RX_ERR_FRC**

Address	Short Description	Register Name	Details
0x2EC30	E-WIS Rx Error Force Control 1	EWIS_RX_ERR_FRC1	Page 312
0x2EC31	E-WIS Rx Error Force Control 2	EWIS_RX_ERR_FRC2	Page 313

Table 645 • **EWIS_Mode_Control**

Address	Short Description	Register Name	Details
0x2EC40	E-WIS Mode Control	EWIS_MODE_CTRL	Page 315

Table 646 • **EWIS_PRBS31_CFG_STAT**

Address	Short Description	Register Name	Details
0x2EC50	E-WIS PRBS31 Analyzer Control	EWIS_PRBS31_ANA_CTRL	Page 316
0x2EC51	E-WIS PRBS31 Analyzer Status	EWIS_PRBS31_ANA_STAT	Page 316

Table 647 • **EWIS_Performance_Monitor_Control**

Address	Short Description	Register Name	Details
0x2EC60	E-WIS Performance Monitor Control	EWIS_PMTICK_CTRL	Page 317

Table 648 • **EWIS_Counter_Configuration**

Address	Short Description	Register Name	Details
0x2EC61	E-WIS Counter Configuration	EWIS_CNT_CFG	Page 318

Table 649 • **EWIS_Counter_Status**

Address	Short Description	Register Name	Details
0x2EC62	E-WIS Counter Status	EWIS_CNT_STAT	Page 318

Table 650 • **EWIS_REIP_CNT**

Address	Short Description	Register Name	Details
0x2EC80	E-WIS P-REI Counter 1 MSW	EWIS_REIP_CNT1	Page 319
0x2EC81	E-WIS P-REI Counter 0 LSW	EWIS_REIP_CNT0	Page 319

Table 651 • **EWIS_REIL_CNT**

Address	Short Description	Register Name	Details
0x2EC90	E-WIS L-REI Counter 1 MSW	EWIS_REIL_CNT1	Page 319
0x2EC91	E-WIS L-REI Counter 0 LSW	EWIS_REIL_CNT0	Page 319

Table 652 • **EWIS_B1_ERR_CNT**

Address	Short Description	Register Name	Details
0x2ECB0	E-WIS S-BIP Error Counter 1 MSW	EWIS_B1_ERR_CNT1	Page 320
0x2ECB1	E-WIS S-BIP Error Counter 0 LSW	EWIS_B1_ERR_CNT0	Page 320

Table 653 • **EWIS_B2_ERR_CNT**

Address	Short Description	Register Name	Details
0x2ECB2	E-WIS L-BIP Error Counter 1 MSW	EWIS_B2_ERR_CNT1	Page 320
0x2ECB3	E-WIS L-BIP Error Counter 0 LSW	EWIS_B2_ERR_CNT0	Page 320

Table 654 • **EWIS_Rx_to_Tx_Control**

Address	Short Description	Register Name	Details
0x2EDFF	E-WIS Rx to Tx Control	EWIS_RXTX_CTRL	Page 321

Table 655 • **EWIS_Interrupt_Pending_1**

Address	Short Description	Register Name	Details
0x2EE00	E-WIS Interrupt Pending 1	EWIS_INTR_PEND1	Page 322

Table 656 • **EWIS_Interrupt_Mask_1**

Address	Short Description	Register Name	Details
0x2EE01	E-WIS Interrupt Mask A 1	EWIS_INTR_MASKA_1	Page 324
0x2EE02	E-WIS Interrupt Mask B 1	EWIS_INTR_MASKB_1	Page 325

Table 657 • **EWIS_Interrupt_Status_2**

Address	Short Description	Register Name	Details
0x2EE03	E-WIS Interrupt Status 2	EWIS_INTR_STAT2	Page 326

Table 658 • **EWIS_Interrupt_Pending_2**

Address	Short Description	Register Name	Details
0x2EE04	E-WIS Interrupt Pending 2	EWIS_INTR_PEND2	Page 327

Table 659 • **EWIS_Interrupt_Mask_2**

Address	Short Description	Register Name	Details
0x2EE05	E-WIS Interrupt Mask A 2	EWIS_INTR_MASKA_2	Page 329
0x2EE06	E-WIS Interrupt Mask B 2	EWIS_INTR_MASKB_2	Page 330

Table 660 • **WIS_FAULT_MASK**

Address	Short Description	Register Name	Details
0x2EE07	WIS_FAULT_MASK	WIS_FAULT_MASK	Page 331

Table 661 • **EWIS_Interrupt_Pending_3**

Address	Short Description	Register Name	Details
0x2EE08	E-WIS Interrupt Pending 3	EWIS_INTR_PEND3	Page 332

Table 662 • **EWIS_Interrupt_Mask_3**

Address	Short Description	Register Name	Details
0x2EE09	E-WIS Interrupt Mask A 3	EWIS_INTR_MASKA_3	Page 333
0x2EE0A	E-WIS Interrupt Mask B 3	EWIS_INTR_MASKB_3	Page 334

Table 663 • **Threshold_Error_Status**

Address	Short Description	Register Name	Details
0x2EE0B	Threshold Error Status	THRESH_ERR_STAT	Page 334

Table 664 • **PMTICK_Cntr_Intr_Threshold_Levels**

Address	Short Description	Register Name	Details
0x2EE10	WIS REI-P Threshold Level 1	WIS_REIP_THRESH_LVL1	Page 335
0x2EE11	WIS REI-P Threshold Level 0	WIS_REIP_THRESH_LVL0	Page 335
0x2EE12	WIS REI-L Threshold Level 1	WIS_REIL_THRESH_LVL1	Page 336
0x2EE13	WIS REI-L Threshold Level 0	WIS_REIL_THRESH_LVL0	Page 336

Table 664 • **PMTICK_Cntr_Intr_Threshold_Levels *(continued)***

Address	Short Description	Register Name	Details
0x2EE14	WIS B1 Threshold Level 1	WIS_B1_THRESH_LVL1	Page 336
0x2EE15	WIS B1 Threshold Level 0	WIS_B1_THRESH_LVL0	Page 336
0x2EE16	WIS B2 Threshold Level 1	WIS_B2_THRESH_LVL1	Page 337
0x2EE17	WIS B2 Threshold Level 0	WIS_B2_THRESH_LVL0	Page 337
0x2EE18	WIS B3 Threshold Level 1	WIS_B3_THRESH_LVL1	Page 337
0x2EE19	WIS B3 Threshold Level 0	WIS_B3_THRESH_LVL0	Page 337

2.9.1 WIS Configuration and Status

2.9.1.1 WIS Control 1

Short Name:WIS_CTRL1

Address:0x20000

Table 665 • **WIS Control 1**

Bit	Name	Access	Description	Default
15	SOFT_RST	One-shot	MDIO Manageable Device (MMD) software reset. Reset all logic in the channel between the host side PMA and the line side PMA, regardless of the cross-connect configuration. Data path logic and configuration registers are reset. 0 = Normal operation 1 = Reset	0x0
14	LPBK_H4	R/W	Enables WIS system loopback (loopback H4) 0 = Disable 1 = Enable	0x0
13	SPEED_SEL_A	R/O	Speed selection 0 = Unspecified 1 = Operates at 10 Gbps or above	0x1
11	LOW_PWR_WIS	R/W	The channel's data path is placed into low power mode with this register. The PMA in this channel is also placed into low power mode regardless of the channel cross connect configuration. The PMD_TRANSMIT_DISABLE.GLOBAL_PMD_TRANSMIT_DISABLE register state can can be transmitted from a GPIO pin to shut off an optics module's Tx driver. 0 = Normal Operation 1 = Low Power Mode.	0x0
6	SPEED_SEL_B	R/O	Speed selection 0 = Unspecified 1 = Operates at 10 Gbps or above	0x1
5:2	SPEED_SEL_C	R/O	Speed selection 1xxx: Reserved. x1xx: Reserved. xx1x: Reserved. 0001: Reserved. 0000: 10 Gbps	0x0

2.9.1.2 WIS Status 1

Short Name:WIS_STAT1

Address:0x20001

Table 666 • **WIS Status 1**

Bit	Name	Access	Description	Default
7	FAULT	R/O	WIS fault status. The alarm conditions that cause the WIS fault status to be asserted are configured in the WIS_FAULT_MASK register. Based on the WIS_FAULT_MASK setting, the WIS fault status can be asserted when the following alarm conditions exist: OOF, LOS, LOF, LOP-P, AIS-L, AIS-P, LCD-P, PLM-P, RDI-L, far-end AIS-P and far-end PLM-P. This is a sticky bit that latches the high state. The latch-high bit is cleared when the register is read. 0 = No faults asserted 1 = Fault asserted	0x0
2	LNK_STAT	R/O	WIS receive link status. Link up means no AIS-P, AIS-L, PLM-P, LOP-P or SEF alarms. This is a sticky bit that latches the low state. The latch-low bit is cleared when the register is read. 0 = WIS link down. (AIS-P=1 OR AIS-L=1 OR PLM-P=1 OR WIS SEF=1 or LOP-P=1) 1 = WIS link up. (AIS-P=0 AND AIS-L=0 AND PLM-P=0 AND SEF=0 AND LOP-P=0)	0x1
1	LOW_PWR_ABILITY	R/O	Low power mode support ability. 0 = Supported 1 = Not supported	0x1

2.9.1.3 WIS Device Identifier 1

Short Name:WIS_DEVID1

Address:0x20002

Table 667 • **WIS Device Identifier 1**

Bit	Name	Access	Description	Default
15:0	DEV_ID_MSW	R/O	Upper 16 bits of a 32-bit unique WIS device identifier. Bits 3-18 of the device manufacturer's OUI.	0x0007

2.9.1.4 WIS Device Identifier 2

Short Name:WIS_DEVID2

Address:0x20003

Table 668 • **WIS Device Identifier 2**

Bit	Name	Access	Description	Default
15:0	DEV_ID_LSW	R/O	Lower 16 bits of a 32-bit unique WIS device identifier. Bits 19-24 of the device manufacturer's OUI. Six-bit model number, and a four-bit revision number.	0x0400

2.9.1.5 WIS Speed Capability

Short Name:WIS_SPEED

Address:0x20004

Table 669 • **WIS Speed Capability**

Bit	Name	Access	Description	Default
0	RATE_ABILITY	R/O	WIS rate capability 0 = Not capable of 10Gbps 1 = Capable of 10Gbps	0x1

2.9.1.6 WIS Devices in Package 1

Short Name:WIS_DEVPKG1

Address:0x20005

Table 670 • **WIS Devices in Package 1**

Bit	Name	Access	Description	Default
5	DTE_XS_PRES	R/O	Indicates whether DTE XS is present in the package 0 = Not present 1 = Present	0x0
4	PHY_XS_PRES	R/O	Indicates whether PHY XS is present in the package 0 = Not present 1 = Present	0x1
3	PCS_PRES	R/O	Indicates whether PCS is present in the package 0 = Not present 1 = Present	0x1
2	WIS_PRES	R/O	Indicates whether WIS is present in the package 0 = Not present 1 = Present	0x1
1	PMD_PMA_PRES	R/O	Indicates whether PMA/PMD is present in the package 0 = Not present 1 = Present	0x1
0	CLS22_PRES	R/O	Indicates whether Clause 22 registers are present in the package 0 = Not present 1 = Present	0x0

2.9.1.7 WIS Devices in Package 2

Short Name:WIS_DEVPKG2

Address:0x20006

Table 671 • **WIS Devices in Package 2**

Bit	Name	Access	Description	Default
15	Vendor_spec_dev_2_present	R/O	Indicates whether vendor specific device 2 is present in the package 0 = Not present 1 = Present	0x0

Table 671 • **WIS Devices in Package 2 *(continued)***

Bit	Name	Access	Description	Default
14	Vendor_spec_dev_1_present	R/O	Indicates whether vendor specific device 1 is present in the package 0 = Not present 1 = Present	0x0

2.9.1.8 WIS Control 2

Short Name:WIS_CTRL2

Address:0x20007

Table 672 • **WIS Control 2**

Bit	Name	Access	Description	Default
5	TEST_PRBS31_ANA	R/W	Enable WIS PRBS31 test pattern checking function 0 = Disable 1 = Enable	0x0
4	TEST_PRBS31_GEN	R/W	Enable WIS PRBS31 test pattern generation function. Transmission of the PRBS31 pattern has priority over the square wave and mixed frequency test patterns if TEST_PAT_GEN in this register is also high. 0 = Disable 1 = Enable	0x0
3	TEST_PAT_SEL	R/W	Selects the pattern type sent by the transmitter when bit TEST_PAT_GEN in this register is high. 0 = Mixed frequency test pattern 1 = Square wave	0x0
2	TEST_PAT_ANA	R/W	Enables the WIS test pattern checker. Doing so prevents the loss of code-group delineation (LCD-P) alarm from being set while the WIS is receiving the mixed frequency test pattern. 0 = Disable 1 = Enable	0x0
1	TEST_PAT_GEN	R/W	Enable WIS test pattern generation 0 = Disable 1 = Enable	0x0
0	WAN_MODE	R/W	Enable 10GBASE-W logic and sets the speed of the WIS-PMA interface to 9.95328 Gbps. The proper reference clock frequency must be provided to set the data rate. Note: there are multiple ways to enable WAN mode. 0 = Disable 1 = Enable	0x0

2.9.1.9 WIS Status 2

Short Name:WIS_STAT2

Address:0x20008

Table 673 • **WIS Status 2**

Bit	Name	Access	Description	Default
15:14	DEV_PRES	R/O	Reflects the presence of a MMD responding at this address 00: No device responding at this address 01: No device responding at this address 10: Device responding at this address 11: No device responding at this address	0xA
1	PRBS31_ABILITY	R/O	Indicates if WIS supports PRBS31 pattern testing 0 = Not supported 1 = Supported	0x1
0	BASE_R_ABILITY	R/O	Indicates if WIS supports a bypass to allow support of 10GBASE-R 0 = Not supported 1 = Supported	0x1

2.9.1.10 WIS Test Pattern Error Counter

Short Name:WIS_TSTPAT_CNT

Address:0x20009

Table 674 • **WIS Test Pattern Error Counter**

Bit	Name	Access	Description	Default
15:0	TSTPAT_CNT	R/O	PRBS31 test pattern error counter. The saturating counter is cleared when the register is read. The error count is not valid until the sync status in register bit EWIS_PRBS31_ANA_STAT.PRBS31_ANA_STATE is asserted. The error count in this register can be incremented while the checker is acquiring sync. Read this register to clear the invalid error count when sync is achieved. Once synchronization is achieved, any future loss of synchronization will not prevent the error counter from accumulating.	0x0000

2.9.1.11 WIS Package Identifier 1

Short Name:WIS_PKGID1

Address:0x2000E

Table 675 • **WIS Package Identifier 1**

Bit	Name	Access	Description	Default
15:0	PKG_ID_MSW	R/O	Upper 16 bits of a 32-bit unique WIS package identifier. Bits 3-18 of the device manufacturer's OUI. Six-bit model number and a four-bit revision number.	0x0000

2.9.1.12 WIS Package Identifier 2

Short Name:WIS_PKGID2

Address:0x2000F

Table 676 • **WIS Package Identifier 2**

Bit	Name	Access	Description	Default
15:0	PKG_ID_LSW	R/O	Lower 16 bits of a 32-bit unique WIS package identifier. Bits 19-24 of the device manufacturer's OUI. Six-bit model number and a four-bit revision number.	0x0000

2.9.1.13 WIS Status 3

Short Name:WIS_STAT3

Address:0x20021

Table 677 • **WIS Status 3**

Bit	Name	Access	Description	Default
11	SEF	R/O	Severely errored frame. This is a sticky bit that latches the high state. The latch-high bit is cleared when the register is read. 0 = No SEF detected 1 = SEF detected	0x0
10	FEPLMP_LCDP	R/O	Indicates far-end PLM-P/LCD-P defect in WIS Rx. The latch-high bit is cleared when the register is read. 0 = No far-end path label mismatch / Loss of code-group delineation 1 = far-end path label mismatch / Loss of code-group delineation	0x0
9	FEAISP_LOPP	R/O	Indicates far-end AIS-P/LOP-P defect in WIS Rx. The latch-high bit is cleared when the register is read. 0 = far-end path Alarm Indication Signal / Path Loss of Pointer 1 = No far-end path alarm indication signal / Path loss of pointer	0x0
7	LOF	R/O	Loss of frame . The latch-high bit is cleared when the register is read. 0 = Loss of frame flag lowered 1 = Loss of frame flag raised	0x0
6	LOS	R/O	Loss of signal . The latch-high bit is cleared when the register is read. 0 = Loss of signal flag lowered 1 = Loss of signal flag raised	0x0
5	RDIL	R/O	Line remote defect indication. The latch-high bit is cleared when the register is read. 0 = Line remote defect flag lowered 1 = Line remote defect flag raised	0x0
4	AISL	R/O	Line alarm indication signal. The latch-high bit is cleared when the register is read. 0 = Line alarm indication flag lowered 1 = Line alarm indication flag raised	0x0

Table 677 • **WIS Status 3 *(continued)***

Bit	Name	Access	Description	Default
3	LCDP	R/O	Path loss of code-group delineation. The latch-high bit is cleared when the register is read. 0 = Path loss of code-group delineation flag lowered 1 = Path loss of code-group delineation flag raised	0x0
2	PLMP	R/O	Path label mismatch. The latch-high bit is cleared when the register is read. 0 = Path label mismatch flag lowered 1 = Path label mismatch flag raised	0x0
1	AISP	R/O	Path alarm indication signal. The latch-high bit is cleared when the register is read. 0 = Path alarm indication signal lowered 1 = Path alarm indication signal raised	0x0
0	LOPP	R/O	Loss of pointer. The latch-high bit is cleared when the register is read. 0 = Loss of pointer flag lowered 1 = Loss of pointer flag raised	0x0

2.9.1.14 WIS Far-End Path Block Error Count

Short Name:WIS_REIP_CNT

Address:0x20025

Table 678 • **WIS Far-End Path Block Error Count**

Bit	Name	Access	Description	Default
15:0	REIP_CNT	R/O	Far end path block error count. Counter wraps around to 0 when it is incremented beyond its maximum error count of 65,535. Cleared on channel reset.	0x0000

2.9.2 Tx Path Trace Message Octets

The number of octets present in the transmitted path trace message is determined by EWIS_TX_MSGLEN.J1_TXLEN. Octet 0 is used when the trace message length is 1 byte. When a 16 byte trace message length is selected, octet 0 is the first octet transmitted, octet 15 is the last octet. When a 64 byte trace message length is selected, octet 0 is the first octet transmitted, octet 63 is the last octet. Octets 16 to 63 are located in registers EWIS_Tx_J1_Octets_17_16 to EWIS_Tx_J1_Octets_63_62.

2.9.2.1 WIS Tx J1 Octets 1-0

Short Name:WIS_Tx_J1_Octets_1_0

Address:0x20027

Table 679 • **WIS Tx J1 Octets 1-0**

Bit	Name	Access	Description	Default
15:8	TX_J1_octet_1	R/W	Contains octet 1 of the transmitted path trace message.	0x00
7:0	TX_J1_octet_0	R/W	Contains octet 0 of the transmitted path trace message.	0x00

2.9.2.2 WIS Tx J1 Octets 3-2

Short Name:WIS_Tx_J1_Octets_3_2

Address:0x20028

Table 680 • **WIS Tx J1 Octets 3-2**

Bit	Name	Access	Description	Default
15:8	TX_J1_octet_3	R/W	Contains octet 3 of the transmitted path trace message.	0x00
7:0	TX_J1_octet_2	R/W	Contains octet 2 of the transmitted path trace message.	0x00

2.9.2.3 WIS Tx J1 Octets 5-4

Short Name:WIS_Tx_J1_Octets_5_4

Address:0x20029

Table 681 • **WIS Tx J1 Octets 5-4**

Bit	Name	Access	Description	Default
15:8	TX_J1_octet_5	R/W	Contains octet 5 of the transmitted path trace message.	0x00
7:0	TX_J1_octet_4	R/W	Contains octet 4 of the transmitted path trace message.	0x00

2.9.2.4 WIS Tx J1 Octets 7-6

Short Name:WIS_Tx_J1_Octets_7_6

Address:0x2002A

Table 682 • **WIS Tx J1 Octets 7-6**

Bit	Name	Access	Description	Default
15:8	TX_J1_octet_7	R/W	Contains octet 7 of the transmitted path trace message.	0x00
7:0	TX_J1_octet_6	R/W	Contains octet 6 of the transmitted path trace message.	0x00

2.9.2.5 WIS Tx J1 Octets 9-8

Short Name:WIS_Tx_J1_Octets_9_8

Address:0x2002B

Table 683 • **WIS Tx J1 Octets 9-8**

Bit	Name	Access	Description	Default
15:8	TX_J1_octet_9	R/W	Contains octet 9 of the transmitted path trace message.	0x00
7:0	TX_J1_octet_8	R/W	Contains octet 8 of the transmitted path trace message.	0x00

2.9.2.6 WIS Tx J1 Octets 11-10

Short Name:WIS_Tx_J1_Octets_11_10

Address:0x2002C

Table 684 • **WIS Tx J1 Octets 11-10**

Bit	Name	Access	Description	Default
15:8	TX_J1_octet_11	R/W	Contains octet 11 of the transmitted path trace message.	0x00
7:0	TX_J1_octet_10	R/W	Contains octet 10 of the transmitted path trace message.	0x00

2.9.2.7 WIS Tx J1 Octets 13-12

Short Name:WIS_Tx_J1_Octets_13_12

Address:0x2002D

Table 685 • **WIS Tx J1 Octets 13-12**

Bit	Name	Access	Description	Default
15:8	TX_J1_octet_13	R/W	Contains octet 13 of the transmitted path trace message.	0x00
7:0	TX_J1_octet_12	R/W	Contains octet 12 of the transmitted path trace message.	0x00

2.9.2.8 WIS Tx J1 Octets 15-14

Short Name:WIS_Tx_J1_Octets_15_14

Address:0x2002E

Table 686 • **WIS Tx J1 Octets 15-14**

Bit	Name	Access	Description	Default
15:8	TX_J1_octet_15	R/W	Contains octet 15 of the transmitted path trace message.	0x89
7:0	TX_J1_octet_14	R/W	Contains octet 14 of the transmitted path trace message.	0x00

2.9.3 Rx Path Trace Message Octets

The number of octets present in the received path trace message is determined by EWIS_RX_MSGLEN.J1_RX_LEN. Octet 0 is used when the trace message length is 1 byte. When a 16 byte trace message length is selected, octet 0 is the first octet received, octet 15 is the last octet. When a 64 byte trace message length is selected, octet 0 is the first octet received, octet 63 is the last octet. Octets 16 to 63 are located in registers EWIS_Rx_J1_Octets_17_16 to EWIS_Rx_J1_Octets_63_62.

2.9.3.1 WIS Rx J1 Octets 1-0

Short Name:WIS_Rx_J1_Octets_1_0

Address:0x2002F

Table 687 • **WIS Rx J1 Octets 1-0**

Bit	Name	Access	Description	Default
15:8	RX_J1_octet_1	R/O	Contains octet 1 of the received path trace message	0x00

Table 687 • **WIS Rx J1 Octets 1-0 *(continued)***

Bit	Name	Access	Description	Default
7:0	RX_J1_octet_0	R/O	Contains octet 0 of the received path trace message	0x00

2.9.3.2 WIS Rx J1 Octets 3-2

Short Name:WIS_Rx_J1_Octets_3_2

Address:0x20030

Table 688 • **WIS Rx J1 Octets 3-2**

Bit	Name	Access	Description	Default
15:8	RX_J1_octet_3	R/O	Contains octet 3 of the received path trace message	0x00
7:0	RX_J1_octet_2	R/O	Contains octet 2 of the received path trace message	0x00

2.9.3.3 WIS Rx J1 Octets 5-4

Short Name:WIS_Rx_J1_Octets_5_4

Address:0x20031

Table 689 • **WIS Rx J1 Octets 5-4**

Bit	Name	Access	Description	Default
15:8	RX_J1_octet_5	R/O	Contains octet 5 of the received path trace message	0x00
7:0	RX_J1_octet_4	R/O	Contains octet 4 of the received path trace message	0x00

2.9.3.4 WIS Rx J1 Octets 7-6

Short Name:WIS_Rx_J1_Octets_7_6

Address:0x20032

Table 690 • **WIS Rx J1 Octets 7-6**

Bit	Name	Access	Description	Default
15:8	RX_J1_octet_7	R/O	Contains octet 7 of the received path trace message	0x00
7:0	RX_J1_octet_6	R/O	Contains octet 6 of the received path trace message	0x00

2.9.3.5 WIS Rx J1 Octets 9-8

Short Name:WIS_Rx_J1_Octets_9_8

Address:0x20033

Table 691 • **WIS Rx J1 Octets 9-8**

Bit	Name	Access	Description	Default
15:8	RX_J1_octet_9	R/O	Contains octet 9 of the received path trace message	0x00

Table 691 • **WIS Rx J1 Octets 9-8 *(continued)***

Bit	Name	Access	Description	Default
7:0	RX_J1_octet_8	R/O	Contains octet 8 of the received path trace message	0x00

2.9.3.6 WIS Rx J1 Octets 11-10

Short Name:WIS_Rx_J1_Octets_11_10

Address:0x20034

Table 692 • **WIS Rx J1 Octets 11-10**

Bit	Name	Access	Description	Default
15:8	RX_J1_octet_11	R/O	Contains octet 11 of the received path trace message	0x00
7:0	RX_J1_octet_10	R/O	Contains octet 10 of the received path trace message	0x00

2.9.3.7 WIS Rx J1 Octets 13-12

Short Name:WIS_Rx_J1_Octets_13_12

Address:0x20035

Table 693 • **WIS Rx J1 Octets 13-12**

Bit	Name	Access	Description	Default
15:8	RX_J1_octet_13	R/O	Contains octet 13 of the received path trace message	0x00
7:0	RX_J1_octet_12	R/O	Contains octet 12 of the received path trace message	0x00

2.9.3.8 WIS Rx J1 Octets 15-14

Short Name:WIS_Rx_J1_Octets_15_14

Address:0x20036

Table 694 • **WIS Rx J1 Octets 15-14**

Bit	Name	Access	Description	Default
15:8	RX_J1_octet_15	R/O	Contains octet 15 of the received path trace message	0x00
7:0	RX_J1_octet_14	R/O	Contains octet 14 of the received path trace message	0x00

2.9.4 WIS Line Errors Counts

2.9.4.1 WIS Far-End Line BIP Errors 1

Short Name:WIS_REIL_CNT1

Address:0x20037

Table 695 • **WIS Far-End Line BIP Errors 1**

Bit	Name	Access	Description	Default
15:0	REIL_ERR_CNT_MSW	R/O	Most significant word of the WIS far end line BIP error counter. The counter does not saturate when the maximum count has been exceeded. Reading register WIS_REIL_CNT1 latches the 32-bit counter value into a pair of 16-bit registers. The most significant counter bits are located in WIS_REIL_CNT1. The least significant bits are located in WIS_REIL_CNT0. Subsequent reads of address WIS_REIL_CNT0 will return the latched value and will not change the latched register contents. The counter can only be cleared by reseting the WIS logic block.	0x0000

2.9.4.2 WIS Far-End Line BIP Errors 0

Short Name:WIS_REIL_CNT0

Address:0x20038

Table 696 • **WIS Far-End Line BIP Errors 0**

Bit	Name	Access	Description	Default
15:0	REIL_ERR_CNT_LSW	R/O	Least significant word of the WIS far end line BIP error counter. The counter does not saturate when the maximum count has been exceeded. Reading register WIS_REIL_CNT1 latches the 32-bit counter value into a pair of 16-bit registers. The most significant counter bits are located in WIS_REIL_CNT1. The least significant bits are located in WIS_REIL_CNT0. Subsequent reads of address WIS_REIL_CNT0 will return the latched value and will not change the latched register contents. The counter can only be cleared by reseting the WIS logic block.	0x0000

2.9.4.3 WIS L-BIP Error Count 1

Short Name:WIS_B2_CNT1

Address:0x20039

Table 697 • **WIS L-BIP Error Count 1**

Bit	Name	Access	Description	Default
15:0	B2_CNT_MSW	R/O	Most significant word of the WIS line BIP error counter. The counter does not saturate when the maximum count has been exceeded. Reading register WIS_B2_CNT1 latches the 32-bit counter value into a pair of 16-bit registers. The most significant counter bits are associated with WIS_B2_CNT1. The least significant bits appear in WIS_B2_CNT0. Subsequent reads of address WIS_B2_CNT0 will return the latched value and will not change the latched register contents. The counter can only be cleared by reseting the WIS logic block.	0x0000

2.9.4.4 WIS L-BIP Error Count 0

Short Name:WIS_B2_CNT0

Address:0x2003A

Table 698 • **WIS L-BIP Error Count 0**

Bit	Name	Access	Description	Default
15:0	B2_CNT_LSW	R/O	Least significant word of the WIS line BIP error counter. The counter does not saturate when the maximum count has been exceeded. Reading register WIS_B2_CNT1 latches the 32-bit counter value into a pair of 16-bit registers. The most significant counter bits are associated with WIS_B2_CNT1. The least significant bits appear in WIS_B2_CNT0. Subsequent reads of address WIS_B2_CNT0 will return the latched value and will not change the latched register contents. The counter can only be cleared by reseting the WIS logic block.	0x0000

2.9.4.5 WIS P-BIP Block Error Count

Short Name:WIS_B3_CNT

Address:0x2003B

Table 699 • **WIS P-BIP Block Error Count**

Bit	Name	Access	Description	Default
15:0	B3_CNT	R/O	Path block error count. The counter does not saturate when the maximum count has been exceeded. The counter can only be cleared by reseting the WIS logic block.	0x0000

2.9.4.6 WIS S-BIP Error Count

Short Name:WIS_B1_CNT

Address:0x2003C

Table 700 • **WIS S-BIP Error Count**

Bit	Name	Access	Description	Default
15:0	B1_CNT	R/O	Section BIP error count. The counter does not saturate when the maximum count has been exceeded. The counter can only be cleared by reseting the WIS logic block.	0x0000

2.9.5 Tx Section Trace Message Octets

The number of octets present in the transmitted section trace message is determined by EWIS_TX_MSGLEN.J0_TXLEN. Octet 0 is used when the trace message length is 1 byte. When a 16 byte trace message length is selected, octet 0 is the first octet transmitted, octet 15 is the last octet. When a 64 byte trace message length is selected, octet 0 is the first octet transmitted, octet 63 is the last octet. Octets 16 to 63 are located in registers EWIS_Tx_J0_Octets_17_16 to EWIS_Tx_J0_Octets_63_62.

2.9.5.1 WIS Tx J0 Octets 1-0

Short Name:WIS_Tx_J0_Octets_1_0

Address:0x20040

Table 701 • **WIS Tx J0 Octets 1-0**

Bit	Name	Access	Description	Default
15:8	TX_J0_octet_1	R/W	Contains octet 1 of the transmitted Section Trace Message.	0x00
7:0	TX_J0_octet_0	R/W	Contains octet 0 of the transmitted Section Trace Message.	0x00

2.9.5.2 WIS Tx J0 Octets 3-2

Short Name:WIS_Tx_J0_Octets_3_2

Address:0x20041

Table 702 • **WIS Tx J0 Octets 3-2**

Bit	Name	Access	Description	Default
15:8	TX_J0_octet_3	R/W	Contains octet 3 of the transmitted Section Trace Message.	0x00
7:0	TX_J0_octet_2	R/W	Contains octet 2 of the transmitted Section Trace Message.	0x00

2.9.5.3 WIS Tx J0 Octets 5-4

Short Name:WIS_Tx_J0_Octets_5_4

Address:0x20042

Table 703 • **WIS Tx J0 Octets 5-4**

Bit	Name	Access	Description	Default
15:8	TX_J0_octet_5	R/W	Contains octet 5 of the transmitted Section Trace Message.	0x00

Table 703 • **WIS Tx J0 Octets 5-4 *(continued)***

Bit	Name	Access	Description	Default
7:0	TX_J0_octet_4	R/W	Contains octet 4 of the transmitted Section Trace Message.	0x00

2.9.5.4 WIS Tx J0 Octets 7-6

Short Name:WIS_Tx_J0_Octets_7_6

Address:0x20043

Table 704 • **WIS Tx J0 Octets 7-6**

Bit	Name	Access	Description	Default
15:8	TX_J0_octet_7	R/W	Contains octet 7 of the transmitted Section Trace Message.	0x00
7:0	TX_J0_octet_6	R/W	Contains octet 6 of the transmitted Section Trace Message.	0x00

2.9.5.5 WIS Tx J0 Octets 9-8

Short Name:WIS_Tx_J0_Octets_9_8

Address:0x20044

Table 705 • **WIS Tx J0 Octets 9-8**

Bit	Name	Access	Description	Default
15:8	TX_J0_octet_9	R/W	Contains octet 9 of the transmitted Section Trace Message.	0x00
7:0	TX_J0_octet_8	R/W	Contains octet 8 of the transmitted Section Trace Message.	0x00

2.9.5.6 WIS Tx J0 Octets 11-10

Short Name:WIS_Tx_J0_Octets_11_10

Address:0x20045

Table 706 • **WIS Tx J0 Octets 11-10**

Bit	Name	Access	Description	Default
15:8	TX_J0_octet_11	R/W	Contains octet 11 of the transmitted Section Trace Message.	0x00
7:0	TX_J0_octet_10	R/W	Contains octet 10 of the transmitted Section Trace Message.	0x00

2.9.5.7 WIS Tx J0 Octets 13-12

Short Name:WIS_Tx_J0_Octets_13_12

Address:0x20046

Table 707 • **WIS Tx J0 Octets 13-12**

Bit	Name	Access	Description	Default
15:8	TX_J0_octet_13	R/W	Contains octet 13 of the transmitted Section Trace Message.	0x00

Table 707 • **WIS Tx J0 Octets 13-12 *(continued)***

Bit	Name	Access	Description	Default
7:0	TX_J0_octet_12	R/W	Contains octet 12 of the transmitted Section Trace Message.	0x00

2.9.5.8 WIS Tx J0 Octets 15-14

Short Name:WIS_Tx_J0_Octets_15_14

Address:0x20047

Table 708 • **WIS Tx J0 Octets 15-14**

Bit	Name	Access	Description	Default
15:8	TX_J0_octet_15	R/W	Contains octet 15 of the transmitted Section Trace Message.	0x89
7:0	TX_J0_octet_14	R/W	Contains octet 14 of the transmitted Section Trace Message.	0x00

2.9.6 Rx Section Trace Message Octets

The number of octets present in the received section trace message is determined by EWIS_RX_MSGLEN.J0_RX_LEN. Octet 0 is used when the trace message length is 1 byte. When a 16 byte trace message length is selected, octet 0 is the first octet received, octet 15 is the last octet. When a 64 byte trace message length is selected, octet 0 is the first octet received, octet 63 is the last octet. Octets 16 to 63 are located in registers EWIS_Rx_J0_Octets_17_16 to EWIS_Rx_J0_Octets_63_62.

2.9.6.1 WIS Rx J0 Octets 1-0

Short Name:WIS_Rx_J0_Octets_1_0

Address:0x20048

Table 709 • **WIS Rx J0 Octets 1-0**

Bit	Name	Access	Description	Default
15:8	RX_J0_octet_1	R/O	Contains octet 1 of the received Section Trace Message.	0x00
7:0	RX_J0_octet_0	R/O	Contains octet 0 of the received Section Trace Message.	0x00

2.9.6.2 WIS Rx J0 Octets 3-2

Short Name:WIS_Rx_J0_Octets_3_2

Address:0x20049

Table 710 • **WIS Rx J0 Octets 3-2**

Bit	Name	Access	Description	Default
15:8	RX_J0_octet_3	R/O	Contains octet 3 of the received Section Trace Message.	0x00
7:0	RX_J0_octet_2	R/O	Contains octet 2 of the received Section Trace Message.	0x00

2.9.6.3 WIS Rx J0 Octets 5-4

Short Name:WIS_Rx_J0_Octets_5_4

Address:0x2004A

Table 711 • **WIS Rx J0 Octets 5-4**

Bit	Name	Access	Description	Default
15:8	RX_J0_octet_5	R/O	Contains octet 5 of the received Section Trace Message.	0x00
7:0	RX_J0_octet_4	R/O	Contains octet 4 of the received Section Trace Message.	0x00

2.9.6.4 WIS Rx J0 Octets 7-6

Short Name:WIS_Rx_J0_Octets_7_6

Address:0x2004B

Table 712 • **WIS Rx J0 Octets 7-6**

Bit	Name	Access	Description	Default
15:8	RX_J0_octet_7	R/O	Contains octet 7 of the received Section Trace Message.	0x00
7:0	RX_J0_octet_6	R/O	Contains octet 6 of the received Section Trace Message.	0x00

2.9.6.5 WIS Rx J0 Octets 9-8

Short Name:WIS_Rx_J0_Octets_9_8

Address:0x2004C

Table 713 • **WIS Rx J0 Octets 9-8**

Bit	Name	Access	Description	Default
15:8	RX_J0_octet_9	R/O	Contains octet 9 of the received Section Trace Message.	0x00
7:0	RX_J0_octet_8	R/O	Contains octet 8 of the received Section Trace Message.	0x00

2.9.6.6 WIS Rx J0 Octets 11-10

Short Name:WIS_Rx_J0_Octets_11_10

Address:0x2004D

Table 714 • **WIS Rx J0 Octets 11-10**

Bit	Name	Access	Description	Default
15:8	RX_J0_octet_11	R/O	Contains octet 11 of the received Section Trace Message.	0x00
7:0	RX_J0_octet_10	R/O	Contains octet 10 of the received Section Trace Message.	0x00

2.9.6.7 WIS Rx J0 Octets 13-12

Short Name:WIS_Rx_J0_Octets_13_12

Address:0x2004E

Table 715 • **WIS Rx J0 Octets 13-12**

Bit	Name	Access	Description	Default
15:8	RX_J0_octet_13	R/O	Contains octet 13 of the received Section Trace Message.	0x00
7:0	RX_J0_octet_12	R/O	Contains octet 12 of the received Section Trace Message.	0x00

2.9.6.8 WIS Rx J0 Octets 15-14

Short Name:WIS_Rx_J0_Octets_15_14

Address:0x2004F

Table 716 • **WIS Rx J0 Octets 15-14**

Bit	Name	Access	Description	Default
15:8	RX_J0_octet_15	R/O	Contains octet 15 of the received Section Trace Message.	0x00
7:0	RX_J0_octet_14	R/O	Contains octet 14 of the received Section Trace Message.	0x00

2.9.7 E-WIS Configuration

2.9.7.1 E-WIS Tx Control 1

Short Name:EWIS_TXCTRL1

Address:0x2E5FF

Table 717 • **WIS Tx Control 1**

Bit	Name	Access	Description	Default
0	TX_SS	R/W	Contents of SS bits in transmitted H1 overhead bytes 2-192. (State of SS bits in the first H1 byte is determined by EWIS_TX_C2_H1.TX_H1.) 0 = SS bits set to 2'b00. 1 = SS bits set to 2'b10.	0x0

2.9.7.2 E-WIS Tx Control 2

Short Name:EWIS_TXCTRL2

Address:0x2E600

Table 718 • **WIS Tx Control 2**

Bit	Name	Access	Description	Default
15	REIL_TXBLK_MODE	R/W	Selects use of B2 block error count or bit error count mode to generate the M0/M1 bytes for REI-L back reporting 0 = Bit error mode 1 = Block error mode	0x0

Table 718 • **WIS Tx Control 2 *(continued)***

Bit	Name	Access	Description	Default
14	REIP_TXBLK_MODE	R/W	Selects use of B3 block error count or bit error count mode to generate the G1 byte for REI-P back reporting 0 = Bit error mode 1 = Block error mode	0x0
12	SCR	R/W	Enable transmit WIS scrambler 0 = Disable 1 = Enable	0x1
11	FRC_TX_TIMP	R/W	Force transmission of a TIM-P condition within the G1 byte 0 = Normal operation. 1 = Force TIM-P	0x0
10	ERDI_TX_MODE	R/W	Selects ERDI as the transmit WIS G1 byte mode 0 = RDI mode 1 = ERDI mode	0x1
9	SDH_TX_MODE	R/W	Selects the format of the WIS frame structure 0 = SONET mode 1 = SDH mode	0x1
8	TX_CLEAR_B	R/W	WIS transmit clear B	0x0
7:4	SQ_WV_PW	R/W	Select the transmit WIS square wave test pattern length 0000 - 0011: Invalid 0100: 4 zeros and 4 ones 0101: 5 zeros and 5 ones 0110: 6 zeros and 6 ones 0111: 7 zeros and 7 ones 1000: 8 zeros and 8 ones 1001: 9 zeros and 9 ones 1010: 10 zeros and 10 ones 1011: 11 zeros and 11 ones 1100 - 1111: Invalid	0x4
3	TX_PERF_MON	R/W	Performance monitor 0 = Normal operation. 1 = Disable AIS-L	0x0
2	FRC_TX_RDI	R/W	Force transmission of RDI-L in the K2 byte 0 = Normal operation. 1 = Force RDI-L	0x0
1	FRC_TX_AISL	R/W	Force transmission of AIS-L in the K2 byte. AIS-L will take precedence over RDI-L if both are asserted. 0 = Normal operation. 1 = Force AIS-L	0x0

2.9.7.3 LOOP_H4_FIFO_STAT

Short Name:LOOP_H4_FIFO_STAT

Address:0x2E606

Table 719 • **LOOP_H4_FIFO_STAT**

Bit	Name	Access	Description	Default
1	Loop_H4_FIFO_Overflow	R/O	Loopback H4 FIFO overflow status. This is a sticky bit that latches the high state. The latch-high bit is cleared when the register is read. 0 = normal operation 1 = over/under flow condition	0x0
0	Loop_H4_FIFO_Sync_Inhibit	R/W	Selects whether FIFO's sync inhibit feature is enabled 0 = Disabled 1 = Enabled	0x0

2.9.7.4 E-WIS Tx A1/A2 Octets

Short Name:EWIS_TX_A1_A2

Address:0x2E611

Table 720 • **E-WIS Tx A1/A2 Octets**

Bit	Name	Access	Description	Default
15:8	TX_A1	R/W	A1 byte to be transmitted when the TOSI data is inactive.	0xF6
7:0	TX_A2	R/W	A2 byte to be transmitted when the TOSI data is inactive.	0x28

2.9.7.5 E-WIS Tx Z0/E1 Octets

Short Name:EWIS_TX_Z0_E1

Address:0x2E612

Table 721 • **E-WIS Tx Z0/E1 Octets**

Bit	Name	Access	Description	Default
15:8	TX_Z0	R/W	Z0 byte to be transmitted when the TOSI data is inactive	0xCC
7:0	TX_E1	R/W	E1 byte to be transmitted when the TOSI data is inactive	0x00

2.9.7.6 E-WIS Tx F1/D1 Octets

Short Name:EWIS_TX_F1_D1

Address:0x2E613

Table 722 • **E-WIS Tx F1/D1 Octets**

Bit	Name	Access	Description	Default
15:8	TX_F1	R/W	F1 byte to be transmitted when the TOSI data is inactive	0x00
7:0	TX_D1	R/W	D1 byte to be transmitted when the TOSI data is inactive	0x00

2.9.7.7 E-WIS Tx D2/D3 Octets

Short Name:EWIS_TX_D2_D3

Address:0x2E614

Table 723 • **E-WIS Tx D2/D3 Octets**

Bit	Name	Access	Description	Default
15:8	TX_D2	R/W	D2 byte to be transmitted when the TOSI data is inactive	0x00
7:0	TX_D3	R/W	D3 byte to be transmitted when the TOSI data is inactive	0x00

2.9.7.8 E-WIS Tx C2/H1 Octets

Short Name:EWIS_TX_C2_H1

Address:0x2E615

Table 724 • **E-WIS Tx C2/H1 Octets**

Bit	Name	Access	Description	Default
15:8	TX_C2	R/W	C2 byte to be transmitted	0x1A
7:0	TX_H1	R/W	H1 byte to be transmitted	0x62

2.9.7.9 E-WIS Tx H2/H3 Octets

Short Name:EWIS_TX_H2_H3

Address:0x2E616

Table 725 • **E-WIS Tx H2/H3 Octets**

Bit	Name	Access	Description	Default
15:8	TX_H2	R/W	H2 byte to be transmitted when the TOSI data is inactive	0x0A
7:0	TX_H3	R/W	H3 byte to be transmitted when the TOSI data is inactive	0x00

2.9.7.10 E-WIS Tx G1/K1 Octets

Short Name:EWIS_TX_G1_K1

Address:0x2E617

Table 726 • **E-WIS Tx G1/K1 Octets**

Bit	Name	Access	Description	Default
15:8	TX_G1	R/W	G1 byte to be transmitted when the TOSI data is inactive	0x00
7:0	TX_K1	R/W	K1 byte to be transmitted when the TOSI data is inactive	0x00

2.9.7.11 E-WIS Tx K2/F2 Octets

Short Name:EWIS_TX_K2_F2

Address:0x2E618

Table 727 • **E-WIS Tx K2/F2 Octets**

Bit	Name	Access	Description	Default
15:8	TX_K2	R/W	K2 byte to be transmitted when the TOSI data is inactive	0x00
7:0	TX_F2	R/W	F2 byte to be transmitted	0x00

2.9.7.12 E-WIS Tx D4/D5 Octets

Short Name:EWIS_TX_D4_D5

Address:0x2E619

Table 728 • **E-WIS Tx D4/D5 Octets**

Bit	Name	Access	Description	Default
15:8	TX_D4	R/W	D4 byte to be transmitted when the TOSI data is inactive	0x00
7:0	TX_D5	R/W	D5 byte to be transmitted when the TOSI data is inactive	0x00

2.9.7.13 E-WIS Tx D6/H4 Octets

Short Name:EWIS_TX_D6_H4

Address:0x2E61A

Table 729 • **E-WIS Tx D6/H4 Octets**

Bit	Name	Access	Description	Default
15:8	TX_D6	R/W	D6 byte to be transmitted when the TOSI data is inactive	0x00
7:0	TX_H4	R/W	H4 byte to be transmitted	0x00

2.9.7.14 E-WIS Tx D7/D8 Octets

Short Name:EWIS_TX_D7_D8

Address:0x2E61B

Table 730 • **E-WIS Tx D7/D8 Octets**

Bit	Name	Access	Description	Default
15:8	TX_D7	R/W	D7 byte to be transmitted when the TOSI data is inactive	0x00
7:0	TX_D8	R/W	D8 byte to be transmitted when the TOSI data is inactive	0x00

2.9.7.15 E-WIS Tx D9/Z3 Octets

Short Name:EWIS_TX_D9_Z3

Address:0x2E61C

Table 731 • **E-WIS Tx D9/Z3 Octets**

Bit	Name	Access	Description	Default
15:8	TX_D9	R/W	D9 byte to be transmitted when the TOSI data is inactive	0x00
7:0	TX_Z3	R/W	Z3 byte to be transmitted	0x00

2.9.7.16 E-WIS Tx D10/D11 Octets

Short Name:EWIS_TX_D10_D11

Address:0x2E61D

Table 732 • **E-WIS Tx D10/D11 Octets**

Bit	Name	Access	Description	Default
15:8	TX_D10	R/W	D10 byte to be transmitted when the TOSI data is inactive	0x00
7:0	TX_D11	R/W	D11 byte to be transmitted when the TOSI data is inactive	0x00

2.9.7.17 E-WIS Tx D12/Z4 Octets

Short Name:EWIS_TX_D12_Z4

Address:0x2E61E

Table 733 • **E-WIS Tx D12/Z4 Octets**

Bit	Name	Access	Description	Default
15:8	TX_D12	R/W	D12 byte to be transmitted when the TOSI data is inactive	0x00
7:0	TX_Z4	R/W	Z4 byte to be transmitted	0x00

2.9.7.18 E-WIS Tx S1/Z1 Octets

Short Name:EWIS_TX_S1_Z1

Address:0x2E61F

Table 734 • **E-WIS Tx S1/Z1 Octets**

Bit	Name	Access	Description	Default
15:8	TX_S1	R/W	S1 byte to be transmitted when the TOSI data is inactive	0x0F
7:0	TX_Z1	R/W	Z1 byte to be transmitted when the TOSI data is inactive	0x00

2.9.7.19 E-WIS Tx Z2/E2 Octets

Short Name:EWIS_TX_Z2_E2

Address:0x2E620

Table 735 • **E-WIS Tx Z2/E2 Octets**

Bit	Name	Access	Description	Default
15:8	TX_Z2	R/W	Z2 byte to be transmitted when the TOSI data is inactive	0x00
7:0	TX_E2	R/W	E2 byte to be transmitted when the TOSI data is inactive	0x00

2.9.7.20 E-WIS Tx N1 Octet

Short Name:EWIS_TX_N1

Address:0x2E621

Table 736 • **E-WIS Tx N1 Octet**

Bit	Name	Access	Description	Default
15:8	TX_N1	R/W	N1 byte to be transmitted	0x00

2.9.7.21 E-WIS Tx Trace Message Length Control

Short Name:EWIS_TX_MSGLEN

Address:0x2E700

Table 737 • **E-WIS Tx Trace Message Length Control**

Bit	Name	Access	Description	Default
3:2	J0_TXLEN	R/W	Selects length of transmitted section trace message (J0). Trace length: 00: 16 bytes 01: 64 bytes 10: 1 byte 11: 1 byte	0x0
1:0	J1_TXLEN	R/W	Selects length of transmitted path trace message (J1). Trace length: 00: 16 bytes 01: 64 bytes 10: 1 byte 11: 1 byte	0x0

2.9.8 Enhanced Tx Section Trace Message Octets

Transmitted section trace message octets 16 to 63 are used when a 64 byte section trace message is selected in EWIS_TX_MSGLEN.J0_TXLEN. Octet 0 is the first octet transmitted, octet 63 is the last octet. Octets 0 to 15 are located in registers WIS_Tx_J0_Octets_1_0 to WIS_Tx_J0_Octets_15_14.

2.9.8.1 E-WIS Tx J0 Octets 17-16

Short Name:EWIS_Tx_J0_Octets_17_16

Address:0x2E800

Table 738 • **E-WIS Tx J0 Octets 17-16**

Bit	Name	Access	Description	Default
15:8	TX_J0_octet_17	R/W	Contains octet 17 of the transmitted Section Trace Message.	0x00
7:0	TX_J0_octet_16	R/W	Contains octet 16 of the transmitted Section Trace Message.	0x00

2.9.8.2 E-WIS Tx J0 Octets 19-18

Short Name:EWIS_Tx_J0_Octets_19_18

Address:0x2E801

Table 739 • **E-WIS Tx J0 Octets 19-18**

Bit	Name	Access	Description	Default
15:8	TX_J0_octet_19	R/W	Contains octet 19 of the transmitted Section Trace Message.	0x00
7:0	TX_J0_octet_18	R/W	Contains octet 18 of the transmitted Section Trace Message.	0x00

2.9.8.3 E-WIS Tx J0 Octets 21-20

Short Name:EWIS_Tx_J0_Octets_21_20

Address:0x2E802

Table 740 • **E-WIS Tx J0 Octets 21-20**

Bit	Name	Access	Description	Default
15:8	TX_J0_octet_21	R/W	Contains octet 21 of the transmitted Section Trace Message.	0x00
7:0	TX_J0_octet_20	R/W	Contains octet 20 of the transmitted Section Trace Message.	0x00

2.9.8.4 E-WIS Tx J0 Octets 23-22

Short Name:EWIS_Tx_J0_Octets_23_22

Address:0x2E803

Table 741 • **E-WIS Tx J0 Octets 23-22**

Bit	Name	Access	Description	Default
15:8	TX_J0_octet_23	R/W	Contains octet 23 of the transmitted Section Trace Message.	0x00
7:0	TX_J0_octet_22	R/W	Contains octet 22 of the transmitted Section Trace Message.	0x00

2.9.8.5 E-WIS Tx J0 Octets 25-24

Short Name:EWIS_Tx_J0_Octets_25_24

Address:0x2E804

Table 742 • **E-WIS Tx J0 Octets 25-24**

Bit	Name	Access	Description	Default
15:8	TX_J0_octet_25	R/W	Contains octet 25 of the transmitted Section Trace Message.	0x00
7:0	TX_J0_octet_24	R/W	Contains octet 24 of the transmitted Section Trace Message.	0x00

2.9.8.6 E-WIS Tx J0 Octets 27-26

Short Name:EWIS_Tx_J0_Octets_27_26

Address:0x2E805

Table 743 • **E-WIS Tx J0 Octets 27-26**

Bit	Name	Access	Description	Default
15:8	TX_J0_octet_27	R/W	Contains octet 27 of the transmitted Section Trace Message.	0x00
7:0	TX_J0_octet_26	R/W	Contains octet 26 of the transmitted Section Trace Message.	0x00

2.9.8.7 E-WIS Tx J0 Octets 29-28

Short Name:EWIS_Tx_J0_Octets_29_28

Address:0x2E806

Table 744 • **E-WIS Tx J0 Octets 29-28**

Bit	Name	Access	Description	Default
15:8	TX_J0_octet_29	R/W	Contains octet 29 of the transmitted Section Trace Message.	0x00
7:0	TX_J0_octet_28	R/W	Contains octet 28 of the transmitted Section Trace Message.	0x00

2.9.8.8 E-WIS Tx J0 Octets 31-30

Short Name:EWIS_Tx_J0_Octets_31_30

Address:0x2E807

Table 745 • **E-WIS Tx J0 Octets 31-30**

Bit	Name	Access	Description	Default
15:8	TX_J0_octet_31	R/W	Contains octet 31 of the transmitted Section Trace Message.	0x00
7:0	TX_J0_octet_30	R/W	Contains octet 30 of the transmitted Section Trace Message.	0x00

2.9.8.9 E-WIS Tx J0 Octets 33-32

Short Name:EWIS_Tx_J0_Octets_33_32

Address:0x2E808

Table 746 • **E-WIS Tx J0 Octets 33-32**

Bit	Name	Access	Description	Default
15:8	TX_J0_octet_33	R/W	Contains octet 33 of the transmitted Section Trace Message.	0x00
7:0	TX_J0_octet_32	R/W	Contains octet 32 of the transmitted Section Trace Message.	0x00

2.9.8.10 E-WIS Tx J0 Octets 35-34

Short Name:EWIS_Tx_J0_Octets_35_34

Address:0x2E809

Table 747 • **E-WIS Tx J0 Octets 35-34**

Bit	Name	Access	Description	Default
15:8	TX_J0_octet_35	R/W	Contains octet 35 of the transmitted Section Trace Message.	0x00
7:0	TX_J0_octet_34	R/W	Contains octet 34 of the transmitted Section Trace Message.	0x00

2.9.8.11 E-WIS Tx J0 Octets 37-36

Short Name:EWIS_Tx_J0_Octets_37_36

Address:0x2E80A

Table 748 • **E-WIS Tx J0 Octets 37-36**

Bit	Name	Access	Description	Default
15:8	TX_J0_octet_37	R/W	Contains octet 37 of the transmitted Section Trace Message.	0x00
7:0	TX_J0_octet_36	R/W	Contains octet 36 of the transmitted Section Trace Message.	0x00

2.9.8.12 E-WIS Tx J0 Octets 39-38

Short Name:EWIS_Tx_J0_Octets_39_38

Address:0x2E80B

Table 749 • **E-WIS Tx J0 Octets 39-38**

Bit	Name	Access	Description	Default
15:8	TX_J0_octet_39	R/W	Contains octet 39 of the transmitted Section Trace Message.	0x00
7:0	TX_J0_octet_38	R/W	Contains octet 38 of the transmitted Section Trace Message.	0x00

2.9.8.13 E-WIS Tx J0 Octets 41-40

Short Name:EWIS_Tx_J0_Octets_41_40

Address:0x2E80C

Table 750 • **E-WIS Tx J0 Octets 41-40**

Bit	Name	Access	Description	Default
15:8	TX_J0_octet_41	R/W	Contains octet 41 of the transmitted Section Trace Message.	0x00
7:0	TX_J0_octet_40	R/W	Contains octet 40 of the transmitted Section Trace Message.	0x00

2.9.8.14 E-WIS Tx J0 Octets 43-42

Short Name:EWIS_Tx_J0_Octets_43_42

Address:0x2E80D

Table 751 • **E-WIS Tx J0 Octets 43-42**

Bit	Name	Access	Description	Default
15:8	TX_J0_octet_43	R/W	Contains octet 43 of the transmitted Section Trace Message.	0x00
7:0	TX_J0_octet_42	R/W	Contains octet 42 of the transmitted Section Trace Message.	0x00

2.9.8.15 E-WIS Tx J0 Octets 45-44

Short Name:EWIS_Tx_J0_Octets_45_44

Address:0x2E80E

Table 752 • **E-WIS Tx J0 Octets 45-44**

Bit	Name	Access	Description	Default
15:8	TX_J0_octet_45	R/W	Contains octet 45 of the transmitted Section Trace Message.	0x00
7:0	TX_J0_octet_44	R/W	Contains octet 44 of the transmitted Section Trace Message.	0x00

2.9.8.16 E-WIS Tx J0 Octets 47-46

Short Name:EWIS_Tx_J0_Octets_47_46

Address:0x2E80F

Table 753 • **E-WIS Tx J0 Octets 47-46**

Bit	Name	Access	Description	Default
15:8	TX_J0_octet_47	R/W	Contains octet 47 of the transmitted Section Trace Message.	0x00
7:0	TX_J0_octet_46	R/W	Contains octet 46 of the transmitted Section Trace Message.	0x00

2.9.8.17 E-WIS Tx J0 Octets 49-48

Short Name:EWIS_Tx_J0_Octets_49_48

Address:0x2E810

Table 754 • **E-WIS Tx J0 Octets 49-48**

Bit	Name	Access	Description	Default
15:8	TX_J0_octet_49	R/W	Contains octet 49 of the transmitted Section Trace Message.	0x00
7:0	TX_J0_octet_48	R/W	Contains octet 48 of the transmitted Section Trace Message.	0x00

2.9.8.18 E-WIS Tx J0 Octets 51-50

Short Name:EWIS_Tx_J0_Octets_51_50

Address:0x2E811

Table 755 • **E-WIS Tx J0 Octets 51-50**

Bit	Name	Access	Description	Default
15:8	TX_J0_octet_51	R/W	Contains octet 51 of the transmitted Section Trace Message.	0x00
7:0	TX_J0_octet_50	R/W	Contains octet 50 of the transmitted Section Trace Message.	0x00

2.9.8.19 E-WIS Tx J0 Octets 53-52

Short Name:EWIS_Tx_J0_Octets_53_52

Address:0x2E812

Table 756 • **E-WIS Tx J0 Octets 53-52**

Bit	Name	Access	Description	Default
15:8	TX_J0_octet_53	R/W	Contains octet 53 of the transmitted Section Trace Message.	0x00
7:0	TX_J0_octet_52	R/W	Contains octet 52 of the transmitted Section Trace Message.	0x00

2.9.8.20 E-WIS Tx J0 Octets 55-54

Short Name:EWIS_Tx_J0_Octets_55_54

Address:0x2E813

Table 757 • **E-WIS Tx J0 Octets 55-54**

Bit	Name	Access	Description	Default
15:8	TX_J0_octet_55	R/W	Contains octet 55 of the transmitted Section Trace Message.	0x00
7:0	TX_J0_octet_54	R/W	Contains octet 54 of the transmitted Section Trace Message.	0x00

2.9.8.21 E-WIS Tx J0 Octets 57-56

Short Name:EWIS_Tx_J0_Octets_57_56

Address:0x2E814

Table 758 • **E-WIS Tx J0 Octets 57-56**

Bit	Name	Access	Description	Default
15:8	TX_J0_octet_57	R/W	Contains octet 57 of the transmitted Section Trace Message.	0x00
7:0	TX_J0_octet_56	R/W	Contains octet 56 of the transmitted Section Trace Message.	0x00

2.9.8.22 E-WIS Tx J0 Octets 59-58

Short Name:EWIS_Tx_J0_Octets_59_58

Address:0x2E815

Table 759 • **E-WIS Tx J0 Octets 59-58**

Bit	Name	Access	Description	Default
15:8	TX_J0_octet_59	R/W	Contains octet 59 of the transmitted Section Trace Message.	0x00
7:0	TX_J0_octet_58	R/W	Contains octet 58 of the transmitted Section Trace Message.	0x00

2.9.8.23 E-WIS Tx J0 Octets 61-60

Short Name:EWIS_Tx_J0_Octets_61_60

Address:0x2E816

Table 760 • **E-WIS Tx J0 Octets 61-60**

Bit	Name	Access	Description	Default
15:8	TX_J0_octet_61	R/W	Contains octet 61 of the transmitted Section Trace Message.	0x00
7:0	TX_J0_octet_60	R/W	Contains octet 60 of the transmitted Section Trace Message.	0x00

2.9.8.24 E-WIS Tx J0 Octets 63-62

Short Name:EWIS_Tx_J0_Octets_63_62

Address:0x2E817

Table 761 • **E-WIS Tx J0 Octets 63-62**

Bit	Name	Access	Description	Default
15:8	TX_J0_octet_63	R/W	Contains octet 63 of the transmitted Section Trace Message.	0x00
7:0	TX_J0_octet_62	R/W	Contains octet 62 of the transmitted Section Trace Message.	0x00

2.9.9 Enhanced Rx Section Trace Message Octets

Received section trace message octets 16 to 63 are used when a 64 byte section trace message is selected in EWIS_RX_MSGLEN.J0_RX_LEN. Octet 0 is the first octet received, octet 63 is the last octet. Octets 0 to 15 are located in registers WIS_Rx_J0_Octets_3_2 to WIS_Rx_J0_Octets_15_14.

2.9.9.1 E-WIS Rx J0 Octets 17-16

Short Name:EWIS_Rx_J0_Octets_17_16

Address:0x2E900

Table 762 • **E-WIS Rx J0 Octets 17-16**

Bit	Name	Access	Description	Default
15:8	RX_J0_octet_17	R/O	Contains octet 17 of the received Section Trace Message.	0x00
7:0	RX_J0_octet_16	R/O	Contains octet 16 of the received Section Trace Message.	0x00

2.9.9.2 E-WIS Rx J0 Octets 19-18

Short Name:EWIS_Rx_J0_Octets_19_18

Address:0x2E901

Table 763 • **E-WIS Rx J0 Octets 19-18**

Bit	Name	Access	Description	Default
15:8	RX_J0_octet_19	R/O	Contains octet 19 of the received Section Trace Message.	0x00
7:0	RX_J0_octet_18	R/O	Contains octet 18 of the received Section Trace Message.	0x00

2.9.9.3 E-WIS Rx J0 Octets 21-20

Short Name:EWIS_Rx_J0_Octets_21_20

Address:0x2E902

Table 764 • **E-WIS Rx J0 Octets 21-20**

Bit	Name	Access	Description	Default
15:8	RX_J0_octet_21	R/O	Contains octet 21 of the received Section Trace Message.	0x00
7:0	RX_J0_octet_20	R/O	Contains octet 20 of the received Section Trace Message.	0x00

2.9.9.4 E-WIS Rx J0 Octets 23-22

Short Name:EWIS_Rx_J0_Octets_23_22

Address:0x2E903

Table 765 • **E-WIS Rx J0 Octets 23-22**

Bit	Name	Access	Description	Default
15:8	RX_J0_octet_23	R/O	Contains octet 23 of the received Section Trace Message.	0x00
7:0	RX_J0_octet_22	R/O	Contains octet 22 of the received Section Trace Message.	0x00

2.9.9.5 E-WIS Rx J0 Octets 25-24

Short Name:EWIS_Rx_J0_Octets_25_24

Address:0x2E904

Table 766 • **E-WIS Rx J0 Octets 25-24**

Bit	Name	Access	Description	Default
15:8	RX_J0_octet_25	R/O	Contains octet 25 of the received Section Trace Message.	0x00
7:0	RX_J0_octet_24	R/O	Contains octet 24 of the received Section Trace Message.	0x00

2.9.9.6 E-WIS Rx J0 Octets 27-26

Short Name:EWIS_Rx_J0_Octets_27_26

Address:0x2E905

Table 767 • **E-WIS Rx J0 Octets 27-26**

Bit	Name	Access	Description	Default
15:8	RX_J0_octet_27	R/O	Contains octet 27 of the received Section Trace Message.	0x00
7:0	RX_J0_octet_26	R/O	Contains octet 26 of the received Section Trace Message.	0x00

2.9.9.7 E-WIS Rx J0 Octets 29-28

Short Name:EWIS_Rx_J0_Octets_29_28

Address:0x2E906

Table 768 • **E-WIS Rx J0 Octets 29-28**

Bit	Name	Access	Description	Default
15:8	RX_J0_octet_29	R/O	Contains octet 29 of the received Section Trace Message.	0x00
7:0	RX_J0_octet_28	R/O	Contains octet 28 of the received Section Trace Message.	0x00

2.9.9.8 E-WIS Rx J0 Octets 31-30

Short Name:EWIS_Rx_J0_Octets_31_30

Address:0x2E907

Table 769 • **E-WIS Rx J0 Octets 31-30**

Bit	Name	Access	Description	Default
15:8	RX_J0_octet_31	R/O	Contains octet 31 of the received Section Trace Message.	0x00
7:0	RX_J0_octet_30	R/O	Contains octet 30 of the received Section Trace Message.	0x00

2.9.9.9 E-WIS Rx J0 Octets 33-32

Short Name:EWIS_Rx_J0_Octets_33_32

Address:0x2E908

Table 770 • **E-WIS Rx J0 Octets 33-32**

Bit	Name	Access	Description	Default
15:8	RX_J0_octet_33	R/O	Contains octet 33 of the received Section Trace Message.	0x00
7:0	RX_J0_octet_32	R/O	Contains octet 32 of the received Section Trace Message.	0x00

2.9.9.10 E-WIS Rx J0 Octets 35-34

Short Name:EWIS_Rx_J0_Octets_35_34

Address:0x2E909

Table 771 • **E-WIS Rx J0 Octets 35-34**

Bit	Name	Access	Description	Default
15:8	RX_J0_octet_35	R/O	Contains octet 35 of the received Section Trace Message.	0x00
7:0	RX_J0_octet_34	R/O	Contains octet 34 of the received Section Trace Message.	0x00

2.9.9.11 E-WIS Rx J0 Octets 37-36

Short Name:EWIS_Rx_J0_Octets_37_36

Address:0x2E90A

Table 772 • **E-WIS Rx J0 Octets 37-36**

Bit	Name	Access	Description	Default
15:8	RX_J0_octet_37	R/O	Contains octet 37 of the received Section Trace Message.	0x00
7:0	RX_J0_octet_36	R/O	Contains octet 36 of the received Section Trace Message.	0x00

2.9.9.12 E-WIS Rx J0 Octets 39-38

Short Name:EWIS_Rx_J0_Octets_39_38

Address:0x2E90B

Table 773 • **E-WIS Rx J0 Octets 39-38**

Bit	Name	Access	Description	Default
15:8	RX_J0_octet_39	R/O	Contains octet 39 of the received Section Trace Message.	0x00
7:0	RX_J0_octet_38	R/O	Contains octet 38 of the received Section Trace Message.	0x00

2.9.9.13 E-WIS Rx J0 Octets 41-40

Short Name:EWIS_Rx_J0_Octets_41_40

Address:0x2E90C

Table 774 • **E-WIS Rx J0 Octets 41-40**

Bit	Name	Access	Description	Default
15:8	RX_J0_octet_41	R/O	Contains octet 41 of the received Section Trace Message.	0x00
7:0	RX_J0_octet_40	R/O	Contains octet 40 of the received Section Trace Message.	0x00

2.9.9.14 E-WIS Rx J0 Octets 43-42

Short Name:EWIS_Rx_J0_Octets_43_42

Address:0x2E90D

Table 775 • **E-WIS Rx J0 Octets 43-42**

Bit	Name	Access	Description	Default
15:8	RX_J0_octet_43	R/O	Contains octet 43 of the received Section Trace Message.	0x00
7:0	RX_J0_octet_42	R/O	Contains octet 42 of the received Section Trace Message.	0x00

2.9.9.15 E-WIS Rx J0 Octets 45-44

Short Name:EWIS_Rx_J0_Octets_45_44

Address:0x2E90E

Table 776 • **E-WIS Rx J0 Octets 45-44**

Bit	Name	Access	Description	Default
15:8	RX_J0_octet_45	R/O	Contains octet 45 of the received Section Trace Message.	0x00
7:0	RX_J0_octet_44	R/O	Contains octet 44 of the received Section Trace Message.	0x00

2.9.9.16 E-WIS Rx J0 Octets 47-46

Short Name:EWIS_Rx_J0_Octets_47_46

Address:0x2E90F

Table 777 • **E-WIS Rx J0 Octets 47-46**

Bit	Name	Access	Description	Default
15:8	RX_J0_octet_47	R/O	Contains octet 47 of the received Section Trace Message.	0x00
7:0	RX_J0_octet_46	R/O	Contains octet 46 of the received Section Trace Message.	0x00

2.9.9.17 E-WIS Rx J0 Octets 49-48

Short Name:EWIS_Rx_J0_Octets_49_48

Address:0x2E910

Table 778 • **E-WIS Rx J0 Octets 49-48**

Bit	Name	Access	Description	Default
15:8	RX_J0_octet_49	R/O	Contains octet 49 of the received Section Trace Message.	0x00
7:0	RX_J0_octet_48	R/O	Contains octet 48 of the received Section Trace Message.	0x00

2.9.9.18 E-WIS Rx J0 Octets 51-50

Short Name:EWIS_Rx_J0_Octets_51_50

Address:0x2E911

Table 779 • **E-WIS Rx J0 Octets 51-50**

Bit	Name	Access	Description	Default
15:8	RX_J0_octet_51	R/O	Contains octet 51 of the received Section Trace Message.	0x00
7:0	RX_J0_octet_50	R/O	Contains octet 50 of the received Section Trace Message.	0x00

2.9.9.19 E-WIS Rx J0 Octets 53-52

Short Name:EWIS_Rx_J0_Octets_53_52

Address:0x2E912

Table 780 • **E-WIS Rx J0 Octets 53-52**

Bit	Name	Access	Description	Default
15:8	RX_J0_octet_53	R/O	Contains octet 53 of the received Section Trace Message.	0x00
7:0	RX_J0_octet_52	R/O	Contains octet 52 of the received Section Trace Message.	0x00

2.9.9.20 E-WIS Rx J0 Octets 55-54

Short Name:EWIS_Rx_J0_Octets_55_54

Address:0x2E913

Table 781 • **E-WIS Rx J0 Octets 55-54**

Bit	Name	Access	Description	Default
15:8	RX_J0_octet_55	R/O	Contains octet 55 of the received Section Trace Message.	0x00
7:0	RX_J0_octet_54	R/O	Contains octet 54 of the received Section Trace Message.	0x00

2.9.9.21 E-WIS Rx J0 Octets 57-56

Short Name:EWIS_Rx_J0_Octets_57_56

Address:0x2E914

Table 782 • **E-WIS Rx J0 Octets 57-56**

Bit	Name	Access	Description	Default
15:8	RX_J0_octet_57	R/O	Contains octet 57 of the received Section Trace Message.	0x00
7:0	RX_J0_octet_56	R/O	Contains octet 56 of the received Section Trace Message.	0x00

2.9.9.22 E-WIS Rx J0 Octets 59-58

Short Name:EWIS_Rx_J0_Octets_59_58

Address:0x2E915

Table 783 • **E-WIS Rx J0 Octets 59-58**

Bit	Name	Access	Description	Default
15:8	RX_J0_octet_59	R/O	Contains octet 59 of the received Section Trace Message.	0x00
7:0	RX_J0_octet_58	R/O	Contains octet 58 of the received Section Trace Message.	0x00

2.9.9.23 E-WIS Rx J0 Octets 61-60

Short Name:EWIS_Rx_J0_Octets_61_60

Address:0x2E916

Table 784 • **E-WIS Rx J0 Octets 61-60**

Bit	Name	Access	Description	Default
15:8	RX_J0_octet_61	R/O	Contains octet 61 of the received Section Trace Message.	0x00
7:0	RX_J0_octet_60	R/O	Contains octet 60 of the received Section Trace Message.	0x00

2.9.9.24 E-WIS Rx J0 Octets 63-62

Short Name:EWIS_Rx_J0_Octets_63_62

Address:0x2E917

Table 785 • **E-WIS Rx J0 Octets 63-62**

Bit	Name	Access	Description	Default
15:8	RX_J0_octet_63	R/O	Contains octet 63 of the received Section Trace Message.	0x00
7:0	RX_J0_octet_62	R/O	Contains octet 62 of the received Section Trace Message.	0x00

2.9.10 Enhanced Tx Path Trace Message Octets

Transmitted path trace message octets 16 to 63 are used when a 64 byte path trace message is selected in EWIS_TX_MSGLEN.J1_TXLEN. Octet 0 is the first octet transmitted, octet 63 is the last octet. Octets 0 to 15 are located in registers WIS_Tx_J1_Octets_1_0 to WIS_Tx_J1_Octets_15_14.

2.9.10.1 E-WIS Tx J1 Octets 17-16

Short Name:EWIS_Tx_J1_Octets_17_16

Address:0x2EA00

Table 786 • **E-WIS Tx J1 Octets 17-16**

Bit	Name	Access	Description	Default
15:8	TX_J1_octet_17	R/W	Contains octet 17 of the transmitted Section Trace Message.	0x00
7:0	TX_J1_octet_16	R/W	Contains octet 16 of the transmitted Section Trace Message.	0x00

2.9.10.2 E-WIS Tx J1 Octets 19-18

Short Name:EWIS_Tx_J1_Octets_19_18

Address:0x2EA01

Table 787 • **E-WIS Tx J1 Octets 19-18**

Bit	Name	Access	Description	Default
15:8	TX_J1_octet_19	R/W	Contains octet 19 of the transmitted Section Trace Message.	0x00
7:0	TX_J1_octet_18	R/W	Contains octet 18 of the transmitted Section Trace Message.	0x00

2.9.10.3 E-WIS Tx J1 Octets 21-20

Short Name:EWIS_Tx_J1_Octets_21_20

Address:0x2EA02

Table 788 • **E-WIS Tx J1 Octets 21-20**

Bit	Name	Access	Description	Default
15:8	TX_J1_octet_21	R/W	Contains octet 21 of the transmitted Section Trace Message.	0x00
7:0	TX_J1_octet_20	R/W	Contains octet 20 of the transmitted Section Trace Message.	0x00

2.9.10.4 E-WIS Tx J1 Octets 23-22

Short Name:EWIS_Tx_J1_Octets_23_22

Address:0x2EA03

Table 789 • **E-WIS Tx J1 Octets 23-22**

Bit	Name	Access	Description	Default
15:8	TX_J1_octet_23	R/W	Contains octet 23 of the transmitted Section Trace Message.	0x00
7:0	TX_J1_octet_22	R/W	Contains octet 22 of the transmitted Section Trace Message.	0x00

2.9.10.5 E-WIS Tx J1 Octets 25-24

Short Name:EWIS_Tx_J1_Octets_25_24

Address:0x2EA04

Table 790 • **E-WIS Tx J1 Octets 25-24**

Bit	Name	Access	Description	Default
15:8	TX_J1_octet_25	R/W	Contains octet 25 of the transmitted Section Trace Message.	0x00
7:0	TX_J1_octet_24	R/W	Contains octet 24 of the transmitted Section Trace Message.	0x00

2.9.10.6 E-WIS Tx J1 Octets 27-26

Short Name:EWIS_Tx_J1_Octets_27_26

Address:0x2EA05

Table 791 • **E-WIS Tx J1 Octets 27-26**

Bit	Name	Access	Description	Default
15:8	TX_J1_octet_27	R/W	Contains octet 27 of the transmitted Section Trace Message.	0x00
7:0	TX_J1_octet_26	R/W	Contains octet 26 of the transmitted Section Trace Message.	0x00

2.9.10.7 E-WIS Tx J1 Octets 29-28

Short Name:EWIS_Tx_J1_Octets_29_28

Address:0x2EA06

Table 792 • **E-WIS Tx J1 Octets 29-28**

Bit	Name	Access	Description	Default
15:8	TX_J1_octet_29	R/W	Contains octet 29 of the transmitted Section Trace Message.	0x00
7:0	TX_J1_octet_28	R/W	Contains octet 28 of the transmitted Section Trace Message.	0x00

2.9.10.8 E-WIS Tx J1 Octets 31-30

Short Name:EWIS_Tx_J1_Octets_31_30

Address:0x2EA07

Table 793 • **E-WIS Tx J1 Octets 31-30**

Bit	Name	Access	Description	Default
15:8	TX_J1_octet_31	R/W	Contains octet 31 of the transmitted Section Trace Message.	0x00
7:0	TX_J1_octet_30	R/W	Contains octet 30 of the transmitted Section Trace Message.	0x00

2.9.10.9 E-WIS Tx J1 Octets 33-32

Short Name:EWIS_Tx_J1_Octets_33_32

Address:0x2EA08

Table 794 • **E-WIS Tx J1 Octets 33-32**

Bit	Name	Access	Description	Default
15:8	TX_J1_octet_33	R/W	Contains octet 33 of the transmitted Section Trace Message.	0x00
7:0	TX_J1_octet_32	R/W	Contains octet 32 of the transmitted Section Trace Message.	0x00

2.9.10.10 E-WIS Tx J1 Octets 35-34

Short Name:EWIS_Tx_J1_Octets_35_34

Address:0x2EA09

Table 795 • **E-WIS Tx J1 Octets 35-34**

Bit	Name	Access	Description	Default
15:8	TX_J1_octet_35	R/W	Contains octet 35 of the transmitted Section Trace Message.	0x00
7:0	TX_J1_octet_34	R/W	Contains octet 34 of the transmitted Section Trace Message.	0x00

2.9.10.11 E-WIS Tx J1 Octets 37-36

Short Name:EWIS_Tx_J1_Octets_37_36

Address:0x2EA0A

Table 796 • **E-WIS Tx J1 Octets 37-36**

Bit	Name	Access	Description	Default
15:8	TX_J1_octet_37	R/W	Contains octet 37 of the transmitted Section Trace Message.	0x00
7:0	TX_J1_octet_36	R/W	Contains octet 36 of the transmitted Section Trace Message.	0x00

2.9.10.12 E-WIS Tx J1 Octets 39-38

Short Name:EWIS_Tx_J1_Octets_39_38

Address:0x2EA0B

Table 797 • **E-WIS Tx J1 Octets 39-38**

Bit	Name	Access	Description	Default
15:8	TX_J1_octet_39	R/W	Contains octet 39 of the transmitted Section Trace Message.	0x00
7:0	TX_J1_octet_38	R/W	Contains octet 38 of the transmitted Section Trace Message.	0x00

2.9.10.13 E-WIS Tx J1 Octets 41-40

Short Name:EWIS_Tx_J1_Octets_41_40

Address:0x2EA0C

Table 798 • **E-WIS Tx J1 Octets 41-40**

Bit	Name	Access	Description	Default
15:8	TX_J1_octet_41	R/W	Contains octet 41 of the transmitted Section Trace Message.	0x00
7:0	TX_J1_octet_40	R/W	Contains octet 40 of the transmitted Section Trace Message.	0x00

2.9.10.14 E-WIS Tx J1 Octets 43-42

Short Name:EWIS_Tx_J1_Octets_43_42

Address:0x2EA0D

Table 799 • **E-WIS Tx J1 Octets 43-42**

Bit	Name	Access	Description	Default
15:8	TX_J1_octet_43	R/W	Contains octet 43 of the transmitted Section Trace Message.	0x00
7:0	TX_J1_octet_42	R/W	Contains octet 42 of the transmitted Section Trace Message.	0x00

2.9.10.15 E-WIS Tx J1 Octets 45-44

Short Name:EWIS_Tx_J1_Octets_45_44

Address:0x2EA0E

Table 800 • **E-WIS Tx J1 Octets 45-44**

Bit	Name	Access	Description	Default
15:8	TX_J1_octet_45	R/W	Contains octet 45 of the transmitted Section Trace Message.	0x00
7:0	TX_J1_octet_44	R/W	Contains octet 44 of the transmitted Section Trace Message.	0x00

2.9.10.16 E-WIS Tx J1 Octets 47-46

Short Name:EWIS_Tx_J1_Octets_47_46

Address:0x2EA0F

Table 801 • **E-WIS Tx J1 Octets 47-46**

Bit	Name	Access	Description	Default
15:8	TX_J1_octet_47	R/W	Contains octet 47 of the transmitted Section Trace Message.	0x00
7:0	TX_J1_octet_46	R/W	Contains octet 46 of the transmitted Section Trace Message.	0x00

2.9.10.17 E-WIS Tx J1 Octets 49-48

Short Name:EWIS_Tx_J1_Octets_49_48

Address:0x2EA10

Table 802 • **E-WIS Tx J1 Octets 49-48**

Bit	Name	Access	Description	Default
15:8	TX_J1_octet_49	R/W	Contains octet 49 of the transmitted Section Trace Message.	0x00
7:0	TX_J1_octet_48	R/W	Contains octet 48 of the transmitted Section Trace Message.	0x00

2.9.10.18 E-WIS Tx J1 Octets 51-50

Short Name:EWIS_Tx_J1_Octets_51_50

Address:0x2EA11

Table 803 • **E-WIS Tx J1 Octets 51-50**

Bit	Name	Access	Description	Default
15:8	TX_J1_octet_51	R/W	Contains octet 51 of the transmitted Section Trace Message.	0x00
7:0	TX_J1_octet_50	R/W	Contains octet 50 of the transmitted Section Trace Message.	0x00

2.9.10.19 E-WIS Tx J1 Octets 53-52

Short Name:EWIS_Tx_J1_Octets_53_52

Address:0x2EA12

Table 804 • **E-WIS Tx J1 Octets 53-52**

Bit	Name	Access	Description	Default
15:8	TX_J1_octet_53	R/W	Contains octet 53 of the transmitted Section Trace Message.	0x00
7:0	TX_J1_octet_52	R/W	Contains octet 52 of the transmitted Section Trace Message.	0x00

2.9.10.20 E-WIS Tx J1 Octets 55-54

Short Name:EWIS_Tx_J1_Octets_55_54

Address:0x2EA13

Table 805 • **E-WIS Tx J1 Octets 55-54**

Bit	Name	Access	Description	Default
15:8	TX_J1_octet_55	R/W	Contains octet 55 of the transmitted Section Trace Message.	0x00
7:0	TX_J1_octet_54	R/W	Contains octet 54 of the transmitted Section Trace Message.	0x00

2.9.10.21 E-WIS Tx J1 Octets 57-56

Short Name:EWIS_Tx_J1_Octets_57_56

Address:0x2EA14

Table 806 • **E-WIS Tx J1 Octets 57-56**

Bit	Name	Access	Description	Default
15:8	TX_J1_octet_57	R/W	Contains octet 57 of the transmitted Section Trace Message.	0x00
7:0	TX_J1_octet_56	R/W	Contains octet 56 of the transmitted Section Trace Message.	0x00

2.9.10.22 E-WIS Tx J1 Octets 59-58

Short Name:EWIS_Tx_J1_Octets_59_58

Address:0x2EA15

Table 807 • **E-WIS Tx J1 Octets 59-58**

Bit	Name	Access	Description	Default
15:8	TX_J1_octet_59	R/W	Contains octet 59 of the transmitted Section Trace Message.	0x00
7:0	TX_J1_octet_58	R/W	Contains octet 58 of the transmitted Section Trace Message.	0x00

2.9.10.23 E-WIS Tx J1 Octets 61-60

Short Name:EWIS_Tx_J1_Octets_61_60

Address:0x2EA16

Table 808 • **E-WIS Tx J1 Octets 61-60**

Bit	Name	Access	Description	Default
15:8	TX_J1_octet_61	R/W	Contains octet 61 of the transmitted Section Trace Message.	0x00
7:0	TX_J1_octet_60	R/W	Contains octet 60 of the transmitted Section Trace Message.	0x00

2.9.10.24 E-WIS Tx J1 Octets 63-62

Short Name:EWIS_Tx_J1_Octets_63_62

Address:0x2EA17

Table 809 • **E-WIS Tx J1 Octets 63-62**

Bit	Name	Access	Description	Default
15:8	TX_J1_octet_63	R/W	Contains octet 63 of the transmitted Section Trace Message.	0x00
7:0	TX_J1_octet_62	R/W	Contains octet 62 of the transmitted Section Trace Message.	0x00

2.9.11 Enhanced Rx Path Trace Message Octets

Received path trace message octets 16 to 63 are used when a 64 byte path trace message is selected in EWIS_RX_MSGLEN.J1_RX_LEN. Octet 0 is the first octet received, octet 63 is the last octet. Octets 0 to 15 are located in registers WIS_Rx_J1_Octets_1_0 to WIS_Rx_J1_Octets_15_14.

2.9.11.1 E-WIS Rx J1 Octets 17-16

Short Name:EWIS_Rx_J1_Octets_17_16

Address:0x2EB00

Table 810 • **E-WIS Rx J1 Octets 17-16**

Bit	Name	Access	Description	Default
15:8	RX_J1_octet_17	R/O	Contains octet 17 of the received Section Trace Message.	0x00
7:0	RX_J1_octet_16	R/O	Contains octet 16 of the received Section Trace Message.	0x00

2.9.11.2 E-WIS Rx J1 Octets 19-18

Short Name:EWIS_Rx_J1_Octets_19_18

Address:0x2EB01

Table 811 • **E-WIS Rx J1 Octets 19-18**

Bit	Name	Access	Description	Default
15:8	RX_J1_octet_19	R/O	Contains octet 19 of the received Section Trace Message.	0x00
7:0	RX_J1_octet_18	R/O	Contains octet 18 of the received Section Trace Message.	0x00

2.9.11.3 E-WIS Rx J1 Octets 21-20

Short Name:EWIS_Rx_J1_Octets_21_20

Address:0x2EB02

Table 812 • **E-WIS Rx J1 Octets 21-20**

Bit	Name	Access	Description	Default
15:8	RX_J1_octet_21	R/O	Contains octet 21 of the received Section Trace Message.	0x00
7:0	RX_J1_octet_20	R/O	Contains octet 20 of the received Section Trace Message.	0x00

2.9.11.4 E-WIS Rx J1 Octets 23-22

Short Name:EWIS_Rx_J1_Octets_23_22

Address:0x2EB03

Table 813 • **E-WIS Rx J1 Octets 23-22**

Bit	Name	Access	Description	Default
15:8	RX_J1_octet_23	R/O	Contains octet 23 of the received Section Trace Message.	0x00
7:0	RX_J1_octet_22	R/O	Contains octet 22 of the received Section Trace Message.	0x00

2.9.11.5 E-WIS Rx J1 Octets 25-24

Short Name:EWIS_Rx_J1_Octets_25_24

Address:0x2EB04

Table 814 • **E-WIS Rx J1 Octets 25-24**

Bit	Name	Access	Description	Default
15:8	RX_J1_octet_25	R/O	Contains octet 25 of the received Section Trace Message.	0x00
7:0	RX_J1_octet_24	R/O	Contains octet 24 of the received Section Trace Message.	0x00

2.9.11.6 E-WIS Rx J1 Octets 27-26

Short Name:EWIS_Rx_J1_Octets_27_26

Address:0x2EB05

Table 815 • **E-WIS Rx J1 Octets 27-26**

Bit	Name	Access	Description	Default
15:8	RX_J1_octet_27	R/O	Contains octet 27 of the received Section Trace Message.	0x00
7:0	RX_J1_octet_26	R/O	Contains octet 26 of the received Section Trace Message.	0x00

2.9.11.7 E-WIS Rx J1 Octets 29-28

Short Name:EWIS_Rx_J1_Octets_29_28

Address:0x2EB06

Table 816 • **E-WIS Rx J1 Octets 29-28**

Bit	Name	Access	Description	Default
15:8	RX_J1_octet_29	R/O	Contains octet 29 of the received Section Trace Message.	0x00
7:0	RX_J1_octet_28	R/O	Contains octet 28 of the received Section Trace Message.	0x00

2.9.11.8 E-WIS Rx J1 Octets 31-30

Short Name:EWIS_Rx_J1_Octets_31_30

Address:0x2EB07

Table 817 • **E-WIS Rx J1 Octets 31-30**

Bit	Name	Access	Description	Default
15:8	RX_J1_octet_31	R/O	Contains octet 31 of the received Section Trace Message.	0x00
7:0	RX_J1_octet_30	R/O	Contains octet 30 of the received Section Trace Message.	0x00

2.9.11.9 E-WIS Rx J1 Octets 33-32

Short Name:EWIS_Rx_J1_Octets_33_32

Address:0x2EB08

Table 818 • **E-WIS Rx J1 Octets 33-32**

Bit	Name	Access	Description	Default
15:8	RX_J1_octet_33	R/O	Contains octet 33 of the received Section Trace Message.	0x00
7:0	RX_J1_octet_32	R/O	Contains octet 32 of the received Section Trace Message.	0x00

2.9.11.10 E-WIS Rx J1 Octets 35-34

Short Name:EWIS_Rx_J1_Octets_35_34

Address:0x2EB09

Table 819 • **E-WIS Rx J1 Octets 35-34**

Bit	Name	Access	Description	Default
15:8	RX_J1_octet_35	R/O	Contains octet 35 of the received Section Trace Message.	0x00
7:0	RX_J1_octet_34	R/O	Contains octet 34 of the received Section Trace Message.	0x00

2.9.11.11 E-WIS Rx J1 Octets 37-36

Short Name:EWIS_Rx_J1_Octets_37_36

Address:0x2EB0A

Table 820 • **E-WIS Rx J1 Octets 37-36**

Bit	Name	Access	Description	Default
15:8	RX_J1_octet_37	R/O	Contains octet 37 of the received Section Trace Message.	0x00
7:0	RX_J1_octet_36	R/O	Contains octet 36 of the received Section Trace Message.	0x00

2.9.11.12 E-WIS Rx J1 Octets 39-38

Short Name:EWIS_Rx_J1_Octets_39_38

Address:0x2EB0B

Table 821 • **E-WIS Rx J1 Octets 39-38**

Bit	Name	Access	Description	Default
15:8	RX_J1_octet_39	R/O	Contains octet 39 of the received Section Trace Message.	0x00
7:0	RX_J1_octet_38	R/O	Contains octet 38 of the received Section Trace Message.	0x00

2.9.11.13 E-WIS Rx J1 Octets 41-40

Short Name:EWIS_Rx_J1_Octets_41_40

Address:0x2EB0C

Table 822 • **E-WIS Rx J1 Octets 41-40**

Bit	Name	Access	Description	Default
15:8	RX_J1_octet_41	R/O	Contains octet 41 of the received Section Trace Message.	0x00
7:0	RX_J1_octet_40	R/O	Contains octet 40 of the received Section Trace Message.	0x00

2.9.11.14 E-WIS Rx J1 Octets 43-42

Short Name:EWIS_Rx_J1_Octets_43_42

Address:0x2EB0D

Table 823 • **E-WIS Rx J1 Octets 43-42**

Bit	Name	Access	Description	Default
15:8	RX_J1_octet_43	R/O	Contains octet 43 of the received Section Trace Message.	0x00
7:0	RX_J1_octet_42	R/O	Contains octet 42 of the received Section Trace Message.	0x00

2.9.11.15 E-WIS Rx J1 Octets 45-44

Short Name:EWIS_Rx_J1_Octets_45_44

Address:0x2EB0E

Table 824 • **E-WIS Rx J1 Octets 45-44**

Bit	Name	Access	Description	Default
15:8	RX_J1_octet_45	R/O	Contains octet 45 of the received Section Trace Message.	0x00
7:0	RX_J1_octet_44	R/O	Contains octet 44 of the received Section Trace Message.	0x00

2.9.11.16 E-WIS Rx J1 Octets 47-46

Short Name:EWIS_Rx_J1_Octets_47_46

Address:0x2EB0F

Table 825 • **E-WIS Rx J1 Octets 47-46**

Bit	Name	Access	Description	Default
15:8	RX_J1_octet_47	R/O	Contains octet 47 of the received Section Trace Message.	0x00
7:0	RX_J1_octet_46	R/O	Contains octet 46 of the received Section Trace Message.	0x00

2.9.11.17 E-WIS Rx J1 Octets 49-48

Short Name:EWIS_Rx_J1_Octets_49_48

Address:0x2EB10

Table 826 • **E-WIS Rx J1 Octets 49-48**

Bit	Name	Access	Description	Default
15:8	RX_J1_octet_49	R/O	Contains octet 49 of the received Section Trace Message.	0x00
7:0	RX_J1_octet_48	R/O	Contains octet 48 of the received Section Trace Message.	0x00

2.9.11.18 E-WIS Rx J1 Octets 51-50

Short Name:EWIS_Rx_J1_Octets_51_50

Address:0x2EB11

Table 827 • **E-WIS Rx J1 Octets 51-50**

Bit	Name	Access	Description	Default
15:8	RX_J1_octet_51	R/O	Contains octet 51 of the received Section Trace Message.	0x00
7:0	RX_J1_octet_50	R/O	Contains octet 50 of the received Section Trace Message.	0x00

2.9.11.19 E-WIS Rx J1 Octets 53-52

Short Name:EWIS_Rx_J1_Octets_53_52

Address:0x2EB12

Table 828 • **E-WIS Rx J1 Octets 53-52**

Bit	Name	Access	Description	Default
15:8	RX_J1_octet_53	R/O	Contains octet 53 of the received Section Trace Message.	0x00
7:0	RX_J1_octet_52	R/O	Contains octet 52 of the received Section Trace Message.	0x00

2.9.11.20 E-WIS Rx J1 Octets 55-54

Short Name:EWIS_Rx_J1_Octets_55_54

Address:0x2EB13

Table 829 • **E-WIS Rx J1 Octets 55-54**

Bit	Name	Access	Description	Default
15:8	RX_J1_octet_55	R/O	Contains octet 55 of the received Section Trace Message.	0x00
7:0	RX_J1_octet_54	R/O	Contains octet 54 of the received Section Trace Message.	0x00

2.9.11.21 E-WIS Rx J1 Octets 57-56

Short Name:EWIS_Rx_J1_Octets_57_56

Address:0x2EB14

Table 830 • **E-WIS Rx J1 Octets 57-56**

Bit	Name	Access	Description	Default
15:8	RX_J1_octet_57	R/O	Contains octet 57 of the received Section Trace Message.	0x00
7:0	RX_J1_octet_56	R/O	Contains octet 56 of the received Section Trace Message.	0x00

2.9.11.22 E-WIS Rx J1 Octets 59-58

Short Name:EWIS_Rx_J1_Octets_59_58

Address:0x2EB15

Table 831 • **E-WIS Rx J1 Octets 59-58**

Bit	Name	Access	Description	Default
15:8	RX_J1_octet_59	R/O	Contains octet 59 of the received Section Trace Message.	0x00
7:0	RX_J1_octet_58	R/O	Contains octet 58 of the received Section Trace Message.	0x00

2.9.11.23 E-WIS Rx J1 Octets 61-60

Short Name:EWIS_Rx_J1_Octets_61_60

Address:0x2EB16

Table 832 • **E-WIS Rx J1 Octets 61-60**

Bit	Name	Access	Description	Default
15:8	RX_J1_octet_61	R/O	Contains octet 61 of the received Section Trace Message.	0x00
7:0	RX_J1_octet_60	R/O	Contains octet 60 of the received Section Trace Message.	0x00

2.9.11.24 E-WIS Rx J1 Octets 63-62

Short Name:EWIS_Rx_J1_Octets_63_62

Address:0x2EB17

Table 833 • **E-WIS Rx J1 Octets 63-62**

Bit	Name	Access	Description	Default
15:8	RX_J1_octet_63	R/O	Contains octet 63 of the received Section Trace Message.	0x00
7:0	RX_J1_octet_62	R/O	Contains octet 62 of the received Section Trace Message.	0x00

2.9.12 E-WIS Framer Control

2.9.12.1 E-WIS Rx Framer Control 1

Short Name:EWIS_RX_FRM_CTRL1

Address:0x2EC00

Table 834 • **E-WIS Rx Framer Control 1**

Bit	Name	Access	Description	Default
14:10	HUNT_A1	R/W	The number of consecutive A1 octets the receive framer must find before it can exit the HUNT state. 0: Undefined 1-16: 1-16 17-31: Undefined	0x04
9:5	PRESYNC_A1	R/W	The number of consecutive A1 octets in the presync pattern preceding the first A2 octet. 0: 1 1-16: 1-16 17-31: 16	0x10
4:0	PRESYNC_A2	R/W	The number of consecutive A2 octets in the presync pattern following the last A1 octet. 0: Only the four MSB of the first A2 byte are compared 1-16: 1-16 17-31: 16	0x10

2.9.12.2 E-WIS Rx Framer Control 2

Short Name:EWIS_RX_FRM_CTRL2

Address:0x2EC01

Table 835 • **E-WIS Rx Framer Control 2**

Bit	Name	Access	Description	Default
12:8	SYNC_PAT	R/W	Synchronization pattern to be used after the presync pattern has been detected 0: Sync pattern is A1 plus 4 most significant bits of A2 1: Sync pattern is 2 A1s plus 1 A2 (A1A1A2) 2-16: Sync pattern is the number of consecutive A1s followed by the same number of A2s I.e. the sync pattern is A1A1A2A2 when 2 is the setting) 17-31: Undefined	0x02
7:4	SYNC_ENTRY_CNT	R/W	Number of consecutive frame boundaries to be detected after finding the presync pattern before the framer can enter the SYNC state. 0: 1 1-15: 1-15	0x4
3:0	SYNC_EXIT_CNT	R/W	Number of consecutive frame boundary location errors tolerated/detected before exiting the SYNC state. 0: 1 1-15: 1-15	0x4

2.9.12.3 E-WIS Loss of Frame Control 1

Short Name:EWIS_LOF_CTRL1

Address:0x2EC02

Table 836 • **E-WIS Loss of Frame Control 1**

Bit	Name	Access	Description	Default
11:6	LOF_T1	R/W	Defines the number of frames periods (nominally 125 uS) during which OOF must persist to trigger LOF. This is not a count of continuous frames. An integrating counter is used. 0x0: Undefined 0x1: 1 frame time (125us) 0x2: 2 frame times 250us) : 0x18: 24 frame times 3ms) 0x3F: 63 frame times 7.875ms)	0x18
5:0	LOF_T2	R/W	Defines the number of consecutive frame periods (nominally 125 uS) during which OOF status must not be true in order to clear loss of frame set count (the counter associated with EWIS_LOF_CTRL1.LOF_T1). 0x0: Undefined 0x1: 1 frame time (125us) 0x2: 2 frame times 250us) : 0x18: 24 frame times 3ms) 0x3F: 63 frame times 7.875ms)	0x18

2.9.12.4 E-WIS Loss of Frame Control 2

Short Name:EWIS_LOF_CTRL2

Address:0x2EC03

Table 837 • **E-WIS Loss of Frame Control 2**

Bit	Name	Access	Description	Default
6:1	LOF_T3	R/W	Defines number of consecutive frames (nominally 125 uS) for which the receive framer must be in its sync state in order to clear the LOF status 0x0: Undefined 0x1: 1 frame time (125us) 0x2: 2 frame times 250us) : 0x18: 24 frame times 3ms) 0x3F: 63 frame times 7.875ms)	0x18

2.9.12.5 E-WIS Rx Control 1

Short Name:EWIS_RX_CTRL1

Address:0x2EC10

Table 838 • **E-WIS Rx Control 1**

Bit	Name	Access	Description	Default
1	DSCR_ENA	R/W	Enable the WIS descrambler 0 = Disable 1 = Enable	0x1
0	B3_CALC_MODE	R/W	Selects whether or not the fixed stuff bytes are included in the receive Path BIP error calculation 0 = The fixed stuff bytes are excluded from the B3 calculation. 1 = The fixed stuff bytes are included in the B3 calculation.	0x1

2.9.12.6 E-WIS Rx Trace Message Length Control

Short Name:EWIS_RX_MSGLEN

Address:0x2EC20

Table 839 • **E-WIS Rx Trace Message Length Control**

Bit	Name	Access	Description	Default
3:2	J0_RX_LEN	R/W	Selects the expected length of the received section trace message (J0). Trace length: 00: 16 bytes 01: 64 bytes 10: 1 byte 11: 1 byte	0x0
1:0	J1_RX_LEN	R/W	Selects the length of the expected path trace message (J1). Trace length: 00: 16 bytes 01: 64 bytes 10: 1 byte 11: 1 byte	0x0

2.9.12.7 E-WIS Rx Error Force Control 1

Short Name:EWIS_RX_ERR_FRC1

Address:0x2EC30

Table 840 • **E-WIS Rx Error Force Control 1**

Bit	Name	Access	Description	Default
12	FRC_LOPC	R/W	Force a Loss of Optical Carrier (LOPC) condition. The LOPC alarm state is asserted in EWIS_INTR_STAT2.LOPC_STAT when this bit is set and changes the SONET framer to an Out of Frame (OOF) state when RXLOF_ON_LOPC=1. The LOPC interrupt pending register in the GPIO register space is not affected by this bit. 0 = Normal operation 1 = Force LOPC	0x0

Table 840 • **E-WIS Rx Error Force Control 1** ***(continued)***

Bit	Name	Access	Description	Default
11	FRC_LOS	R/W	Force a Loss of Signal (LOS) condition in the WIS receive data path 0 = Normal operation 1 = Forced receive LOS	0x0
10	FRC_OOF	R/W	Force the receive framer into the out-of-frame (OOF) state 0 = Normal operation. 1 = Force receive OOF	0x0
8	RXLOF_ON_LOPC	R/W	Selects whether or not the LOPC input has any effect on alarm conditions detected by the device 0 = A LOPC condition does not effect the state of the LOF or SEF status, nor the state of the receive path framer. 1 = LOF and SEF are asserted and the receive path framer is put into its out-of-frame state during a LOPC condition.	0x0
7:4	APS_THRES	R/W	The number of consecutive frames required to qualify the setting and clearing of AIS-L and RDI-L flags received in the K1/K2 overhead bytes. 3-15: Threshold value All others: Reserved	0x5
3	FRC_RX_AISL	R/W	Force a Line Alarm Indication Signal (AIS-L) condition in the WIS receive data path 0 = Normal operation 1 = Device forced into Rx AIS-L condition	0x0
2	FRC_RX_RDIL	R/W	Force a Line Remote Defect Identifier (RDI-L) condition in the WIS receive data path 0 = Normal operation 1 = Device forced into Rx RDI-L condition	0x0
1	FRC_RX_AISP	R/W	Force a Path Alarm Indication Signal (AIS-P) condition in the WIS receive data path 0 = Normal operation 1 = Device forced into Rx AIS-P condition	0x0
0	FRC_RX_LOP	R/W	Force a Loss of Pointer (LOP) condition to the starting location of the frame's SPE (synchronous payload envelope) in the WIS receive data path 0 = Normal operation 1 = Device forced into Rx LOP condition	0x0

2.9.12.8 E-WIS Rx Error Force Control 2

Short Name:EWIS_RX_ERR_FRC2

Address:0x2EC31

Table 841 • **E-WIS Rx Error Force Control 2**

Bit	Name	Access	Description	Default
15	FRC_RX_UNEQP	R/W	Force a Unequiped Path (UNEQ-P) defect in the WIS receive data path 0 = Normal operation 1 = Device forced into Rx UNEQ-P condition	0x0
14	FRC_RX_PLMP	R/W	Force a Payload Label Mismatch (PLM-P) defect in the WIS receive data path 0 = Normal operation 1 = Device forced into Rx PLM-P condition	0x0
13	FRC_RX_RDIP	R/W	Force a far-end Path Remote Defect Identifier condition in the WIS receive data path 0 = Normal operation 1 = Device forced into Rx far-end RDI-P condition	0x0
12	FRC_RX_FE_AISP	R/W	Force a far-end Path Alarm Indication Signal condition in the WIS receive data path 0 = Normal operation 1 = Device forced into Rx far-end AIS-P condition	0x0
11	FRC_RX_FE_UNEQP	R/W	Force a far-end Unequipped Path defect in the WIS receive data path 0 = Normal operation 1 = Device forced into Rx far-end UNEQ-P condition	0x0
10	FRC_RX_FE_PLMP	R/W	Force a far-end Payload Label Mismatch defect in the WIS receive data path 0 = Normal operation 1 = Device forced into Rx far-end PLM-P condition	0x0
9	FRC_RX_REIP	R/W	Force a Path Remote Error Indication (REI-P) condition in the WIS receive data path. The error is reflected in register EWIS_INTR_STAT2.REIP_STAT. 0 = Normal operation 1 = Device forced into Rx REI-P condition	0x0
8	FRC_RX_REIL	R/W	Force a Line Remote Error Indication (REI-L) condition in the WIS receive data path. The error is reflected in register EWIS_INTR_STAT2.REIL_STAT. 0 = Normal operation 1 = Device forced into Rx REI-L condition	0x0
7	FRC_RX_SEF	R/W	Force a Severely Errored Frame (SEF) condition in the WIS receive data path 0 = Normal operation 1 = Device forced into Rx SEF condition	0x0
6	FRC_RX_LOF	R/W	Force a Loss of Frame (LOF) condition in the WIS receive data path 0 = Normal operation 1 = Device forced into Rx LOF condition	0x0

Table 841 • **E-WIS Rx Error Force Control 2 *(continued)***

Bit	Name	Access	Description	Default
5	FRC_RX_B1	R/W	Force a PMTICK B1 BIP error condition (B1NZ) in the WIS receive data path 0 = Normal operation 1 = Device forced into PMTICK B1 BIP error condition	0x0
4	FRC_RX_B2	R/W	Force a PMTICK B2 BIP error condition (B2NZ) in the WIS receive data path 0 = Normal operation 1 = Device forced into PMTICK B2 BIP error condition	0x0
3	FRC_RX_B3	R/W	Force a PMTICK B3 BIP error condition (B3NZ) in the WIS receive data path 0 = Normal operation 1 = Device forced into PMTICK B3 BIP error condition	0x0
2	FRC_LCDP	R/W	Force a Loss of Code-group Delineation (LCD-P) defect in the WIS receive data path 0 = Normal operation 1 = Device forced into Rx LCD-P condition	0x0
1	FRC_REIL	R/W	Force a far-end line BIP error condition (far-end B2NZ) in the WIS receive data path 0 = Normal operation 1 = Device forced into Rx far-end line BIP error condition	0x0
0	FRC_REIP	R/W	Force a far-end path BIP error condition (far-end B3NZ) in the WIS receive data path 0 = Normal operation 1 = Device forced into Rx far-end path BIP error condition	0x0

2.9.12.9 E-WIS Mode Control

Short Name:EWIS_MODE_CTRL

Address:0x2EC40

Table 842 • **E-WIS Mode Control**

Bit	Name	Access	Description	Default
14	PTR_MODE	R/W	Selects pointer type interpretation mode 0 = SONET mode. All 192 H1 and H2 bytes are used to determine the pointer type. 1 = SDH mode. Only the first 64 H1 and H2 bytes are used to determine the pointer type.	0x0
13	PTR_RULES	R/W	Selects pointer increment/decrement rules. 0 = Pointer increment/ decrement is declared when 8 of the 10 D/I bits in the H1 and H2 bytes match 1 = Pointer increment/ decrement is declared by majority rules	0x0

Table 842 • **E-WIS Mode Control *(continued)***

Bit	Name	Access	Description	Default
12	REI_MODE	R/W	Selects how REI is extracted from the M0/M1 bytes in the WIS receive data path. 0 = SONET mode enabled. Uses M0 only. 1 = SDH mode enabled. Uses M0 and M1.	0x0
11	RX_SS_MODE	R/W	Determines whether the SS bits in the H1 byte are checked when processing the received H1/H2 pointer. 0 = SS bits are ignored 1 = SS bits must match 2'b10 to be considered a valid H1 byte	0x0
8	RX_ERDI_MODE	R/W	Selects how ERDI-P/RDI-P is extracted from the G1 byte in the WIS received data 0 = RDI-P is reported in bit 5. Bits 6 and 7 are unused. 1 = ERDI is reported in bits 5-7	0x1
7:0	C2_EXP	R/W	Expected C2 receive octet. A PLM-P alarm is generated if this octet value is not received.	0x1A

2.9.12.10 E-WIS PRBS31 Analyzer Control

Short Name:EWIS_PRBS31_ANA_CTRL

Address:0x2EC50

Table 843 • **E-WIS PRBS31 Analyzer Control**

Bit	Name	Access	Description	Default
1	PRBS31_FRC_ERR	One-shot	Inject a single bit error into the WIS PRBS31 pattern checker. A single bit error injected in the data stream will result in the error counter incrementing by 3 (1 error for each tap of the checker). 0 = Normal operation 1 = Inject error	0x0
0	PRBS31_FRC_SAT	One-shot	Force the PRBS31 pattern error counter (WIS_TSTPAT_CNT) to a value of 65528. This can be useful for testing the saturating feature of the counter. Forcing the counter to 65528 with this bit has no affect on register EWIS_PRBS31_ANA_STAT.PRBS31_ERR. 0 = Normal operation 1 = Force the PRBS31 error counter to a value of 65528	0x0

2.9.12.11 E-WIS PRBS31 Analyzer Status

Short Name:EWIS_PRBS31_ANA_STAT

Address:0x2EC51

Table 844 • **E-WIS PRBS31 Analyzer Status**

Bit	Name	Access	Description	Default
1	PRBS31_ERR	R/O	Status bit indicating if the WIS PRBS31 error counter is non-zero. 0 = Counter is zero 1 = Counter is non-zero	0x0
0	PRBS31_ANA_STATE	R/O	Indicates when the Rx WIS PRBS31 pattern checker is synchronized to the incoming data. 0 = PRBS31 pattern checker is not synchronized to the data. PRBS31 error counter value is not valid 1 = PRBS31 pattern checker is synchronized to the data	0x0

2.9.12.12 E-WIS Performance Monitor Control

Short Name:EWIS_PMTICK_CTRL

Address:0x2EC60

Table 845 • **E-WIS Performance Monitor Control**

Bit	Name	Access	Description	Default
15:3	PMTICK_DUR	R/W	Sets the interval for updating the PMTICK error counters when the PMTICK_SRC bit is 1. The value represents the number of 125uS increments between PMTICK events. 0: Undefined 1: Undefined 2: 250 uS : 8: 1 mS 8000: 1 sec 8191: 1.024 sec	0x1F40
2	PMTICK_ENA	R/W	Enable the PMTICK counters to be updated on a PMTICK event. The source of the PMTICK event is determined by the PMTICK_SRC bit. 0 = Disable 1 = Enable	0x0
1	PMTICK_SRC	R/W	Selects how the PMTICK counters are updated. The PMTICK counters are updated with the selected source only if the PMTICK enable bit is set. 0 = PMTICK counters updated on a rising edge of the (GPIO) PMTICK pin 1 = PMTICK counters updated when the PMTICK counter reaches its terminal count (PMTICK_DUR).	0x1
0	PMTICK_FRC	One-shot	Force the PMTICK counters to update, regardless of the PMTICK_ENA or PMTICK_SRC settings. 0 = Normal operation 1 = Forces PMTICK event	0x0

2.9.12.13 E-WIS Counter Configuration

Short Name:EWIS_CNT_CFG

Address:0x2EC61

Table 846 • **E-WIS Counter Configuration**

Bit	Name	Access	Description	Default
11	B1_BLK_MODE	R/W	Enable block mode (increment once for each errored frame) counting for the B1 BIP PMTICK counter. 0 = Bit mode 1 = Block mode	0x0
10	B2_BLK_MODE	R/W	Enable block mode (increment once for each errored frame) counting for the B2 BIP PMTICK counter 0 = Bit mode 1 = Block mode	0x0
9	B3_BLK_MODE	R/W	Enable block mode (increment once for each errored frame) counting for the B3 BIP PMTICK counter 0 = Bit mode 1 = Block mode	0x0
5	REIP_BLK_MODE	R/W	Enable block mode (increment once for each errored frame) counting for the REI-P (far-end B3 error count in the G1 byte) PMTICK counter 0 = Bit mode 1 = Block mode	0x0
4	REIL_BLK_MODE	R/W	Enable block mode (increment once for each errored frame) counting for the REI-L (far-end B2 error count in the M0/M1 byte) PMTICK counter 0 = Bit mode 1 = Block mode	0x0

2.9.12.14 E-WIS Counter Status

Short Name:EWIS_CNT_STAT

Address:0x2EC62

Table 847 • **E-WIS Counter Status**

Bit	Name	Access	Description	Default
2	REIP_CNT_STAT	R/O	Status bit indicating if the REI-P (far-end B3) PMTICK counter is non-zero 0 = Counter is zero 1 = Counter is non-zero	0x0
1	REIL_CNT_STAT	R/O	Status bit indicating if the REI-L (far-end B2) PMTICK counter is non-zero 0 = Counter is zero 1 = Counter is non-zero	0x0
0	B2_statistical_error_event	R/O	0 = B2 error counter is zero 1 = B2 error counter is non zero	0x0

2.9.13 E-WIS Counters

2.9.13.1 E-WIS P-REI Counter 1 MSW

Short Name:EWIS_REIP_CNT1

Address:0x2EC80

Table 848 • **E-WIS P-REI Counter 1 MSW**

Bit	Name	Access	Description	Default
15:0	REIP_ERR_CNT_MSW	R/O	PMTICK statistical error count of the far-end B3 errors reported in the G1 byte. 16 MSB are in this register, 16 LSB are in the next register. The count is updated only on a PMTICK event. The counter saturates when the maximum error count is exceeded.	0x0000

2.9.13.2 E-WIS P-REI Counter 0 LSW

Short Name:EWIS_REIP_CNT0

Address:0x2EC81

Table 849 • **E-WIS P-REI Counter 0 LSW**

Bit	Name	Access	Description	Default
15:0	REIP_ERR_CNT_LSW	R/O	PMTICK statistical error count of the far-end B3 errors reported in the G1 byte. 16 LSB are in this register, 16 MSB are in the previous register. The count is updated only on a PMTICK event. The counter saturates when the maximum error count is exceeded.	0x0000

2.9.13.3 E-WIS L-REI Counter 1 MSW

Short Name:EWIS_REIL_CNT1

Address:0x2EC90

Table 850 • **E-WIS L-REI Counter 1 MSW**

Bit	Name	Access	Description	Default
15:0	REIL_ERR_CNT_MSW	R/O	PMTICK statistical error count of the far-end B2 errors reported in the M0/M1 bytes. 16 MSB are in this register, 16 LSB are in the next register. The count is updated only on a PMTICK event. The counter saturates when the maximum error count is exceeded.	0x0000

2.9.13.4 E-WIS L-REI Counter 0 LSW

Short Name:EWIS_REIL_CNT0

Address:0x2EC91

Table 851 • **E-WIS L-REI Counter 0 LSW**

Bit	Name	Access	Description	Default
15:0	REIL_ERR_CNT_LSW	R/O	PMTICK statistical error count of the far-end B2 errors reported in the M0/M1 bytes. 16 LSB are in this register, 16 MSB are in the previous register. The count is updated only on a PMTICK event. The counter saturates when the maximum error count is exceeded.	0x0000

2.9.13.5 E-WIS S-BIP Error Counter 1 MSW

Short Name:EWIS_B1_ERR_CNT1

Address:0x2ECB0

Table 852 • **E-WIS S-BIP Error Counter 1 MSW**

Bit	Name	Access	Description	Default
15:0	B1_ERR_CNT_MSW	R/O	PMTICK statistical error count of the B1 BIP errors. 16 MSB are in this register, 16 LSB are in the next register. The count is updated only on a PMTICK event. The counter saturates when the maximum error count is exceeded.	0x0000

2.9.13.6 E-WIS S-BIP Error Counter 0 LSW

Short Name:EWIS_B1_ERR_CNT0

Address:0x2ECB1

Table 853 • **E-WIS S-BIP Error Counter 0 LSW**

Bit	Name	Access	Description	Default
15:0	B1_ERR_CNT_LSW	R/O	PMTICK statistical error count of the B1 BIP errors. 16 LSB are in this register, 16 MSB are in the previous register. The count is updated only on a PMTICK event. The counter saturates when the maximum error count is exceeded.	0x0000

2.9.13.7 E-WIS L-BIP Error Counter 1 MSW

Short Name:EWIS_B2_ERR_CNT1

Address:0x2ECB2

Table 854 • **E-WIS L-BIP Error Counter 1 MSW**

Bit	Name	Access	Description	Default
15:0	B2_ERR_CNT_MSW	R/O	PMTICK statistical error count of the B2 BIP errors. 16 MSB are in this register, 16 LSB are in the next register. The count is updated only on a PMTICK event. The counter saturates when the maximum error count is exceeded.	0x0000

2.9.13.8 E-WIS L-BIP Error Counter 0 LSW

Short Name:EWIS_B2_ERR_CNT0

Address:0x2ECB3

Table 855 • **E-WIS L-BIP Error Counter 0 LSW**

Bit	Name	Access	Description	Default
15:0	B2_ERR_CNT_LSW	R/O	PMTICK statistical error count of the B2 BIP errors. 16 LSB are in this register, 16 MSB are in the previous register. The count is updated only on a PMTICK event. The counter saturates when the maximum error count is exceeded.	0x0000

2.9.13.9 E-WIS P-BIP Error Counter 1 MSW

Short Name:EWIS_B3_ERR_CNT1

Address:0x2ECB4

Table 856 • **E-WIS P-BIP Error Counter 1 MSW**

Bit	Name	Access	Description	Default
15:0	B3_ERR_CNT_MSW	R/O	PMTICK statistical error count of the B3 BIP errors. 16 MSB are in this register, 16 LSB are in the next register. The count is updated only on a PMTICK event. The counter saturates when the maximum error count is exceeded.	0x0000

2.9.13.10 E-WIS P-BIP Error Counter 0 LSW

Short Name:EWIS_B3_ERR_CNT0

Address:0x2ECB5

Table 857 • **E-WIS P-BIP Error Counter 0 LSW**

Bit	Name	Access	Description	Default
15:0	B3_ERR_CNT_LSW	R/O	PMTICK statistical error count of the B3 BIP errors. 16 LSB are in this register, 16 MSB are in the previous register. The count is updated only on a PMTICK event. The counter saturates when the maximum error count is exceeded.	0x0000

2.9.14 E-WIS Actions and Interrupts

2.9.14.1 E-WIS Rx to Tx Control

Short Name:EWIS_RXTX_CTRL

Address:0x2EDFF

Table 858 • **E-WIS Rx to Tx Control**

Bit	Name	Access	Description	Default
6	RXAISL_ON_LOPC	R/W	Select if a LOPC condition contributes to the Rx AIS-L alarm 0 = A LOPC condition does not cause the AIS-L alarm to be set 1 = A LOPC condition will cause the AIS-L alarm to be set	0x0

Table 858 • **E-WIS Rx to Tx Control *(continued)***

Bit	Name	Access	Description	Default
5	RXAISL_ON_LOS	R/W	Selects if a LOS condition contributes to the Rx AIS-L alarm 0 = A LOS condition does not cause the AIS-L alarm to be set 1 = A LOS condition will cause the AIS-L alarm to be set	0x0
4	RXAISL_ON_LOF	R/W	Select if a LOF condition contributes to the Rx AIS-L alarm 0 = A LOF condition does not cause the AIS-L alarm to be set 1 = A LOF condition will cause the AIS-L alarm to be set	0x0
3	TXRDIL_ON_LOPC	R/W	Select if a RDI-L is reported in the Tx frame's K2 byte when a LOPC condition is detected 0 = RDI-L will not be reported when LOPC is detected 1 = RDI-L will be reported when LOPC is detected	0x0
2	TXRDIL_ON_LOS	R/W	Selects whether or not RDI-L is reported in the Tx frame's K2 byte when a LOS condition is detected 0 = RDI-L will not be reported when LOS is detected 1 = RDI-L will be reported when LOS is detected	0x0
1	TXRDIL_ON_LOF	R/W	Selects whether or not RDI-L is reported in the Tx frame's K2 byte when a LOF condition is detected 0 = RDI-L will not be reported when LOF is detected 1 = RDI-L will be reported when LOF is detected	0x0
0	TXRDIL_ON_AISL	R/W	Selects whether or not RDI-L is reported in the Tx frame's K2 byte when a Rx AIS-L condition is detected 0 = RDI-L will not be reported when a Rx AIS-L condition is detected 1 = RDI-L will be reported when a Rx AIS-L condition is detected	0x0

2.9.14.2 E-WIS Interrupt Pending 1

Short Name:EWIS_INTR_PEND1

Address:0x2EE00

Table 859 • **E-WIS Interrupt Pending 1**

Bit	Name	Access	Description	Default
11	SEF_PEND	Sticky	The interrupt pending bit is asserted when the SEF status changes state. The sticky bit is cleared when a 1 is written to the register bit. 0 = SEF condition has not changed state 1 = SEF condition has changed state	0x0

Table 859 • **E-WIS Interrupt Pending 1** ***(continued)***

Bit	Name	Access	Description	Default
10	FEPLMP_LCDP_PEND	Sticky	The interrupt pending bit is asserted when the far-end path label mismatch (PLM-P) / Loss of Code-group Delineation (LCD-P) condition changes state. The sticky bit is cleared when a 1 is written to the register bit. 0 = PLM-P/LCD-P has not changed state 1 = PLM-P/LCD-P condition has changed state	0x0
9	FEAISP_LOPP_PEND	Sticky	The interrupt pending bit is asserted when the far-end path Alarm Indication Signal (AIS-P)/ Path Loss of Pointer (LOP) condition changes state. The sticky bit is cleared when a 1 is written to the register bit. 0 = Far-end AIS-P/LOP-P condition has not changed state 1 = Far-end AIS-P/LOP-P condition has changed state	0x0
7	LOF_PEND	Sticky	The interrupt pending bit is asserted when the Loss of Frame (LOF) condition changes state. The sticky bit is cleared when a 1 is written to the register bit. 0 = LOF condition has not changed state 1 = LOF condition has changed state	0x0
6	LOS_PEND	Sticky	The interrupt pending bit is asserted when the Loss of Signal (LOS) condition changes state. This bit does not assert if LOPC is asserted at the time LOS changes state. The sticky bit is cleared when a 1 is written to the register bit. 0 = LOS condition has not changed state 1 = LOS condition has changed state	0x0
5	RDIL_PEND	Sticky	The interrupt pending bit is asserted when the Line Remote Defect Indication (RDI-L) status changes state. The sticky bit is cleared when a 1 is written to the register bit. 0 = RDI-L condition has not changed state 1 = RDI-L condition has changed state	0x0
4	AISL_PEND	Sticky	The interrupt pending bit is asserted when Line Alarm Indication Signal (AIS-L) status changes state. This bit does not assert if LOPC, LOS, LOF or SEF are asserted at the time AIS-L changes state. The sticky bit is cleared when a 1 is written to the register bit. 0 = AIS-L condition has not changed state 1 = AIS-L condition has changed state	0x0
3	LCDP_PEND	Sticky	The interrupt pending bit is asserted when the Loss of Code-group Delineation (LCD-P) condition changes state. This bit will not assert if AIS-L, AIS-P, UNEQ-P, or PLM-P are asserted at the time LCD-P changes state. The sticky bit is cleared when a 1 is written to the register bit. 0 = LCD-P condition has not changed state 1 = LCD-P condition has changed state	0x0

Table 859 • **E-WIS Interrupt Pending 1 *(continued)***

Bit	Name	Access	Description	Default
2	PLMP_PEND	Sticky	The interrupt pending bit is asserted when the Path Label Mismatch (PLM-P) condition changes state. This bit will not assert if LOP-P or AIS-P are asserted at the time PLM-P changes state. The sticky bit is cleared when a 1 is written to the register bit. 0 = PLM-P condition has not changed state 1 = PLM-P condition has changed state	0x0
1	AISP_PEND	Sticky	The interrupt pending bit is asserted when the Path Alarm Indication Signal (AIS-P) condition changes state. This bit will not assert if LOPC, LOS, SEF, LOF, or AIS-L are asserted at the time AIS-P changes state. The sticky bit is cleared when a 1 is written to the register bit. 0 = AIS-P condition has not changed state 1 = AIS-P condition has changed state	0x0
0	LOPP_PEND	Sticky	The interrupt pending bit is asserted when the Path Loss of Pointer (LOP-P) condition changes state. The sticky bit is cleared when a 1 is written to the register bit. 0 = LOP-P condition has not changed state 1 = LOP-P condition has changed state	0x0

2.9.14.3 E-WIS Interrupt Mask A 1

Short Name:EWIS_INTR_MASKA_1

Address:0x2EE01

Table 860 • **E-WIS Interrupt Mask A 1**

Bit	Name	Access	Description	Default
11	SEF_MASKA	R/W	Enable propagation of SEF_PEND to the WIS0 interrupt 0 = Disable 1 = Enable	0x0
10	FEPLMP_LCDP_MASKA	R/W	Enable propagation of FEPLMP_LCDP_PEND to the WIS0 interrupt 0 = Disable 1 = Enable	0x0
9	FEAISP_LOPP_MASKA	R/W	Enable propagation of FEAISP_LOPP_PEND to the WIS0 interrupt 0 = Disable 1 = Enable	0x0
7	LOF_MASKA	R/W	Enable propagation of LOF_PEND to the WIS0 interrupt 0 = Disable 1 = Enable	0x0
6	LOS_MASKA	R/W	Enable propagation of LOS_PEND to the WIS0 interrupt 0 = Disable 1 = Enable	0x0

Table 860 • **E-WIS Interrupt Mask A 1 *(continued)***

Bit	Name	Access	Description	Default
5	RDIL_MASKA	R/W	Enable propagation of RDIL_PEND to the WIS0 interrupt 0 = Disable 1 = Enable	0x0
4	AISL_MASKA	R/W	Enable propagation of AISL_PEND to the WIS0 interrupt 0 = Disable 1 = Enable	0x0
3	LCDP_MASKA	R/W	Enable propagation of LCDP_PEND to the WIS0 interrupt 0 = Disable 1 = Enable	0x0
2	PLMP_MASKA	R/W	Enable propagation of PLMP_PEND to the WIS0 interrupt 0 = Disable 1 = Enable	0x0
1	AISP_MASKA	R/W	Enable propagation of AISP_PEND to the WIS0 interrupt 0 = Disable 1 = Enable	0x0
0	LOPP_MASKA	R/W	Enable propagation of LOPP_PEND to the WIS0 interrupt 0 = Disable 1 = Enable	0x0

2.9.14.4 E-WIS Interrupt Mask B 1

Short Name:EWIS_INTR_MASKB_1

Address:0x2EE02

Table 861 • **E-WIS Interrupt Mask B 1**

Bit	Name	Access	Description	Default
11	SEF_MASKB	R/W	Enable propagation of SEF_PEND to the WIS1 interrupt 0 = Disable 1 = Enable	0x0
10	FEPLMP_LCDP_MASKB	R/W	Enable propagation of FEPLMP_LCDP_PEND to the WIS1 interrupt 0 = Disable 1 = Enable	0x0
9	FEAISP_LOPP_MASKB	R/W	Enable propagation of FEAISP_LOPP_PEND to the WIS1 interrupt 0 = Disable 1 = Enable	0x0
7	LOF_MASKB	R/W	Enable propagation of LOF_PEND to the WIS1 interrupt 0 = Disable 1 = Enable	0x0

Table 861 • **E-WIS Interrupt Mask B 1 *(continued)***

Bit	Name	Access	Description	Default
6	LOS_MASKB	R/W	Enable propagation of LOS_PEND to the WIS1 interrupt 0 = Disable 1 = Enable	0x0
5	RDIL_MASKB	R/W	Enable propagation of RDIL_PEND to the WIS1 interrupt 0 = Disable 1 = Enable	0x0
4	AISL_MASKB	R/W	Enable propagation of AISL_PEND to the WIS1 interrupt 0 = Disable 1 = Enable	0x0
3	LCDP_MASKB	R/W	Enable propagation of LCDP_PEND to the WIS1 interrupt 0 = Disable 1 = Enable	0x0
2	PLMP_MASKB	R/W	Enable propagation of PLMP_PEND to the WIS1 interrupt 0 = Disable 1 = Enable	0x0
1	AISP_MASKB	R/W	Enable propagation of AISP_PEND to the WIS1 interrupt 0 = Disable 1 = Enable	0x0
0	LOPP_MASKB	R/W	Enable propagation of LOPP_PEND to the WIS1 interrupt 0 = Disable 1 = Enable	0x0

2.9.14.5 E-WIS Interrupt Status 2

Short Name:EWIS_INTR_STAT2

Address:0x2EE03

Table 862 • **E-WIS Interrupt Status 2**

Bit	Name	Access	Description	Default
11	LOPC_STAT	R/O	Loss of Optical Carrier (LOPC) status 0 = The LOPC input pin is de-asserted 1 = The LOPC input pin is asserted	0x0
10	UNEQP_STAT	R/O	Unequipped Path (UNEQ-P) status 0 = UNEQ-P is de-asserted 1 = UNEQ-P is asserted	0x0
9	FEUNEQP_STAT	R/O	Far-end Unequipped Path (UNEQ-P) status 0 = Far-end UNEQ-P is de-asserted 1 = Far-end UNEQ-P is asserted	0x0
8	FERDIP_STAT	R/O	Far-end Path Remote Defect Identifier (RDI-P) status 0 = Far-end RDI-P is de-asserted 1 = Far-end RDI-P is asserted	0x0

Table 862 • **E-WIS Interrupt Status 2 *(continued)***

Bit	Name	Access	Description	Default
7	B1_NZ_STAT	R/O	PMTICK B1 BIP (B1_ERR_CNT) counter status 0 = B1_ERR_CNT is zero 1 = B1_ERR_CNT is non-zero	0x0
6	B2_NZ_STAT	R/O	PMTICK B2 BIP (B2_ERR_CNT) counter status 0 = B2_ERR_CNT is zero 1 = B2_ERR_CNT is non-zero	0x0
5	B3_NZ_STAT	R/O	PMTICK B3 BIP (B3_ERR_CNT) counter status 0 = B3_ERR_CNT is zero 1 = B3_ERR_CNT is non-zero	0x0
4	REIL_STAT	R/O	Line Remote Error Indication (REI-L) value status 0 = The REI-L value in the last received frame reported no errors 1 = The REI-L value in the last received frame reported errors	0x0
3	REIP_STAT	R/O	Path Remote Error Indication (REI-P) value status 0 = The REI-P value in the last received frame reported no errors 1 = The REI-P value in the last received frame reported errors	0x0
2	REIL_NZ_STAT	R/O	PMTICK REI-L (REIL_ERR_CNT) counter status 0 = REIL_ERR_CNT is zero 1 = REIL_ERR_CNT is non-zero	0x0
1	REIP_NZ_STAT	R/O	PMTICK REI-P (REIP_ERR_CNT) counter status 0 = REIP_ERR_CNT is zero 1 = REIP_ERR_CNT is non-zero	0x0

2.9.14.6 E-WIS Interrupt Pending 2

Short Name:EWIS_INTR_PEND2

Address:0x2EE04

Table 863 • **E-WIS Interrupt Pending 2**

Bit	Name	Access	Description	Default
14	PMTICK_PEND	Sticky	The interrupt pending bit is asserted when a PMTICK event (regardless of the source) has occurred. The sticky bit is cleared when a 1 is written to the register bit. 0 = A PMTICK event has not occurred 1 = A PMTICK event occurred	0x0
10	UNEQP_PEND	Sticky	The interrupt pending bit is asserted when the Unequipped Path (UNEQP_STAT) status changes state. This bit does not assert if LOP-P or AIS-P are asserted at the time UNEQ-P changes state. The sticky bit is cleared when a 1 is written to the register bit. 0 = UNEQP_STAT has not changed state 1 = UNEQP_STAT has changed state	0x0

Table 863 • **E-WIS Interrupt Pending 2** ***(continued)***

Bit	Name	Access	Description	Default
9	FEUNEQP_PEND	Sticky	The interrupt pending bit is asserted when the Far-end Unequipped Path (FEUNEQP_STAT) status changes state. The sticky bit is cleared when a 1 is written to the register bit. 0 = FEUNEQP_STAT has not changed state 1 = FEUNEQP_STAT has changed state	0x0
8	FERDIP_PEND	Sticky	The interrupt pending bit is asserted when the Far-end Path Remote Defect Identifier (FERDIP_STAT) status changes state. The sticky bit is cleared when a 1 is written to the register bit. 0 = FERDIP_STAT has not changed state 1 = FERDIP_STAT has changed state	0x0
7	B1_NZ_PEND	Sticky	The interrupt pending bit is asserted when the PMTICK B1 error counter (B1_ERR_CNT) has changed from zero to a non-zero value. This bit will not assert if LOS or LOF are asserted at the time B1_NZ_STAT changes state. The sticky bit is cleared when a 1 is written to the register bit. 0 = B1_NZ_STAT has not changed from a 0 to 1 state 1 = B1_NZ_STAT has changed from a 0 to 1 state	0x0
6	B2_NZ_PEND	Sticky	The interrupt pending bit is asserted when the PMTICK B2 error counter (B2_ERR_CNT) has changed from zero to a non-zero value. This bit will not assert if AIS-L is asserted at the time B2_NZ_STAT changes state. The sticky bit is cleared when a 1 is written to the register bit. 0 = B2_NZ_STAT has not changed from a 0 to 1 state 1 = B2_NZ_STAT has changed from a 0 to 1 state	0x0
5	B3_NZ_PEND	Sticky	The interrupt pending bit is asserted when the PMTICK B3 error counter (B3_ERR_CNT) has changed from zero to a non-zero value. This bit will not assert if LOP-P or AIS-P are asserted at the time B3_NZ_STAT changes state. The sticky bit is cleared when a 1 is written to the register bit. 0 = B3_NZ_STAT has not changed from a 0 to 1 state 1 = B3_NZ_STAT has changed from a 0 to 1 state	0x0
4	REIL_PEND	Sticky	The interrupt pending bit is asserted when a non-zero REI-L value is received. The sticky bit is cleared when a 1 is written to the register bit. 0 = REI-L has not received a non-zero value 1 = REI-L has received a non-zero value	0x0

Table 863 • **E-WIS Interrupt Pending 2 *(continued)***

Bit	Name	Access	Description	Default
3	REIP_PEND	Sticky	The interrupt pending bit is asserted when a non-zero REI-P value is received. The sticky bit is cleared when 1 is written to the register bit. 0 = REI-P has not received a non-zero value 1 = REI-P has received a non-zero value	0x0
2	REIL_NZ_PEND	Sticky	The interrupt pending bit is asserted when the PMTICK far-end B2 error counter (REIL_ERR_CNT) has changed from zero to a non-zero value status changes state. The sticky bit is cleared when a 1 is written to the register bit. 0 = REIL_NZ_STAT has not changed from a 0 to 1 state 1 = REIL_NZ_STAT has changed from a 0 to 1 state	0x0
1	REIP_NZ_PEND	Sticky	The interrupt pending bit is asserted when the PMTICK far-end B3 error counter (REIP_ERR_CNT) has changed from zero to a non-zero value. The sticky bit is cleared when a 1 is written to the register bit. 0 = REIP_NZ_STAT has changed from a 0 to 1 state 1 = REIP_NZ_STAT has changed from a 0 to 1 state	0x0

2.9.14.7 E-WIS Interrupt Mask A 2

Short Name:EWIS_INTR_MASKA_2

Address:0x2EE05

Table 864 • **E-WIS Interrupt Mask A 2**

Bit	Name	Access	Description	Default
14	PMTICK_MASKA	R/W	Enable propagation of PMTICK_PEND to the WIS0 interrupt 0 = Disable 1 = Enable	0x0
10	UNEQP_MASKA	R/W	Enable propagation of UNEQP_PEND to the WIS0 interrupt 0 = Disable 1 = Enable	0x0
9	FEUNEQP_MASKA	R/W	Enable propagation of FEUNEQP_PEND to the WIS0 interrupt 0 = Disable 1 = Enable	0x0
8	FERDIP_MASKA	R/W	Enable propagation of FERDIP_PEND to the WIS0 interrupt 0 = Disable 1 = Enable	0x0

Table 864 • **E-WIS Interrupt Mask A 2 *(continued)***

Bit	Name	Access	Description	Default
7	B1_NZ_MASKA	R/W	Enable propagation of B1_NZ_PEND to the WIS0 interrupt 0 = Disable 1 = Enable	0x0
6	B2_NZ_MASKA	R/W	Enable propagation of B2_NZ_PEND to the WIS0 interrupt 0 = Disable 1 = Enable	0x0
5	B3_NZ_MASKA	R/W	Enable propagation of B3_NZ_PEND to the WIS0 interrupt 0 = Disable 1 = Enable	0x0
4	REIL_MASKA	R/W	Enable propagation of REIL_PEND to the WIS0 interrupt 0 = Disable 1 = Enable	0x0
3	REIP_MASKA	R/W	Enable propagation of REIP_PEND to the WIS0 interrupt 0 = Disable 1 = Enable	0x0
2	REIL_NZ_MASKA	R/W	Enable propagation of REIL_NZ_PEND to the WIS0 interrupt 0 = Disable 1 = Enable	0x0
1	REIP_NZ_MASKA	R/W	Enable propagation of REIP_NZ_PEND to the WIS0 interrupt 0 = Disable 1 = Enable	0x0

2.9.14.8 E-WIS Interrupt Mask B 2

Short Name:EWIS_INTR_MASKB_2

Address:0x2EE06

Table 865 • **E-WIS Interrupt Mask B 2**

Bit	Name	Access	Description	Default
14	PMTICK_MASKB	R/W	Enable propagation of PMTICK_PEND to the WIS1 interrupt 0 = Disable 1 = Enable	0x0
10	UNEQP_MASKB	R/W	Enable propagation of UNEQP_PEND to the WIS1 interrupt 0 = Disable 1 = Enable	0x0
9	FEUNEQP_MASKB	R/W	Enable propagation of FEUNEQP_PEND to the WIS1 interrupt 0 = Disable 1 = Enable	0x0

Table 865 • **E-WIS Interrupt Mask B 2 *(continued)***

Bit	Name	Access	Description	Default
8	FERDIP_MASKB	R/W	Enable propagation of FERDIP_PEND to the WIS1 interrupt 0 = Disable 1 = Enable	0x0
7	B1_NZ_MASKB	R/W	Enable propagation of B1_NZ_PEND to the WIS1 interrupt 0 = Disable 1 = Enable	0x0
6	B2_NZ_MASKB	R/W	Enable propagation of B2_NZ_PEND to the WIS1 interrupt 0 = Disable 1 = Enable	0x0
5	B3_NZ_MASKB	R/W	Enable propagation of B3_NZ_PEND to the WIS1 interrupt 0 = Disable 1 = Enable	0x0
4	REIL_MASKB	R/W	Enable propagation of REIL_PEND to the WIS1 interrupt 0 = Disable 1 = Enable	0x0
3	REIP_MASKB	R/W	Enable propagation of REIP_PEND to the WIS1 interrupt 0 = Disable 1 = Enable	0x0
2	REIL_NZ_MASKB	R/W	Enable propagation of REIL_NZ_PEND to the WIS1 interrupt 0 = Disable 1 = Enable	0x0
1	REIP_NZ_MASKB	R/W	Enable propagation of REIP_NZ_PEND to the WIS1 interrupt 0 = Disable 1 = Enable	0x0

2.9.14.9 WIS Fault Mask

Short Name:WIS_FAULT_MASK

Address:0x2EE07

Table 866 • **WIS_FAULT_MASK**

Bit	Name	Access	Description	Default
10	WIS_FAULT_ON_FEPLMP	R/W	Selects if the far-end PLM-P condition triggers the WIS fault alarm (WIS_STAT1.FAULT register) 0 = No trigger 1 = Triggers WIS_FAULT	0x0
9	WIS_FAULT_ON_FEAISP	R/W	Selects if the far-end AIS-P condition triggers the WIS fault alarm (WIS_STAT1.FAULT register) 0 = No trigger 1 = Triggers WIS_FAULT	0x0

Table 866 • **WIS_FAULT_MASK *(continued)***

Bit	Name	Access	Description	Default
8	WIS_FAULT_ON_RDIL	R/W	Selects if the RDI-L condition triggers the WIS fault alarm (WIS_STAT1.FAULT register) 0 = No trigger 1 = Triggers WIS_FAULT	0x0
7	WIS_FAULT_ON_SEF	R/W	Selects if the SEF condition triggers the WIS fault alarm (WIS_STAT1.FAULT register) 0 = No trigger 1 = Triggers WIS_FAULT	0x1
6	WIS_FAULT_ON_LOF	R/W	Selects if the LOF condition triggers the WIS fault alarm (WIS_STAT1.FAULT register) 0 = No trigger 1 = Triggers WIS_FAULT	0x1
5	WIS_FAULT_ON_LOS	R/W	Selects if the LOS condition triggers the WIS fault alarm (WIS_STAT1.FAULT register) 0 = No trigger 1 = Triggers WIS_FAULT	0x1
4	WIS_FAULT_ON_AISL	R/W	Selects if the AIS-L condition triggers the WIS fault alarm (WIS_STAT1.FAULT register) 0 = No trigger 1 = Triggers WIS_FAULT	0x1
3	WIS_FAULT_ON_LCDP	R/W	Selects if the LCD-P condition triggers the WIS fault alarm (WIS_STAT1.FAULT register) 0 = No trigger 1 = Triggers WIS_FAULT	0x1
2	WIS_FAULT_ON_PLMP	R/W	Selects if the PLM-P condition triggers the WIS fault alarm (WIS_STAT1.FAULT register) 0 = No trigger 1 = Triggers WIS_FAULT	0x1
1	WIS_FAULT_ON_AISP	R/W	Selects if the AIS-P condition triggers the WIS fault alarm (WIS_STAT1.FAULT register) 0 = No trigger 1 = Triggers WIS_FAULT	0x1
0	WIS_FAULT_ON_LOPP	R/W	Selects if the LOP-P condition triggers the WIS fault alarm (WIS_STAT1.FAULT register) 0 = No trigger 1 = Triggers WIS_FAULT	0x1

2.9.14.10 E-WIS Interrupt Pending 3

Short Name:EWIS_INTR_PEND3

Address:0x2EE08

Table 867 • **E-WIS Interrupt Pending 3**

Bit	Name	Access	Description	Default
4	REIP_THRESH_PEND	Sticky	The interrupt pending bit is asserted when the REI-P threshold error level is exceeded (REIP_THRESH_ERR=1). The sticky bit is cleared when a 1 is written to the register bit. 0 = A counter threshold error has not occurred 1 = A counter threshold error occurred	0x0

Table 867 • **E-WIS Interrupt Pending 3 *(continued)***

Bit	Name	Access	Description	Default
3	REIL_THRESH_PEND	Sticky	The interrupt pending bit is asserted when the REI-L threshold error level is exceeded (REIL_THRESH_ERR=1). The sticky bit is cleared when a 1 is written to the register bit. 0 = A counter threshold error has not occurred 1 = A counter threshold error occurred	0x0
2	B1_THRESH_PEND	Sticky	The interrupt pending bit is asserted when the B1 PMTICK threshold error level is exceeded (B1_THRESH_ERR=1). The sticky bit is cleared when a 1 is written to the register bit. 0 = A counter threshold error has not occurred 1 = A counter threshold error occurred	0x0
1	B2_THRESH_PEND	Sticky	The interrupt pending bit is asserted when the B2 PMTICK threshold error level is exceeded (B2_THRESH_ERR=1). The sticky bit is cleared when a 1 is written to the register bit. 0 = A counter threshold error has not occurred 1 = A counter threshold error occurred	0x0
0	B3_THRESH_PEND	Sticky	The interrupt pending bit is asserted when the B3 PMTICK threshold error level is exceeded (B3_THRESH_ERR=1). The sticky bit is cleared when a 1 is written to the register bit. 0 = A counter threshold error has not occurred 1 = A counter threshold error occurred	0x0

2.9.14.11 E-WIS Interrupt Mask A 3

Short Name:EWIS_INTR_MASKA_3

Address:0x2EE09

Table 868 • **E-WIS Interrupt Mask A 3**

Bit	Name	Access	Description	Default
4	REIP_THRESH_MASKA	R/W	Enable propagation of REIP_THRESH_PEND to the WIS0 interrupt 0 = Disable 1 = Enable	0x0
3	REIL_THRESH_MASKA	R/W	Enable propagation of REIL_THRESH_PEND to the WIS0 interrupt 0 = Disable 1 = Enable	0x0
2	B1_THRESH_MASKA	R/W	Enable propagation of B1_THRESH_PEND to the WIS0 interrupt 0 = Disable 1 = Enable	0x0
1	B2_THRESH_MASKA	R/W	Enable propagation of B2_THRESH_PEND to the WIS0 interrupt 0 = Disable 1 = Enable	0x0

Table 868 • **E-WIS Interrupt Mask A 3 *(continued)***

Bit	Name	Access	Description	Default
0	B3_THRESH_MASKA	R/W	Enable propagation of B3_THRESH_PEND to the WIS0 interrupt 0 = Disable 1 = Enable	0x0

2.9.14.12 E-WIS Interrupt Mask B 3

Short Name:EWIS_INTR_MASKB_3

Address:0x2EE0A

Table 869 • **E-WIS Interrupt Mask B 3**

Bit	Name	Access	Description	Default
4	REIP_THRESH_MASKB	R/W	Enable propagation of REIP_THRESH_PEND to the WIS1 interrupt 0 = Disable 1 = Enable	0x0
3	REIL_THRESH_MASKB	R/W	Enable propagation of REIL_THRESH_PEND to the WIS1 interrupt 0 = Disable 1 = Enable	0x0
2	B1_THRESH_MASKB	R/W	Enable propagation of B1_THRESH_PEND to the WIS1 interrupt 0 = Disable 1 = Enable	0x0
1	B2_THRESH_MASKB	R/W	Enable propagation of B2_THRESH_PEND to the WIS1 interrupt 0 = Disable 1 = Enable	0x0
0	B3_THRESH_MASKB	R/W	Enable propagation of B3_THRESH_PEND to the WIS1 interrupt 0 = Disable 1 = Enable	0x0

2.9.14.13 Threshold Error Status

Short Name:THRESH_ERR_STAT

Address:0x2EE0B

Table 870 • **Threshold Error Status**

Bit	Name	Access	Description	Default
4	REIP_THRESH_ERR	R/O	Indicates when the REI-P PMTICK counter exceeds the threshold level defined in REIP_THRESH_ERR. The threshold is compared to an internal error accumulator, not the value captured and stored in REIP_ERR_CNT. 0 = Counter does not exceed threshold level 1 = Counter exceeds threshold level	0x0

Table 870 • **Threshold Error Status *(continued)***

Bit	Name	Access	Description	Default
3	REIL_THRESH_ERR	R/O	Indicates when the REI-L PMTICK counter exceeds the threshold level defined in REIL_THRESH_ERR. The threshold is compared to an internal error accumulator, not the value captured and stored in REIL_ERR_CNT. 0 = Counter does not exceed threshold level 1 = Counter exceeds threshold level	0x0
2	B1_THRESH_ERR	R/O	Indicates when the B1 PMTICK counter exceeds the threshold level defined in B1_THRESH_ERR. The threshold is compared to an internal error accumulator, not the value captured and stored in B1_ERR_CNT. 0 = Counter does not exceed threshold level 1 = Counter exceeds threshold level	0x0
1	B2_THRESH_ERR	R/O	Indicates when the B2 PMTICK counter exceeds the threshold level defined in B2_THRESH_ERR. The threshold is compared to an internal error accumulator, not the value captured and stored in B2_ERR_CNT. 0 = Counter does not exceed threshold level 1 = Counter exceeds threshold level	0x0
0	B3_THRESH_ERR	R/O	Indicates when the B3 PMTICK counter exceeds the threshold level defined in B3_THRESH_ERR. The threshold is compared to an internal error accumulator, not the value captured and stored in B3_ERR_CNT. 0 = Counter does not exceed threshold level 1 = Counter exceeds threshold level	0x0

2.9.14.14 WIS REI-P Threshold Level 1

Short Name:WIS_REIP_THRESH_LVL1

Address:0x2EE10

Table 871 • **WIS REI-P Threshold Level 1**

Bit	Name	Access	Description	Default
15:0	REIP_THRESH_LVL_MSW	R/W	REIP_THRESH_ERR is asserted when the REI-P PMTICK error counter is greater than the REI-P threshold level defined by this register and the next register.	0xFFFF

2.9.14.15 WIS REI-P Threshold Level 0

Short Name:WIS_REIP_THRESH_LVL0

Address:0x2EE11

Table 872 • **WIS REI-P Threshold Level 0**

Bit	Name	Access	Description	Default
15:0	REIP_THRESH_LVL_LSW	R/W	REIP_THRESH_ERR is asserted when the REI-P PMTICK error counter is greater than the REI-P threshold level defined by this register and the previous register.	0xFFFF

2.9.14.16 WIS REI-L Threshold Level 1

Short Name:WIS_REIL_THRESH_LVL1

Address:0x2EE12

Table 873 • **WIS REI-L Threshold Level 1**

Bit	Name	Access	Description	Default
15:0	REIL_THRESH_LVL_MSW	R/W	REIL_THRESH_ERR is asserted when the REI-L PMTICK error counter is greater than the REI-L threshold level defined by this register and the next register.	0xFFFF

2.9.14.17 WIS REI-L Threshold Level 0

Short Name:WIS_REIL_THRESH_LVL0

Address:0x2EE13

Table 874 • **WIS REI-L Threshold Level 0**

Bit	Name	Access	Description	Default
15:0	REIL_THRESH_LVL_LSW	R/W	REIL_THRESH_ERR is asserted when the REI-L PMTICK error counter is greater than the REI-L threshold level defined by this register and the previous register.	0xFFFF

2.9.14.18 WIS B1 Threshold Level 1

Short Name:WIS_B1_THRESH_LVL1

Address:0x2EE14

Table 875 • **WIS B1 Threshold Level 1**

Bit	Name	Access	Description	Default
15:0	B1_THRESH_LVL_MSW	R/W	B1_THRESH_ERR is asserted when the B1 PMTICK error counter is greater than the B1 threshold level defined by this register and the next register.	0xFFFF

2.9.14.19 WIS B1 Threshold Level 0

Short Name:WIS_B1_THRESH_LVL0

Address:0x2EE15

Table 876 • **WIS B1 Threshold Level 0**

Bit	Name	Access	Description	Default
15:0	B1_THRESH_LVL_LSW	R/W	B1_THRESH_ERR is asserted when the B1 PMTICK error counter is greater than the B1 threshold level defined by this register and the previous register.	0xFFFF

2.9.14.20 WIS B2 Threshold Level 1

Short Name:WIS_B2_THRESH_LVL1

Address:0x2EE16

Table 877 • **WIS B2 Threshold Level 1**

Bit	Name	Access	Description	Default
15:0	B2_THRESH_LVL_MSW	R/W	B2_THRESH_ERR is asserted when the B2 PMTICK error counter is greater than the B2 threshold level defined by this register and the next register.	0xFFFF

2.9.14.21 WIS B2 Threshold Level 0

Short Name:WIS_B2_THRESH_LVL0

Address:0x2EE17

Table 878 • **WIS B2 Threshold Level 0**

Bit	Name	Access	Description	Default
15:0	B2_THRESH_LVL_LSW	R/W	B2_THRESH_ERR is asserted when the B2 PMTICK error counter is greater than the B2 threshold level defined by this register and the previous register.	0xFFFF

2.9.14.22 WIS B3 Threshold Level 1

Short Name:WIS_B3_THRESH_LVL1

Address:0x2EE18

Table 879 • **WIS B3 Threshold Level 1**

Bit	Name	Access	Description	Default
15:0	B3_THRESH_LVL_MSW	R/W	B3_THRESH_ERR is asserted when the B3 PMTICK error counter is greater than the B3 threshold level defined by this register and the next register.	0xFFFF

2.9.14.23 WIS B3 Threshold Level 0

Short Name:WIS_B3_THRESH_LVL0

Address:0x2EE19

Table 880 • **WIS B3 Threshold Level 0**

Bit	Name	Access	Description	Default
15:0	B3_THRESH_LVL_LSW	R/W	B3_THRESH_ERR is asserted when the B3 PMTICK error counter is greater than the B3 threshold level defined by this register and the previous register.	0xFFFF

2.10 LINE_PCS10G (Device 0x3)

Table 881 • **PCS_Control_1**

Address	Short Description	Register Name	Details
0x30000	PCS Control 1	PCS_Control_1	Page 343

Table 882 • **PCS_Status_1**

Address	Short Description	Register Name	Details
0x30001	PCS Status 1	PCS_Status_1	Page 344

Table 883 • **PCS_Device_Identifier**

Address	Short Description	Register Name	Details
0x30002	PCS Device Identifier 1	PCS_Device_Identifier_1	Page 344
0x30003	PCS Device Identifier 2	PCS_Device_Identifier_2	Page 345

Table 884 • **PCS_Speed_Ability**

Address	Short Description	Register Name	Details
0x30004	PCS Speed Ability	PCS_Speed_Ability	Page 345

Table 885 • **PCS_Devices_in_Package_1**

Address	Short Description	Register Name	Details
0x30005	PCS Devices in Package 1	PCS_Devices_in_Package_1	Page 345

Table 886 • **PCS_Devices_in_Package_2**

Address	Short Description	Register Name	Details
0x30006	PCS Devices in Package 2	PCS_Devices_in_Package_2	Page 346

Table 887 • **PCS_Control_2**

Address	Short Description	Register Name	Details
0x30007	PCS Control 2	PCS_Control_2	Page 346

Table 888 • **PCS_Status_2**

Address	Short Description	Register Name	Details
0x30008	PCS Status 2	PCS_Status_2	Page 346

Table 889 • **PCS_Package_Identifier**

Address	Short Description	Register Name	Details
0x3000E	PCS Package Identifier 1	PCS_Package_Identifier_1	Page 347
0x3000F	PCS Package Identifier 2	PCS_Package_Identifier_2	Page 347

Table 890 • **Eth_10Gbase_X_Status**

Address	Short Description	Register Name	Details
0x30018	Eth_10Gbase-X Status	Eth_10Gbase_X_Status	Page 348

Table 891 • **Eth_10Gbase_X_Control**

Address	Short Description	Register Name	Details
0x30019	Eth_10Gbase-X Control	Eth_10Gbase_X_Control	Page 348

Table 892 • **Eth_10GBASE_R_PCS_Status_1**

Address	Short Description	Register Name	Details
0x30020	Eth_10Gbase-R PCS Status 1	Eth_10GBASE_R_PCS_Status_1	Page 348

Table 893 • **Eth_10GBASE_R_PCS_Status_2**

Address	Short Description	Register Name	Details
0x30021	Eth_10Gbase-R PCS Status 2	Eth_10GBASE_R_PCS_Status_2	Page 348

Table 894 • **Eth_10GBASE_R_PCS_Test_Pattern_Seed_A**

Address	Short Description	Register Name	Details
0x30022	Eth_10Gbase-R PCS Test Pattern Seed A 0	Eth_10GBASE_R_PCS_Test_Pattern_Seed_A_0	Page 349
0x30023	Eth_10Gbase-R PCS Test Pattern Seed A 1	Eth_10GBASE_R_PCS_Test_Pattern_Seed_A_1	Page 349
0x30024	Eth_10Gbase-R PCS Test Pattern Seed A 2	Eth_10GBASE_R_PCS_Test_Pattern_Seed_A_2	Page 349

Table 894 • **Eth_10GBASE_R_PCS_Test_Pattern_Seed_A *(continued)***

Address	Short Description	Register Name	Details
0x30025	Eth_10Gbase-R PCS Test Pattern Seed A 3	Eth_10GBASE_R_PCS_Test_Pattern_Seed_A_3	Page 349

Table 895 • **Eth_10GBASE_R_PCS_Test_Pattern_Seed_B**

Address	Short Description	Register Name	Details
0x30026	Eth_10Gbase-R PCS Test Pattern Seed B 0	Eth_10GBASE_R_PCS_Test_Pattern_Seed_B_0	Page 350
0x30027	Eth_10Gbase-R PCS Test Pattern Seed B 1	Eth_10GBASE_R_PCS_Test_Pattern_Seed_B_1	Page 350
0x30028	Eth_10Gbase-R PCS Test Pattern Seed B 2	Eth_10GBASE_R_PCS_Test_Pattern_Seed_B_2	Page 350
0x30029	Eth_10Gbase-R PCS Test Pattern Seed B 3	Eth_10GBASE_R_PCS_Test_Pattern_Seed_B_3	Page 350

Table 896 • **Eth_10GBASE_R_PCS_test_pattern_control**

Address	Short Description	Register Name	Details
0x3002A	Eth_10Gbase-R PCS Test-Pattern Control	Eth_10GBASE_R_PCS_test_pattern_control	Page 350

Table 897 • **Eth_10GBASE_R_PCS_test_pattern_counter**

Address	Short Description	Register Name	Details
0x3002B	Eth_10Gbase-R PCS Test-Pattern Counter	Eth_10GBASE_R_PCS_test_pattern_counter	Page 351

Table 898 • **USR_Test**

Address	Short Description	Register Name	Details
0x38000	USR Test 0	USR_Test_0	Page 351
0x38001	USR Test 1	USR_Test_1	Page 352
0x38002	USR Test 2	USR_Test_2	Page 352
0x38003	USR Test 3	USR_Test_3	Page 352

Table 899 • **Square_Wave_Pulse_Width**

Address	Short Description	Register Name	Details
0x38004	Square Wave Pulse Width	Square_Wave_Pulse_Width	Page 352

Table 900 • **PCS_Control_3**

Address	Short Description	Register Name	Details
0x38005	PCS Control 3	PCS_Control_3	Page 352

Table 901 • **Test_Error_Counter**

Address	Short Description	Register Name	Details
0x38007	Test Error Counter 0	Test_Error_Counter_0	Page 353
0x38008	Test Error Counter 1	Test_Error_Counter_1	Page 353

Table 902 • **PCS_TX_SEQ_ERR_CNT**

Address	Short Description	Register Name	Details
0x38010	PCS Tx Sequencing Error Count	PCS_TX_SEQ_ERR_CNT	Page 354

Table 903 • **PCS_RX_SEQ_ERR_CNT**

Address	Short Description	Register Name	Details
0x38011	PCS Rx Sequencing Error Count	PCS_RX_SEQ_ERR_CNT	Page 354

Table 904 • **PCS_TX_BLK_ENC_ERR_CNT**

Address	Short Description	Register Name	Details
0x38012	PCS Tx Block Encode Error Count	PCS_TX_BLK_ENC_ERR_CNT	Page 354

Table 905 • **PCS_PCS_RX_BLK_DEC_ERR_CNT**

Address	Short Description	Register Name	Details
0x38013	PCS Rx Block Decode Error Count	PCS_PCS_RX_BLK_DEC_ERR_CNT	Page 354

Table 906 • **PCS_TX_CHAR_ENC_ERR_CNT**

Address	Short Description	Register Name	Details
0x38014	PCS Tx Character Encode Error Count	PCS_TX_CHAR_ENC_ERR_CNT	Page 355

Table 907 • **PCS_RX_CHAR_DEC_ERR_CNT**

Address	Short Description	Register Name	Details
0x38015	PCS Rx Character Decode Error Count	PCS_RX_CHAR_DEC_ERR_CNT	Page 355

Table 908 • **Loopback_FIFOs_Stat_Ctrl**

Address	Short Description	Register Name	Details
0x38016	Loopback FIFOs Stat/Ctrl	Loopback_FIFOs_Stat_Ctrl	Page 355

Table 909 • **PCS_Control_4**

Address	Short Description	Register Name	Details
0x38600	PCS Control 4	PCS_Control_4	Page 355

Table 910 • **PCS_Control_5**

Address	Short Description	Register Name	Details
0x38601	PCS Control 5	PCS_Control_5	Page 356

Table 911 • **PCS_LF_filt_linkup_timer**

Address	Short Description	Register Name	Details
0x38602	PCS LF_filt linkup Timer	PCS_LF_filt_linkup_timer	Page 356

Table 912 • **PCS_LF_filt_linkdown_timer**

Address	Short Description	Register Name	Details
0x38603	PCS LF_filt Linkdown Timer	PCS_LF_filt_linkdown_timer	Page 356

Table 913 • **PCS_INTR_PEND1**

Address	Short Description	Register Name	Details
0x38E00	PCS Interrupt Pending 1	PCS_INTR_PEND1	Page 357

Table 914 • **PCS_INTR_MASK1**

Address	Short Description	Register Name	Details
0x38E01	PCS Interrupt Mask 1	PCS_INTR_MASK1	Page 358

Table 915 • **PCS_INTR_STATUS**

Address	Short Description	Register Name	Details
0x38E03	PCS Interrupt Status Signals	PCS_INTR_STATUS	Page 359

Table 916 • **INTR_THRESHOLD_LEVEL**

Address	Short Description	Register Name	Details
0x38E04	Tx Sequencing Error Count Threshold	TX_SEQ_ERR_CNT_THRESH	Page 361

Table 916 • **INTR_THRESHOLD_LEVEL *(continued)***

Address	Short Description	Register Name	Details
0x38E05	Rx Sequencing Error Count Threshold	RX_SEQ_ERR_CNT_THRESH	Page 361
0x38E06	Tx Block Encode Error Count Threshold	TX_BLK_ENC_ERR_CNT_THRESH	Page 361
0x38E07	Rx Block Decode Error Count Threshold	RX_BLK_DEC_ERR_CNT_THRESH	Page 362
0x38E08	Tx Character Encode Error Count Threshold	TX_CHAR_ENC_ERR_CNT_THRESH	Page 362
0x38E09	Rx Character Decode Error Count Threshold	RX_CHAR_DEC_ERR_CNT_THRESH	Page 362
0x38E0A	FEC Fixed Error Count Threshold 1	FEC_FIXED_ERR_CNT_THRESH1	Page 362
0x38E0B	FEC Fixed Error Count Threshold 0	FEC_FIXED_ERR_CNT_THRESH0	Page 362
0x38E0C	FEC Unfixable Error Count Threshold 1	FEC_UNFIXED_ERR_CNT_THRESH1	Page 363
0x38E0D	FEC Unfixable Error Count Threshold 0	FEC_UNFIXED_ERR_CNT_THRESH0	Page 363

2.10.1 Standard PCS-10G

2.10.1.1 PCS Control 1

Short Name:PCS_Control_1

Address:0x30000

Table 917 • **PCS Control 1**

Bit	Name	Access	Description	Default
15	SOFT_RST	One-shot	MDIO Manageable Device (MMD) software reset. Reset all logic in the channel between the host side PMA and the line side PMA, regardless of the cross-connect configuration. Data path logic and configuration registers are reset. 0: Normal operation 1: Reset	0x0
14	PCS_System_loopback	R/W	PCS System loopback. Loopback of 64b encoded and scrambled data 0: Disable PCS loopback mode 1: Enable PCS loopback mode	0x0
13	Speed_selection	R/O	0: Unspecified 1: Operation at 10 Gb/s and above	0x1

Table 917 • **PCS Control 1 *(continued)***

Bit	Name	Access	Description	Default
11	LOW_PWR_PCS	R/W	The channel's data path is placed into low power mode with this register. The PMA in this channel is also placed into low power mode regardless of the channel cross connect configuration. The PMD_TRANSMIT_DISABLE.GLOBAL_PMD_TRANSMIT_DISABLE register state can can be transmitted from a GPIO pin to shut off an optics module's Tx driver. 0: Normal Operation 1: Low Power Mode	0x0
6	Speed_selection_idx2	R/O	0: Unspecified 1: Operation at 10 Gb/s and above	0x1
5:2	Speed_selection_idx3	R/O	1xxx: Reserved. x1xx: Reserved. xx1x: Reserved. 0001: Reserved. 0000: 10 Gbps	0x0

2.10.1.2 PCS Status 1

Short Name:PCS_Status_1

Address:0x30001

Table 918 • **PCS Status 1**

Bit	Name	Access	Description	Default
7	Fault	R/O	0: Fault condition not detected. (PCS receive local fault (PCS_Status_2.Receive_fault) = 0) AND (PCS transmit local fault (PCS_Status_2.Transmit_fault) = 0) 1: Fault condition detected. (PCS receive local fault (PCS_Status_2.Receive_fault) = 1) OR (PCS transmit local fault (PCS_Status_2.Transmit_fault) = 1)	0x0
2	PCS_receive_link_status	R/O	This is a sticky bit that latches the low state. The latch-low bit is cleared when the register is read. 0: PCS received link down. BLOCK_LOCK=0 OR HI_BER=1 1: PCS receive link up. BLOCK_LOCK=1 AND HI_BER=0.	0x1
1	Low_power_ability	R/O	0: PCS does not support low power mode 1: PCS supports low power mode	0x1

2.10.1.3 PCS Device Identifier 1

Short Name:PCS_Device_Identifier_1

Address:0x30002

Table 919 • **PCS Device Identifier 1**

Bit	Name	Access	Description	Default
15:0	PCS_Device_Identifier_1	R/O	Upper 16 bits of a 32-bit unique PCS device identifier. Bits 3-18 of the device manufacturer's OUI.	0x0007

2.10.1.4 PCS Device Identifier 2

Short Name:PCS_Device_Identifier_2

Address:0x30003

Table 920 • **PCS Device Identifier 2**

Bit	Name	Access	Description	Default
15:0	PCS_Device_Identifier_2	R/O	Lower 16 bits of a 32-bit unique PCS device identifier. Bits 19-24 of the device manufacturer's OUI. Six-bit model number, and a four-bit revision number.	0x0400

2.10.1.5 PCS Speed Ability

Short Name:PCS_Speed_Ability

Address:0x30004

Table 921 • **PCS Speed Ability**

Bit	Name	Access	Description	Default
0	is_10G_capable	R/O	0: Not capable of 10Gbps 1: Capable of 10Gbps	0x1

2.10.1.6 PCS Devices in Package 1

Short Name:PCS_Devices_in_Package_1

Address:0x30005

Table 922 • **PCS Devices in Package 1**

Bit	Name	Access	Description	Default
5	DTE_XS_present	R/O	Indicates whether DTE XS is present in the package 0: Not present 1: Present	0x0
4	PHY_XS_present	R/O	Indicates whether PHY XS is present in the package 0: Not present 1: Present	0x1
3	PCS_present	R/O	Indicates whether PCS is present in the package 0: Not present 1: Present	0x1

Table 922 • **PCS Devices in Package 1 *(continued)***

Bit	Name	Access	Description	Default
2	WIS_present	R/O	Indicates whether WIS is present in the package 0: Not present 1: Present	0x1
1	PMD_PMA_present	R/O	Indicates whether PMA/PMD is present in the package 0: Not present 1: Present	0x1
0	Clause_22_registers_present	R/O	Indicates whether Clause 22 registers are present in the package 0: Not present 1: Present	0x0

2.10.1.7 PCS Devices in Package 2

Short Name:PCS_Devices_in_Package_2

Address:0x30006

Table 923 • **PCS Devices in Package 2**

Bit	Name	Access	Description	Default
15	Vendor_spec_dev_2_present	R/O	Indicates whether vendor specific device 2 is present in the package 0: Not present 1: Present	0x0
14	Vendor_spec_dev_1_present	R/O	Indicates whether vendor specific device 1 is present in the package 0: Not present 1: Present	0x0

2.10.1.8 PCS Control 2

Short Name:PCS_Control_2

Address:0x30007

Table 924 • **PCS Control 2**

Bit	Name	Access	Description	Default
1:0	Select_WAN_mode_or_10GBASE_R	R/W	Indicates the PCS type selected 11: Reserved 10: 10GBASE-W PCS 01: Reserved 00: 10GBASE-R PCS	0x0

2.10.1.9 PCS Status 2

Short Name:PCS_Status_2

Address:0x30008

Table 925 • **PCS Status 2**

Bit	Name	Access	Description	Default
15:14	Device_present	R/O	00: No device responding at this address 01: No device responding at this address 10: Device responding at this address 11: No device responding at this address	0xA
11	Transmit_fault	R/O	This is a sticky bit that latches the high state. The latch-high bit is cleared when the register is read. 0: No fault condition on transmit path 1: Fault condition on transmit path	0x0
10	Receive_fault	R/O	This is a sticky bit that latches the high state. The latch-high bit is cleared when the register is read. 0: No fault condition on receive path 1: Fault condition on receive path	0x0
2	is_10GBASE_W_ability	R/O	0: Not supported 1: Supported	0x1
1	is_10GBASE_X_ability	R/O	0: Not supported 1: Supported	0x0
0	is_10GBASE_R_ability	R/O	0: Not supported 1: Supported	0x1

2.10.1.10 PCS Package Identifier 1

Short Name:PCS_Package_Identifier_1

Address:0x3000E

Table 926 • **PCS Package Identifier 1**

Bit	Name	Access	Description	Default
15:0	PCS_package_identifier_1	R/O	Upper 16 bits of a 32-bit unique PCS package identifier. Bits 3-18 of the device manufacturer's OUI. Six-bit model number and a four-bit revision number.	0x0000

2.10.1.11 PCS Package Identifier 2

Short Name:PCS_Package_Identifier_2

Address:0x3000F

Table 927 • **PCS Package Identifier 2**

Bit	Name	Access	Description	Default
15:0	PCS_package_identifier_2	R/O	Lower 16 bits of a 32-bit unique PCS package identifier. Bits 19-24 of the device manufacturer's OUI. Six-bit model number and a four-bit revision number.	0x0000

2.10.1.12 Ethernet 10Gbase-X Status

Short Name: Eth_10Gbase_X_Status

Address:0x30018

Table 928 • **Eth_10Gbase-X Status**

Bit	Name	Access	Description	Default
15:0	is_10Gbase_X_Status	R/O	Not supported	0x0000

2.10.1.13 Ethernet 10Gbase-X Control

Short Name: Eth_10Gbase_X_Control

Address:0x30019

Table 929 • **Eth_10Gbase-X Control**

Bit	Name	Access	Description	Default
15:0	is_10Gbase_X_Control	R/O	Not supported	0x0000

2.10.1.14 Ethernet 10Gbase-R PCS Status 1

Short Name: Eth_10GBASE_R_PCS_Status_1

Address:0x30020

Table 930 • **Eth_10GBASE-R PCS Status 1**

Bit	Name	Access	Description	Default
12	is_10GBASE_R_receive_lock_status	R/O	0: 10GBASE-R PCS receive link down BLOCK_LOCK (Eth_10GBASE_R_PCS_Status_1.is_10GBASE_R_PCS_block_lock) = 0 OR BER_HI (Eth_10GBASE_R_PCS_Status_1.is_10GBASE_R_PCS_high_BER) = 1 1: 10GBASE-R PCS receive link up BLOCK_LOCK (Eth_10GBASE_R_PCS_Status_1.is_10GBASE_R_PCS_block_lock) = 1 AND BER_HI (Eth_10GBASE_R_PCS_Status_1.is_10GBASE_R_PCS_high_BER) = 0	0x0
2	PRBS31_pattern_testing_ability	R/O	0: PCS does not support PRBS31 pattern testing 1: PCS is able to support PRBS31 pattern testing	0x1
1	is_10GBASE_R_PCS_high_BER	R/O	0: 10GBASE-R PCS not reporting a high BER. 1: 10GBASE-R PCS reporting a high BER.	0x0
0	is_10GBASE_R_PCS_block_lock	R/O	0: 10GBASE-R PCS is not locked to receive blocks. 1: 10GBASE-R PCS is locked to receive blocks.	0x0

2.10.1.15 Ethernet 10Gbase-R PCS Status 2

Short Name: Eth_10GBASE_R_PCS_Status_2

Address:0x30021

Table 931 • **Eth_10GBASE-R PCS Status 2**

Bit	Name	Access	Description	Default
15	BLOCK_LOCK	R/O	This is a sticky bit that latches the low state. The latch-low bit is cleared when the register is read. 0: 10GBASE-R PCS does not have block lock 1: 10GBASE-R PCS has block lock	0x1
14	PCS_HIGHBER	R/O	This is a sticky bit that latches the high state. The latch-high bit is cleared when the register is read. 0: 10GBASE-R PCS has not reported a high BER 1: 10GBASE-R PCS has reported a high BER	0x0
13:8	BER	R/O	BER counter. The counter saturates when the maximum value is exceeded. The counter is cleared when the register is read.	0x00
7:0	PCS_ERRORED_BLOCKS	R/O	Errored blocks counter. The counter saturates when the maximum value is exceeded. The counter is cleared when the register is read.	0x00

2.10.1.16 Ethernet 10Gbase-R PCS Test Pattern Seed A 0

Short Name: Eth_10GBASE_R_PCS_Test_Pattern_Seed_A_0

Address:0x30022

Table 932 • **Eth_10Gbase-R PCS Test Pattern Seed A 0**

Bit	Name	Access	Description	Default
15:0	PCS_SEEDA_0	R/W	Test pattern seed A bits 0-15	0x0000

2.10.1.17 Ethernet 10Gbase-R PCS Test Pattern Seed A 1

Short Name: Eth_10GBASE_R_PCS_Test_Pattern_Seed_A_1

Address:0x30023

Table 933 • **Eth_10Gbase-R PCS Test Pattern Seed A 1**

Bit	Name	Access	Description	Default
15:0	PCS_SEEDA_1	R/W	Test pattern seed A bits 16-31	0x0000

2.10.1.18 Ethernet 10Gbase-R PCS Test Pattern Seed A 2

Short Name: Eth_10GBASE_R_PCS_Test_Pattern_Seed_A_2

Address:0x30024

Table 934 • **Eth_10Gbase-R PCS Test Pattern Seed A 2**

Bit	Name	Access	Description	Default
15:0	PCS_SEEDA_2	R/W	Test pattern seed A bits 32-47	0x0000

2.10.1.19 Ethernet 10Gbase-R PCS Test Pattern Seed A 3

Short Name: Eth_10GBASE_R_PCS_Test_Pattern_Seed_A_3

Address:0x30025

Table 935 • **Eth_10Gbase-R PCS Test Pattern Seed A 3**

Bit	Name	Access	Description	Default
9:0	PCS_SEEDA_3	R/W	Test pattern seed A bits 48-57	0x000

2.10.1.20 Ethernet 10Gbase-R PCS Test Pattern Seed B 0

Short Name: Eth_10GBASE_R_PCS_Test_Pattern_Seed_B_0

Address:0x30026

Table 936 • **Eth_10Gbase-R PCS Test Pattern Seed B 0**

Bit	Name	Access	Description	Default
15:0	PCS_SEEDB_0	R/W	Test pattern seed B bits 0-15	0x0000

2.10.1.21 Ethernet 10Gbase-R PCS Test Pattern Seed B 1

Short Name: Eth_10GBASE_R_PCS_Test_Pattern_Seed_B_1

Address:0x30027

Table 937 • **Eth_10Gbase-R PCS Test Pattern Seed B 1**

Bit	Name	Access	Description	Default
15:0	PCS_SEEDB_1	R/W	Test pattern seed B bits 16-31	0x0000

2.10.1.22 Ethernet 10GBASE-R PCS Test Pattern Seed B 2

Short Name: Eth_10GBASE_R_PCS_Test_Pattern_Seed_B_2

Address:0x30028

Table 938 • **Eth_10GBASE-R PCS Test Pattern Seed B 2**

Bit	Name	Access	Description	Default
15:0	PCS_SEEDB_2	R/W	Test pattern seed B bits 32-47	0x0000

2.10.1.23 Ethernet 10Gbase-R PCS Test Pattern Seed B 3

Short Name: Eth_10GBASE_R_PCS_Test_Pattern_Seed_B_3

Address:0x30029

Table 939 • **Eth_10Gbase-R PCS Test Pattern Seed B 3**

Bit	Name	Access	Description	Default
9:0	PCS_SEEDB_3	R/W	Test pattern seed B bits 48-57	0x000

2.10.1.24 Ethernet 10Gbase-R PCS Test Pattern Control

Short Name: Eth_10GBASE_R_PCS_test_pattern_control

Address:0x3002A

Table 940 • **Eth_10Gbase-R PCS Test-Pattern Control**

Bit	Name	Access	Description	Default
5	PCS_PRBS31_ANA	R/W	0: Disable PRBS31 test pattern mode on the receive path 1: Enable PRBS31 test pattern mode on the receive path	0x0
4	PCS_PRBS31_GEN	R/W	0: Disable PRBS31 test pattern mode on the transmit path 1: Enable PRBS31 test pattern mode on the transmit path	0x0
3	PCS_TSTPAT_GEN	R/W	0: Disable transmit test pattern 1: Enable transmit test pattern	0x0
2	PCS_TSTPAT_ENA	R/W	0: Disable receive test pattern 1: Enable receive test pattern	0x0
1	PCS_TSTPAT_SEL	R/W	0: Pseudo random test pattern 1: Square wave test pattern	0x0
0	PCS_TSTDAT_SEL	R/W	0: LF data pattern 1: Zero data pattern	0x0

2.10.1.25 Ethernet 10GBASE-R PCS Test Pattern Counter

Short Name: Eth_10GBASE_R_PCS_test_pattern_counter

Address:0x3002B

Table 941 • **Eth_10Gbase-R PCS Test-Pattern Counter**

Bit	Name	Access	Description	Default
15:0	PCS_ERR_CNT	R/O	(COR) Error counter This is the 16-bit test pattern error counter defined by IEEE. The counter is cleared upon read of this register. There is a 32-bit version of this counter in registers Test_Error_Counter_0 and Test_Error_Counter_1. If reading the 32-bit version, read Test_Error_Counter_1, followed by Test_Error_Counter_0. A read of register Test_Error_Counter_0 or Eth_10GBASE_R_PCS_test_pattern_counter will clear the 32-bit error counter.	0x0000

2.10.2 Extended PCS-10G

2.10.2.1 USR Test 0

Short Name:USR_Test_0

Address:0x38000

Table 942 • **USR Test 0**

Bit	Name	Access	Description	Default
15:0	PCS_USRPAT_0	R/W	User-defined data pattern [15:0]	0x0000

2.10.2.2 USR Test 1

Short Name:USR_Test_1

Address:0x38001

Table 943 • **USR Test 1**

Bit	Name	Access	Description	Default
15:0	PCS_USRPAT_1	R/W	User-defined data pattern [31:16]	0x0000

2.10.2.3 USR Test 2

Short Name:USR_Test_2

Address:0x38002

Table 944 • **USR Test 2**

Bit	Name	Access	Description	Default
15:0	PCS_USRPAT_2	R/W	User-defined data pattern [47:32]	0x0000

2.10.2.4 USR Test 3

Short Name:USR_Test_3

Address:0x38003

Table 945 • **USR Test 3**

Bit	Name	Access	Description	Default
15:0	PCS_USRPAT_3	R/W	User-defined data pattern [63:48]	0x0000

2.10.2.5 Square Wave Pulse Width

Short Name: Square_Wave_Pulse_Width

Address:0x38004

Table 946 • **Square Wave Pulse Width**

Bit	Name	Access	Description	Default
3:0	PCS_SQPW	R/W	Square wave pulse width	0x0

2.10.2.6 PCS Control 3

Short Name:PCS_Control_3

Address:0x38005

Table 947 • **PCS Control 3**

Bit	Name	Access	Description	Default
10	DSCR_DIS	R/W	0: Enable 1: Disable	0x0
9	SCR_DIS	R/W	0: Enable 1: Disable	0x0
5	Disable_RX_block_sequence_check	R/W	0: Blocks errors are generated when an invalid block sequence is encountered in the Rx path 1: Blocks errors are not generated when an invalid block sequence is encountered in the Rx path	0x0
4	Disable_TX_block_sequence_check	R/W	0: Blocks errors are generated when an invalid block sequence is encountered in the Tx path 1: Blocks errors are not generated when an invalid block sequence is encountered in the Tx path	0x0
0	PCS_USRPAT_ENA	R/W	User test pattern enable 0: Disable 1: Enable	0x0

2.10.2.7 Test Error Counter 0

Short Name: Test_Error_Counter_0

Address:0x38007

Table 948 • **Test Error Counter 0**

Bit	Name	Access	Description	Default
15:0	PCS_VSERR_CNT_0	R/O	(COR) Lower 16 bits of 32-bit version of PCS_ERR_CNT (Eth_10GBASE_R_PCS_test_pattern_counter) This register should only be read directly after reading Test_Error_Counter_1. Upon read of this register or Eth_10GBASE_R_PCS_test_pattern_counter, the 32-bit error counter is cleared.	0x0000

2.10.2.8 Test Error Counter 1

Short Name: Test_Error_Counter_1

Address:0x38008

Table 949 • **Test Error Counter 1**

Bit	Name	Access	Description	Default
15:0	PCS_VSERR_CNT_1	R/O	(COR) Upper 16 bits of 32-bit version of PCS_ERR_CNT (Eth_10GBASE_R_PCS_test_pattern_counter) This register should be read, followed immediately by Test_Error_Counter_0. Upon read of Test_Error_Counter_0 or Eth_10GBASE_R_PCS_test_pattern_counter, the 32-bit error counter is cleared.	0x0000

2.10.2.9 PCS Tx Sequencing Error Count

Short Name:PCS_TX_SEQ_ERR_CNT

Address:0x38010

Table 950 • **PCS Tx Sequencing Error Count**

Bit	Name	Access	Description	Default
15:0	TX_SEQ_ERR_CNT	R/O	Tx sequencing error count. The counter saturates when the maximum value is exceeded. The counter is cleared when the register is read.	0x0000

2.10.2.10 PCS Rx Sequencing Error Count

Short Name:PCS_RX_SEQ_ERR_CNT

Address:0x38011

Table 951 • **PCS Rx Sequencing Error Count**

Bit	Name	Access	Description	Default
15:0	RX_SEQ_ERR_CNT	R/O	Rx sequencing error count. The counter saturates when the maximum value is exceeded. The counter is cleared when the register is read.	0x0000

2.10.2.11 PCS Tx Block Encode Error Count

Short Name:PCS_TX_BLK_ENC_ERR_CNT

Address:0x38012

Table 952 • **PCS Tx Block Encode Error Count**

Bit	Name	Access	Description	Default
15:0	TX_BLK_ENC_ERR_CNT	R/O	Tx block encode error count. The counter saturates when the maximum value is exceeded. The counter is cleared when the register is read.	0x0000

2.10.2.12 PCS Rx Block Decode Error Count

Short Name:PCS_PCS_RX_BLK_DEC_ERR_CNT

Address:0x38013

Table 953 • **PCS Rx Block Decode Error Count**

Bit	Name	Access	Description	Default
15:0	PCS_RX_BLK_DEC_ERR_CNT	R/O	Rx block decode error count. The counter saturates when the maximum value is exceeded. The counter is cleared when the register is read.	0x0000

2.10.2.13 PCS Tx Character Encode Error Count

Short Name:PCS_TX_CHAR_ENC_ERR_CNT

Address:0x38014

Table 954 • **PCS Tx Character Encode Error Count**

Bit	Name	Access	Description	Default
15:0	TX_CHAR_ENC_ERR_CNT	R/O	Tx character encode error count. The counter saturates when the maximum value is exceeded. The counter is cleared when the register is read.	0x0000

2.10.2.14 PCS Rx Character Decode Error Count

Short Name:PCS_RX_CHAR_DEC_ERR_CNT

Address:0x38015

Table 955 • **PCS Rx Character Decode Error Count**

Bit	Name	Access	Description	Default
15:0	RX_CHAR_DEC_ERR_CNT	R/O	Rx character decode error count. The counter saturates when the maximum value is exceeded. The counter is cleared when the register is read.	0x0000

2.10.2.15 Loopback FIFO Status and Control

Short Name: Loopback_FIFOs_Stat_Ctrl

Address:0x38016

Table 956 • **Loopback FIFOs Stat/Ctrl**

Bit	Name	Access	Description	Default
1	Loop_64b_FIFO_Overflow	R/O	Loopback_64b FIFO overflow status. This is a sticky bit that latches the high state. The latch-high bit is cleared when the register is read. 0: normal operation 1: over/under flow condition	0x0
0	Loop_64b_FIFO_Sync_Inhibit	R/W	Selects whether loopback_64b FIFO's sync inhibit feature is enabled. 0: Disabled 1: Enabled	0x0

2.10.2.16 PCS Control 4

Short Name:PCS_Control_4

Address:0x38600

Table 957 • **PCS Control 4**

Bit	Name	Access	Description	Default
1	Disable_inversion_of_input_pattern	R/W	0: Inversion is enabled 1: Disable inversion of input pattern during PRBS58 test pattern generation	0x0
0	RX_fault_sel	R/W	0: rx_status = block_lock 1: rx_status = block_lock * !hi_ber (IEEE compliant)	0x0

2.10.2.17 PCS Control 5

Short Name:PCS_Control_5

Address:0x38601

Table 958 • **PCS Control 5**

Bit	Name	Access	Description	Default
1	TX_LF_FILT_EN	R/W	Enables re-mapping of Local_Faults to Idles in Tx path 0: Disable re-mapping 1: Enable re-mapping	0x0
0	RX_LF_FILT_EN	R/W	Enable re-mapping of Local_Faults to Idles in Rx path 0: Disable re-mapping 1: Enable re-mapping	0x1

2.10.2.18 PCS LF_filt Linkup Timer

Short Name:PCS_LF_filt_linkup_timer

Address:0x38602

Table 959 • **PCS LF_filt Linkup Timer**

Bit	Name	Access	Description	Default
15:0	LF_FILT_UP_TMR	R/W	When no LF's, the filt_timer block will count up to this value before enabling filters. The counter increments once every 49.6ns	0x0064

2.10.2.19 PCS LF_filt Linkdown Timer

Short Name:PCS_LF_filt_linkdown_timer

Address:0x38603

Table 960 • **PCS LF_filt Linkdown Timer**

Bit	Name	Access	Description	Default
15:0	LF_FILT_DOWN_TMR	R/W	Upon stream of LF's, the filt_timer block will count up to this value before disabling filters. The counter increments once every 49.6ns	0x012C

2.10.2.20 PCS Interrupt Pending 1

Short Name:PCS_INTR_PEND1

Address:0x38E00

Table 961 • **PCS Interrupt Pending 1**

Bit	Name	Access	Description	Default
9	RX_LINK_STAT_INTR_PEND	Sticky	The interrupt pending bit is asserted when the status signal driving PCS_Status_1::PCS_RECEIVE_LINK_STATUS changes state. The sticky bit is cleared when a 1 is written to the register bit. 0: An interrupt event has not occurred. 1: An interrupt event has occurred.	0x0
8	HIGHBER_INTR_PEND	Sticky	The interrupt pending bit is asserted when Eth_10GBASE_R_PCS_Status_2::PCS_HIGHBER status changes state. The sticky bit is cleared when a 1 is written to the register bit. 0: An interrupt event has not occurred. 1: An interrupt event has occurred.	0x0
7	FEC_FIXED_CNT_THRESH_INTR_PEND	Sticky	This interrupt pending register bit is asserted when the KR_FEC_CORRECTED_BLOCKS counter exceeds the FEC_FIXED_ERR_CNT_THRESH value. The bit is asserted when the counter transitions from being less than the threshold to being greater than the threshold. The sticky bit is cleared when a 1 is written to the bit. 0: An interrupt event has not occurred. 1: An interrupt event has occurred.	0x0
6	FEC_UNFIXED_CNT_THRESH_INTR_PEND	Sticky	This interrupt pending register bit is asserted when the KR_FEC_UNCORRECTED_BLOCKS counter exceeds the FEC_UNFIXED_ERR_CNT_THRESH value. The bit is asserted when the counter transitions from being less than the threshold to being greater than the threshold. The sticky bit is cleared when a 1 is written to the bit. 0: An interrupt event has not occurred. 1: An interrupt event has occurred.	0x0
5	TX_SEQ_CNT_THRESH_INTR_PEND	Sticky	This interrupt pending register bit is asserted when the PCS_TX_SEQ_ERR_CNT counter exceeds the TX_SEQ_ERR_CNT_THRESH value. The bit is asserted when the counter transitions from being less than the threshold to being greater than the threshold. The sticky bit is cleared when a 1 is written to the bit. 0: An interrupt event has not occurred. 1: An interrupt event has occurred.	0x0

Table 961 • **PCS Interrupt Pending 1** ***(continued)***

Bit	Name	Access	Description	Default
4	RX_SEQ_CNT_THRESH_INTR_PEND	Sticky	This interrupt pending register bit is asserted when the PCS_RX_SEQ_ERR_CNT counter exceeds the RX_SEQ_ERR_CNT_THRESH value. The bit is asserted when the counter transitions from being less than the threshold to being greater than the threshold. The sticky bit is cleared when a 1 is written to the bit. 0: An interrupt event has not occurred. 1: An interrupt event has occurred.	0x0
3	TX_BLK_ENC_CNT_THRESH_INTR_PEND	Sticky	This interrupt pending register bit is asserted when the PCS_TX_BLK_ENC_ERR_CNT counter exceeds the TX_BLK_ENC_ERR_CNT_THRESH value. The bit is asserted when the counter transitions from being less than the threshold to being greater than the threshold. The sticky bit is cleared when a 1 is written to the bit. 0: An interrupt event has not occurred. 1: An interrupt event has occurred.	0x0
2	RX_BLK_DEC_CNT_THRESH_INTR_PEND	Sticky	This interrupt pending register bit is asserted when the PCS_RX_BLK_DEC_ERR_CNT counter exceeds the RX_BLK_DEC_ERR_CNT_THRESH value. The bit is asserted when the counter transitions from being less than the threshold to being greater than the threshold. The sticky bit is cleared when a 1 is written to the bit. 0: An interrupt event has not occurred. 1: An interrupt event has occurred.	0x0
1	TX_CHAR_ENC_CNT_THRESH_INTR_PEND	Sticky	This interrupt pending register bit is asserted when the PCS_TX_CHAR_ENC_ERR_CNT counter exceeds the TX_CHAR_ENC_ERR_CNT_THRESH value. The bit is asserted when the counter transitions from being less than the threshold to being greater than the threshold. The sticky bit is cleared when a 1 is written to the bit. 0: An interrupt event has not occurred. 1: An interrupt event has occurred.	0x0
0	RX_CHAR_DEC_CNT_THRESH_INTR_PEND	Sticky	This interrupt pending register bit is asserted when the PCS_RX_CHAR_DEC_ERR_CNT counter exceeds the RX_CHAR_DEC_ERR_CNT_THRESH value. The bit is asserted when the counter transitions from being less than the threshold to being greater than the threshold. The sticky bit is cleared when a 1 is written to the bit. 0: An interrupt event has not occurred. 1: An interrupt event has occurred.	0x0

2.10.2.21 PCS Interrupt Mask 1

Short Name:PCS_INTR_MASK1

Address:0x38E01

Table 962 • **PCS Interrupt Mask 1**

Bit	Name	Access	Description	Default
9	RX_LINK_STAT_MASK	R/W	Interrupt mask for RX_LINK_STAT_INTR_PEND. 0: Interrupt disabled 1: Interrupt enabled	0x0
8	HIGHBER_MASK	R/W	Interrupt mask for HIGHBER_INTR_PEND. 0: Interrupt disabled 1: Interrupt enabled	0x0
7	FEC_FIXED_CNT_THRESH_MASK	R/W	Interrupt mask for KR_FEC_CORRECTED_BLOCKS error counter exceeding threshold level. 0: Interrupt disabled 1: Interrupt enabled	0x0
6	FEC_UNFIXED_CNT_THRESH_MASK	R/W	Interrupt mask for KR_FEC_UNCORRECTED_BLOCKS error counter exceeding threshold level. 0: Interrupt disabled 1: Interrupt enabled	0x0
5	TX_SEQ_CNT_THRESH_MASK	R/W	Interrupt mask for PCS_TX_SEQ_ERR_CNT exceeding threshold level. 0: Interrupt disabled 1: Interrupt enabled	0x0
4	RX_SEQ_CNT_THRESH_MASK	R/W	Interrupt mask for PCS_RX_SEQ_ERR_CNT exceeding threshold level. 0: Interrupt disabled 1: Interrupt enabled	0x0
3	TX_BLK_ENC_CNT_THRESH_MASK	R/W	Interrupt mask for PCS_TX_BLK_ENC_ERR_CNT exceeding threshold level. 0: Interrupt disabled 1: Interrupt enabled	0x0
2	RX_BLK_DEC_CNT_THRESH_MASK	R/W	Interrupt mask for PCS_RX_BLK_DEC_ERR_CNT exceeding threshold level. 0: Interrupt disabled 1: Interrupt enabled	0x0
1	TX_CHAR_ENC_CNT_THRESH_MASK	R/W	Interrupt mask for PCS_TX_CHAR_ENC_ERR_CNT exceeding threshold level. 0: Interrupt disabled 1: Interrupt enabled	0x0
0	RX_CHAR_DEC_CNT_THRESH_MASK	R/W	Interrupt mask for PCS_RX_CHAR_DEC_ERR_CNT exceeding threshold level. 0: Interrupt disabled 1: Interrupt enabled	0x0

2.10.2.22 PCS Interrupt Status Signals

Short Name:PCS_INTR_STATUS

Address:0x38E03

Table 963 • **PCS Interrupt Status Signals**

Bit	Name	Access	Description	Default
9	PCS_receive_link_status	R/O	This is the status signal used to assert the RX_LINK_STAT_INTR_PEND register. It is the same status used to assert the latch-low PCS_Status_1::PCS_RECEIVE_LINK_STATUS register. 0: PCS received link down. BLOCK_LOCK=0 OR HI_BER=1 1: PCS receive link up. BLOCK_LOCK=1 AND HI_BER=0.	0x1
8	PCS_HIGHBER	R/O	This is the status signal used to assert the HIGHBER_INTR_PEND register. It is the same status used to assert the latch-high Eth_10GBASE_R_PCS_Status_2::PCS_HIGHBER register. 0: 10GBASE-R PCS has not reported a high BER 1: 10GBASE-R PCS has reported a high BER	0x0
7	FEC_FIXED_THRESH_COMP	R/O	Present result of comparing KR FEC's corrected block count (KR_FEC_CORRECTED_UPPER/KR_FEC_CORRECTED_LOWER) to the threshold setting in FEC_FIXED_ERR_CNT_THRESH1/FEC_FIXED_ERR_CNT_THRESH0. 0: counter does not exceed threshold setting 1: counter exceeds threshold setting	0x0
6	FEC_UNFIXED_THRESH_COMP	R/O	Present result of comparing KR FEC's uncorrectable block count (KR_FEC_UNCORRECTED_UPPER/KR_FEC_UNCORRECTED_LOWER) to the threshold setting in FEC_UNFIXED_ERR_CNT_THRESH1/FEC_UNFIXED_ERR_CNT_THRESH0. 0: counter does not exceed threshold setting 1: counter exceeds threshold setting	0x0
5	TX_SEQ_THRESH_COMP	R/O	Present result of comparing Tx sequencing error count (PCS_TX_SEQ_ERR_CNT) to the threshold setting in register TX_SEQ_ERR_CNT_THRESH. 0: counter does not exceed threshold setting 1: counter exceeds threshold setting	0x0
4	RX_SEQ_THRESH_COMP	R/O	Present result of comparing Rx sequencing error count (PCS_RX_SEQ_ERR_CNT) to the threshold setting in register RX_SEQ_ERR_CNT_THRESH. 0: counter does not exceed threshold setting 1: counter exceeds threshold setting	0x0

Table 963 • **PCS Interrupt Status Signals *(continued)***

Bit	Name	Access	Description	Default
3	TX_BLK_ENC_THRESH_COMP	R/O	Present result of comparing Tx block encode error count (PCS_TX_BLK_ENC_ERR_CNT) to the threshold setting in register TX_BLK_ENC_ERR_CNT_THRESH. 0: counter does not exceed threshold setting 1: counter exceeds threshold setting	0x0
2	RX_BLK_DEC_THRESH_COMP	R/O	Present result of comparing Rx block decode error count (PCS_RX_BLK_DEC_ERR_CNT) to the threshold setting in register RX_BLK_DEC_ERR_CNT_THRESH. 0: counter does not exceed threshold setting 1: counter exceeds threshold setting	0x0
1	TX_CHAR_ENC_THRESH_COMP	R/O	Present result of comparing Tx character encode error count (PCS_TX_CHAR_ENC_ERR_CNT) to the threshold setting in register TX_CHAR_ENC_ERR_CNT_THRESH. 0: counter does not exceed threshold setting 1: counter exceeds threshold setting	0x0
0	RX_CHAR_DEC_THRESH_COMP	R/O	Present result of comparing Rx character decode error count (PCS_RX_CHAR_DEC_ERR_CNT) to the threshold setting in register RX_CHAR_DEC_ERR_CNT_THRESH. 0: counter does not exceed threshold setting 1: counter exceeds threshold setting	0x0

2.10.2.23 Tx Sequencing Error Count Threshold

Short Name:TX_SEQ_ERR_CNT_THRESH

Address:0x38E04

Table 964 • **Tx Sequencing Error Count Threshold**

Bit	Name	Access	Description	Default
15:0	TX_SEQ_ERR_CNT_THRESH	R/W	Tx sequencing error count threshold	0xFFFF

2.10.2.24 Rx Sequencing Error Count Threshold

Short Name:RX_SEQ_ERR_CNT_THRESH

Address:0x38E05

Table 965 • **Rx Sequencing Error Count Threshold**

Bit	Name	Access	Description	Default
15:0	RX_SEQ_ERR_CNT_THRESH	R/W	Rx sequencing error count threshold	0xFFFF

2.10.2.25 Tx Block Encode Error Count Threshold

Short Name:TX_BLK_ENC_ERR_CNT_THRESH

Address:0x38E06

Table 966 • **Tx Block Encode Error Count Threshold**

Bit	Name	Access	Description	Default
15:0	TX_BLK_ENC_ERR_CNT_THRESH	R/W	Tx block encode error count threshold	0xFFFF

2.10.2.26 Rx Block Decode Error Count Threshold

Short Name:RX_BLK_DEC_ERR_CNT_THRESH

Address:0x38E07

Table 967 • **Rx Block Decode Error Count Threshold**

Bit	Name	Access	Description	Default
15:0	RX_BLK_DEC_ERR_CNT_THRESH	R/W	Rx block decode error count threshold	0xFFFF

2.10.2.27 Tx Character Encode Error Count Threshold

Short Name:TX_CHAR_ENC_ERR_CNT_THRESH

Address:0x38E08

Table 968 • **Tx Character Encode Error Count Threshold**

Bit	Name	Access	Description	Default
15:0	TX_CHAR_ENC_ERR_CNT_THRESH	R/W	Tx character encode error count threshold	0xFFFF

2.10.2.28 Rx Character Decode Error Count Threshold

Short Name:RX_CHAR_DEC_ERR_CNT_THRESH

Address:0x38E09

Table 969 • **Rx Character Decode Error Count Threshold**

Bit	Name	Access	Description	Default
15:0	RX_CHAR_DEC_ERR_CNT_THRESH	R/W	Rx character decode error count threshold	0xFFFF

2.10.2.29 FEC Fixed Error Count Threshold 1

Short Name:FEC_FIXED_ERR_CNT_THRESH1

Address:0x38E0A

Table 970 • **FEC Fixed Error Count Threshold 1**

Bit	Name	Access	Description	Default
15:0	FEC_FIXED_ERR_CNT_THRESH1	R/W	FEC fixed error count Threshold[31:16]	0xFFFF

2.10.2.30 FEC Fixed Error Count Threshold 0

Short Name:FEC_FIXED_ERR_CNT_THRESH0

Address:0x38E0B

Table 971 • **FEC Fixed Error Count Threshold 0**

Bit	Name	Access	Description	Default
15:0	FEC_FIXED_ERR_CNT_THRESH0	R/W	FEC fixed error count Threshold[15:0]	0xFFFF

2.10.2.31 FEC Unfixable Error Count Threshold 1

Short Name:FEC_UNFIXED_ERR_CNT_THRESH1

Address:0x38E0C

Table 972 • **FEC Unfixable Error Count Threshold 1**

Bit	Name	Access	Description	Default
15:0	FEC_UNFIXED_ERR_CNT_THRESH1	R/W	FEC unfixable error count Threshold[31:16]	0xFFFF

2.10.2.32 FEC Unfixable Error Count Threshold 0

Short Name:FEC_UNFIXED_ERR_CNT_THRESH0

Address:0x38E0D

Table 973 • **FEC Unfixable Error Count Threshold 0**

Bit	Name	Access	Description	Default
15:0	FEC_UNFIXED_ERR_CNT_THRESH0	R/W	FEC unfixable error count Threshold[15:0]	0xFFFF

2.11 HOST_PCS10G (Device 0xB)

Table 974 • **PCS_Control_1**

Address	Short Description	Register Name	Details
0xB0000	PCS Control 1	PCS_Control_1	Page 368

Table 975 • **PCS_Status_1**

Address	Short Description	Register Name	Details
0xB0001	PCS Status 1	PCS_Status_1	Page 369

Table 976 • **PCS_Device_Identifier**

Address	Short Description	Register Name	Details
0xB0002	PCS Device Identifier 1	PCS_Device_Identifier_1	Page 369
0xB0003	PCS Device Identifier 2	PCS_Device_Identifier_2	Page 370

Table 977 • **PCS_Speed_Ability**

Address	Short Description	Register Name	Details
0xB0004	PCS Speed Ability	PCS_Speed_Ability	Page 370

Table 978 • **PCS_Devices_in_Package_1**

Address	Short Description	Register Name	Details
0xB0005	PCS Devices in Package 1	PCS_Devices_in_Package_1	Page 370

Table 979 • **PCS_Devices_in_Package_2**

Address	Short Description	Register Name	Details
0xB0006	PCS Devices in Package 2	PCS_Devices_in_Package_2	Page 371

Table 980 • **PCS_Control_2**

Address	Short Description	Register Name	Details
0xB0007	PCS Control 2	PCS_Control_2	Page 371

Table 981 • **PCS_Status_2**

Address	Short Description	Register Name	Details
0xB0008	PCS Status 2	PCS_Status_2	Page 371

Table 982 • **PCS_Package_Identifier**

Address	Short Description	Register Name	Details
0xB000E	PCS Package Identifier 1	PCS_Package_Identifier_1	Page 372
0xB000F	PCS Package Identifier 2	PCS_Package_Identifier_2	Page 372

Table 983 • **Eth_10Gbase_X_Status**

Address	Short Description	Register Name	Details
0xB0018	Eth_10Gbase-X Status	Eth_10Gbase_X_Status	Page 373

Table 984 • **Eth_10Gbase_X_Control**

Address	Short Description	Register Name	Details
0xB0019	Eth_10Gbase-X Control	Eth_10Gbase_X_Control	Page 373

Table 985 • **Eth_10Gbase_R_PCS_Status_1**

Address	Short Description	Register Name	Details
0xB0020	Eth_10Gbase-R PCS Status 1	Eth_10GBASE_R_PCS_Status_1	Page 373

Table 986 • **Eth_10Gbase_R_PCS_Status_2**

Address	Short Description	Register Name	Details
0xB0021	Eth_10Gbase-R PCS Status 2	Eth_10GBASE_R_PCS_Status_2	Page 373

Table 987 • **Eth_10Gbase_R_PCS_Test_Pattern_Seed_A**

Address	Short Description	Register Name	Details
0xB0022	Eth_10Gbase-R PCS Test Pattern Seed A 0	Eth_10GBASE_R_PCS_Test_Pattern_Seed_A_0	Page 374
0xB0023	Eth_10Gbase-R PCS Test Pattern Seed A 1	Eth_10GBASE_R_PCS_Test_Pattern_Seed_A_1	Page 374
0xB0024	Eth_10Gbase-R PCS Test Pattern Seed A 2	Eth_10GBASE_R_PCS_Test_Pattern_Seed_A_2	Page 374
0xB0025	Eth_10Gbase-R PCS Test Pattern Seed A 3	Eth_10GBASE_R_PCS_Test_Pattern_Seed_A_3	Page 374

Table 988 • **Eth_10Gbase_R_PCS_Test_Pattern_Seed_B**

Address	Short Description	Register Name	Details
0xB0026	Eth_10Gbase-R PCS Test Pattern Seed B 0	Eth_10GBASE_R_PCS_Test_Pattern_Seed_B_0	Page 375
0xB0027	Eth_10Gbase-R PCS Test Pattern Seed B 1	Eth_10GBASE_R_PCS_Test_Pattern_Seed_B_1	Page 375
0xB0028	Eth_10Gbase-R PCS Test Pattern Seed B 2	Eth_10GBASE_R_PCS_Test_Pattern_Seed_B_2	Page 375
0xB0029	Eth_10Gbase-R PCS Test Pattern Seed B 3	Eth_10GBASE_R_PCS_Test_Pattern_Seed_B_3	Page 375

Table 989 • **Eth_10Gbase_R_PCS_test_pattern_control**

Address	Short Description	Register Name	Details
0xB002A	Eth_10Gbase-R PCS Test-Pattern Control	Eth_10GBASE_R_PCS_test_pattern_control	Page 375

Table 990 • **Eth_10Gbase_R_PCS_test_pattern_counter**

Address	Short Description	Register Name	Details
0xB002B	Eth_10Gbase-R PCS Test-Pattern Counter	Eth_10GBASE_R_PCS_test_pattern_counter	Page 376

Table 991 • **USR_Test**

Address	Short Description	Register Name	Details
0xB8000	USR Test 0	USR_Test_0	Page 376
0xB8001	USR Test 1	USR_Test_1	Page 377
0xB8002	USR Test 2	USR_Test_2	Page 377
0xB8003	USR Test 3	USR_Test_3	Page 377

Table 992 • **Square_Wave_Pulse_Width**

Address	Short Description	Register Name	Details
0xB8004	Square Wave Pulse Width	Square_Wave_Pulse_Width	Page 377

Table 993 • **PCS_Control_3**

Address	Short Description	Register Name	Details
0xB8005	PCS Control 3	PCS_Control_3	Page 377

Table 994 • **Test_Error_Counter**

Address	Short Description	Register Name	Details
0xB8007	Test Error Counter 0	Test_Error_Counter_0	Page 378
0xB8008	Test Error Counter 1	Test_Error_Counter_1	Page 378

Table 995 • **PCS_TX_SEQ_ERR_CNT**

Address	Short Description	Register Name	Details
0xB8010	PCS Tx Sequencing Error Count	PCS_TX_SEQ_ERR_CNT	Page 379

Table 996 • **PCS_RX_SEQ_ERR_CNT**

Address	Short Description	Register Name	Details
0xB8011	PCS Rx Sequencing Error Count	PCS_RX_SEQ_ERR_CNT	Page 379

Table 997 • **PCS_TX_BLK_ENC_ERR_CNT**

Address	Short Description	Register Name	Details
0xB8012	PCS Tx Block Encode Error Count	PCS_TX_BLK_ENC_ERR_CNT	Page 379

Table 998 • **PCS_PCS_RX_BLK_DEC_ERR_CNT**

Address	Short Description	Register Name	Details
0xB8013	PCS Rx Block Decode Error Count	PCS_PCS_RX_BLK_DEC_ERR_CNT	Page 379

Table 999 • **PCS_TX_CHAR_ENC_ERR_CNT**

Address	Short Description	Register Name	Details
0xB8014	PCS Tx Character Encode Error Count	PCS_TX_CHAR_ENC_ERR_CNT	Page 380

Table 1000 • **PCS_RX_CHAR_DEC_ERR_CNT**

Address	Short Description	Register Name	Details
0xB8015	PCS Rx Character Decode Error Count	PCS_RX_CHAR_DEC_ERR_CNT	Page 380

Table 1001 • **Loopback_FIFOs_Stat_Ctrl**

Address	Short Description	Register Name	Details
0xB8016	Loopback FIFOs Stat/Ctrl	Loopback_FIFOs_Stat_Ctrl	Page 380

Table 1002 • **PCS_Control_4**

Address	Short Description	Register Name	Details
0xB8600	PCS Control 4	PCS_Control_4	Page 380

Table 1003 • **PCS_Control_5**

Address	Short Description	Register Name	Details
0xB8601	PCS Control 5	PCS_Control_5	Page 381

Table 1004 • **PCS_LF_filt_linkup_timer**

Address	Short Description	Register Name	Details
0xB8602	PCS LF_filt Linkup Timer	PCS_LF_filt_linkup_timer	Page 381

Table 1005 • **PCS_LF_filt_linkdown_timer**

Address	Short Description	Register Name	Details
0xB8603	PCS LF_filt Linkdown Timer	PCS_LF_filt_linkdown_timer	Page 381

Table 1006 • **PCS_INTR_PEND1**

Address	Short Description	Register Name	Details
0xB8E00	PCS Interrupt Pending 1	PCS_INTR_PEND1	Page 382

Table 1007 • **PCS_INTR_MASK1**

Address	Short Description	Register Name	Details
0xB8E01	PCS Interrupt Mask 1	PCS_INTR_MASK1	Page 383

Table 1008 • **PCS_INTR_STATUS**

Address	Short Description	Register Name	Details
0xB8E03	PCS Interrupt Status Signals	PCS_INTR_STATUS	Page 384

Table 1009 • **INTR_THRESHOLD_LEVEL**

Address	Short Description	Register Name	Details
0xB8E04	Tx Sequencing Error Count Threshold	TX_SEQ_ERR_CNT_THRESH	Page 386
0xB8E05	Rx Sequencing Error Count Threshold	RX_SEQ_ERR_CNT_THRESH	Page 386
0xB8E06	Tx Block Encode Error Count Threshold	TX_BLK_ENC_ERR_CNT_THRESH	Page 386
0xB8E07	Rx Block Decode Error Count Threshold	RX_BLK_DEC_ERR_CNT_THRESH	Page 387
0xB8E08	Tx Character Encode Error Count Threshold	TX_CHAR_ENC_ERR_CNT_THRESH	Page 387
0xB8E09	Rx Character Decode Error Count Threshold	RX_CHAR_DEC_ERR_CNT_THRESH	Page 387
0xB8E0A	FEC Fixed Error Count Threshold 1	FEC_FIXED_ERR_CNT_THRESH1	Page 387
0xB8E0B	FEC Fixed Error Count Threshold 0	FEC_FIXED_ERR_CNT_THRESH0	Page 387
0xB8E0C	FEC Unfixable Error Count Threshold 1	FEC_UNFIXED_ERR_CNT_THRESH1	Page 388
0xB8E0D	FEC Unfixable Error Count Threshold 0	FEC_UNFIXED_ERR_CNT_THRESH0	Page 388

2.11.1 Standard PCS-10G

2.11.1.1 PCS Control 1

Short Name:PCS_Control_1

Address:0xB0000

Table 1010 • **PCS Control 1**

Bit	Name	Access	Description	Default
15	SOFT_RST	One-shot	MDIO Manageable Device (MMD) software reset. Reset all logic in the channel between the host side PMA and the line side PMA, regardless of the cross-connect configuration. Data path logic and configuration registers are reset. 0: Normal operation 1: Reset	0x0
14	PCS_System_loopback	R/W	PCS System loopback. Loopback of 64b encoded and scrambled data 0: Disable PCS loopback mode 1: Enable PCS loopback mode	0x0

Table 1010 • **PCS Control 1 *(continued)***

Bit	Name	Access	Description	Default
13	Speed_selection	R/O	0: Unspecified 1: Operation at 10 Gb/s and above	0x1
11	LOW_PWR_PCS	R/W	The channel's data path is placed into low power mode with this register. The PMA in this channel is also placed into low power mode regardless of the channel cross connect configuration. The PMD_TRANSMIT_DISABLE.GLOBAL_PMD_TRANSMIT_DISABLE register state can can be transmitted from a GPIO pin to shut off an optics module's Tx driver. 0: Normal Operation 1: Low Power Mode	0x0
6	Speed_selection_idx2	R/O	0: Unspecified 1: Operation at 10 Gb/s and above	0x1
5:2	Speed_selection_idx3	R/O	1xxx: Reserved. x1xx: Reserved. xx1x: Reserved. 0001: Reserved. 0000: 10 Gbps	0x0

2.11.1.2 PCS Status 1

Short Name:PCS_Status_1

Address:0xB0001

Table 1011 • **PCS Status 1**

Bit	Name	Access	Description	Default
7	Fault	R/O	0: Fault condition not detected. (PCS receive local fault (PCS_Status_2.Receive_fault) = 0) AND (PCS transmit local fault (PCS_Status_2.Transmit_fault) = 0) 1: Fault condition detected. (PCS receive local fault (PCS_Status_2.Receive_fault) = 1) OR (PCS transmit local fault (PCS_Status_2.Transmit_fault) = 1)	0x0
2	PCS_receive_link_status	R/O	This is a sticky bit that latches the low state. The latch-low bit is cleared when the register is read. 0: PCS received link down. BLOCK_LOCK=0 OR HI_BER=1 1: PCS receive link up. BLOCK_LOCK=1 AND HI_BER=0.	0x1
1	Low_power_ability	R/O	0: PCS does not support low power mode 1: PCS supports low power mode	0x1

2.11.1.3 PCS Device Identifier 1

Short Name:PCS_Device_Identifier_1

Address:0xB0002

***Table 1012* • PCS Device Identifier 1**

Bit	Name	Access	Description	Default
15:0	PCS_Device_Identifier_1	R/O	Upper 16 bits of a 32-bit unique PCS device identifier. Bits 3-18 of the device manufacturer's OUI.	0x0007

2.11.1.4 PCS Device Identifier 2

Short Name:PCS_Device_Identifier_2

Address:0xB0003

***Table 1013* • PCS Device Identifier 2**

Bit	Name	Access	Description	Default
15:0	PCS_Device_Identifier_2	R/O	Lower 16 bits of a 32-bit unique PCS device identifier. Bits 19-24 of the device manufacturer's OUI. Six-bit model number, and a four-bit revision number.	0x0400

2.11.1.5 PCS Speed Ability

Short Name:PCS_Speed_Ability

Address:0xB0004

***Table 1014* • PCS Speed Ability**

Bit	Name	Access	Description	Default
0	is_10G_capable	R/O	0: Not capable of 10Gbps 1: Capable of 10Gbps	0x1

2.11.1.6 PCS Devices in Package 1

Short Name:PCS_Devices_in_Package_1

Address:0xB0005

***Table 1015* • PCS Devices in Package 1**

Bit	Name	Access	Description	Default
5	DTE_XS_present	R/O	Indicates whether DTE XS is present in the package 0: Not present 1: Present	0x0
4	PHY_XS_present	R/O	Indicates whether PHY XS is present in the package 0: Not present 1: Present	0x1
3	PCS_present	R/O	Indicates whether PCS is present in the package 0: Not present 1: Present	0x1

Table 1015 • **PCS Devices in Package 1 *(continued)***

Bit	Name	Access	Description	Default
2	WIS_present	R/O	Indicates whether WIS is present in the package 0: Not present 1: Present	0x1
1	PMD_PMA_present	R/O	Indicates whether PMA/PMD is present in the package 0: Not present 1: Present	0x1
0	Clause_22_registers_present	R/O	Indicates whether Clause 22 registers are present in the package 0: Not present 1: Present	0x0

2.11.1.7 PCS Devices in Package 2

Short Name:PCS_Devices_in_Package_2

Address:0xB0006

Table 1016 • **PCS Devices in Package 2**

Bit	Name	Access	Description	Default
15	Vendor_spec_dev_2_present	R/O	Indicates whether vendor specific device 2 is present in the package 0: Not present 1: Present	0x0
14	Vendor_spec_dev_1_present	R/O	Indicates whether vendor specific device 1 is present in the package 0: Not present 1: Present	0x0

2.11.1.8 PCS Control 2

Short Name:PCS_Control_2

Address:0xB0007

Table 1017 • **PCS Control 2**

Bit	Name	Access	Description	Default
1:0	Select_WAN_mode_or_10GBASE_R	R/W	Indicates the PCS type selected 11: Reserved 10: 10GBASE-W PCS 01: Reserved 00: 10GBASE-R PCS	0x0

2.11.1.9 PCS Status 2

Short Name:PCS_Status_2

Address:0xB0008

Table 1018 **• PCS Status 2**

Bit	Name	Access	Description	Default
15:14	Device_present	R/O	00: No device responding at this address 01: No device responding at this address 10: Device responding at this address 11: No device responding at this address	0xA
11	Transmit_fault	R/O	This is a sticky bit that latches the high state. The latch-high bit is cleared when the register is read. 0: No fault condition on transmit path 1: Fault condition on transmit path	0x0
10	Receive_fault	R/O	This is a sticky bit that latches the high state. The latch-high bit is cleared when the register is read. 0: No fault condition on receive path 1: Fault condition on receive path	0x0
2	is_10GBASE_W_ability	R/O	0: Not supported 1: Supported	0x1
1	is_10GBASE_X_ability	R/O	0: Not supported 1: Supported	0x0
0	is_10GBASE_R_ability	R/O	0: Not supported 1: Supported	0x1

2.11.1.10 PCS Package Identifier 1

Short Name:PCS_Package_Identifier_1

Address:0xB000E

Table 1019 **• PCS Package Identifier 1**

Bit	Name	Access	Description	Default
15:0	PCS_package_identifier_1	R/O	Upper 16 bits of a 32-bit unique PCS package identifier. Bits 3-18 of the device manufacturer's OUI. Six-bit model number and a four-bit revision number.	0x0000

2.11.1.11 PCS Package Identifier 2

Short Name:PCS_Package_Identifier_2

Address:0xB000F

Table 1020 **• PCS Package Identifier 2**

Bit	Name	Access	Description	Default
15:0	PCS_package_identifier_2	R/O	Lower 16 bits of a 32-bit unique PCS package identifier. Bits 19-24 of the device manufacturer's OUI. Six-bit model number and a four-bit revision number.	0x0000

2.11.1.12 Ethernet 10Gbase-X Status

Short Name: Eth_10Gbase_X_Status

Address:0xB0018

Table 1021 • **Eth_10Gbase-X Status**

Bit	Name	Access	Description	Default
15:0	is_10Gbase_X_Status	R/O	Not supported	0x0000

2.11.1.13 Ethernet 10Gbase-X Control

Short Name: Eth_10Gbase_X_Control

Address:0xB0019

Table 1022 • **Eth_10Gbase-X Control**

Bit	Name	Access	Description	Default
15:0	is_10Gbase_X_Control	R/O	Not supported	0x0000

2.11.1.14 Ethernet 10Gbase-R PCS Status 1

Short Name: Eth_10GBASE_R_PCS_Status_1

Address:0xB0020

Table 1023 • **Eth_10Gbase-R PCS Status 1**

Bit	Name	Access	Description	Default
12	is_10GBASE_R_receive_lock_status	R/O	0: 10GBASE-R PCS receive link down BLOCK_LOCK (Eth_10GBASE_R_PCS_Status_1.is_10GBASE_R_PCS_block_lock) = 0 OR BER_HI (Eth_10GBASE_R_PCS_Status_1.is_10GBASE_R_PCS_high_BER) = 1 1: 10GBASE-R PCS receive link up BLOCK_LOCK (Eth_10GBASE_R_PCS_Status_1.is_10GBASE_R_PCS_block_lock) = 1 AND BER_HI (Eth_10GBASE_R_PCS_Status_1.is_10GBASE_R_PCS_high_BER) = 0	0x0
2	PRBS31_pattern_testing_ability	R/O	0: PCS does not support PRBS31 pattern testing 1: PCS is able to support PRBS31 pattern testing	0x1
1	is_10GBASE_R_PCS_high_BER	R/O	0: 10GBASE-R PCS not reporting a high BER. 1: 10GBASE-R PCS reporting a high BER.	0x0
0	is_10GBASE_R_PCS_block_lock	R/O	0: 10GBASE-R PCS is not locked to receive blocks. 1: 10GBASE-R PCS is locked to receive blocks.	0x0

2.11.1.15 Ethernet 10Gbase-R PCS Status 2

Short Name: Eth_10GBASE_R_PCS_Status_2

Address:0xB0021

***Table 1024* • Eth_10Gbase-R PCS Status 2**

Bit	Name	Access	Description	Default
15	BLOCK_LOCK	R/O	This is a sticky bit that latches the low state. The latch-low bit is cleared when the register is read. 0: 10GBASE-R PCS does not have block lock 1: 10GBASE-R PCS has block lock	0x1
14	PCS_HIGHBER	R/O	This is a sticky bit that latches the high state. The latch-high bit is cleared when the register is read. 0: 10GBASE-R PCS has not reported a high BER 1: 10GBASE-R PCS has reported a high BER	0x0
13:8	BER	R/O	BER counter. The counter saturates when the maximum value is exceeded. The counter is cleared when the register is read.	0x00
7:0	PCS_ERRORED_BLOCKS	R/O	Errored blocks counter. The counter saturates when the maximum value is exceeded. The counter is cleared when the register is read.	0x00

2.11.1.16 Ethernet 10Gbase-R PCS Test Pattern Seed A 0

Short Name: Eth_10GBASE_R_PCS_Test_Pattern_Seed_A_0

Address:0xB0022

***Table 1025* • Eth_10Gbase-R PCS Test Pattern Seed A 0**

Bit	Name	Access	Description	Default
15:0	PCS_SEEDA_0	R/W	Test pattern seed A bits 0-15	0x0000

2.11.1.17 Ethernet 10Gbase-R PCS Test Pattern Seed A 1

Short Name: Eth_10GBASE_R_PCS_Test_Pattern_Seed_A_1

Address:0xB0023

***Table 1026* • Eth_10Gbase-R PCS Test Pattern Seed A 1**

Bit	Name	Access	Description	Default
15:0	PCS_SEEDA_1	R/W	Test pattern seed A bits 16-31	0x0000

2.11.1.18 Ethernet 10Gbase-R PCS Test Pattern Seed A 2

Short Name: Eth_10GBASE_R_PCS_Test_Pattern_Seed_A_2

Address:0xB0024

***Table 1027* • Eth_10Gbase-R PCS Test Pattern Seed A 2**

Bit	Name	Access	Description	Default
15:0	PCS_SEEDA_2	R/W	Test pattern seed A bits 32-47	0x0000

2.11.1.19 Ethernet 10Gbase-R PCS Test Pattern Seed A 3

Short Name: Eth_10GBASE_R_PCS_Test_Pattern_Seed_A_3

Address:0xB0025

Table 1028 **• Eth_10Gbase-R PCS Test Pattern Seed A 3**

Bit	Name	Access	Description	Default
9:0	PCS_SEEDA_3	R/W	Test pattern seed A bits 48-57	0x000

2.11.1.20 Ethernet 10Gbase-R PCS Test Pattern Seed B 0

Short Name: Eth_10GBASE_R_PCS_Test_Pattern_Seed_B_0

Address:0xB0026

Table 1029 **• Eth_10Gbase-R PCS Test Pattern Seed B 0**

Bit	Name	Access	Description	Default
15:0	PCS_SEEDB_0	R/W	Test pattern seed B bits 0-15	0x0000

2.11.1.21 Ethernet 10Gbase-R PCS Test Pattern Seed B 1

Short Name: Eth_10GBASE_R_PCS_Test_Pattern_Seed_B_1

Address:0xB0027

Table 1030 **• Eth_10Gbase-R PCS Test Pattern Seed B 1**

Bit	Name	Access	Description	Default
15:0	PCS_SEEDB_1	R/W	Test pattern seed B bits 16-31	0x0000

2.11.1.22 Ethernet 10Gbase-R PCS Test Pattern Seed B 2

Short Name: Eth_10GBASE_R_PCS_Test_Pattern_Seed_B_2

Address:0xB0028

Table 1031 **• Eth_10Gbase-R PCS Test Pattern Seed B 2**

Bit	Name	Access	Description	Default
15:0	PCS_SEEDB_2	R/W	Test pattern seed B bits 32-47	0x0000

2.11.1.23 Ethernet 10Gbase-R PCS Test Pattern Seed B 3

Short Name: Eth_10GBASE_R_PCS_Test_Pattern_Seed_B_3

Address:0xB0029

Table 1032 **• Eth_10Gbase-R PCS Test Pattern Seed B 3**

Bit	Name	Access	Description	Default
9:0	PCS_SEEDB_3	R/W	Test pattern seed B bits 48-57	0x000

2.11.1.24 Ethernet 10Gbase-R PCS Test-Pattern Control

Short Name: Eth_10GBASE_R_PCS_test_pattern_control

Address:0xB002A

Table 1033 **• Eth_10Gbase-R PCS Test-Pattern Control**

Bit	Name	Access	Description	Default
5	PCS_PRBS31_ANA	R/W	0: Disable PRBS31 test pattern mode on the receive path 1: Enable PRBS31 test pattern mode on the receive path	0x0
4	PCS_PRBS31_GEN	R/W	0: Disable PRBS31 test pattern mode on the transmit path 1: Enable PRBS31 test pattern mode on the transmit path	0x0
3	PCS_TSTPAT_GEN	R/W	0: Disable transmit test pattern 1: Enable transmit test pattern	0x0
2	PCS_TSTPAT_ENA	R/W	0: Disable receive test pattern 1: Enable receive test pattern	0x0
1	PCS_TSTPAT_SEL	R/W	0: Pseudo random test pattern 1: Square wave test pattern	0x0
0	PCS_TSTDAT_SEL	R/W	0: LF data pattern 1: Zero data pattern	0x0

2.11.1.25 Ethernet 10Gbase-R PCS Test-Pattern Counter

Short Name: Eth_10GBASE_R_PCS_test_pattern_counter

Address:0xB002B

Table 1034 **• Eth_10Gbase-R PCS Test-Pattern Counter**

Bit	Name	Access	Description	Default
15:0	PCS_ERR_CNT	R/O	(COR) Error counter This is the 16-bit test pattern error counter defined by IEEE. The counter is cleared upon read of this register. There is a 32-bit version of this counter in registers Test_Error_Counter_0 and Test_Error_Counter_1. If reading the 32-bit version, read Test_Error_Counter_1, followed by Test_Error_Counter_0. A read of register Test_Error_Counter_0 or Eth_10GBASE_R_PCS_test_pattern_counter will clear the 32-bit error counter.	0x0000

2.11.2 Extended PCS-10G

2.11.2.1 USR Test 0

Short Name:USR_Test_0

Address:0xB8000

***Table 1035* • USR Test 0**

Bit	Name	Access	Description	Default
15:0	PCS_USRPAT_0	R/W	User-defined data pattern [15:0]	0x0000

2.11.2.2 USR Test 1

Short Name:USR_Test_1

Address:0xB8001

***Table 1036* • USR Test 1**

Bit	Name	Access	Description	Default
15:0	PCS_USRPAT_1	R/W	User-defined data pattern [31:16]	0x0000

2.11.2.3 USR Test 2

Short Name:USR_Test_2

Address:0xB8002

***Table 1037* • USR Test 2**

Bit	Name	Access	Description	Default
15:0	PCS_USRPAT_2	R/W	User-defined data pattern [47:32]	0x0000

2.11.2.4 USR Test 3

Short Name:USR_Test_3

Address:0xB8003

***Table 1038* • USR Test 3**

Bit	Name	Access	Description	Default
15:0	PCS_USRPAT_3	R/W	User-defined data pattern [63:48]	0x0000

2.11.2.5 Square Wave Pulse Width

Short Name: Square_Wave_Pulse_Width

Address:0xB8004

***Table 1039* • Square Wave Pulse Width**

Bit	Name	Access	Description	Default
3:0	PCS_SQPW	R/W	Square wave pulse width	0x0

2.11.2.6 PCS Control 3

Short Name:PCS_Control_3

Address:0xB8005

***Table 1040* • PCS Control 3**

Bit	Name	Access	Description	Default
10	DSCR_DIS	R/W	0: Enable 1: Disable	0x0
9	SCR_DIS	R/W	0: Enable 1: Disable	0x0
5	Disable_RX_block_sequence_check	R/W	0: Blocks errors are generated when an invalid block sequence is encountered in the Rx path 1: Blocks errors are not generated when an invalid block sequence is encountered in the Rx path	0x0
4	Disable_TX_block_sequence_check	R/W	0: Blocks errors are generated when an invalid block sequence is encountered in the Tx path 1: Blocks errors are not generated when an invalid block sequence is encountered in the Tx path	0x0
0	PCS_USRPAT_ENA	R/W	User test pattern enable 0: Disable 1: Enable	0x0

2.11.2.7 Test Error Counter 0

Short Name: Test_Error_Counter_0

Address:0xB8007

***Table 1041* • Test Error Counter 0**

Bit	Name	Access	Description	Default
15:0	PCS_VSERR_CNT_0	R/O	(COR) Lower 16 bits of 32-bit version of PCS_ERR_CNT (Eth_10GBASE_R_PCS_test_pattern_counter) This register should only be read directly after reading Test_Error_Counter_1. Upon read of this register or Eth_10GBASE_R_PCS_test_pattern_counter, the 32-bit error counter is cleared.	0x0000

2.11.2.8 Test Error Counter 1

Short Name: Test_Error_Counter_1

Address:0xB8008

Table 1042 **• Test Error Counter 1**

Bit	Name	Access	Description	Default
15:0	PCS_VSERR_CNT_1	R/O	(COR) Upper 16 bits of 32-bit version of PCS_ERR_CNT (Eth_10GBASE_R_PCS_test_pattern_counter) This register should be read, followed immediately by Test_Error_Counter_0. Upon read of Test_Error_Counter_0 or Eth_10GBASE_R_PCS_test_pattern_counter, the 32-bit error counter is cleared.	0x0000

2.11.2.9 PCS Tx Sequencing Error Count

Short Name:PCS_TX_SEQ_ERR_CNT

Address:0xB8010

Table 1043 **• PCS Tx Sequencing Error Count**

Bit	Name	Access	Description	Default
15:0	TX_SEQ_ERR_CNT	R/O	Tx sequencing error count. The counter saturates when the maximum value is exceeded. The counter is cleared when the register is read.	0x0000

2.11.2.10 PCS Rx Sequencing Error Count

Short Name:PCS_RX_SEQ_ERR_CNT

Address:0xB8011

Table 1044 **• PCS Rx Sequencing Error Count**

Bit	Name	Access	Description	Default
15:0	RX_SEQ_ERR_CNT	R/O	Rx sequencing error count. The counter saturates when the maximum value is exceeded. The counter is cleared when the register is read.	0x0000

2.11.2.11 PCS Tx Block Encode Error Count

Short Name:PCS_TX_BLK_ENC_ERR_CNT

Address:0xB8012

Table 1045 **• PCS Tx Block Encode Error Count**

Bit	Name	Access	Description	Default
15:0	TX_BLK_ENC_ERR_CNT	R/O	Tx block encode error count. The counter saturates when the maximum value is exceeded. The counter is cleared when the register is read.	0x0000

2.11.2.12 PCS Rx Block Decode Error Count

Short Name:PCS_PCS_RX_BLK_DEC_ERR_CNT

Address:0xB8013

***Table 1046* • PCS Rx Block Decode Error Count**

Bit	Name	Access	Description	Default
15:0	PCS_RX_BLK_DEC_ERR_CNT	R/O	Rx block decode error count. The counter saturates when the maximum value is exceeded. The counter is cleared when the register is read.	0x0000

2.11.2.13 PCS Tx Character Encode Error Count

Short Name:PCS_TX_CHAR_ENC_ERR_CNT

Address:0xB8014

***Table 1047* • PCS Tx Character Encode Error Count**

Bit	Name	Access	Description	Default
15:0	TX_CHAR_ENC_ERR_CNT	R/O	Tx character encode error count. The counter saturates when the maximum value is exceeded. The counter is cleared when the register is read.	0x0000

2.11.2.14 PCS Rx Character Decode Error Count

Short Name:PCS_RX_CHAR_DEC_ERR_CNT

Address:0xB8015

***Table 1048* • PCS Rx Character Decode Error Count**

Bit	Name	Access	Description	Default
15:0	RX_CHAR_DEC_ERR_CNT	R/O	Rx character decode error count. The counter saturates when the maximum value is exceeded. The counter is cleared when the register is read.	0x0000

2.11.2.15 Loopback FIFO Status and Control

Short Name: Loopback_FIFOs_Stat_Ctrl

Address:0xB8016

***Table 1049* • Loopback FIFO Status and Control**

Bit	Name	Access	Description	Default
1	Loop_64b_FIFO_Overflow	R/O	Loopback_64b FIFO overflow status. This is a sticky bit that latches the high state. The latch-high bit is cleared when the register is read. 0: normal operation 1: over/under flow condition	0x0
0	Loop_64b_FIFO_Sync_Inhibit	R/W	Selects whether loopback_64b FIFO's sync inhibit feature is enabled. 0: Disabled 1: Enabled	0x0

2.11.2.16 PCS Control 4

Short Name:PCS_Control_4

Address:0xB8600

***Table 1050* • PCS Control 4**

Bit	Name	Access	Description	Default
1	Disable_inversion_of_input_pattern	R/W	0: Inversion is enabled 1: Disable inversion of input pattern during PRBS58 test pattern generation	0x0
0	RX_fault_sel	R/W	0: rx_status = block_lock 1: rx_status = block_lock * !hi_ber (IEEE compliant)	0x0

2.11.2.17 PCS Control 5

Short Name:PCS_Control_5

Address:0xB8601

***Table 1051* • PCS Control 5**

Bit	Name	Access	Description	Default
1	TX_LF_FILT_EN	R/W	Enables re-mapping of Local_Faults to Idles in Tx path 0: Disable re-mapping 1: Enable re-mapping	0x0
0	RX_LF_FILT_EN	R/W	Enable re-mapping of Local_Faults to Idles in Rx path 0: Disable re-mapping 1: Enable re-mapping	0x1

2.11.2.18 PCS LF_filt Linkup Timer

Short Name:PCS_LF_filt_linkup_timer

Address:0xB8602

***Table 1052* • PCS LF_filt Linkup Timer**

Bit	Name	Access	Description	Default
15:0	LF_FILT_UP_TMR	R/W	When no LF's, the filt_timer block will count up to this value before enabling filters. The counter increments once every 49.6ns	0x0064

2.11.2.19 PCS LF_filt Linkdown Timer

Short Name:PCS_LF_filt_linkdown_timer

Address:0xB8603

***Table 1053* • PCS LF_filt Linkdown Timer**

Bit	Name	Access	Description	Default
15:0	LF_FILT_DOWN_TMR	R/W	Upon stream of LF's, the filt_timer block will count up to this value before disabling filters. The counter increments once every 49.6ns	0x012C

2.11.2.20 PCS Interrupt Pending 1

Short Name:PCS_INTR_PEND1

Address:0xB8E00

***Table 1054* • PCS Interrupt Pending 1**

Bit	Name	Access	Description	Default
9	RX_LINK_STAT_INTR_PEND	Sticky	The interrupt pending bit is asserted when the status signal driving PCS_Status_1::PCS_RECEIVE_LINK_STATUS changes state. The sticky bit is cleared when a 1 is written to the register bit. 0: An interrupt event has not occurred. 1: An interrupt event has occurred.	0x0
8	HIGHBER_INTR_PEND	Sticky	The interrupt pending bit is asserted when Eth_10GBASE_R_PCS_Status_2::PCS_HIGHBER status changes state. The sticky bit is cleared when a 1 is written to the register bit. 0: An interrupt event has not occurred. 1: An interrupt event has occurred.	0x0
7	FEC_FIXED_CNT_THRESH_INTR_PEND	Sticky	This interrupt pending register bit is asserted when the KR_FEC_CORRECTED_BLOCKS counter exceeds the FEC_FIXED_ERR_CNT_THRESH value. The bit is asserted when the counter transitions from being less than the threshold to being greater than the threshold. The sticky bit is cleared when a 1 is written to the bit. 0: An interrupt event has not occurred. 1: An interrupt event has occurred.	0x0
6	FEC_UNFIXED_CNT_THRESH_INTR_PEND	Sticky	This interrupt pending register bit is asserted when the KR_FEC_UNCORRECTED_BLOCKS counter exceeds the FEC_UNFIXED_ERR_CNT_THRESH value. The bit is asserted when the counter transitions from being less than the threshold to being greater than the threshold. The sticky bit is cleared when a 1 is written to the bit. 0: An interrupt event has not occurred. 1: An interrupt event has occurred.	0x0
5	TX_SEQ_CNT_THRESH_INTR_PEND	Sticky	This interrupt pending register bit is asserted when the PCS_TX_SEQ_ERR_CNT counter exceeds the TX_SEQ_ERR_CNT_THRESH value. The bit is asserted when the counter transitions from being less than the threshold to being greater than the threshold. The sticky bit is cleared when a 1 is written to the bit. 0: An interrupt event has not occurred. 1: An interrupt event has occurred.	0x0

Table 1054 • **PCS Interrupt Pending 1** ***(continued)***

Bit	Name	Access	Description	Default
4	RX_SEQ_CNT_THRESH_INTR_PEND	Sticky	This interrupt pending register bit is asserted when the PCS_RX_SEQ_ERR_CNT counter exceeds the RX_SEQ_ERR_CNT_THRESH value. The bit is asserted when the counter transitions from being less than the threshold to being greater than the threshold. The sticky bit is cleared when a 1 is written to the bit. 0: An interrupt event has not occurred. 1: An interrupt event has occurred.	0x0
3	TX_BLK_ENC_CNT_THRESH_INTR_PEND	Sticky	This interrupt pending register bit is asserted when the PCS_TX_BLK_ENC_ERR_CNT counter exceeds the TX_BLK_ENC_ERR_CNT_THRESH value. The bit is asserted when the counter transitions from being less than the threshold to being greater than the threshold. The sticky bit is cleared when a 1 is written to the bit. 0: An interrupt event has not occurred. 1: An interrupt event has occurred.	0x0
2	RX_BLK_DEC_CNT_THRESH_INTR_PEND	Sticky	This interrupt pending register bit is asserted when the PCS_RX_BLK_DEC_ERR_CNT counter exceeds the RX_BLK_DEC_ERR_CNT_THRESH value. The bit is asserted when the counter transitions from being less than the threshold to being greater than the threshold. The sticky bit is cleared when a 1 is written to the bit. 0: An interrupt event has not occurred. 1: An interrupt event has occurred.	0x0
1	TX_CHAR_ENC_CNT_THRESH_INTR_PEND	Sticky	This interrupt pending register bit is asserted when the PCS_TX_CHAR_ENC_ERR_CNT counter exceeds the TX_CHAR_ENC_ERR_CNT_THRESH value. The bit is asserted when the counter transitions from being less than the threshold to being greater than the threshold. The sticky bit is cleared when a 1 is written to the bit. 0: An interrupt event has not occurred. 1: An interrupt event has occurred.	0x0
0	RX_CHAR_DEC_CNT_THRESH_INTR_PEND	Sticky	This interrupt pending register bit is asserted when the PCS_RX_CHAR_DEC_ERR_CNT counter exceeds the RX_CHAR_DEC_ERR_CNT_THRESH value. The bit is asserted when the counter transitions from being less than the threshold to being greater than the threshold. The sticky bit is cleared when a 1 is written to the bit. 0: An interrupt event has not occurred. 1: An interrupt event has occurred.	0x0

2.11.2.21 PCS Interrupt Mask 1

Short Name:PCS_INTR_MASK1

Address:0xB8E01

***Table 1055* • PCS Interrupt Mask 1**

Bit	Name	Access	Description	Default
9	RX_LINK_STAT_MASK	R/W	Interrupt mask for RX_LINK_STAT_INTR_PEND. 0: Interrupt disabled 1: Interrupt enabled	0x0
8	HIGHBER_MASK	R/W	Interrupt mask for HIGHBER_INTR_PEND. 0: Interrupt disabled 1: Interrupt enabled	0x0
7	FEC_FIXED_CNT_THRESH_MASK	R/W	Interrupt mask for KR_FEC_CORRECTED_BLOCKS error counter exceeding threshold level. 0: Interrupt disabled 1: Interrupt enabled	0x0
6	FEC_UNFIXED_CNT_THRESH_MASK	R/W	Interrupt mask for KR_FEC_UNCORRECTED_BLOCKS error counter exceeding threshold level. 0: Interrupt disabled 1: Interrupt enabled	0x0
5	TX_SEQ_CNT_THRESH_MASK	R/W	Interrupt mask for PCS_TX_SEQ_ERR_CNT exceeding threshold level. 0: Interrupt disabled 1: Interrupt enabled	0x0
4	RX_SEQ_CNT_THRESH_MASK	R/W	Interrupt mask for PCS_RX_SEQ_ERR_CNT exceeding threshold level. 0: Interrupt disabled 1: Interrupt enabled	0x0
3	TX_BLK_ENC_CNT_THRESH_MASK	R/W	Interrupt mask for PCS_TX_BLK_ENC_ERR_CNT exceeding threshold level. 0: Interrupt disabled 1: Interrupt enabled	0x0
2	RX_BLK_DEC_CNT_THRESH_MASK	R/W	Interrupt mask for PCS_RX_BLK_DEC_ERR_CNT exceeding threshold level. 0: Interrupt disabled 1: Interrupt enabled	0x0
1	TX_CHAR_ENC_CNT_THRESH_MASK	R/W	Interrupt mask for PCS_TX_CHAR_ENC_ERR_CNT exceeding threshold level. 0: Interrupt disabled 1: Interrupt enabled	0x0
0	RX_CHAR_DEC_CNT_THRESH_MASK	R/W	Interrupt mask for PCS_RX_CHAR_DEC_ERR_CNT exceeding threshold level. 0: Interrupt disabled 1: Interrupt enabled	0x0

2.11.2.22 PCS Interrupt Status Signals

Short Name:PCS_INTR_STATUS

Address:0xB8E03

***Table 1056* • PCS Interrupt Status Signals**

Bit	Name	Access	Description	Default
9	PCS_receive_link_status	R/O	This is the status signal used to assert the RX_LINK_STAT_INTR_PEND register. It is the same status used to assert the latch-low PCS_Status_1::PCS_RECEIVE_LINK_STATUS register. 0: PCS received link down. BLOCK_LOCK=0 OR HI_BER=1 1: PCS receive link up. BLOCK_LOCK=1 AND HI_BER=0.	0x1
8	PCS_HIGHBER	R/O	This is the status signal used to assert the HIGHBER_INTR_PEND register. It is the same status used to assert the latch-high Eth_10GBASE_R_PCS_Status_2::PCS_HIGHBER register. 0: 10GBASE-R PCS has not reported a high BER 1: 10GBASE-R PCS has reported a high BER	0x0
7	FEC_FIXED_THRESH_COMP	R/O	Present result of comparing KR FEC's corrected block count (KR_FEC_CORRECTED_UPPER/KR_FEC_CORRECTED_LOWER) to the threshold setting in FEC_FIXED_ERR_CNT_THRESH1/FEC_FIXED_ERR_CNT_THRESH0. 0: counter does not exceed threshold setting 1: counter exceeds threshold setting	0x0
6	FEC_UNFIXED_THRESH_COMP	R/O	Present result of comparing KR FEC's uncorrectable block count (KR_FEC_UNCORRECTED_UPPER/KR_FEC_UNCORRECTED_LOWER) to the threshold setting in FEC_UNFIXED_ERR_CNT_THRESH1/FEC_UNFIXED_ERR_CNT_THRESH0. 0: counter does not exceed threshold setting 1: counter exceeds threshold setting	0x0
5	TX_SEQ_THRESH_COMP	R/O	Present result of comparing Tx sequencing error count (PCS_TX_SEQ_ERR_CNT) to the threshold setting in register TX_SEQ_ERR_CNT_THRESH. 0: counter does not exceed threshold setting 1: counter exceeds threshold setting	0x0
4	RX_SEQ_THRESH_COMP	R/O	Present result of comparing Rx sequencing error count (PCS_RX_SEQ_ERR_CNT) to the threshold setting in register RX_SEQ_ERR_CNT_THRESH. 0: counter does not exceed threshold setting 1: counter exceeds threshold setting	0x0

Table 1056 • **PCS Interrupt Status Signals *(continued)***

Bit	Name	Access	Description	Default
3	TX_BLK_ENC_THRESH_COMP	R/O	Present result of comparing Tx block encode error count (PCS_TX_BLK_ENC_ERR_CNT) to the threshold setting in register TX_BLK_ENC_ERR_CNT_THRESH. 0: counter does not exceed threshold setting 1: counter exceeds threshold setting	0x0
2	RX_BLK_DEC_THRESH_COMP	R/O	Present result of comparing Rx block decode error count (PCS_RX_BLK_DEC_ERR_CNT) to the threshold setting in register RX_BLK_DEC_ERR_CNT_THRESH. 0: counter does not exceed threshold setting 1: counter exceeds threshold setting	0x0
1	TX_CHAR_ENC_THRESH_COMP	R/O	Present result of comparing Tx character encode error count (PCS_TX_CHAR_ENC_ERR_CNT) to the threshold setting in register TX_CHAR_ENC_ERR_CNT_THRESH. 0: counter does not exceed threshold setting 1: counter exceeds threshold setting	0x0
0	RX_CHAR_DEC_THRESH_COMP	R/O	Present result of comparing Rx character decode error count (PCS_RX_CHAR_DEC_ERR_CNT) to the threshold setting in register RX_CHAR_DEC_ERR_CNT_THRESH. 0: counter does not exceed threshold setting 1: counter exceeds threshold setting	0x0

2.11.2.23 Tx Sequencing Error Count Threshold

Short Name:TX_SEQ_ERR_CNT_THRESH

Address:0xB8E04

Table 1057 • **Tx Sequencing Error Count Threshold**

Bit	Name	Access	Description	Default
15:0	TX_SEQ_ERR_CNT_THRESH	R/W	Tx sequencing error count threshold	0xFFFF

2.11.2.24 Rx Sequencing Error Count Threshold

Short Name:RX_SEQ_ERR_CNT_THRESH

Address:0xB8E05

Table 1058 • **Rx Sequencing Error Count Threshold**

Bit	Name	Access	Description	Default
15:0	RX_SEQ_ERR_CNT_THRESH	R/W	Rx sequencing error count threshold	0xFFFF

2.11.2.25 Tx Block Encode Error Count Threshold

Short Name:TX_BLK_ENC_ERR_CNT_THRESH

Address:0xB8E06

Table 1059 **• Tx Block Encode Error Count Threshold**

Bit	Name	Access	Description	Default
15:0	TX_BLK_ENC_ERR_CNT_THRESH	R/W	Tx block encode error count threshold	0xFFFF

2.11.2.26 Rx Block Decode Error Count Threshold

Short Name:RX_BLK_DEC_ERR_CNT_THRESH

Address:0xB8E07

Table 1060 **• Rx Block Decode Error Count Threshold**

Bit	Name	Access	Description	Default
15:0	RX_BLK_DEC_ERR_CNT_THRESH	R/W	Rx block decode error count threshold	0xFFFF

2.11.2.27 Tx Character Encode Error Count Threshold

Short Name:TX_CHAR_ENC_ERR_CNT_THRESH

Address:0xB8E08

Table 1061 **• Tx Character Encode Error Count Threshold**

Bit	Name	Access	Description	Default
15:0	TX_CHAR_ENC_ERR_CNT_THRESH	R/W	Tx character encode error count threshold	0xFFFF

2.11.2.28 Rx Character Decode Error Count Threshold

Short Name:RX_CHAR_DEC_ERR_CNT_THRESH

Address:0xB8E09

Table 1062 **• Rx Character Decode Error Count Threshold**

Bit	Name	Access	Description	Default
15:0	RX_CHAR_DEC_ERR_CNT_THRESH	R/W	Rx character decode error count threshold	0xFFFF

2.11.2.29 FEC Fixed Error Count Threshold 1

Short Name:FEC_FIXED_ERR_CNT_THRESH1

Address:0xB8E0A

Table 1063 **• FEC Fixed Error Count Threshold 1**

Bit	Name	Access	Description	Default
15:0	FEC_FIXED_ERR_CNT_THRESH1	R/W	FEC fixed error count Threshold[31:16]	0xFFFF

2.11.2.30 FEC Fixed Error Count Threshold 0

Short Name:FEC_FIXED_ERR_CNT_THRESH0

Address:0xB8E0B

***Table 1064* • FEC Fixed Error Count Threshold 0**

Bit	Name	Access	Description	Default
15:0	FEC_FIXED_ERR_CNT_THRESH0	R/W	FEC fixed error count Threshold[15:0]	0xFFFF

2.11.2.31 FEC Unfixable Error Count Threshold 1

Short Name:FEC_UNFIXED_ERR_CNT_THRESH1

Address:0xB8E0C

***Table 1065* • FEC Unfixable Error Count Threshold 1**

Bit	Name	Access	Description	Default
15:0	FEC_UNFIXED_ERR_CNT_THRESH1	R/W	FEC unfixable error count Threshold[31:16]	0xFFFF

2.11.2.32 FEC Unfixable Error Count Threshold 0

Short Name:FEC_UNFIXED_ERR_CNT_THRESH0

Address:0xB8E0D

***Table 1066* • FEC Unfixable Error Count Threshold 0**

Bit	Name	Access	Description	Default
15:0	FEC_UNFIXED_ERR_CNT_THRESH0	R/W	FEC unfixable error count Threshold[15:0]	0xFFFF

2.12 HOST_PCS1G (Device 0x3)

***Table 1067* • PCS1G_CFG_STATUS**

Address	Short Description	Register Name	Details
0x3E000	PCS1G Configuration	PCS1G_CFG	Page 389
0x3E001	PCS1G Mode Configuration	PCS1G_MODE_CFG	Page 389
0x3E002	PCS1G Signal Detect Configuration	PCS1G_SD_CFG	Page 390
0x3E003	PCS1G Aneg Configuration	PCS1G_ANEG_CFG	Page 390
0x3E004	PCS1G Aneg Configuration	PCS1G_ANEG_CFG2	Page 391
0x3E005	PCS1G Aneg Next Page Configuration	PCS1G_ANEG_NP_CFG	Page 391
0x3E006	PCS1G Aneg Next Page Configuration	PCS1G_ANEG_NP_CFG2	Page 391
0x3E007	PCS1G Loopback Configuration	PCS1G_LB_CFG	Page 392
0x3E00A	PCS1G ANEG Status	PCS1G_ANEG_STATUS	Page 392
0x3E00B	PCS1G ANEG Status 2	PCS1G_ANEG_STATUS2	Page 392
0x3E00C	PCS1G Aneg Next Page Status	PCS1G_ANEG_NP_STATUS	Page 393
0x3E00D	PCS1G Link Status	PCS1G_LINK_STATUS	Page 393
0x3E00E	PCS1G Link Down Counter	PCS1G_LINK_DOWN_CNT	Page 393
0x3E00F	PCS1G Sticky	PCS1G_STICKY	Page 394

Table 1067 • **PCS1G_CFG_STATUS *(continued)***

Address	Short Description	Register Name	Details
0x3E011	PCS1G Low Power Idle Configuration	PCS1G_LPI_CFG	Page 394
0x3E012	PCS1G Low Power Idle Configuration	PCS1G_LPI_CFG2	Page 395
0x3E013	PCS1G Wake Error Counter	PCS1G_LPI_WAKE_ERROR_CNT	Page 395
0x3E014	PCS1G Low Power Idle Status	PCS1G_LPI_STATUS	Page 395

Table 1068 • **PCS1G_TSTPAT_CFG_STATUS**

Address	Short Description	Register Name	Details
0x3E015	PCS1G TSTPAT MODE CFG	PCS1G_TSTPAT_MODE_CFG	Page 396
0x3E016	PCS1G TSTPAT STATUS	PCS1G_TSTPAT_STATUS	Page 396

Table 1069 • **PCS1G_XGMII_CFG_STATUS**

Address	Short Description	Register Name	Details
0x3E017	PCS1G XGMII Configuration	PCS1G_XGMII_CFG	Page 397

2.12.1 1G Configuration and Status

Configuration and status register set for PCS1G

2.12.1.1 PCS1G Configuration

Short Name:PCS1G_CFG

Address:0x3E000

PCS1G main configuration register

Table 1070 • **PCS1G Configuration**

Bit	Name	Access	Description	Default
4	LINK_STATUS_TYPE	R/W	Set type of link_status indication at CPU-System 0: Sync_status (from PCS synchronization state machine) 1: Bit 15 of PCS1G_ANEG_STATUS.lp_adv_ability (Link up/down)	0x0
0	PCS_ENA	R/W	PCS enable 0: Disable PCS 1: Enable PCS	0x0

2.12.1.2 PCS1G Mode Configuration

Short Name:PCS1G_MODE_CFG

Address:0x3E001

PCS1G mode configuration

***Table 1071* • PCS1G Mode Configuration**

Bit	Name	Access	Description	Default
4	UNIDIR_MODE_ENA	R/W	Unidirectional mode enable. Implementation of 802.3, Clause 66. When asserted, this enables MAC to transmit data independent of the state of the receive link. 0: Unidirectional mode disabled 1: Unidirectional mode enabled	0x0
0	SGMII_MODE_ENA	R/W	Selection of PCS operation 0: PCS is used in SERDES mode 1: PCS is used in SGMII mode. Configuration bit PCS1G_ANEG_CFG.SW_RESOLVE_ENA must be set additionally	0x1

2.12.1.3 PCS1G Signal Detect Configuration

Short Name:PCS1G_SD_CFG

Address:0x3E002

PCS1G signal_detect configuration

***Table 1072* • PCS1G Signal Detect Configuration**

Bit	Name	Access	Description	Default
8	SD_SEL	R/W	Signal detect selection (select input for internal signal_detect line) 0: Select signal_detect line from hardmacro 1: Select external signal_detect line	0x0
4	SD_POL	R/W	Signal detect polarity: The signal level on signal_detect input pin must be equal to SD_POL to indicate signal detection (SD_ENA must be set) 0: Signal Detect input pin must be '0' to indicate a signal detection 1: Signal Detect input pin must be '1' to indicate a signal detection	0x1
0	SD_ENA	R/W	Signal Detect Enable 0: The Signal Detect input pin is ignored. The PCS assumes an active Signal Detect at all times 1: The Signal Detect input pin is used to determine if a signal is detected	0x1

2.12.1.4 PCS1G Aneg Configuration

Short Name:PCS1G_ANEG_CFG

Address:0x3E003

PCS1G Auto-negotiation configuration register

Table 1073 **• PCS1G Aneg Configuration**

Bit	Name	Access	Description	Default
8	SW_RESOLVE_ENA	R/W	Software Resolve Abilities 0: If Auto Negotiation fails (no matching HD or FD capabilities) the link is disabled 1: The result of an Auto Negotiation is ignored - the link can be setup via software. This bit must be set in SGMII mode.	0x0
1	ANEG_RESTART_ONE_SHOT	One-shot	Auto Negotiation Restart 0: No action 1: Restart Auto Negotiation	0x0
0	ANEG_ENA	R/W	Auto Negotiation Enable 0: Auto Negotiation Disabled 1: Auto Negotiation Enabled	0x0

2.12.1.5 PCS1G Aneg Configuration 2

Short Name:PCS1G_ANEG_CFG2

Address:0x3E004

PCS1G Auto-negotiation configuration register

Table 1074 **• PCS1G Aneg Configuration**

Bit	Name	Access	Description	Default
15:0	ADV_ABILITY	R/W	Advertised Ability Register: Holds the capabilities of the device as described IEEE 802.3, Clause 37. If SGMII mode is selected (PCS1G_MODE_CFG.SGMII_MODE_ENA = 1), SW_RESOLVE_ENA must be set.	0x0000

2.12.1.6 PCS1G Aneg Next Page Configuration

Short Name:PCS1G_ANEG_NP_CFG

Address:0x3E005

PCS1G Auto-negotiation configuration register for next-page function

Table 1075 **• PCS1G Aneg Next Page Configuration**

Bit	Name	Access	Description	Default
0	NP_LOADED_ONE_SHOT	One-shot	Next page loaded 0: next page is free and can be loaded 1: next page register has been filled (to be set after np_tx has been filled)	0x0

2.12.1.7 PCS1G Aneg Next Page Configuration

Short Name:PCS1G_ANEG_NP_CFG2

Address:0x3E006

PCS1G Auto-negotiation configuration register for next-page function

Table 1076 **• PCS1G Aneg Next Page Configuration**

Bit	Name	Access	Description	Default
15:0	NP_TX	R/W	Next page register: Holds the next-page information as described in IEEE 802.3, Clause 37	0x0000

2.12.1.8 PCS1G Loopback Configuration

Short Name:PCS1G_LB_CFG

Address:0x3E007

PCS1G Loop-Back configuration register

Table 1077 **• PCS1G Loopback Configuration**

Bit	Name	Access	Description	Default
0	TBI_HOST_LB_ENA	R/W	Loops data in PCS (TBI side) from egress direction to ingress direction. The Rx clock is automatically set equal to the Tx clock 0: TBI Loopback Disabled 1:TBI Loopback Enabled	0x0

2.12.1.9 PCS1G ANEG Status

Short Name:PCS1G_ANEG_STATUS

Address:0x3E00A

PCS1G Auto-negotiation status register

Table 1078 **• PCS1G ANEG Status**

Bit	Name	Access	Description	Default
4	PR	R/O	Resolve priority 0: ANEG is in progress 1: ANEG nearly finished - priority can be resolved (via software)	0x0
3	PAGE_RX_STICKY	Sticky	Status indicating whether a new page has been received. 0: No new page received 1: New page received Bit is cleared by writing a 1 to this position.	0x0
0	ANEG_COMPLETE	R/O	Auto Negotiation Complete 0: No Auto Negotiation has been completed 1: Indicates that an Auto Negotiation has completed successfully	0x0

2.12.1.10 PCS1G ANEG Status 2

Short Name:PCS1G_ANEG_STATUS2

Address:0x3E00B

PCS1G Auto-negotiation status register

Table 1079 **• PCS1G ANEG Status Register**

Bit	Name	Access	Description	Default
15:0	LP_ADV_ABILITY	R/O	Advertised abilities from link partner as described in IEEE 802.3, Clause 37	0x0000

2.12.1.11 PCS1G Aneg Next Page Status

Short Name:PCS1G_ANEG_NP_STATUS

Address:0x3E00C

PCS1G Auto-negotiation next page status register

Table 1080 **• PCS1G Aneg Next Page Status Register**

Bit	Name	Access	Description	Default
15:0	LP_NP_RX	R/O	Next page ability register from link partner as described in IEEE 802.3, Clause 37	0x0000

2.12.1.12 PCS1G Link Status

Short Name:PCS1G_LINK_STATUS

Address:0x3E00D

PCS1G link status register

Table 1081 **• PCS1G link status**

Bit	Name	Access	Description	Default
8	SIGNAL_DETECT	R/O	Indicates whether or not the selected Signal Detect input line is asserted 0: No signal detected 1: Signal detected	0x0
4	LINK_STATUS	R/O	Indicates whether the link is up or down. A link is up when ANEG state machine is in state LINK_OK or AN_DISABLE_LINK_OK 0: Link down 1: Link up	0x0
0	SYNC_STATUS	R/O	Indicates if PCS has successfully synchronized 0: PCS is out of sync 1: PCS has synchronized	0x0

2.12.1.13 PCS1G Link Down Counter

Short Name:PCS1G_LINK_DOWN_CNT

Address:0x3E00E

PCS1G link down counter register

Table 1082 **• PCS1G Link Down Counter**

Bit	Name	Access	Description	Default
7:0	LINK_DOWN_CNT	R/W	Link Down Counter. A counter that counts the number of times a link has been down. The counter does not saturate at 255 and is only cleared when writing 0 to the register	0x00

2.12.1.14 PCS1G Sticky

Short Name:PCS1G_STICKY

Address:0x3E00F

PCS1G status register for sticky bits

Table 1083 **• PCS1G Sticky**

Bit	Name	Access	Description	Default
4	LINK_DOWN_STICKY	Sticky	The sticky bit is set when the link has been down - i.e. if the ANEG state machine has not been in the AN_DISABLE_LINK_OK or LINK_OK state for one or more clock cycles. This occurs if e.g. ANEG is restarted or for example if signal-detect or synchronization has been lost for more than 10 ms (1.6 ms in SGMII mode). By setting the UDLT bit, the required down time can be reduced to 9,77 us (1.56 us) 0: Link is up 1: Link has been down Bit is cleared by writing a 1 to this position.	0x0
0	OUT_OF_SYNC_STICKY	Sticky	Sticky bit indicating if PCS synchronization has been lost 0: Synchronization has not been lost at any time 1: Synchronization has been lost for one or more clock cycles Bit is cleared by writing a 1 to this position.	0x0

2.12.1.15 PCS1G Low Power Idle Configuration

Short Name:PCS1G_LPI_CFG

Address:0x3E011

Configuration register for Low Power Idle (Energy Efficient Ethernet)

Table 1084 **• PCS1G Low Power Idle Configuration**

Bit	Name	Access	Description	Default
5:4	LPI_RX_WTIM	R/W	Max wake-up time before link_fail 00: 10 us 01: 13 us 10: 17 us 11: 20 us	0x3
0	TX_ASSERT_LPIDLE	R/W	Assert Low-Power Idle (LPI) in transmit mode 0: Disable LPI transmission 1: Enable LPI transmission	0x0

2.12.1.16 PCS1G Low Power Idle Configuration

Short Name:PCS1G_LPI_CFG2

Address:0x3E012

Configuration register for Low Power Idle (Energy Efficient Ethernet)

***Table 1085* • PCS1G Low Power Idle Configuration**

Bit	Name	Access	Description	Default
4	QSGMII_MS_SEL	R/W	QSGMII master/slave selection (only one master allowed per QSGMII). The master drives LPI timing on serdes 0: Slave 1: Master	0x1

2.12.1.17 PCS1G Wake Error Counter

Short Name:PCS1G_LPI_WAKE_ERROR_CNT

Address:0x3E013

PCS1G Low Power Idle wake error counter (Energy Efficient Ethernet)

***Table 1086* • PCS1G Wake Error Counter**

Bit	Name	Access	Description	Default
15:0	WAKE_ERROR_CNT	R/W	Wake Error Counter. A counter that is incremented when the link partner does not send wake-up burst in due time. The counter saturates at 65535 and is cleared when writing 0 to the register	0x0000

2.12.1.18 PCS1G Low Power Idle Status

Short Name:PCS1G_LPI_STATUS

Address:0x3E014

Status register for Low Power Idle (Energy Efficient Ethernet)

***Table 1087* • PCS1G Low Power Idle Status**

Bit	Name	Access	Description	Default
15	RX_LPI_FAIL	R/O	Receiver has failed to recover from Low-Power Idle mode 0: No failure 1: Failed to recover from LPI mode	0x0
12	RX_LPI_EVENT_STICKY	Sticky	Receiver Low-Power idle occurrence 0: No LPI symbols received 1: Receiver has received LPI symbols Bit is cleared by writing a 1 to this position.	0x0
9	RX_QUIET	R/O	Receiver Low-Power Quiet mode 0: Receiver not in quiet mode 1: Receiver is in quiet mode	0x0
8	RX_LPI_MODE	R/O	Receiver Low-Power Idle mode 0: Receiver not in low power idle mode 1: Receiver is in low power idle mode	0x0

Table 1087 • **PCS1G Low Power Idle Status *(continued)***

Bit	Name	Access	Description	Default
4	TX_LPI_EVENT_STICKY	Sticky	Transmitter Low-Power idle occurrence 0: No LPI symbols transmitted 1: Transmitter has transmitted LPI symbols Bit is cleared by writing a 1 to this position.	0x0
1	TX_QUIET	R/O	Transmitter Low-Power Quiet mode 0: Transmitter not in quiet mode 1: Transmitter is in quiet mode	0x0
0	TX_LPI_MODE	R/O	Transmitter Low-Power Idle mode 0: Transmitter not in low power idle mode 1: Transmitter is in low power idle mode	0x0

2.12.1.19 PCS1G Test Pattern Mode Configuration

Short Name:PCS1G_TSTPAT_MODE_CFG

Address:0x3E015

PCS1G testpattern mode configuration register (Frame based pattern 4 and 5 might be not available depending on chip type)

Table 1088 • **PCS1G TSTPAT MODE CFG**

Bit	Name	Access	Description	Default
2:0	JTP_SEL	R/W	Jitter Test Pattern Select: Enables and selects the jitter test pattern to be transmitted. The jitter test patterns are according to the IEEE 802.3, Annex 36A 0: Disable transmission of test patterns 1: High frequency test pattern - repeated transmission of D21.5 code group 2: Low frequency test pattern - repeated transmission of K28.7 code group 3: Mixed frequency test pattern - repeated transmission of K28.5 code group 4: Long continuous random test pattern (packet length is 1524 bytes) 5: Short continuous random test pattern (packet length is 360 bytes)	0x0

2.12.1.20 PCS1G Test Pattern Status

Short Name:PCS1G_TSTPAT_STATUS

Address:0x3E016

PCS1G testpattern status register

Table 1089 • **PCS1G TSTPAT STATUS**

Bit	Name	Access	Description	Default
15:8	JTP_ERR_CNT	R/W	Jitter Test Pattern Error Counter. Due to re-sync measures it might happen that single errors are not counted (applies for 2.5gpbs mode). The counter saturates at 255 and is only cleared when writing 0 to the register	0x00

Table 1089 • **PCS1G TSTPAT STATUS *(continued)***

Bit	Name	Access	Description	Default
4	JTP_ERR	R/O	Jitter Test Pattern Error 0: Jitter pattern checker has found no error 1: Jitter pattern checker has found an error	0x0
0	JTP_LOCK	R/O	Jitter Test Pattern Lock 0: Jitter pattern checker has not locked 1: Jitter pattern checker has locked	0x0

2.12.1.21 PCS1G XGMII Configuration

Short Name:PCS1G_XGMII_CFG

Address:0x3E017

Table 1090 • **PCS1G XGMII Configuration**

Bit	Name	Access	Description	Default
8	RESERVED	R/W	Must be set to its default.	0x1
0	REGEN_PREAMBLE_ENA	R/W	Enable the PCS to regenerate the full preamble when a reduced preamble is detected on the received packet 0=Preamble is not modified 1=Preceeding IDLEs are replaced preamble bytes for the 7 bytes before a start of frame delimiter	0x1

2.13 LINE_PCS1G (Device 0x3)

Table 1091 • **PCS1G_CFG_STATUS**

Address	Short Description	Register Name	Details
0x3E100	PCS1G Configuration	PCS1G_CFG	Page 398
0x3E101	PCS1G Mode Configuration	PCS1G_MODE_CFG	Page 398
0x3E102	PCS1G Signal Detect Configuration	PCS1G_SD_CFG	Page 399
0x3E103	PCS1G Aneg Configuration	PCS1G_ANEG_CFG	Page 399
0x3E104	PCS1G Aneg Configuration	PCS1G_ANEG_CFG2	Page 400
0x3E105	PCS1G Aneg Next Page Configuration	PCS1G_ANEG_NP_CFG	Page 400
0x3E106	PCS1G Aneg Next Page Configuration	PCS1G_ANEG_NP_CFG2	Page 400
0x3E107	PCS1G Loopback Configuration	PCS1G_LB_CFG	Page 401
0x3E10A	PCS1G ANEG Status Register	PCS1G_ANEG_STATUS	Page 401
0x3E10B	PCS1G ANEG Status Register	PCS1G_ANEG_STATUS2	Page 401
0x3E10C	PCS1G Aneg Next Page Status Register	PCS1G_ANEG_NP_STATUS	Page 402
0x3E10D	PCS1G link status	PCS1G_LINK_STATUS	Page 402
0x3E10E	PCS1G link down counter	PCS1G_LINK_DOWN_CNT	Page 402
0x3E10F	PCS1G sticky	PCS1G_STICKY	Page 403
0x3E111	PCS1G Low Power Idle Configuration	PCS1G_LPI_CFG	Page 403

Table 1091 • **PCS1G_CFG_STATUS *(continued)***

Address	Short Description	Register Name	Details
0x3E112	PCS1G Low Power Idle Configuration	PCS1G_LPI_CFG2	Page 404
0x3E113	PCS1G wake error counter	PCS1G_LPI_WAKE_ERROR_CNT	Page 404
0x3E114	PCS1G Low Power Idle Status	PCS1G_LPI_STATUS	Page 404

Table 1092 • **PCS1G_TSTPAT_CFG_STATUS**

Address	Short Description	Register Name	Details
0x3E115	PCS1G TSTPAT MODE CFG	PCS1G_TSTPAT_MODE_CFG	Page 405
0x3E116	PCS1G TSTPAT STATUS	PCS1G_TSTPAT_STATUS	Page 405

Table 1093 • **PCS1G_XGMII_CFG_STATUS**

Address	Short Description	Register Name	Details
0x3E117	PCS1G XGMII Configuration	PCS1G_XGMII_CFG	Page 406

2.13.1 1G Configuration and Status

2.13.1.1 PCS1G Configuration

Short Name:PCS1G_CFG

Address:0x3E100

PCS1G main configuration register

Table 1094 • **PCS1G Configuration**

Bit	Name	Access	Description	Default
4	LINK_STATUS_TYPE	R/W	Set type of link_status indication at CPU-System 0: Sync_status (from PCS synchronization state machine) 1: Bit 15 of PCS1G_ANEG_STATUS.lp_adv_ability (Link up/down)	0x0
0	PCS_ENA	R/W	PCS enable 0: Disable PCS 1: Enable PCS	0x0

2.13.1.2 PCS1G Mode Configuration

Short Name:PCS1G_MODE_CFG

Address:0x3E101

PCS1G mode configuration

Table 1095 **• PCS1G Mode Configuration**

Bit	Name	Access	Description	Default
4	UNIDIR_MODE_ENA	R/W	Unidirectional mode enable. Implementation of 802.3, Clause 66. When asserted, this enables MAC to transmit data independent of the state of the receive link. 0: Unidirectional mode disabled 1: Unidirectional mode enabled	0x0
0	SGMII_MODE_ENA	R/W	Selection of PCS operation 0: PCS is used in SERDES mode 1: PCS is used in SGMII mode. Configuration bit PCS1G_ANEG_CFG.SW_RESOLVE_ENA must be set additionally	0x1

2.13.1.3 PCS1G Signal Detect Configuration

Short Name:PCS1G_SD_CFG

Address:0x3E102

PCS1G signal_detect configuration

Table 1096 **• PCS1G Signal Detect Configuration**

Bit	Name	Access	Description	Default
8	SD_SEL	R/W	Signal detect selection (select input for internal signal_detect line) 0: Select signal_detect line from hardmacro 1: Select external signal_detect line	0x0
4	SD_POL	R/W	Signal detect polarity: The signal level on signal_detect input pin must be equal to SD_POL to indicate signal detection (SD_ENA must be set) 0: Signal Detect input pin must be '0' to indicate a signal detection 1: Signal Detect input pin must be '1' to indicate a signal detection	0x1
0	SD_ENA	R/W	Signal Detect Enable 0: The Signal Detect input pin is ignored. The PCS assumes an active Signal Detect at all times 1: The Signal Detect input pin is used to determine if a signal is detected	0x1

2.13.1.4 PCS1G Aneg Configuration

Short Name:PCS1G_ANEG_CFG

Address:0x3E103

PCS1G Auto-negotiation configuration register

Table 1097 **• PCS1G Aneg Configuration**

Bit	Name	Access	Description	Default
8	SW_RESOLVE_ENA	R/W	Software Resolve Abilities 0: If Auto Negotiation fails (no matching HD or FD capabilities) the link is disabled 1: The result of an Auto Negotiation is ignored - the link can be setup via software. This bit must be set in SGMII mode.	0x0
1	ANEG_RESTART_ONE_SHOT	One-shot	Auto Negotiation Restart 0: No action 1: Restart Auto Negotiation	0x0
0	ANEG_ENA	R/W	Auto Negotiation Enable 0: Auto Negotiation Disabled 1: Auto Negotiation Enabled	0x0

2.13.1.5 PCS1G Aneg Configuration 2

Short Name:PCS1G_ANEG_CFG2

Address:0x3E104

PCS1G Auto-negotiation configuration register

Table 1098 **• PCS1G Aneg Configuration**

Bit	Name	Access	Description	Default
15:0	ADV_ABILITY	R/W	Advertised Ability Register: Holds the capabilities of the device as described IEEE 802.3, Clause 37. If SGMII mode is selected (PCS1G_MODE_CFG.SGMII_MODE_ENA = 1), SW_RESOLVE_ENA must be set.	0x0000

2.13.1.6 PCS1G Aneg Next Page Configuration

Short Name:PCS1G_ANEG_NP_CFG

Address:0x3E105

PCS1G Auto-negotiation configuration register for next-page function

Table 1099 **• PCS1G Aneg Next Page Configuration**

Bit	Name	Access	Description	Default
0	NP_LOADED_ONE_SHOT	One-shot	Next page loaded 0: next page is free and can be loaded 1: next page register has been filled (to be set after np_tx has been filled)	0x0

2.13.1.7 PCS1G Aneg Next Page Configuration 2

Short Name:PCS1G_ANEG_NP_CFG2

Address:0x3E106

PCS1G Auto-negotiation configuration register for next-page function

Table 1100 **• PCS1G Aneg Next Page Configuration**

Bit	Name	Access	Description	Default
15:0	NP_TX	R/W	Next page register: Holds the next-page information as described in IEEE 802.3, Clause 37	0x0000

2.13.1.8 PCS1G Loopback Configuration

Short Name:PCS1G_LB_CFG

Address:0x3E107

PCS1G Loop-Back configuration register

Table 1101 **• PCS1G Loopback Configuration**

Bit	Name	Access	Description	Default
0	TBI_HOST_LB_ENA	R/W	Loops data in PCS (TBI side) from egress direction to ingress direction. The Rx clock is automatically set equal to the Tx clock 0: TBI Loopback Disabled 1:TBI Loopback Enabled	0x0

2.13.1.9 PCS1G ANEG Status

Short Name:PCS1G_ANEG_STATUS

Address:0x3E10A

PCS1G Auto-negotiation status register

Table 1102 **• PCS1G ANEG Status Register**

Bit	Name	Access	Description	Default
4	PR	R/O	Resolve priority 0: ANEG is in progress 1: ANEG nearly finished - priority can be resolved (via software)	0x0
3	PAGE_RX_STICKY	Sticky	Status indicating whether a new page has been received. 0: No new page received 1: New page received Bit is cleared by writing a 1 to this position.	0x0
0	ANEG_COMPLETE	R/O	Auto Negotiation Complete 0: No Auto Negotiation has been completed 1: Indicates that an Auto Negotiation has completed successfully	0x0

2.13.1.10 PCS1G ANEG Status 2

Short Name:PCS1G_ANEG_STATUS2

Address:0x3E10B

PCS1G Auto-negotiation status register

Table 1103 **• PCS1G ANEG Status Register**

Bit	Name	Access	Description	Default
15:0	LP_ADV_ABILITY	R/O	Advertised abilities from link partner as described in IEEE 802.3, Clause 37	0x0000

2.13.1.11 PCS1G Aneg Next Page Status

Short Name:PCS1G_ANEG_NP_STATUS

Address:0x3E10C

PCS1G Auto-negotiation next page status register

Table 1104 **• PCS1G Aneg Next Page Status**

Bit	Name	Access	Description	Default
15:0	LP_NP_RX	R/O	Next page ability register from link partner as described in IEEE 802.3, Clause 37	0x0000

2.13.1.12 PCS1G Link Status

Short Name:PCS1G_LINK_STATUS

Address:0x3E10D

PCS1G link status register

Table 1105 **• PCS1G link status**

Bit	Name	Access	Description	Default
8	SIGNAL_DETECT	R/O	Indicates whether or not the selected Signal Detect input line is asserted 0: No signal detected 1: Signal detected	0x0
4	LINK_STATUS	R/O	Indicates whether the link is up or down. A link is up when ANEG state machine is in state LINK_OK or AN_DISABLE_LINK_OK 0: Link down 1: Link up	0x0
0	SYNC_STATUS	R/O	Indicates if PCS has successfully synchronized 0: PCS is out of sync 1: PCS has synchronized	0x0

2.13.1.13 PCS1G Link Down Counter

Short Name:PCS1G_LINK_DOWN_CNT

Address:0x3E10E

PCS1G link down counter register

Table 1106 **• PCS1G Link Down Counter**

Bit	Name	Access	Description	Default
7:0	LINK_DOWN_CNT	R/W	Link Down Counter. A counter that counts the number of times a link has been down. The counter does not saturate at 255 and is only cleared when writing 0 to the register	0x00

2.13.1.14 PCS1G Sticky

Short Name:PCS1G_STICKY

Address:0x3E10F

PCS1G status register for sticky bits

Table 1107 **• PCS1G Sticky**

Bit	Name	Access	Description	Default
4	LINK_DOWN_STICKY	Sticky	The sticky bit is set when the link has been down - i.e. if the ANEG state machine has not been in the AN_DISABLE_LINK_OK or LINK_OK state for one or more clock cycles. This occurs if e.g. ANEG is restarted or for example if signal-detect or synchronization has been lost for more than 10 ms (1.6 ms in SGMII mode). By setting the UDLT bit, the required down time can be reduced to 9,77 us (1.56 us) 0: Link is up 1: Link has been down Bit is cleared by writing a 1 to this position.	0x0
0	OUT_OF_SYNC_STICKY	Sticky	Sticky bit indicating if PCS synchronization has been lost 0: Synchronization has not been lost at any time 1: Synchronization has been lost for one or more clock cycles Bit is cleared by writing a 1 to this position.	0x0

2.13.1.15 PCS1G Low Power Idle Configuration

Short Name:PCS1G_LPI_CFG

Address:0x3E111

Configuration register for Low Power Idle (Energy Efficient Ethernet)

Table 1108 **• PCS1G Low Power Idle Configuration**

Bit	Name	Access	Description	Default
5:4	LPI_RX_WTIM	R/W	Max wake-up time before link_fail 00: 10 us 01: 13 us 10: 17 us 11: 20 us	0x3
0	TX_ASSERT_LPIDLE	R/W	Assert Low-Power Idle (LPI) in transmit mode 0: Disable LPI transmission 1: Enable LPI transmission	0x0

2.13.1.16 PCS1G Low Power Idle Configuration 2

Short Name:PCS1G_LPI_CFG2

Address:0x3E112

Configuration register for Low Power Idle (Energy Efficient Ethernet)

Table 1109 **• PCS1G Low Power Idle Configuration 2**

Bit	Name	Access	Description	Default
4	QSGMII_MS_SEL	R/W	QSGMII master/slave selection (only one master allowed per QSGMII). The master drives LPI timing on serdes 0: Slave 1: Master	0x1

2.13.1.17 PCS1G Wake Error Counter

Short Name:PCS1G_LPI_WAKE_ERROR_CNT

Address:0x3E113

PCS1G Low Power Idle wake error counter (Energy Efficient Ethernet)

Table 1110 **• PCS1G Wake Error Counter**

Bit	Name	Access	Description	Default
15:0	WAKE_ERROR_CNT	R/W	Wake Error Counter. A counter that is incremented when the link partner does not send wake-up burst in due time. The counter saturates at 65535 and is cleared when writing 0 to the register	0x0000

2.13.1.18 PCS1G Low Power Idle Status

Short Name:PCS1G_LPI_STATUS

Address:0x3E114

Status register for Low Power Idle (Energy Efficient Ethernet)

Table 1111 **• PCS1G Low Power Idle Status**

Bit	Name	Access	Description	Default
15	RX_LPI_FAIL	R/O	Receiver has failed to recover from Low-Power Idle mode 0: No failure 1: Failed to recover from LPI mode	0x0
12	RX_LPI_EVENT_STICKY	Sticky	Receiver Low-Power idle occurrence 0: No LPI symbols received 1: Receiver has received LPI symbols Bit is cleared by writing a 1 to this position.	0x0
9	RX_QUIET	R/O	Receiver Low-Power Quiet mode 0: Receiver not in quiet mode 1: Receiver is in quiet mode	0x0
8	RX_LPI_MODE	R/O	Receiver Low-Power Idle mode 0: Receiver not in low power idle mode 1: Receiver is in low power idle mode	0x0

Table 1111 • **PCS1G Low Power Idle Status *(continued)***

Bit	Name	Access	Description	Default
4	TX_LPI_EVENT_STICKY	Sticky	Transmitter Low-Power idle occurrence 0: No LPI symbols transmitted 1: Transmitter has transmitted LPI symbols Bit is cleared by writing a 1 to this position.	0x0
1	TX_QUIET	R/O	Transmitter Low-Power Quiet mode 0: Transmitter not in quiet mode 1: Transmitter is in quiet mode	0x0
0	TX_LPI_MODE	R/O	Transmitter Low-Power Idle mode 0: Transmitter not in low power idle mode 1: Transmitter is in low power idle mode	0x0

2.13.1.19 PCS1G Test Pattern Mode Configuration

Short Name:PCS1G_TSTPAT_MODE_CFG

Address:0x3E115

PCS1G testpattern mode configuration register (Frame based pattern 4 and 5 might be not available depending on chip type)

Table 1112 • **PCS1G Test Pattern Mode Configuration**

Bit	Name	Access	Description	Default
2:0	JTP_SEL	R/W	Jitter Test Pattern Select: Enables and selects the jitter test pattern to be transmitted. The jitter test patterns are according to the IEEE 802.3, Annex 36A 0: Disable transmission of test patterns 1: High frequency test pattern - repeated transmission of D21.5 code group 2: Low frequency test pattern - repeated transmission of K28.7 code group 3: Mixed frequency test pattern - repeated transmission of K28.5 code group 4: Long continuous random test pattern (packet length is 1524 bytes) 5: Short continuous random test pattern (packet length is 360 bytes)	0x0

2.13.1.20 PCS1G Test Pattern Status

Short Name:PCS1G_TSTPAT_STATUS

Address:0x3E116

PCS1G testpattern status register

Table 1113 • **PCS1G Test Pattern Status**

Bit	Name	Access	Description	Default
15:8	JTP_ERR_CNT	R/W	Jitter Test Pattern Error Counter. Due to re-sync measures it might happen that single errors are not counted (applies for 2.5gpbs mode). The counter saturates at 255 and is only cleared when writing 0 to the register	0x00

Table 1113 • **PCS1G Test Pattern Status *(continued)***

Bit	Name	Access	Description	Default
4	JTP_ERR	R/O	Jitter Test Pattern Error 0: Jitter pattern checker has found no error 1: Jitter pattern checker has found an error	0x0
0	JTP_LOCK	R/O	Jitter Test Pattern Lock 0: Jitter pattern checker has not locked 1: Jitter pattern checker has locked	0x0

2.13.1.21 PCS1G XGMII Configuration

Short Name:PCS1G_XGMII_CFG

Address:0x3E117

Table 1114 • **PCS1G XGMII Configuration**

Bit	Name	Access	Description	Default
8	RESERVED	R/W	Must be set to its default.	0x1
0	REGEN_PREAMBLE_ENA	R/W	Enable the PCS to regenerate the full preamble when a reduced preamble is detected on the received packet 0=Preamble is not modified 1=Preceeding IDLEs are replaced preamble bytes for the 7 bytes before a start of frame delimiter	0x1

2.14 MAC_FC_BUFFER (Device 0x3)

Table 1115 • **CONFIG**

Address	Short Description	Register Name	Details
0x3F000	Enable Flow Control Buffer Operation	FC_ENA_CFG	Page 407
0x3F001	Flow Control Mode Configuration	FC_MODE_CFG	Page 407
0x3F002	PPM Rate Adaptation Threshold Configuration	PPM_RATE_ADAPT_THRESH_CFG	Page 408
0x3F003	Tx Control Queue Configuration	TX_CTRL_QUEUE_CFG	Page 408
0x3F004	Tx Data Queue Configuration	TX_DATA_QUEUE_CFG	Page 409
0x3F005	Rx Data Queue Configuration	RX_DATA_QUEUE_CFG	Page 409
0x3F006	Tx Flow Control Buffer Pause Frame Generation Thresholds	TX_BUFF_XON_XOFF_THRESH_CFG	Page 409
0x3F007	Flow Control Buffer Read Threshold	FC_READ_THRESH_CFG	Page 410
0x3F008	Tx Frame Gap Compensation	TX_FRM_GAP_COMP	Page 410

Table 1116 • **STATUS**

Address	Short Description	Register Name	Details
0x3F009	Sticky Bits	STICKY	Page 410

Table 1116 • **STATUS** ***(continued)***

Address	Short Description	Register Name	Details
0x3F00A	Sticky Bits Interrupt Mask	STICKY_MASK	Page 411
0x3F00B	Tx Control Queue Overflow Frame Drop Counter	TX_CTRL_QUEUE_OVERFLOW_DROP_CNT	Page 412
0x3F00C	Tx Control Queue Underflow Frame Drop Counter	TX_CTRL_QUEUE_UNDERFLOW_DROP_CNT	Page 412
0x3F00D	Tx Uncorrected Control Frame Drop Counter	TX_CTRL_UNCORRECTED_FRM_DROP_CNT	Page 413
0x3F00E	Tx Data Queue Overflow Drop Counter	TX_DATA_QUEUE_OVERFLOW_DROP_CNT	Page 413
0x3F00F	Tx Data Queue Underflow Drop Counter	TX_DATA_QUEUE_UNDERFLOW_DROP_CNT	Page 413
0x3F010	Tx Uncorrected Data Frame Drop Counter	TX_DATA_UNCORRECTED_FRM_DROP_CNT	Page 413
0x3F011	Rx Overflow Frame Drop Counter	RX_OVERFLOW_DROP_CNT	Page 413
0x3F012	Rx Underflow Frame Drop Counter	RX_UNDERFLOW_DROP_CNT	Page 414
0x3F013	Rx Uncorrected Frame Drop Counter	RX_UNCORRECTED_FRM_DROP_CNT	Page 414

2.14.1 Flow Control Buffer Configuration

Flow control buffer configuration registers

2.14.1.1 Enable Flow Control Buffer Operation

Short Name:FC_ENA_CFG

Address:0x3F000

Enable flow control buffer in ingress and egress paths

Table 1117 • **Enable Flow Control Buffer Operation**

Bit	Name	Access	Description	Default
0	TX_ENA	R/W	Enable egress flow control buffer 0: Disabled 1: Enabled	0x0
4	RX_ENA	R/W	Enable ingress flow control buffer 0: Disabled 1: Enabled	0x0

2.14.1.2 Flow Control Mode Configuration

Short Name:FC_MODE_CFG

Address:0x3F001

Table 1118 • **Flow Control Mode Configuration**

Bit	Name	Access	Description	Default
8	PAUSE_REACT_ENA	R/W	Enable pause reaction and pause timer maintenance in egress flow control buffer 0: Disable pause reaction and pause timer 1: Enable pause reaction and pause timer	0x0

Table 1118 • **Flow Control Mode Configuration** ***(continued)***

Bit	Name	Access	Description	Default
12	RX_PPM_RATE_ADAPT_ENA	R/W	Enable PPM rate adaptation in ingress flow control buffer. This is achieved by asserting shrint_ipg_shot signal towards host MAC10G after the ingress flow control buffer crosses RX_PPM_RATE_ADAPT_THRES value. 0: Disable PPM rate adaptation 1: Enable PPM rate adaptation	0x0
16	TX_PPM_RATE_ADAPT_ENA	R/W	Enable PPM rate adaptation in egress flow control buffer. This is achieved by asserting shrint_ipg_shot signal towards line MAC10G after egress flow control buffer crosses RX_PPM_RATE_ADAPT_THRES value. This is applicable only to data queue. 0: Disable PPM rate adaptation 1: Enable PPM rate adaptation	0x0
20	TX_CTRL_QUEUE_ENA	R/W	Enable using of control queue in egress flow control buffer 0: Disable control queue 1: Enable control queue	0x0
24	PAUSE_GEN_ENA	R/W	Enable XON and XOFF pause frames based on XON and XOFF thresholds 0: Disable XON/XOFF generation 1: Enable XON/XOFF generation	0x0
28	INCLUDE_PAUSE_RCVD_IN_PAUSE_GEN	R/W	Enable use of pause received signals from line MAC in XON/XOFF generation 0: Disable pause received in XON/XOFF generation 1: Enable pause received in XON/XOFF generation	0x0

2.14.1.3 PPM Rate Adaptation Threshold Configuration

Short Name:PPM_RATE_ADAPT_THRESH_CFG

Address:0x3F002

Table 1119 • **PPM Rate Adaptation Threshold Configuration**

Bit	Name	Access	Description	Default
15:0	TX_PPM_RATE_ADAPT_THRESH	R/W	Threshold of data queue in egress flow control buffer after which IPG will be shrunk by 8 bytes to compensate read and write clocks PPM differences. The recommended value is 2+TX_READ_THRESH.	0x0000
31:20	RX_PPM_RATE_ADAPT_THRESH	R/W	Threshold of data queue in ingress flow control buffer after which IPG shrink is asserted to host MAC10G. The recommended value is 2+RX_READ_THRESH.	0x000

2.14.1.4 Tx Control Queue Configuration

Short Name:TX_CTRL_QUEUE_CFG

Address:0x3F003

***Table 1120* • Tx Control Queue Configuration**

Bit	Name	Access	Description	Default
15:0	TX_CTRL_QUEUE_START	R/W	Start address/location for control queue in egress flow control buffer where control frames are stored	0x0000
31:16	TX_CTRL_QUEUE_END	R/W	End address/location for control queue in egress flow control buffer where control frames are stored	0x03FF

2.14.1.5 Tx data queue configuration

Short Name:TX_DATA_QUEUE_CFG

Address:0x3F004

***Table 1121* • Tx data queue configuration**

Bit	Name	Access	Description	Default
15:0	TX_DATA_QUEUE_START	R/W	Start address/location for data queue in egress flow control buffer where data frames are stored	0x0400
31:16	TX_DATA_QUEUE_END	R/W	End address/location for data queue in egress flow control buffer where data frames are stored	0x13FF

2.14.1.6 Rx data queue configuration

Short Name:RX_DATA_QUEUE_CFG

Address:0x3F005

***Table 1122* • Rx data queue configuration**

Bit	Name	Access	Description	Default
15:0	RX_DATA_QUEUE_START	R/W	Start address/location for data queue in ingress flow control buffer where data frames are stored	0x0000
31:16	RX_DATA_QUEUE_END	R/W	End address/location for data queue in ingress flow control buffer where data frames are stored	0x027F

2.14.1.7 Tx Flow Control Buffer Pause Frame Generation Thresholds

Short Name:TX_BUFF_XON_XOFF_THRESH_CFG

Address:0x3F006

***Table 1123* • Tx Flow Control Buffer Pause Frame Generation Thresholds**

Bit	Name	Access	Description	Default
15:0	TX_XOFF_THRESH	R/W	Egress data buffer threshold for generating XOFF pause frame to host (Pause transmission from host, for example). The recommended value is 1792.	0x0700
31:16	TX_XON_THRESH	R/W	Egress data buffer threshold for generating XON pause frame to host (Transmission resumed, for example). The recommended value is 1280.	0x0500

2.14.1.8 Flow Control Buffer Read Threshold

Short Name:FC_READ_THRESH_CFG

Address:0x3F007

***Table 1124* • Flow Control Buffer Read Threshold**

Bit	Name	Access	Description	Default
15:0	TX_READ_THRESH	R/W	Egress flow control data buffer minimum threshold after which frames are read from the flow control buffer and transmitted to the line. Recommended values:- LAN mode: 5 WAN mode: 2	0x0004
31:16	RX_READ_THRESH	R/W	Ingress flow control buffer minimum threshold after which frames are read from the flow control buffer and transmitted to the host. Recommended values:- LAN mode: 4 WAN mode: 127	0x0005

2.14.1.9 Tx Frame Gap Compensation

Short Name:TX_FRM_GAP_COMP

Address:0x3F008

***Table 1125* • Tx Frame Gap Compensation**

Bit	Name	Access	Description	Default
15:0	TX_FRM_GAP_COMP	R/W	Tx frame gap compensation	0x0018

2.14.2 Flow Control Buffer Status

2.14.2.1 Sticky Bits

Short Name:STICKY

Address:0x3F009

***Table 1126* • Sticky Bits**

Bit	Name	Access	Description	Default
2	TX_UNCORRECTED_FRM_DROP_STICKY	Sticky	Indicates one or more frames in the egress flow control buffer were dropped due to ECC failure. This bit is cleared by writing a 1. 0: No frame with ECC error was detected 1: One or more frames with ECC error were detected	0x0
3	RX_UNCORRECTED_FRM_DROP_STICKY	Sticky	Indicates one or more frames in the ingress flow control buffer were dropped due to ECC failure. This bit is cleared by writing a 1. 0: No frame with ECC error was detected 1: One or more frames with ECC error were detected	0x0

Table 1126 • **Sticky Bits** ***(continued)***

Bit	Name	Access	Description	Default
16	TX_CTRL_QUEUE_OVERFLOW_DROP_STICKY	Sticky	Indicates an overflow has occurred in the control queue of an egress flow control buffer. This bit is cleared by writing a 1. 0: No overflow was detected 1: One or more overflows were detected	0x0
17	TX_CTRL_QUEUE_UNDERFLOW_DROP_STICKY	Sticky	Indicates an underflow has occurred in the control queue of an egress flow control buffer. This bit is cleared by writing a 1. 0: No underflow was detected 1: One or more underflows were detected	0x0
18	TX_DATA_QUEUE_OVERFLOW_DROP_STICKY	Sticky	Indicates an overflow has occurred in the data queue of an egress flow control buffer. This bit is cleared by writing a 1. 0: No overflow is detected 1: One or more overflow were detected	0x0
19	TX_DATA_QUEUE_UNDERFLOW_DROP_STICKY	Sticky	Indicates an underflow has occurred in the data queue of an egress flow control buffer. This bit is cleared by writing a 1. 0: No underflow is detected 1: One or more underflow were detected	0x0
20	RX_OVERFLOW_DROP_STICKY	Sticky	Indicates an overflow has occurred in the ingress flow control buffer. This bit is cleared by writing a 1. 0: No overflow is detected 1: One or more overflow were detected	0x0
21	RX_UNDERFLOW_DROP_STICKY	Sticky	Indicates an underflow has occurred in the ingress flow control buffer. This bit is cleared by writing a 1. 0: No underflow is detected 1: One or more underflow were detected	0x0

2.14.2.2 Sticky Bits Interrupt Mask

Short Name:STICKY_MASK

Address:0x3F00A

Table 1127 • **Sticky Bits Interrupt Mask**

Bit	Name	Access	Description	Default
2	TX_UNCORRECTED_FRM_DROP_STICKY_MASK	R/W	Interrupt mask for TX_UNCORRECTED_FRM_DROP_STICKY 0: Disable interrupt 1: Enable interrupt	0x0
3	RX_UNCORRECTED_FRM_DROP_STICKY_MASK	R/W	Interrupt mask for RX_UNCORRECTED_FRM_DROP_STICKY 0: Disable interrupt 1: Enable interrupt	0x0

Table 1127 • **Sticky Bits Interrupt Mask *(continued)***

Bit	Name	Access	Description	Default
16	TX_CTRL_QUEUE_OVERFLOW_DROP_STICKY_MASK	R/W	Interrupt mask for TX_CTRL_QUEUE_OVERFLOW_DROP_STICKY 0: Disable interrupt 1: Enable interrupt	0x0
17	TX_CTRL_QUEUE_UNDERFLOW_DROP_STICKY_MASK	R/W	Interrupt mask for TX_CTRL_QUEUE_UNDERFLOW_DROP_STICKY 0: Disable interrupt 1: Enable interrupt	0x0
18	TX_DATA_QUEUE_OVERFLOW_DROP_STICKY_MASK	R/W	Interrupt mask for TX_DATA_QUEUE_OVERFLOW_DROP_STICKY 0: Disable interrupt 1: Enable interrupt	0x0
19	TX_DATA_QUEUE_UNDERFLOW_DROP_STICKY_MASK	R/W	Interrupt mask for TX_DATA_QUEUE_UNDERFLOW_DROP_STICKY 0: Disable interrupt 1: Enable interrupt	0x0
20	RX_OVERFLOW_DROP_STICKY_MASK	R/W	Interrupt mask for RX_OVERFLOW_DROP_STICKY 0: Disable interrupt 1: Enable interrupt	0x0
21	RX_UNDERFLOW_DROP_STICKY_MASK	R/W	Interrupt mask for RX_UNDERFLOW_DROP_STICKY 0: Disable interrupt 1: Enable interrupt	0x0

2.14.2.3 Tx Control Queue Overflow Frame Drop Counter

Short Name:TX_CTRL_QUEUE_OVERFLOW_DROP_CNT

Address:0x3F00B

Table 1128 • **Tx Control Queue Overflow Frame Drop Counter**

Bit	Name	Access	Description	Default
31:0	TX_CTRL_QUEUE_OVERFLOW_DROP_CNT	R/W	Number of times an overflow occurred in the control queue of the egress flow control buffer. Counter can be written by software.	0x00000000

2.14.2.4 Tx Control Queue Underflow Frame Drop Counter

Short Name:TX_CTRL_QUEUE_UNDERFLOW_DROP_CNT

Address:0x3F00C

Table 1129 • **Tx Control Queue Underflow Frame Drop Counter**

Bit	Name	Access	Description	Default
31:0	TX_CTRL_QUEUE_UNDERFLOW_DROP_CNT	R/W	Number of times an underflow occurred in the control queue of the egress flow control buffer. Counter can be written by software.	0x00000000

2.14.2.5 Tx Uncorrected Control Frame Drop Counter

Short Name:TX_CTRL_UNCORRECTED_FRM_DROP_CNT

Address:0x3F00D

***Table 1130* • Tx Uncorrected Control Frame Drop Counter**

Bit	Name	Access	Description	Default
31:0	TX_CTRL_UNCORRECTED_FRM_DROP_CNT	R/W	Number of control frames aborted due to ECC check fail during reading from RAM. Counter can be written by software.	0x00000000

2.14.2.6 Tx Data Queue Overflow Drop Counter

Short Name:TX_DATA_QUEUE_OVERFLOW_DROP_CNT

Address:0x3F00E

***Table 1131* • Tx Data Queue Overflow Drop Counter**

Bit	Name	Access	Description	Default
31:0	TX_DATA_QUEUE_OVERFLOW_DROP_CNT	R/W	Number of times an overflow occurred in the data queue of the egress flow control buffer. Counter can be written by software.	0x00000000

2.14.2.7 Tx Data Queue Underflow Drop Counter

Short Name:TX_DATA_QUEUE_UNDERFLOW_DROP_CNT

Address:0x3F00F

***Table 1132* • Tx Data Queue Underflow Drop Counter**

Bit	Name	Access	Description	Default
31:0	TX_DATA_QUEUE_UNDERFLOW_DROP_CNT	R/W	Number of times an underflow occurred in the data queue of the egress flow control buffer. Counter can be written by software.	0x00000000

2.14.2.8 Tx Uncorrected Data Frame Drop Counter

Short Name:TX_DATA_UNCORRECTED_FRM_DROP_CNT

Address:0x3F010

***Table 1133* • Tx Uncorrected Data Frame Drop Counter**

Bit	Name	Access	Description	Default
31:0	TX_DATA_UNCORRECTED_FRM_DROP_CNT	R/W	Number of data frames aborted due to ECC check fail during reading from RAM. Counter can be written by software.	0x00000000

2.14.2.9 Rx Overflow Frame Drop Counter

Short Name:RX_OVERFLOW_DROP_CNT

Address:0x3F011

Table 1134 **• Rx Overflow Frame Drop Counter**

Bit	Name	Access	Description	Default
31:0	RX_OVERFLOW_DROP_CNT	R/W	Number of times an overflow occurred in the ingress flow control buffer. Counter can be written by software.	0x00000000

2.14.2.10 Rx Underflow Frame Drop Counter

Short Name:RX_UNDERFLOW_DROP_CNT

Address:0x3F012

Table 1135 **• Rx Underflow Frame Drop Counter**

Bit	Name	Access	Description	Default
31:0	RX_UNDERFLOW_DROP_CNT	R/W	Number of times an underflow occurred in the ingress flow control buffer. Counter can be written by software.	0x00000000

2.14.2.11 Rx Uncorrected Frame Drop Counter

Short Name:RX_UNCORRECTED_FRM_DROP_CNT

Address:0x3F013

Table 1136 **• Rx Uncorrected Frame Drop Counter**

Bit	Name	Access	Description	Default
31:0	RX_UNCORRECTED_FRM_DROP_CNT	R/W	Number of frames aborted due to ECC check fail during reading from RAM. Counter can be written by software.	0x00000000

2.15 HOST_MAC 10G (Device 0x3)

Full duplex (half duplex is not supported) 10/100/1000/10000 MAC registers.

Table 1137 **• CONFIG**

Address	Short Description	Register Name	Details
0x3F100	MAC Enable	MAC_ENA_CFG	Page 416
0x3F101	Mode Configuration	MAC_MODE_CFG	Page 417
0x3F102	Maximum Length Configuration	MAC_MAXLEN_CFG	Page 417
0x3F103	Tag Number Configuration	MAC_NUM_TAGS_CFG	Page 418
0x3F104 - 0x3F106	VLAN/Service Tag Configuration	MAC_TAGS_CFG	Page 418
0x3F107	Advanced Check Configuration	MAC_ADV_CHK_CFG	Page 419
0x3F108	Link Fault Signaling	MAC_LFS_CFG	Page 420
0x3F10A	Packet Interface Configuration	MAC_PKTINF_CFG	Page 421

Table 1138 • **PAUSE_CFG**

Address	Short Description	Register Name	Details
0x3F10B	Transmit Pause Frame Control	PAUSE_TX_FRAME_CONTROL	Page 422
0x3F10C	Transmit Pause Frame Control 2	PAUSE_TX_FRAME_CONTROL_2	Page 423
0x3F10D	Receive Pause Frame Control	PAUSE_RX_FRAME_CONTROL	Page 423
0x3F10E	Pause Detector State	PAUSE_STATE	Page 424
0x3F10F	MAC Address LSB	MAC_ADDRESS_LSB	Page 424
0x3F110	MAC Address MSB	MAC_ADDRESS_MSB	Page 425

Table 1139 • **STATUS**

Address	Short Description	Register Name	Details
0x3F115	Sticky Bit	MAC_STICKY	Page 425
0x3F116	MAC Sticky Bits Interrupt Mask	MAC_STICKY_MASK	Page 426

Table 1140 • **STATISTICS_32BIT**

Address	Short Description	Register Name	Details
0x3F117	RX_HIH Checksum Error Counter	RX_HIH_CKSM_ERR_CNT	Page 427
0x3F118	Rx XGMII Protocol Error Counter	RX_XGMII_PROT_ERR_CNT	Page 428
0x3F119	Rx Symbol Carrier Error Counter	RX_SYMBOL_ERR_CNT	Page 428
0x3F11A	Rx Pause Frame Counter	RX_PAUSE_CNT	Page 428
0x3F11B	Rx Control Frame Counter	RX_UNSUP_OPCODE_CNT	Page 428
0x3F11C	Rx Unicast Frame Counter	RX_UC_CNT	Page 429
0x3F11D	Rx Multicast Frame Counter	RX_MC_CNT	Page 429
0x3F11E	Rx Broadcast Frame Counter	RX_BC_CNT	Page 429
0x3F11F	Rx CRC Error Counter	RX_CRC_ERR_CNT	Page 429
0x3F120	Rx Undersize Counter (Valid Frame Format)	RX_UNDERSIZE_CNT	Page 429
0x3F121	Rx Undersize Counter (CRC Error)	RX_FRAGMENTS_CNT	Page 430
0x3F122	Rx In-range Length Error Counter	RX_IN_RANGE_LEN_ERR_CNT	Page 430
0x3F123	Rx Out-of-range Length Error Counter	RX_OUT_OF_RANGE_LEN_ERR_CNT	Page 430
0x3F124	Rx Oversize Counter (Valid Frame Format)	RX_OVERSIZE_CNT	Page 430
0x3F125	Rx Jabbers Counter	RX_JABBERS_CNT	Page 430
0x3F126	Rx 64 Byte Frame Counter	RX_SIZE64_CNT	Page 431
0x3F127	Rx 65-127 Byte Frame Counter	RX_SIZE65TO127_CNT	Page 431
0x3F128	Rx 128-255 Byte Frame Counter	RX_SIZE128TO255_CNT	Page 431
0x3F129	Rx 256-511 Byte Frame Counter	RX_SIZE256TO511_CNT	Page 431
0x3F12A	Rx 512-1023 Byte Frame Counter	RX_SIZE512TO1023_CNT	Page 431

Table 1140 • **STATISTICS_32BIT** *(continued)*

Address	Short Description	Register Name	Details
0x3F12B	Rx 1024-1518 Byte Frame Counter	RX_SIZE1024TO1518_CNT	Page 432
0x3F12C	Rx 1519 to Max Length Byte Frame Counter	RX_SIZE1519TOMAX_CNT	Page 432
0x3F12D	Rx Inter Packet Gap Shrink Counter	RX_IPG_SHRINK_CNT	Page 432
0x3F12E	Tx Pause Frame Counter	TX_PAUSE_CNT	Page 432
0x3F12F	Tx Unicast Frame Counter	TX_UC_CNT	Page 433
0x3F130	Tx Multicast Frame Counter	TX_MC_CNT	Page 433
0x3F131	Tx Broadcast Frame Counter	TX_BC_CNT	Page 433
0x3F132	Tx 64 Byte Frame Counter	TX_SIZE64_CNT	Page 433
0x3F133	Tx 65-127 Byte Frame Counter	TX_SIZE65TO127_CNT	Page 433
0x3F134	Tx 128-255 Byte Frame Counter	TX_SIZE128TO255_CNT	Page 434
0x3F135	Tx 256-511 Byte Frame Counter	TX_SIZE256TO511_CNT	Page 434
0x3F136	Tx 512-1023 Byte Frame Counter	TX_SIZE512TO1023_CNT	Page 434
0x3F137	Tx 1024-1518 Byte Frame Counter	TX_SIZE1024TO1518_CNT	Page 434
0x3F138	Tx 1519 to Max Length Byte Frame Counter	TX_SIZE1519TOMAX_CNT	Page 435

Table 1141 • **STATISTICS_40BIT**

Address	Short Description	Register Name	Details
0x3F139	Rx Bad Bytes Counter (LSB)	RX_BAD_BYTES_CNT	Page 435
0x3F13A	Rx Bad Bytes Counter (MSB)	RX_BAD_BYTES_MSB_CNT	Page 435
0x3F13B	Rx OK Bytes Counter (LSB)	RX_OK_BYTES_CNT	Page 435
0x3F13C	Rx OK Bytes Counter (MSB)	RX_OK_BYTES_MSB_CNT	Page 436
0x3F13D	Rx Bytes Received Counter (LSB)	RX_IN_BYTES_CNT	Page 436
0x3F13E	Rx Bytes Received Counter (MSB)	RX_IN_BYTES_MSB_CNT	Page 436
0x3F13F	Tx OK Bytes Counter (LSB)	TX_OK_BYTES_CNT	Page 436
0x3F140	Tx OK Bytes Counter (MSB)	TX_OK_BYTES_MSB_CNT	Page 437
0x3F141	Tx Bytes Transmitted Counter (LSB)	TX_OUT_BYTES_CNT	Page 437
0x3F142	Tx Bytes Transmitted Counter (MSB)	TX_OUT_BYTES_MSB_CNT	Page 437

2.15.1 10G MAC Configuration

Registers that reflect the configuration of 10G MAC

2.15.1.1 MAC Enable

Short Name:MAC_ENA_CFG

Address:0x3F100

Table 1142 • **MAC Enable**

Bit	Name	Access	Description	Default
0	RX_CLK_ENA	R/W	MAC Rx clock enable 0: All clocks for this module with the exception of CSR clock are disabled 1: All clocks for this module are enabled	0x0

Table 1142 • **MAC Enable** *(continued)*

Bit	Name	Access	Description	Default
4	TX_CLK_ENA	R/W	MAC Tx clock enable 0: All clocks for this module with the exception of CSR clock are disabled 1: All clocks for this module are enabled	0x0
8	RX_SW_RST	R/W	MAC Rx software reset 0: Block operates normally 1: All logic (other than CSR target) is held in reset, clocks are not disabled	0x1
12	TX_SW_RST	R/W	MAC Tx software reset 0: Block operates normally 1: All logic (other than CSR target) is held in reset, clocks are not disabled	0x1
16	RX_ENA	R/W	Enable receiver 0: Disabled 1: Enabled	0x0
20	TX_ENA	R/W	Enable transmitter 0: Disabled 1: Enabled	0x0

2.15.1.2 Mode Configuration

Short Name:MAC_MODE_CFG

Address:0x3F101

Table 1143 • **Mode Configuration**

Bit	Name	Access	Description	Default
29:20	RESERVED	R/W	Must be set to its default.	0x040
1	UNDERSIZED_FRAME_DROP_DIS	R/W	According to IEEE 802.3 clause 49, MAC drops frames whose length is less than 64 bytes. So to allow these frames this bit needs to be set to '1'. Note: 1) MAC statistics will still reflect these frames as undersized frames. 2) Undersized frames with valid FCS are only allowed when this bit is set to '1'. Frames with FCS error are still dropped. 0: MAC drops undersized frames 1: MAC passes through undersized frames	0x0
0	DISABLE_DIC	R/W	When this value is 0 MAC10G follows 0-3 DIC algorithm to insert IPG, averaging to 12. When this value is 1 MAC10G does not follow DIC algorithm for IPG insertion and, as a result, back pressure to host block from kernel is not issued. 0: IPG insertion in MAC10G is enabled 1: IPG insertion in MAC10G is disabled	0x0

2.15.1.3 Maximum Length Configuration

Short Name:MAC_MAXLEN_CFG

Address:0x3F102

Table 1144 **• Maximum Length Configuration**

Bit	Name	Access	Description	Default
16	MAX_LEN_TAG_CHK	R/W	Configures the maximum length check to consider the number of Q tags when assessing if a frame is too long. 0: Check max frame length against MAX_LEN 1: Add 4 bytes to MAX_LEN when checking a single tagged frame for max frame length Add 8 bytes to MAX_LEN when checking a double tagged frame for max frame length Add 12 bytes to MAX_LEN when checking a triple tagged frame for max frame length	0x0
15:0	MAX_LEN	R/W	Maximum frame length accepted by the receive module. If the length is exceeded, it is indicated in the statistics engine (LONG_FRAME). The maximum length is automatically adjusted to accommodate maximum sized frames containing a VLAN tag, given that the MAC is configured to be VLAN-aware by default. The maximum size is 10056 Bytes. This includes all encapsulations and TAGs. Does not include IFH.	0x07D0

2.15.1.4 Tag Number Configuration

Short Name:MAC_NUM_TAGS_CFG

Address:0x3F103

Table 1145 **• Tag Number Configuration**

Bit	Name	Access	Description	Default
1:0	NUM_TAGS	R/W	Number of consecutive VLAN tags supported by the MAC. The maximum value is 3 0: No tags are detected by MAC n: Maximum of n consecutive VLAN Tags are detected by the MAC and accordingly MAX LEN is modified for frame length calculations	0x0

2.15.1.5 VLAN Service Tag Configuration

Short Name:MAC_TAGS_CFG

Addresses:0x3F104 - 0x3F106

The MAC can be configured to accept 0, 1, 2, and 3 tags and the TAG value can be user-defined.

Table 1146 **• VLAN Service Tag Configuration**

Bit	Name	Access	Description	Default
31:16	TAG_ID	R/W	Value (other than 0x8100 or 0x88A8) that is regarded as a VLAN/Service tag. This value is used for all all tag positions. A double tagged frame can have the following INNER_TAG and OUTER_TAG values: 0x8100 and 0x8100 0x8100 and TAG_ID TAG_ID and TAG_ID 0x8100: Standard Ethernet bridge Ethertype (C-tag) 0x88A8: Provider Bridge Ethertype (S-tag)	0x88A8
4	TAG_ENA	R/W	Enables TAG_ID other than 0x8100 and 0x88A8 for tag comparison. 0: The MAC does not take TAG_ID for tag identification 1: The MAC looks for tag according to encoding of TAG_ID	0x0

2.15.1.6 Advanced Check Configuration

Short Name:MAC_ADV_CHK_CFG

Address:0x3F107

Table 1147 **• Advanced Check Configuration**

Bit	Name	Access	Description	Default
24	EXT_EOP_CHK_ENA	R/W	Extended end of packet check. Specifies the requirement for the Rx column when holding an EOP character. 0: Ignore the values of the remaining Rx lanes of a column holding an EOP. For example, if lane 1 holds an EOP, the value of lanes 2 and 3 are ignored. 1: A received frame is error-marked if an Error character is received in any lane of the column holding the EOP character. For example, if lane 1 holds an EOP, the frame is error-marked if lanes 0, 2, or 3 hold an Error character.	0x0
20	EXT_SOP_CHK_ENA	R/W	Enable extended start of packet check. Specifies the requirement for the Rx column prior to the start of packet character. 0: Ignore the value of Rx column at the XGMII interface before a start of packet character. 1: An IDLE column at the XGMII interface must be received before a start of packet character for the MAC to detect a start of frame.	0x0

Table 1147 • **Advanced Check Configuration** ***(continued)***

Bit	Name	Access	Description	Default
16	SFD_CHK_ENA	R/W	Enable start of frame delimiter check. Specifies the requirements for a successful frame reception. 0: Skip SFD check MAC10G assumes that preamble is 8 bytes (including SOP & SFD) when SOP is received. No checking of SFD is carried out. 1: Enforce strict SFD check The SFD must be D5 for a successful frame reception. MAC10G searches for SFD in lane 3/7 after reception of SOP, before accepting frame data. MAC10G searches for SFD until SFD is found or a control character is encountered.	0x1
12	RESERVED	R/W	Must be set to its default.	0x1
8	PRM_CHK_ENA	R/W	Enable preamble check. Specifies the preamble requirements for a successful frame reception. 0: Skip preamble check. A SOP control character is sufficient for a successful frame reception. The minimum allowed preamble size is still 8 bytes (including SOP and SFD) but the preamble bytes between the SOP and the SFD can have any data value. 1: Enable strict preamble check The last 6 bytes of a preamble prior to the SFD must all be equal to 0x55 for a successful frame reception. For preambles larger than 8 bytes, only the last 6 preamble bytes prior to the SFD are checked when this bit is set to 1.	0x0
4	OOR_ERR_ENA	R/W	Enable out of range error check. Determines whether a received frame should be discarded if the frame length field is out of range. 0: Ignore out of range errors 1: Discard frame if the frame length field value is out of range	0x0
0	INR_ERR_ENA	R/W	Enable in-range error check. Determines whether a received frame should be discarded if the frame length does not match the frame PDU size. 0: Do not error-mark frames with a frame length field that is inconsistent with the actual frame length. 1: Error-mark frames with inconsistent frame length fields and discard them using the Rx queue system.	0x0

2.15.1.7 Link Fault Signaling

Short Name:MAC_LFS_CFG

Address:0x3F108

***Table 1148* • Link Fault Signaling**

Bit	Name	Access	Description	Default
3	LFS_UNIDIR_ENA	R/W	Enable unidirectional mode for link fault signaling. Enables the MAC to transmit data during reception of local fault and remote fault ordered sets from the PHY. In the unidirectional mode, frames are transmitted separated by remote fault ordered sets when receiving local fault. They are transmitted separated by IDLE symbols when receiving remote fault. 0: Disable unidirectional mode link fault signaling. 1: Enable unidirectional mode link fault signaling.	0x0
1	RESERVED	R/W	Must be set to its default.	0x1
0	LFS_MODE_ENA	R/W	Enable link fault signaling mode. Configure how the transmitter reacts on received link fault indications. 0: Ignore link faults detected by the MAC receiver module. 1: React on detected link faults and transmit the appropriate sequence ordered set.	0x1

2.15.1.8 Packet Interface Configuration

Short Name:MAC_PKTINF_CFG

Address:0x3F10A

Packet interface module configuration register

***Table 1149* • Packet Interface Configuration**

Bit	Name	Access	Description	Default
0	STRIP_FCS_ENA	R/W	Enables stripping of FCS in ingress traffic. 0: FCS is not stripped. 1: FCS is stripped in ingress.	0x0
4	INSERT_FCS_ENA	R/W	Enables FCS insertion in egress traffic. 0: FCS is not added. 1: FCS is added in egress direction.	0x0
8	STRIP_PREAMBLE_ENA	R/W	Enables stripping of preamble from MAC frame in the ingress direction. 0: Preamble is unaltered. 1: Preamble is stripped in ingress direction.	0x0
12	INSERT_PREAMBLE_ENA	R/W	Enables addition of standard preamble in egress direction. 0: Standard preamble is not inserted. 1: Standard preamble is added in egress direction.	0x0
16	LPI_RELAY_ENA	R/W	Enables signaling of LPI received. 0: Disable LPI received status. 1: Enable LPI received status signaling.	0x0

Table 1149 • **Packet Interface Configuration** ***(continued)***

Bit	Name	Access	Description	Default
20	LF_RELAY_ENA	R/W	Enables signaling of local fault state. 0: Disable signaling of local fault state. 1: Enable local fault state signaling.	0x0
24	RF_RELAY_ENA	R/W	Enables signaling of remote fault state. 0: Disable signaling of remote fault state. 1: Enable remote fault state signaling.	0x0
25	ENABLE_TX_PADDING	R/W	Enables padding frames during transmission. Frames with length less than 64 are padded with zeros. 0: Disable padding. 1: Enable padding.	0x0
27	ENABLE_4BYTE_PREAMBLE	R/W	Enables insertion of 4 byte preamble if INSERT_PREAMBLE_ENA is set. Followed by 4 byte preamble is DMAC. Preamble will be 4 bytes only if per frame signal host_tx_4byte_preamble_i (at MAC10G packet interface) is also asserted along with this configuration. 0: Disable 4 byte preamble. 1: Enable insertion of 4 byte preamble.	0x0

2.15.2 10G MAC Pause Configuration

Registers that reflect the configuration and status of pause block in 10G MAC.

2.15.2.1 Transmit Pause Frame Control

Short Name:PAUSE_TX_FRAME_CONTROL

Address:0x3F10B

Table 1150 • **Transmit Pause Frame Control**

Bit	Name	Access	Description	Default
31:16	MAC_TX_PAUSE_VALUE	R/W	Pause value used when generating pause frames (except XON frames in mode 2).	0x0000
12	MAC_TX_WAIT_FOR_LPI_LOW	R/W	Enables pause-generate module to wait for 10 clocks (for idle insertion) before generating XOFF pause frame if MAC 10G is transmitting LPI idles. This bit should be set only if LPI generation is forced in Kernel 10G and a pause frame needs to be transmitted. 0: No idles are inserted before pause frame. 1: Idles are inserted before pause frame.	0x0
8	MAC_TX_USE_PAUSE_STALL_ENA	R/W	Enables generation of stall signal when inserting XOFF/XON pause frame into transmission stream or MAC Tx is in pause state. This can be used to upper blocks as clock enables so that their pipeline is paused. 0: Disable stall generation. 1: Enable stall generation.	0x0

Table 1150 • **Transmit Pause Frame Control** ***(continued)***

Bit	Name	Access	Description	Default
1:0	MAC_TX_PAUSE_MODE	R/W	Determines the mode that the pause frame generator operates in 0: Pause frame generation is disabled 1: Pause frames are generated only with the pause-value specified in the MAC_PAUSE_VALUE register 2: XON mode, pause frames with a pause value of 0 are generated when traffic is to be restarted, in addition to generating pause frames as in mode 1 3: Reserved	0x0

2.15.2.2 Transmit Pause Frame Control 2

Short Name:PAUSE_TX_FRAME_CONTROL_2

Address:0x3F10C

Table 1151 • **Transmit Pause Frame Control 2**

Bit	Name	Access	Description	Default
15:0	MAC_TX_PAUSE_INTERVAL	R/W	Pause frame interval. Each count in the pause frame interval value corresponds to one cycle of the MAC clock (PCS clock divided by 2), typically 156.25 MHz (6.4 ns period). The interval is counted from the end of one pause frame to the beginning of the next (assuming no other Tx traffic). The internal pause interval timer is cleared when an XON pause frame is sent in Tx pause mode 2. The pause interval value of 0xffff gives the same pause frame interval as the pause interval value of 0xfffe. Do not use a value of 0.	0x000A

2.15.2.3 Receive Pause Frame Control

Short Name:PAUSE_RX_FRAME_CONTROL

Address:0x3F10D

Table 1152 • **Receive Pause Frame Control**

Bit	Name	Access	Description	Default
16	MAC_RX_EARLY_PAUSE_DETECT_ENA	R/W	Enable pause frame detection at XGMII interface 0: Disable pause frame detection at XGMII interface 1: Enable pause frame detection at XGMII interface	0x0

Table 1152 • **Receive Pause Frame Control** ***(continued)***

Bit	Name	Access	Description	Default
20	MAC_RX_PRE_CRC_MODE	R/W	Configuration for XOFF indication before CRC check to meet pause reaction time. XOFF detection is done at XGMII interface depending on MAC_RX_EARLY_PAUSE_DETECT_ENA. Information of CRC check failed for the XOFF pause frame is also passed with a separate side band signal and so that the pause timer is reloaded with previous pause value. This bit is unused if XOFF detection is done after the MAC. 0: XOFF indication at XGMII is done after CRC check. 1: XOFF indication ar XGMII is done before CRC check.	0x0
12	MAC_RX_PAUSE_TIMER_ENA	R/W	Enables pause timer implementation in MAC Rx clock domain for the received pause frame. 0: Disable pause timer implementation 1: Enables pause timer implementation	0x0
8	MAC_TX_PAUSE_REACT_ENA	R/W	Enables pausing of transmission when a pause frame is received. 0: Disable pause reaction 1: Enables pause reaction	0x0
4	MAC_RX_PAUSE_FRAME_DROP_ENA	R/W	Enables dropping of pause frames in the pause frame detector. 0: Pause frames are not dropped 1: Pause frames are dropped	0x1
0	MAC_RX_PAUSE_MODE	R/W	Controls pause frame detection in receive path. 0: Pause frame detection is disabled 1: Pause frame detection is enabled	0x1

2.15.2.4 Pause Detector State

Short Name:PAUSE_STATE

Address:0x3F10E

Table 1153 • **Pause Detector State**

Bit	Name	Access	Description	Default
0	PAUSE_STATE	R/O	Pause state indicator. Interface is paused when the pause timer is a non-zero value. 0: Not paused 1: Paused	0x0

2.15.2.5 MAC Address LSB

Short Name:MAC_ADDRESS_LSB

Address:0x3F10F

***Table 1154* • MAC Address LSB**

Bit	Name	Access	Description	Default
31:0	MAC_ADDRESS_LSB	R/W	Lower 32 bits of the MAC address	0x00000000

2.15.2.6 MAC Address MSB

Short Name:MAC_ADDRESS_MSB

Address:0x3F110

***Table 1155* • MAC Address MSB**

Bit	Name	Access	Description	Default
15:0	MAC_ADDRESS_MSB	R/W	Upper 16 bits of the MAC address	0x0000

2.15.3 10G MAC Status

Registers that reflect the status of 10G MAC

2.15.3.1 Sticky Bits

Short Name:MAC_STICKY

Address:0x3F115

Clear the sticky bits by writing a 0 in the relevant bitgroups (writing a 1 sets the bit)

***Table 1156* • Sticky Bits**

Bit	Name	Access	Description	Default
9	RX_IPG_SHRINK_STICKY	Sticky	Indicates an inter packet gap shrink was detected (IPG < 12 bytes). Write 1 to clear the bit. 0: No IPG shrink was detected 1: one or more IPG shrinks were detected	0x0
8	RX_PREAM_SHRINK_STICKY	Sticky	Indicates that a preamble shrink was detected (preamble < 8 bytes). This sticky bit can only be set when the port is setup in 10 Gbps mode, where frames with, for example, a 4 bytes preamble are discarded. In addition, it requires that PRM_SHK_CHK_DIS = 0 and SFD_CHK_ENA = 1. In SGMII mode, all preamble sizes down to 3 bytes (including SFD) are accepted and do not cause this sticky bit to be set. Write 1 to clear the bit. 0: No preamble shrink was detected 1: one or more preamble shrinks were detected	0x0

Table 1156 • **Sticky Bits** ***(continued)***

Bit	Name	Access	Description	Default
7	RX_PREAM_MISMATCH_STICKY	Sticky	This bit is set if a preamble check is enabled, an SOP is received, and the following bytes do not match a 5555555555..55D5 pattern. A 12 byte preamble of 55555555.55555555.555555D5 will not cause this sticky bit to be set. This sticky bit can only be set when the port is set up in 10 Gbps mode. Write 1 to clear the bit. 0: No preamble mismatch was detected 1: one or more preamble matches were detected	0x0
6	RX_PREAM_ERR_STICKY	Sticky	This bit is set if an SOP is received and a following control character is received within the preamble. (No data is passed to the host interface of the MAC). Write 1 to clear the bit. 0: No preamble error was detected. 1: One or more preamble errors were detected.	0x0
5	RX_NON_STD_PREAM_STICKY	Sticky	Indicates that a frame was received with a non-standard preamble. Write 1 to clear the bit. 0: No MAC frame with non-standard preamble is received. 1: One or more MAC frames are received with non-standard preamble.	0x0
4	RX_MPLS_MC_STICKY	Sticky	Indicates that a frame with MPLS multicast was received. Write 1 to clear the bit. 0: No MPLS multicast frame is received. 1: One or more MPLS multicast frames are received.	0x0
3	RX_MPLS_UC_STICKY	Sticky	Indicates that a frame with MPLS unicast was received. Write 1 to clear the bit. 0: No MPLS unicast frame is received. 1: One or more MPLS unicast frames are received.	0x0
2	RX_TAG_STICKY	Sticky	Indicates that a frame was received with a VLAN tag. Write 1 to clear the bit. 0: No VLAN tagged frame is received. 1: One or more VLAN tagged frames are received.	0x0
1	TX_UFLW_STICKY	Sticky	Sticky bit indicating that the MAC transmit FIFO has dropped one or more frames because of underrun. Write 1 to clear the bit. 0: No MAC Tx FIFO underrun has occurred. 1: One or more MAC Tx FIFO underruns have occurred.	0x0
0	TX_ABORT_STICKY	Sticky	Indicates that the transmit host initiated abort was executed. Write 1 to clear the bit. 0: No Tx frames aborted. 1: Tx frames aborted.	0x0

2.15.3.2 MAC Sticky Bits Interrupt Mask

Short Name:MAC_STICKY_MASK

Address:0x3F116

***Table 1157* • MAC Sticky Bits Interrupt Mask**

Bit	Name	Access	Description	Default
9	RX_IPG_SHRINK_STICKY_MASK	R/W	Interrupt mask for RX_IPG_SHRINK_STICKY 0: Disable interrupt 1: Enable interrupt	0x0
8	RX_PREAM_SHRINK_STICKY_MASK	R/W	Interrupt mask for RX_PREAM_SHRINK_STICKY 0: Disable interrupt 1: Enable interrupt	0x0
7	RX_PREAM_MISMATCH_STICKY_MASK	R/W	Interrupt mask for RX_PREAM_MISMATCH_STICKY 0: Disable interrupt 1: Enable interrupt	0x0
6	RX_PREAM_ERR_STICKY_MASK	R/W	Interrupt mask for RX_PREAM_ERR_STICKY 0: Disable interrupt 1: Enable interrupt	0x0
5	RX_NON_STD_PREAM_STICKY_MASK	R/W	Interrupt mask for RX_NON_STD_PREAM_STICKY 0: Disable interrupt 1: Enable interrupt	0x0
4	RX_MPLS_MC_STICKY_MASK	R/W	Interrupt mask for RX_MPLS_MC_STICKY 0: Disable interrupt 1: Enable interrupt	0x0
3	RX_MPLS_UC_STICKY_MASK	R/W	Interrupt mask for RX_MPLS_UC_STICKY 0: Disable interrupt 1: Enable interrupt	0x0
2	RX_TAG_STICKY_MASK	R/W	Interrupt mask for RX_TAG_STICKY 0: Disable interrupt 1: Enable interrupt	0x0
1	TX_UFLW_STICKY_MASK	R/W	Interrupt mask for TX_UFLW_STICKY 0: Disable interrupt 1: Enable interrupt	0x0
0	TX_ABORT_STICKY_MASK	R/W	Interrupt mask for TX_ABORT_STICKY 0: Disable interrupt 1: Enable interrupt	0x0

Each MAC generates a statistics vector when receiving or transmitting a frame. This vector is used to generate the port statistics. All counters are 32 bits wide and are not reset when read. It is up to software to detect when a counter has wrapped around. When written, the counter assumes the written value.

2.15.3.3 RX_HIH Checksum Error Counter

Short Name:RX_HIH_CKSM_ERR_CNT

Address:0x3F117

If HIH CRC checking is enabled, this counter counts the number of frames discarded because of HIH CRC errors.

Table 1158 **• RX_HIH Checksum Error Counter**

Bit	Name	Access	Description	Default
31:0	RX_HIH_CKSM_ERR_CNT	R/W	Number of frames discarded due to errors in HIH checksum. Counter can be written by software.	0x00000000

2.15.3.4 Rx XGMII Protocol Error Counter

Short Name:RX_XGMII_PROT_ERR_CNT

Address:0x3F118

Table 1159 **• Rx XGMII Protocol Error Counter**

Bit	Name	Access	Description	Default
31:0	RX_XGMII_PROT_ERR_CNT	R/W	Number of XGMII protocol errors detected. Counter can be written by software.	0x00000000

2.15.3.5 Rx Symbol Carrier Error Counter

Short Name:RX_SYMBOL_ERR_CNT

Address:0x3F119

Table 1160 **• Rx Symbol Carrier Error Counter**

Bit	Name	Access	Description	Default
31:0	RX_SYMBOL_ERR_CNT	R/W	The number of frames received with one or more symbol errors. Counter can be written by software.	0x00000000

2.15.3.6 Rx Pause Frame Counter

Short Name:RX_PAUSE_CNT

Address:0x3F11A

Table 1161 **• Rx Pause Frame Counter**

Bit	Name	Access	Description	Default
31:0	RX_PAUSE_CNT	R/W	Number of pause control frames received. Counter can be written by software.	0x00000000

2.15.3.7 Rx Control Frame Counter

Short Name:RX_UNSUP_OPCODE_CNT

Address:0x3F11B

Table 1162 **• Rx control frame counter**

Bit	Name	Access	Description	Default
31:0	RX_UNSUP_OPCODE_CNT	R/W	Number of control frames with unsupported opcode received. Counter can be written by software.	0x00000000

2.15.3.8 Rx Unicast Frame Counter

Short Name:RX_UC_CNT

Address:0x3F11C

***Table 1163* • Rx Unicast Frame Counter**

Bit	Name	Access	Description	Default
31:0	RX_UC_CNT	R/W	The number of good unicast frames received. Counter can be written by software.	0x00000000

2.15.3.9 Rx Multicast Frame Counter

Short Name:RX_MC_CNT

Address:0x3F11D

***Table 1164* • Rx Multicast Frame Counter**

Bit	Name	Access	Description	Default
31:0	RX_MC_CNT	R/W	The number of good multicast frames received. Counter can be written by software.	0x00000000

2.15.3.10 Rx Broadcast Frame Counter

Short Name:RX_BC_CNT

Address:0x3F11E

***Table 1165* • Rx Broadcast Frame Counter**

Bit	Name	Access	Description	Default
31:0	RX_BC_CNT	R/W	The number of good broadcast frames received. Counter can be written by software.	0x00000000

2.15.3.11 Rx CRC Error Counter

Short Name:RX_CRC_ERR_CNT

Address:0x3F11F

***Table 1166* • Rx CRC Error Counter**

Bit	Name	Access	Description	Default
31:0	RX_CRC_ERR_CNT	R/W	The number of frames received with CRC error only. Counter can be written by software.	0x00000000

2.15.3.12 Rx Undersize Counter (Valid Frame Format)

Short Name:RX_UNDERSIZE_CNT

Address:0x3F120

***Table 1167* • Rx Undersize Counter (Valid Frame Format)**

Bit	Name	Access	Description	Default
31:0	RX_UNDERSIZE_CNT	R/W	The number of undersize but well-formed frames received. Counter can be written by software.	0x00000000

2.15.3.13 Rx Undersize Counter (CRC Error)

Short Name:RX_FRAGMENTS_CNT

Address:0x3F121

***Table 1168* • Rx Undersize Counter (CRC Error)**

Bit	Name	Access	Description	Default
31:0	RX_FRAGMENTS_CNT	R/W	The number of undersize frames with CRC error received. Counter can be written by software.	0x00000000

2.15.3.14 Rx In-Range Length Error Counter

Short Name:RX_IN_RANGE_LEN_ERR_CNT

Address:0x3F122

***Table 1169* • Rx In-Range Length Error Counter**

Bit	Name	Access	Description	Default
31:0	RX_IN_RANGE_LEN_ERR_CNT	R/W	The number of frames with legal length field that don't match length of MAC client data. Counter can be written by software.	0x00000000

2.15.3.15 Rx Out-of-Range Length Error Counter

Short Name:RX_OUT_OF_RANGE_LEN_ERR_CNT

Address:0x3F123

***Table 1170* • Rx Out-of-Range Length Error Counter**

Bit	Name	Access	Description	Default
31:0	RX_OUT_OF_RANGE_LEN_ERR_CNT	R/W	The number of frames with illegal length field (frames using type field are not counted here). Counter can be written by software.	0x00000000

2.15.3.16 Rx Oversize Counter (Valid Frame Format)

Short Name:RX_OVERSIZE_CNT

Address:0x3F124

***Table 1171* • Rx Oversize Counter (Valid Frame Format)**

Bit	Name	Access	Description	Default
31:0	RX_OVERSIZE_CNT	R/W	The number of oversize well-formed frames received. Counter can be written by software.	0x00000000

2.15.3.17 Rx Jabbers Counter

Short Name:RX_JABBERS_CNT

Address:0x3F125

Table 1172 **• Rx Jabbers Counter**

Bit	Name	Access	Description	Default
31:0	RX_JABBERS_CNT	R/W	The number of oversize frames with CRC error received. Counter can be written by software.	0x00000000

2.15.3.18 Rx 64 Byte Frame Counter

Short Name:RX_SIZE64_CNT

Address:0x3F126

Table 1173 **• Rx 64 Byte Frame Counter**

Bit	Name	Access	Description	Default
31:0	RX_SIZE64_CNT	R/W	The number of 64 bytes frames received. Counter can be written by software.	0x00000000

2.15.3.19 Rx 65-127 Byte Frame Counter

Short Name:RX_SIZE65TO127_CNT

Address:0x3F127

Table 1174 **• Rx 65-127 Byte Frame Counter**

Bit	Name	Access	Description	Default
31:0	RX_SIZE65TO127_CNT	R/W	The number of 65 to 127 bytes frames received. Counter can be written by software.	0x00000000

2.15.3.20 Rx 128-255 Byte Frame Counter

Short Name:RX_SIZE128TO255_CNT

Address:0x3F128

Table 1175 **• Rx 128-255 Byte Frame Counter**

Bit	Name	Access	Description	Default
31:0	RX_SIZE128TO255_CNT	R/W	The number of 128 to 255 bytes frames received. Counter can be written by software.	0x00000000

2.15.3.21 Rx 256-511 Byte Frame Counter

Short Name:RX_SIZE256TO511_CNT

Address:0x3F129

Table 1176 **• Rx 256-511 Byte Frame Counter**

Bit	Name	Access	Description	Default
31:0	RX_SIZE256TO511_CNT	R/W	The number of 256 to 511 bytes frames received. Counter can be written by software.	0x00000000

2.15.3.22 Rx 512-1023 Byte Frame Counter

Short Name:RX_SIZE512TO1023_CNT

Address:0x3F12A

***Table 1177* • Rx 512-1023 Byte Frame Counter**

Bit	Name	Access	Description	Default
31:0	RX_SIZE512TO1023_CNT	R/W	The number of 512 to 1023 bytes frames received. Counter can be written by software.	0x00000000

2.15.3.23 Rx 1024-1518 Byte Frame Counter

Short Name:RX_SIZE1024TO1518_CNT

Address:0x3F12B

***Table 1178* • Rx 1024-1518 Byte Frame Counter**

Bit	Name	Access	Description	Default
31:0	RX_SIZE1024TO1518_CNT	R/W	The number of 1024 to 1518 bytes frames received. Counter can be written by software.	0x00000000

2.15.3.24 Rx 1519 to Max Length Byte Frame Counter

Short Name:RX_SIZE1519TOMAX_CNT

Address:0x3F12C

***Table 1179* • Rx 1519 to Max Length Byte Frame Counter**

Bit	Name	Access	Description	Default
31:0	RX_SIZE1519TOMAX_CNT	R/W	The number of frames received that are longer than 1518 bytes but not longer than the maximum length register (maximum length register + 4 if the frame is VLAN tagged). Counter can be written by software.	0x00000000

2.15.3.25 Rx Inter Packet Gap Shrink Counter

Short Name:RX_IPG_SHRINK_CNT

Address:0x3F12D

***Table 1180* • Rx Inter Packet Gap Shrink Counter**

Bit	Name	Access	Description	Default
31:0	RX_IPG_SHRINK_CNT	R/W	Number of inter packet gap shrinks detected (IPG < 12 bytes). Counter can be written by software.	0x00000000

2.15.3.26 Tx Pause Frame Counter

Short Name:TX_PAUSE_CNT

Address:0x3F12E

Table 1181 **• Tx Pause Frame Counter**

Bit	Name	Access	Description	Default
31:0	TX_PAUSE_CNT	R/W	The number of pause control frames transmitted. Counter can be written by software.	0x00000000

2.15.3.27 Tx Unicast Frame Counter

Short Name:TX_UC_CNT

Address:0x3F12F

Table 1182 **• Tx Unicast Frame Counter**

Bit	Name	Access	Description	Default
31:0	TX_UC_CNT	R/W	The number of unicast frames transmitted. Counter can be written by software.	0x00000000

2.15.3.28 Tx Multicast Frame Counter

Short Name:TX_MC_CNT

Address:0x3F130

Table 1183 **• Tx Multicast Frame Counter**

Bit	Name	Access	Description	Default
31:0	TX_MC_CNT	R/W	The number of multicast frames transmitted. Counter can be written by software.	0x00000000

2.15.3.29 Tx Broadcast Frame Counter

Short Name:TX_BC_CNT

Address:0x3F131

Table 1184 **• Tx Broadcast Frame Counter**

Bit	Name	Access	Description	Default
31:0	TX_BC_CNT	R/W	The number of broadcast frames transmitted. Counter can be written by software.	0x00000000

2.15.3.30 Tx 64 Byte Frame Counter

Short Name:TX_SIZE64_CNT

Address:0x3F132

Table 1185 **• Tx 64 Byte Frame Counter**

Bit	Name	Access	Description	Default
31:0	TX_SIZE64_CNT	R/W	The number of 64 bytes frames transmitted. Counter can be written by software.	0x00000000

Tx 65-127 byte frame counter

Short Name:TX_SIZE65TO127_CNT

Address:0x3F133

Table 1186 **• Tx 65-127 Byte Frame Counter**

Bit	Name	Access	Description	Default
31:0	TX_SIZE65TO127_CNT	R/W	The number of 65 to 127 bytes frames transmitted. Counter can be written by software.	0x00000000

2.15.3.31 Tx 128-255 Byte Frame Counter

Short Name:TX_SIZE128TO255_CNT

Address:0x3F134

Table 1187 **• Tx 128-255 Byte Frame Counter**

Bit	Name	Access	Description	Default
31:0	TX_SIZE128TO255_CNT	R/W	The number of 128 to 255 bytes frames transmitted. Counter can be written by software.	0x00000000

2.15.3.32 Tx 256-511 Byte Frame Counter

Short Name:TX_SIZE256TO511_CNT

Address:0x3F135

Table 1188 **• Tx 256-511 Byte Frame Counter**

Bit	Name	Access	Description	Default
31:0	TX_SIZE256TO511_CNT	R/W	The number of 256 to 511 bytes frames transmitted. Counter can be written by software.	0x00000000

2.15.3.33 Tx 512-1023 Byte Frame Counter

Short Name:TX_SIZE512TO1023_CNT

Address:0x3F136

Table 1189 **• Tx 512-1023 Byte Frame Counter**

Bit	Name	Access	Description	Default
31:0	TX_SIZE512TO1023_CNT	R/W	The number of 512 to 1023 bytes frames transmitted. Counter can be written by software.	0x00000000

2.15.3.34 Tx 1024-1518 Byte Frame Counter

Short Name:TX_SIZE1024TO1518_CNT

Address:0x3F137

Table 1190 **• Tx 1024-1518 Byte Frame Counter**

Bit	Name	Access	Description	Default
31:0	TX_SIZE1024TO1518_CNT	R/W	The number of 1024 to 1518 bytes frames transmitted. Counter can be written by software.	0x00000000

2.15.3.35 Tx 1519 to Max Length Byte Frame Counter

Short Name:TX_SIZE1519TOMAX_CNT

Address:0x3F138

***Table 1191* • Tx 1519 to Max Length Byte Frame Counter**

Bit	Name	Access	Description	Default
31:0	TX_SIZE1519TOMAX_CNT	R/W	The number of frames transmitted that are longer than 1518 bytes but not longer than the maximum length register (maximum length register + 4 if the frame is VLAN tagged). Counter can be written by software.	0x00000000

Each MAC generates a statistics vector when receiving or transmitting a frame. This vector is used to generate the port statistics. All counters are 40 bits wide and are not reset when read. It is up to software to detect when a counter has wrapped around. When written, the counter assumes the written value.

2.15.3.36 Rx Bad Bytes Counter (LSB)

Short Name:RX_BAD_BYTES_CNT

Address:0x3F139

The number of received bytes in bad frames (LSBs only).

***Table 1192* • Rx Bad Bytes Counter (LSB)**

Bit	Name	Access	Description	Default
31:0	RX_BAD_BYTES_CNT	R/W	The number of received bytes in bad frames (LSBs only). Counter can be written by software.	0x00000000

2.15.3.37 Rx Bad Bytes Counter (MSB)

Short Name:RX_BAD_BYTES_MSB_CNT

Address:0x3F13A

The number of received bytes in bad frames (MSBs only).

***Table 1193* • Rx Bad Bytes Counter (MSB)**

Bit	Name	Access	Description	Default
7:0	RX_BAD_BYTES_MSB_CNT	R/W	The number of received bytes in bad frames (MSBs only). Counter can be written by software.	0x00

2.15.3.38 Rx OK Bytes Counter (LSB)

Short Name:RX_OK_BYTES_CNT

Address:0x3F13B

The number of received bytes in good frames (LSBs only).

Table 1194 **• Rx OK Bytes Counter (LSB)**

Bit	Name	Access	Description	Default
31:0	RX_OK_BYTES_CNT	R/W	The number of received bytes in good frames (LSBs only). Counter can be written by software.	0x00000000

2.15.3.39 Rx OK Bytes Counter (MSB)

Short Name:RX_OK_BYTES_MSB_CNT

Address:0x3F13C

The number of received bytes in good frames (MSBs only).

Table 1195 **• Rx OK Bytes Counter (MSB)**

Bit	Name	Access	Description	Default
7:0	RX_OK_BYTES_MSB_CNT	R/W	The number of received bytes in good frames (MSBs only). Counter can be written by software.	0x00

2.15.3.40 Rx Bytes Received Counter (LSB)

Short Name:RX_IN_BYTES_CNT

Address:0x3F13D

The number of good, bad, and framing bytes received (LSBs only).

Table 1196 **• Rx Bytes Received Counter (LSB)**

Bit	Name	Access	Description	Default
31:0	RX_IN_BYTES_CNT	R/W	The number of good, bad, and framing bytes received (LSBs only). Counter can be written by software.	0x00000000

2.15.3.41 Rx Bytes Received Counter (MSB)

Short Name:RX_IN_BYTES_MSB_CNT

Address:0x3F13E

The number of good, bad, and framing bytes received (MSBs only).

Table 1197 **• Rx Bytes Received Counter (MSB)**

Bit	Name	Access	Description	Default
7:0	RX_IN_BYTES_MSB_CNT	R/W	The number of good, bad, and framing bytes received (MSBs only). Counter can be written by software.	0x00

2.15.3.42 Tx OK Bytes Counter (LSB)

Short Name:TX_OK_BYTES_CNT

Address:0x3F13F

The number of bytes transmitted successfully (LSBs only).

Table 1198 **• Tx OK Bytes Counter (LSB)**

Bit	Name	Access	Description	Default
31:0	TX_OK_BYTES_CNT	R/W	The number of bytes transmitted successfully (LSBs only). Counter can be written by software.	0x00000000

2.15.3.43 Tx OK Bytes Counter (MSB)

Short Name:TX_OK_BYTES_MSB_CNT

Address:0x3F140

The number of bytes transmitted successfully (MSBs only).

Table 1199 **• Tx OK Bytes Counter (MSB)**

Bit	Name	Access	Description	Default
7:0	TX_OK_BYTES_MSB_CNT	R/W	The number of bytes transmitted successfully (MSBs only). Counter can be written by software.	0x00

2.15.3.44 Tx Bytes Transmitted Counter (LSB)

Short Name:TX_OUT_BYTES_CNT

Address:0x3F141

The number of good, bad, and framing bytes transmitted (LSBs only).

Table 1200 **• Tx Bytes Transmitted Counter (LSB)**

Bit	Name	Access	Description	Default
31:0	TX_OUT_BYTES_CNT	R/W	The number of good, bad, and framing bytes transmitted (LSBs only). Counter can be written by software.	0x00000000

2.15.3.45 Tx Bytes Transmitted Counter (MSB)

Short Name:TX_OUT_BYTES_MSB_CNT

Address:0x3F142

The number of good, bad, and framing bytes transmitted (MSBs only).

Table 1201 **• Tx Bytes Transmitted Counter (MSB)**

Bit	Name	Access	Description	Default
7:0	TX_OUT_BYTES_MSB_CNT	R/W	The number of good, bad, and framing bytes transmitted (MSBs only). Counter can be written by software.	0x00

2.16 LINE_MAC 10G (Device 0x3)

Full duplex (half duplex is not supported) 10/100/1000/10000 MAC registers.

Table 1202 • **CONFIG**

Address	Short Description	Register Name	Details
0x3F200	MAC Enable	MAC_ENA_CFG	Page 440
0x3F201	Mode Configuration	MAC_MODE_CFG	Page 440
0x3F202	Maximum Length Configuration	MAC_MAXLEN_CFG	Page 441
0x3F203	Tag Number Configuration	MAC_NUM_TAGS_CFG	Page 441
0x3F204 - 0x3F206	VLAN/Service Tag Configuration	MAC_TAGS_CFG	Page 442
0x3F207	Advanced Check Configuration	MAC_ADV_CHK_CFG	Page 442
0x3F208	Link Fault Signaling	MAC_LFS_CFG	Page 444
0x3F20A	Packet Interface Configuration	MAC_PKTINF_CFG	Page 444

Table 1203 • **PAUSE_CFG**

Address	Short Description	Register Name	Details
0x3F20B	Transmit Pause Frame Control	PAUSE_TX_FRAME_CONTROL	Page 445
0x3F20C	Transmit Pause Frame Control 2	PAUSE_TX_FRAME_CONTROL_2	Page 446
0x3F20D	Receive Pause Frame Control	PAUSE_RX_FRAME_CONTROL	Page 447
0x3F20E	Pause Detector State	PAUSE_STATE	Page 447
0x3F20F	MAC Address LSB	MAC_ADDRESS_LSB	Page 448
0x3F210	MAC Address MSB	MAC_ADDRESS_MSB	Page 448

Table 1204 • **STATUS**

Address	Short Description	Register Name	Details
0x3F215	Sticky Bit	MAC_STICKY	Page 448
0x3F216	MAC Sticky Bits Interrupt Mask	MAC_STICKY_MASK	Page 450

Table 1205 • **STATISTICS_32BIT**

Address	Short Description	Register Name	Details
0x3F217	RX_HIH Checksum Error Counter	RX_HIH_CKSM_ERR_CNT	Page 451
0x3F218	Rx XGMII Protocol Error Counter	RX_XGMII_PROT_ERR_CNT	Page 451
0x3F219	Rx Symbol Carrier Error Counter	RX_SYMBOL_ERR_CNT	Page 451
0x3F21A	Rx Pause Frame Counter	RX_PAUSE_CNT	Page 451
0x3F21B	Rx Control Frame Counter	RX_UNSUP_OPCODE_CNT	Page 452
0x3F21C	Rx Unicast Frame Counter	RX_UC_CNT	Page 452
0x3F21D	Rx Multicast Frame Counter	RX_MC_CNT	Page 452
0x3F21E	Rx Broadcast Frame Counter	RX_BC_CNT	Page 452

Table 1205 • **STATISTICS_32BIT** ***(continued)***

Address	Short Description	Register Name	Details
0x3F21F	Rx CRC Error Counter	RX_CRC_ERR_CNT	Page 452
0x3F220	Rx Undersize Counter (Valid Frame Format)	RX_UNDERSIZE_CNT	Page 453
0x3F221	Rx Undersize Counter (CRC Error)	RX_FRAGMENTS_CNT	Page 453
0x3F222	Rx In-Range Length Error Counter	RX_IN_RANGE_LEN_ERR_CNT	Page 453
0x3F223	Rx Out-of-Range Length Error Counter	RX_OUT_OF_RANGE_LEN_ERR_CNT	Page 453
0x3F224	Rx Oversize Counter (Valid Frame Format)	RX_OVERSIZE_CNT	Page 454
0x3F225	Rx Jabbers Counter	RX_JABBERS_CNT	Page 454
0x3F226	Rx 64 Byte Frame Counter	RX_SIZE64_CNT	Page 454
0x3F227	Rx 65-127 Byte Frame Counter	RX_SIZE65TO127_CNT	Page 454
0x3F228	Rx 128-255 Byte Frame Counter	RX_SIZE128TO255_CNT	Page 454
0x3F229	Rx 256-511 Byte Frame Counter	RX_SIZE256TO511_CNT	Page 455
0x3F22A	Rx 512-1023 Byte Frame Counter	RX_SIZE512TO1023_CNT	Page 455
0x3F22B	Rx 1024-1518 Byte Frame Counter	RX_SIZE1024TO1518_CNT	Page 455
0x3F22C	Rx 1519 to Max Length Byte Frame Counter	RX_SIZE1519TOMAX_CNT	Page 455
0x3F22D	Rx Inter Packet Gap Shrink Counter	RX_IPG_SHRINK_CNT	Page 455
0x3F22E	Tx Pause Frame Counter	TX_PAUSE_CNT	Page 456
0x3F22F	Tx Unicast Frame Counter	TX_UC_CNT	Page 456
0x3F230	Tx Multicast Frame Counter	TX_MC_CNT	Page 456
0x3F231	Tx Broadcast Frame Counter	TX_BC_CNT	Page 456
0x3F232	Tx 64 Byte Frame Counter	TX_SIZE64_CNT	Page 456
0x3F233	Tx 65-127 Byte Frame Counter	TX_SIZE65TO127_CNT	Page 457
0x3F234	Tx 128-255 Byte Frame Counter	TX_SIZE128TO255_CNT	Page 457
0x3F235	Tx 256-511 Byte Frame Counter	TX_SIZE256TO511_CNT	Page 457
0x3F236	Tx 512-1023 Byte Frame Counter	TX_SIZE512TO1023_CNT	Page 457
0x3F237	Tx 1024-1518 Byte Frame Counter	TX_SIZE1024TO1518_CNT	Page 458
0x3F238	Tx 1519 to Max Length Byte Frame Counter	TX_SIZE1519TOMAX_CNT	Page 458

Table 1206 • **STATISTICS_40BIT**

Address	Short Description	Register Name	Details
0x3F239	Rx Bad Bytes Counter (LSB)	RX_BAD_BYTES_CNT	Page 458
0x3F23A	Rx Bad Bytes Counter (MSB)	RX_BAD_BYTES_MSB_CNT	Page 458
0x3F23B	Rx OK Bytes Counter (LSB)	RX_OK_BYTES_CNT	Page 459
0x3F23C	Rx OK Bytes Counter (MSB)	RX_OK_BYTES_MSB_CNT	Page 459
0x3F23D	Rx Bytes Received Counter (LSB)	RX_IN_BYTES_CNT	Page 459
0x3F23E	Rx Bytes Received Counter (MSB)	RX_IN_BYTES_MSB_CNT	Page 459
0x3F23F	Tx OK Bytes Counter (LSB)	TX_OK_BYTES_CNT	Page 459
0x3F240	Tx OK Bytes Counter (MSB)	TX_OK_BYTES_MSB_CNT	Page 460

Table 1206 • **STATISTICS_40BIT *(continued)***

Address	Short Description	Register Name	Details
0x3F241	Tx bytes transmitted counter (LSB)	TX_OUT_BYTES_CNT	Page 460
0x3F242	Tx bytes transmitted counter (MSB)	TX_OUT_BYTES_MSB_CNT	Page 460

2.16.1 10G MAC Configuration

Registers that reflect the configuration of 10G MAC

2.16.1.1 MAC Enable

Short Name:MAC_ENA_CFG

Address:0x3F200

Table 1207 • **MAC Enable**

Bit	Name	Access	Description	Default
0	RX_CLK_ENA	R/W	MAC Rx clock enable 0: All clocks for this module with the exception of CSR clock are disabled 1: All clocks for this module are enabled	0x0
4	TX_CLK_ENA	R/W	MAC Tx clock enable 0: All clocks for this module with the exception of CSR clock are disabled 1: All clocks for this module are enabled	0x0
8	RX_SW_RST	R/W	MAC Rx software reset 0: Block operates normally 1: All logic (other than CSR target) is held in reset, clocks are not disabled	0x1
12	TX_SW_RST	R/W	MAC Tx software reset 0: Block operates normally 1: All logic (other than CSR target) is held in reset, clocks are not disabled	0x1
16	RX_ENA	R/W	Enable receiver 0: Disabled 1: Enabled	0x0
20	TX_ENA	R/W	Enable transmitter 0: Disabled 1: Enabled	0x0

2.16.1.2 Mode Configuration

Short Name:MAC_MODE_CFG

Address:0x3F201

Table 1208 • **Mode Configuration**

Bit	Name	Access	Description	Default
29:20	RESERVED	R/W	Must be set to its default.	0x040

Table 1208 • **Mode Configuration** ***(continued)***

Bit	Name	Access	Description	Default
1	UNDERSIZED_FRAME_DROP_DIS	R/W	According to IEEE 802.3 clause 49, MAC drops frames whose length is less than 64 bytes. So to allow these frames this bit needs to be set to '1'. Note: 1) MAC statistics will still reflect these frames as undersized frames. 2) Undersized frames with valid FCS are only allowed when this bit is set to '1'. Frames with FCS error are still dropped. 0: MAC drops undersized frames 1: MAC passes through undersized frames	0x0
0	DISABLE_DIC	R/W	When this value is 0 MAC10G follows 0-3 DIC algorithm to insert IPG, averaging to 12. When this value is 1 MAC10G does not follow DIC algorithm for IPG insertion and, as a result, back pressure to host block from kernel is not issued. 0: IPG insertion in MAC10G is enabled 1: IPG insertion in MAC10G is disabled	0x0

2.16.1.3 Maximum Length Configuration

Short Name:MAC_MAXLEN_CFG

Address:0x3F202

Table 1209 • **Maximum Length Configuration**

Bit	Name	Access	Description	Default
16	MAX_LEN_TAG_CHK	R/W	Configures the maximum length check to consider the number of Q tags when assessing if a frame is too long. 0: Check max frame length against MAX_LEN 1: Add 4 bytes to MAX_LEN when checking a single tagged frame for max frame length Add 8 bytes to MAX_LEN when checking a double tagged frame for max frame length Add 12 bytes to MAX_LEN when checking a triple tagged frame for max frame length	0x0
15:0	MAX_LEN	R/W	Maximum frame length accepted by the receive module. If the length is exceeded, it is indicated in the statistics engine (LONG_FRAME). The maximum length is automatically adjusted to accommodate maximum sized frames containing a VLAN tag, given that the MAC is configured to be VLAN-aware by default. The maximum size is 10056 Bytes. This includes all encapsulations and TAGs. Does not include IFH.	0x07D0

2.16.1.4 Tag Number Configuration

Short Name:MAC_NUM_TAGS_CFG

Address:0x3F203

Table 1210 **• Tag Number Configuration**

Bit	Name	Access	Description	Default
1:0	NUM_TAGS	R/W	Number of consecutive VLAN tags supported by the MAC. The maximum value is 3 0: No tags are detected by MAC n: Maximum of n consecutive VLAN Tags are detected by the MAC and accordingly MAX LEN is modified for frame length calculations	0x0

2.16.1.5 VLAN Service Tag Configuration

Short Name:MAC_TAGS_CFG

Addresses:0x3F204 - 0x3F206

The MAC can be configured to accept 0, 1, 2, and 3 tags and the TAG value can be user-defined.

Table 1211 **• VLAN Service Tag Configuration**

Bit	Name	Access	Description	Default
31:16	TAG_ID	R/W	Value (other than 0x8100 or 0x88A8) that is regarded as a VLAN/Service tag. This value is used for all all tag positions. A double tagged frame can have the following INNER_TAG and OUTER_TAG values: 0x8100 and 0x8100 0x8100 and TAG_ID TAG_ID and TAG_ID 0x8100: Standard Ethernet bridge Ethertype (C-tag) 0x88A8: Provider Bridge Ethertype (S-tag)	0x88A8
4	TAG_ENA	R/W	Enables TAG_ID other than 0x8100 and 0x88A8 for tag comparison. 0: The MAC does not take TAG_ID for tag identification 1: The MAC looks for tag according to encoding of TAG_ID	0x0

2.16.1.6 Advanced Check Configuration

Short Name:MAC_ADV_CHK_CFG

Address:0x3F207

***Table 1212* • Advanced check configuration**

Bit	Name	Access	Description	Default
24	EXT_EOP_CHK_ENA	R/W	Extended end of packet check. Specifies the requirement for the Rx column when holding an EOP character. 0: Ignore the values of the remaining Rx lanes of a column holding an EOP. For example, if lane 1 holds an EOP, the value of lanes 2 and 3 are ignored. 1: A received frame is error-marked if an Error character is received in any lane of the column holding the EOP character. For example, if lane 1 holds an EOP, the frame is error-marked if lanes 0, 2, or 3 hold an Error character.	0x0
20	EXT_SOP_CHK_ENA	R/W	Enable extended start of packet check. Specifies the requirement for the Rx column prior to the start of packet character. 0: Ignore the value of Rx column at the XGMII interface before a start of packet character. 1: An IDLE column at the XGMII interface must be received before a start of packet character for the MAC to detect a start of frame.	0x0
16	SFD_CHK_ENA	R/W	Enable start of frame delimiter check. Specifies the requirements for a successful frame reception. 0: Skip SFD check MAC10G assumes that preamble is 8 bytes (including SOP & SFD) when SOP is received. No checking of SFD is carried out. 1: Enforce strict SFD check The SFD must be D5 for a successful frame reception. MAC10G searches for SFD in lane 3/7 after reception of SOP, before accepting frame data. MAC10G searches for SFD until SFD is found or a control character is encountered.	0x1
12	RESERVED	R/W	Must be set to its default.	0x1
8	PRM_CHK_ENA	R/W	Enable preamble check. Specifies the preamble requirements for a successful frame reception. 0: Skip preamble check. A SOP control character is sufficient for a successful frame reception. The minimum allowed preamble size is still 8 bytes (including SOP and SFD) but the preamble bytes between the SOP and the SFD can have any data value. 1: Enable strict preamble check The last 6 bytes of a preamble prior to the SFD must all be equal to 0x55 for a successful frame reception. For preambles larger than 8 bytes, only the last 6 preamble bytes prior to the SFD are checked when this bit is set to 1.	0x0

Table 1212 • **Advanced check configuration** ***(continued)***

Bit	Name	Access	Description	Default
4	OOR_ERR_ENA	R/W	Enable out of range error check. Determines whether a received frame should be discarded if the frame length field is out of range. 0: Ignore out of range errors 1: Discard frame if the frame length field value is out of range	0x0
0	INR_ERR_ENA	R/W	Enable in-range error check. Determines whether a received frame should be discarded if the frame length does not match the frame PDU size. 0: Do not error-mark frames with a frame length field that is inconsistent with the actual frame length. 1: Error-mark frames with inconsistent frame length fields and discard them using the Rx queue system.	0x0

2.16.1.7 Link Fault Signaling

Short Name:MAC_LFS_CFG

Address:0x3F208

Table 1213 • **Link Fault Signaling**

Bit	Name	Access	Description	Default
3	LFS_UNIDIR_ENA	R/W	Enable unidirectional mode for link fault signaling. Enables the MAC to transmit data during reception of local fault and remote fault ordered sets from the PHY. In the unidirectional mode, frames are transmitted separated by remote fault ordered sets when receiving local fault. They are transmitted separated by IDLE symbols when receiving remote fault. 0: Disable unidirectional mode link fault signaling. 1: Enable unidirectional mode link fault signaling.	0x0
1	RESERVED	R/W	Must be set to its default.	0x1
0	LFS_MODE_ENA	R/W	Enable link fault signaling mode. Configure how the transmitter reacts on received link fault indications. 0: Ignore link faults detected by the MAC receiver module. 1: React on detected link faults and transmit the appropriate sequence ordered set.	0x1

2.16.1.8 Packet Interface Configuration

Short Name:MAC_PKTINF_CFG

Address:0x3F20A

Packet interface module configuration register

Table 1214 **• Packet Interface Configuration**

Bit	Name	Access	Description	Default
0	STRIP_FCS_ENA	R/W	Enables stripping of FCS in ingress traffic. 0: FCS is not stripped. 1: FCS is stripped in ingress.	0x0
4	INSERT_FCS_ENA	R/W	Enables FCS insertion in egress traffic. 0: FCS is not added. 1: FCS is added in egress direction.	0x0
8	STRIP_PREAMBLE_ENA	R/W	Enables stripping of preamble from MAC frame in the ingress direction. 0: Preamble is unaltered. 1: Preamble is stripped in ingress direction.	0x0
12	INSERT_PREAMBLE_ENA	R/W	Enables addition of standard preamble in egress direction. 0: Standard preamble is not inserted. 1: Standard preamble is added in egress direction.	0x0
16	LPI_RELAY_ENA	R/W	Enables signaling of LPI received. 0: Disable LPI received status. 1: Enable LPI received status signaling.	0x0
20	LF_RELAY_ENA	R/W	Enables signaling of local fault state. 0: Disable signaling of local fault state. 1: Enable local fault state signaling.	0x0
24	RF_RELAY_ENA	R/W	Enables signaling of remote fault state. 0: Disable signaling of remote fault state. 1: Enable remote fault state signaling.	0x0
25	ENABLE_TX_PADDING	R/W	Enables padding frames during transmission. Frames with length less than 64 are padded with zeros. 0: Disable padding. 1: Enable padding.	0x0
27	ENABLE_4BYTE_PREAMBLE	R/W	Enables insertion of 4 byte preamble if INSERT_PREAMBLE_ENA is set. Followed by 4 byte preamble is DMAC. Preamble will be 4 bytes only if per frame signal host_tx_4byte_preamble_i (at MAC10G packet interface) is also asserted along with this configuration. 0: Disable 4 byte preamble. 1: Enable insertion of 4 byte preamble.	0x0

2.16.2 10G MAC Pause Configuration

Registers that reflect the configuration and status of pause block in 10G MAC.

2.16.2.1 Transmit Pause Frame Control

Short Name:PAUSE_TX_FRAME_CONTROL

Address:0x3F20B

***Table 1215* • Transmit Pause Frame Control**

Bit	Name	Access	Description	Default
31:16	MAC_TX_PAUSE_VALUE	R/W	Pause value used when generating pause frames (except XON frames in mode 2).	0x0000
12	MAC_TX_WAIT_FOR_LPI_LOW	R/W	Enables pause-generate module to wait for 10 clocks (for idle insertion) before generating XOFF pause frame if MAC 10G is transmitting LPI idles. This bit should be set only if LPI generation is forced in Kernel 10G and a pause frame needs to be transmitted. 0: No idles are inserted before pause frame. 1: Idles are inserted before pause frame.	0x0
8	MAC_TX_USE_PAUSE_STALL_ENA	R/W	Enables generation of stall signal when inserting XOFF/XON pause frame into transmission stream or MAC Tx is in pause state. This can be used to upper blocks as clock enables so that their pipeline is paused. 0: Disable stall generation. 1: Enable stall generation.	0x0
1:0	MAC_TX_PAUSE_MODE	R/W	Determines the mode that the pause frame generator operates in 0: Pause frame generation is disabled 1: Pause frames are generated only with the pause-value specified in the MAC_PAUSE_VALUE register 2: XON mode, pause frames with a pause value of 0 are generated when traffic is to be restarted, in addition to generating pause frames as in mode 1 3: Reserved	0x0

2.16.2.2 Transmit Pause Frame Control Part 2

Short Name:PAUSE_TX_FRAME_CONTROL_2

Address:0x3F20C

***Table 1216* • Transmit Pause Frame Control Part 2**

Bit	Name	Access	Description	Default
15:0	MAC_TX_PAUSE_INTERVAL	R/W	Pause frame interval. Each count in the pause frame interval value corresponds to one cycle of the MAC clock (PCS clock divided by 2), typically 156.25 MHz (6.4 ns period). The interval is counted from the end of one pause frame to the beginning of the next (assuming no other Tx traffic). The internal pause interval timer is cleared when an XON pause frame is sent in Tx pause mode 2. The pause interval value of 0xffff gives the same pause frame interval as the pause interval value of 0xfffe. Do not use a value of 0.	0x000A

2.16.2.3 Receive Pause Frame Control

Short Name:PAUSE_RX_FRAME_CONTROL

Address:0x3F20D

***Table 1217* • Receive Pause Frame Control**

Bit	Name	Access	Description	Default
16	MAC_RX_EARLY_PAUSE_DETECT_ENA	R/W	Enable pause frame detection at XGMII interface 0: Disable pause frame detection at XGMII interface 1: Enable pause frame detection at XGMII interface	0x0
20	MAC_RX_PRE_CRC_MODE	R/W	Configuration for XOFF indication before CRC check to meet pause reaction time. XOFF detection is done at XGMII interface depending on MAC_RX_EARLY_PAUSE_DETECT_ENA. Information of CRC check failed for the XOFF pause frame is also passed with a separate side band signal and so that the pause timer is reloaded with previous pause value. This bit is unused if XOFF detection is done after the MAC. 0: XOFF indication at XGMII is done after CRC check. 1: XOFF indication ar XGMII is done before CRC check.	0x0
12	MAC_RX_PAUSE_TIMER_ENA	R/W	Enables pause timer implementation in MAC Rx clock domain for the received pause frame. 0: Disable pause timer implementation 1: Enables pause timer implementation	0x0
8	MAC_TX_PAUSE_REACT_ENA	R/W	Enables pausing of transmission when a pause frame is received. 0: Disable pause reaction 1: Enables pause reaction	0x0
4	MAC_RX_PAUSE_FRAME_DROP_ENA	R/W	Enables dropping of pause frames in the pause frame detector. 0: Pause frames are not dropped 1: Pause frames are dropped	0x1
0	MAC_RX_PAUSE_MODE	R/W	Controls pause frame detection in receive path. 0: Pause frame detection is disabled 1: Pause frame detection is enabled	0x1

2.16.2.4 Pause Detector State

Short Name:PAUSE_STATE

Address:0x3F20E

***Table 1218* • Pause Detector State**

Bit	Name	Access	Description	Default
0	PAUSE_STATE	R/O	Pause state indicator. Interface is paused when the pause timer is a non-zero value. 0: Not paused 1: Paused	0x0

2.16.2.5 MAC Address LSB

Short Name:MAC_ADDRESS_LSB

Address:0x3F20F

***Table 1219* • MAC Address LSB**

Bit	Name	Access	Description	Default
31:0	MAC_ADDRESS_LSB	R/W	Lower 32 bits of the MAC address	0x00000000

2.16.2.6 MAC Address MSB

Short Name:MAC_ADDRESS_MSB

Address:0x3F210

***Table 1220* • MAC Address MSB**

Bit	Name	Access	Description	Default
15:0	MAC_ADDRESS_MSB	R/W	Upper 16 bits of the MAC address	0x0000

2.16.3 10G MAC Status

Registers that reflect the status of 10G MAC

2.16.3.1 Sticky Bit

Short Name:MAC_STICKY

Address:0x3F215

Clear the sticky bits by writing a 0 in the relevant bitgroups (writing a 1 sets the bit)

***Table 1221* • Sticky Bit**

Bit	Name	Access	Description	Default
9	RX_IPG_SHRINK_STICKY	Sticky	Indicates an inter packet gap shrink was detected (IPG < 12 bytes). Write 1 to clear the bit. 0: No IPG shrink was detected 1: one or more IPG shrinks were detected	0x0

Table 1221 • **Sticky Bit** ***(continued)***

Bit	Name	Access	Description	Default
8	RX_PREAM_SHRINK_STICKY	Sticky	Indicates that a preamble shrink was detected (preamble < 8 bytes). This sticky bit can only be set when the port is setup in 10 Gbps mode, where frames with, for example, a 4 bytes preamble are discarded. In addition, it requires that PRM_SHK_CHK_DIS = 0 and SFD_CHK_ENA = 1. In SGMII mode, all preamble sizes down to 3 bytes (including SFD) are accepted and do not cause this sticky bit to be set. Write 1 to clear the bit. 0: No preamble shrink was detected 1: one or more preamble shrinks were detected	0x0
7	RX_PREAM_MISMATCH_STICKY	Sticky	This bit is set if a preamble check is enabled, an SOP is received, and the following bytes do not match a 5555555555..55D5 pattern. A 12 byte preamble of 55555555.55555555.555555D5 will not cause this sticky bit to be set. This sticky bit can only be set when the port is set up in 10 Gbps mode. Write 1 to clear the bit. 0: No preamble mismatch was detected 1: one or more preamble matches were detected	0x0
6	RX_PREAM_ERR_STICKY	Sticky	This bit is set if an SOP is received and a following control character is received within the preamble. (No data is passed to the host interface of the MAC). Write 1 to clear the bit. 0: No preamble error was detected. 1: One or more preamble errors were detected.	0x0
5	RX_NON_STD_PREAM_STICKY	Sticky	Indicates that a frame was received with a non-standard preamble. Write 1 to clear the bit. 0: No MAC frame with non-standard preamble is received. 1: One or more MAC frames are received with non-standard preamble.	0x0
4	RX_MPLS_MC_STICKY	Sticky	Indicates that a frame with MPLS multicast was received. Write 1 to clear the bit. 0: No MPLS multicast frame is received. 1: One or more MPLS multicast frames are received.	0x0
3	RX_MPLS_UC_STICKY	Sticky	Indicates that a frame with MPLS unicast was received. Write 1 to clear the bit. 0: No MPLS unicast frame is received. 1: One or more MPLS unicast frames are received.	0x0
2	RX_TAG_STICKY	Sticky	Indicates that a frame was received with a VLAN tag. Write 1 to clear the bit. 0: No VLAN tagged frame is received. 1: One or more VLAN tagged frames are received.	0x0

Table 1221 • **Sticky Bit** ***(continued)***

Bit	Name	Access	Description	Default
1	TX_UFLW_STICKY	Sticky	Sticky bit indicating that the MAC transmit FIFO has dropped one or more frames because of underrun. Write 1 to clear the bit. 0: No MAC Tx FIFO underrun has occurred. 1: One or more MAC Tx FIFO underruns have occurred.	0x0
0	TX_ABORT_STICKY	Sticky	Indicates that the transmit host initiated abort was executed. Write 1 to clear the bit. 0: No Tx frames aborted. 1: Tx frames aborted.	0x0

2.16.3.2 MAC Sticky Bits Interrupt Mask

Short Name:MAC_STICKY_MASK

Address:0x3F216

Table 1222 • **MAC Sticky Bits Interrupt Mask**

Bit	Name	Access	Description	Default
9	RX_IPG_SHRINK_STICKY_MASK	R/W	Interrupt mask for RX_IPG_SHRINK_STICKY 0: Disable interrupt 1: Enable interrupt	0x0
8	RX_PREAM_SHRINK_STICKY_MASK	R/W	Interrupt mask for RX_PREAM_SHRINK_STICKY 0: Disable interrupt 1: Enable interrupt	0x0
7	RX_PREAM_MISMATCH_STICKY_MASK	R/W	Interrupt mask for RX_PREAM_MISMATCH_STICKY 0: Disable interrupt 1: Enable interrupt	0x0
6	RX_PREAM_ERR_STICKY_MASK	R/W	Interrupt mask for RX_PREAM_ERR_STICKY 0: Disable interrupt 1: Enable interrupt	0x0
5	RX_NON_STD_PREAM_STICKY_MASK	R/W	Interrupt mask for RX_NON_STD_PREAM_STICKY 0: Disable interrupt 1: Enable interrupt	0x0
4	RX_MPLS_MC_STICKY_MASK	R/W	Interrupt mask for RX_MPLS_MC_STICKY 0: Disable interrupt 1: Enable interrupt	0x0
3	RX_MPLS_UC_STICKY_MASK	R/W	Interrupt mask for RX_MPLS_UC_STICKY 0: Disable interrupt 1: Enable interrupt	0x0
2	RX_TAG_STICKY_MASK	R/W	Interrupt mask for RX_TAG_STICKY 0: Disable interrupt 1: Enable interrupt	0x0
1	TX_UFLW_STICKY_MASK	R/W	Interrupt mask for TX_UFLW_STICKY 0: Disable interrupt 1: Enable interrupt	0x0

Table 1222 • **MAC Sticky Bits Interrupt Mask** ***(continued)***

Bit	Name	Access	Description	Default
0	TX_ABORT_STICKY_MASK	R/W	Interrupt mask for TX_ABORT_STICKY 0: Disable interrupt 1: Enable interrupt	0x0

Each MAC generates a statistics vector when receiving or transmitting a frame. This vector is used to generate the port statistics. All counters are 32 bits wide and are not reset when read. It is up to software to detect when a counter has wrapped around. When written, the counter assumes the written value.

2.16.3.3 RX_HIH Checksum Error Counter

Short Name:RX_HIH_CKSM_ERR_CNT

Address:0x3F217

If HIH CRC checking is enabled, this counter counts the number of frames discarded because of HIH CRC errors.

Table 1223 • **RX_HIH Checksum Error Counter**

Bit	Name	Access	Description	Default
31:0	RX_HIH_CKSM_ERR_CNT	R/W	Number of frames discarded due to errors in HIH checksum. Counter can be written by software.	0x00000000

2.16.3.4 Rx XGMII Protocol Error Counter

Short Name:RX_XGMII_PROT_ERR_CNT

Address:0x3F218

Table 1224 • **Rx XGMII Protocol Error Counter**

Bit	Name	Access	Description	Default
31:0	RX_XGMII_PROT_ERR_CNT	R/W	Number of XGMII protocol errors detected. Counter can be written by software.	0x00000000

2.16.3.5 Rx Symbol Carrier Error Counter

Short Name:RX_SYMBOL_ERR_CNT

Address:0x3F219

Table 1225 • **Rx Symbol Carrier Error Counter**

Bit	Name	Access	Description	Default
31:0	RX_SYMBOL_ERR_CNT	R/W	The number of frames received with one or more symbol errors. Counter can be written by software.	0x00000000

2.16.3.6 Rx Pause Frame Counter

Short Name:RX_PAUSE_CNT

Address:0x3F21A

***Table 1226* • Rx Pause Frame Counter**

Bit	Name	Access	Description	Default
31:0	RX_PAUSE_CNT	R/W	Number of pause control frames received. Counter can be written by software.	0x00000000

2.16.3.7 Rx Control Frame Counter

Short Name:RX_UNSUP_OPCODE_CNT

Address:0x3F21B

***Table 1227* • Rx Control Frame Counter**

Bit	Name	Access	Description	Default
31:0	RX_UNSUP_OPCODE_CNT	R/W	Number of control frames with unsupported opcode received. Counter can be written by software.	0x00000000

2.16.3.8 Rx Unicast Frame Counter

Short Name:RX_UC_CNT

Address:0x3F21C

***Table 1228* • Rx Unicast Frame Counter**

Bit	Name	Access	Description	Default
31:0	RX_UC_CNT	R/W	The number of good unicast frames received. Counter can be written by software.	0x00000000

2.16.3.9 Rx Multicast Frame Counter

Short Name:RX_MC_CNT

Address:0x3F21D

***Table 1229* • Rx Multicast Frame Counter**

Bit	Name	Access	Description	Default
31:0	RX_MC_CNT	R/W	The number of good multicast frames received. Counter can be written by software.	0x00000000

2.16.3.10 Rx Broadcast Frame Counter

Short Name:RX_BC_CNT

Address:0x3F21E

***Table 1230* • Rx Broadcast Frame Counter**

Bit	Name	Access	Description	Default
31:0	RX_BC_CNT	R/W	The number of good broadcast frames received. Counter can be written by software.	0x00000000

2.16.3.11 Rx CRC Error Counter

Short Name:RX_CRC_ERR_CNT

Address:0x3F21F

***Table 1231* • Rx CRC Error Counter**

Bit	Name	Access	Description	Default
31:0	RX_CRC_ERR_CNT	R/W	The number of frames received with CRC error only. Counter can be written by software.	0x00000000

2.16.3.12 Rx Undersize Counter (Valid Frame Format)

Short Name:RX_UNDERSIZE_CNT

Address:0x3F220

***Table 1232* • Rx Undersize Counter (Valid Frame Format)**

Bit	Name	Access	Description	Default
31:0	RX_UNDERSIZE_CNT	R/W	The number of undersize but well-formed frames received. Counter can be written by software.	0x00000000

2.16.3.13 Rx Undersize Counter (CRC Error)

Short Name:RX_FRAGMENTS_CNT

Address:0x3F221

***Table 1233* • Rx Undersize Counter (CRC Error)**

Bit	Name	Access	Description	Default
31:0	RX_FRAGMENTS_CNT	R/W	The number of undersize frames with CRC error received. Counter can be written by software.	0x00000000

2.16.3.14 Rx In-Range Length Error Counter

Short Name:RX_IN_RANGE_LEN_ERR_CNT

Address:0x3F222

***Table 1234* • Rx In-Range Length Error Counter**

Bit	Name	Access	Description	Default
31:0	RX_IN_RANGE_LEN_ERR_CNT	R/W	The number of frames with legal length field that don't match length of MAC client data. Counter can be written by software.	0x00000000

2.16.3.15 Rx Out-of-Range Length Error Counter

Short Name:RX_OUT_OF_RANGE_LEN_ERR_CNT

Address:0x3F223

***Table 1235* • Rx Out-of-Range Length Error Counter**

Bit	Name	Access	Description	Default
31:0	RX_OUT_OF_RANGE_LEN_ERR_CNT	R/W	The number of frames with illegal length field (frames using type field are not counted here). Counter can be written by software.	0x00000000

2.16.3.16 Rx Oversize Counter (Valid Frame Format)

Short Name:RX_OVERSIZE_CNT

Address:0x3F224

***Table 1236* • Rx Oversize Counter (Valid Frame Format)**

Bit	Name	Access	Description	Default
31:0	RX_OVERSIZE_CNT	R/W	The number of oversize well-formed frames received. Counter can be written by software.	0x00000000

2.16.3.17 Rx Jabbers Counter

Short Name:RX_JABBERS_CNT

Address:0x3F225

***Table 1237* • Rx Jabbers Counter**

Bit	Name	Access	Description	Default
31:0	RX_JABBERS_CNT	R/W	The number of oversize frames with CRC error received. Counter can be written by software.	0x00000000

2.16.3.18 Rx 64 Byte Frame Counter

Short Name:RX_SIZE64_CNT

Address:0x3F226

***Table 1238* • Rx 64 Byte Frame Counter**

Bit	Name	Access	Description	Default
31:0	RX_SIZE64_CNT	R/W	The number of 64 bytes frames received. Counter can be written by software.	0x00000000

2.16.3.19 Rx 65-127 Byte Frame Counter

Short Name:RX_SIZE65TO127_CNT

Address:0x3F227

***Table 1239* • Rx 65-127 Byte Frame Counter**

Bit	Name	Access	Description	Default
31:0	RX_SIZE65TO127_CNT	R/W	The number of 65 to 127 bytes frames received. Counter can be written by software.	0x00000000

2.16.3.20 Rx 128-255 Byte Frame Counter

Short Name:RX_SIZE128TO255_CNT

Address:0x3F228

***Table 1240* • Rx 128-255 Byte Frame Counter**

Bit	Name	Access	Description	Default
31:0	RX_SIZE128TO255_CNT	R/W	The number of 128 to 255 bytes frames received. Counter can be written by software.	0x00000000

2.16.3.21 Rx 256-511 Byte Frame Counter

Short Name:RX_SIZE256TO511_CNT

Address:0x3F229

***Table 1241* • Rx 256-511 Byte Frame Counter**

Bit	Name	Access	Description	Default
31:0	RX_SIZE256TO511_CNT	R/W	The number of 256 to 511 bytes frames received. Counter can be written by software.	0x00000000

2.16.3.22 Rx 512-1023 Byte Frame Counter

Short Name:RX_SIZE512TO1023_CNT

Address:0x3F22A

***Table 1242* • Rx 512-1023 Byte Frame Counter**

Bit	Name	Access	Description	Default
31:0	RX_SIZE512TO1023_CNT	R/W	The number of 512 to 1023 bytes frames received. Counter can be written by software.	0x00000000

2.16.3.23 Rx 1024-1518 Byte Frame Counter

Short Name:RX_SIZE1024TO1518_CNT

Address:0x3F22B

***Table 1243* • Rx 1024-1518 Byte Frame Counter**

Bit	Name	Access	Description	Default
31:0	RX_SIZE1024TO1518_CNT	R/W	The number of 1024 to 1518 bytes frames received. Counter can be written by software.	0x00000000

2.16.3.24 Rx 1519 to Max Length Byte Frame Counter

Short Name:RX_SIZE1519TOMAX_CNT

Address:0x3F22C

***Table 1244* • Rx 1519 to Max Length Byte Frame Counter**

Bit	Name	Access	Description	Default
31:0	RX_SIZE1519TOMAX_CNT	R/W	The number of frames received that are longer than 1518 bytes but not longer than the maximum length register (maximum length register + 4 if the frame is VLAN tagged). Counter can be written by software.	0x00000000

2.16.3.25 Rx Inter Packet Gap Shrink Counter

Short Name:RX_IPG_SHRINK_CNT

Address:0x3F22D

Table 1245 **• Rx Inter Packet Gap Shrink Counter**

Bit	Name	Access	Description	Default
31:0	RX_IPG_SHRINK_CNT	R/W	Number of inter packet gap shrinks detected (IPG < 12 bytes). Counter can be written by software.	0x00000000

2.16.3.26 Tx Pause Frame Counter

Short Name:TX_PAUSE_CNT

Address:0x3F22E

Table 1246 **• Tx Pause Frame Counter**

Bit	Name	Access	Description	Default
31:0	TX_PAUSE_CNT	R/W	The number of pause control frames transmitted. Counter can be written by software.	0x00000000

2.16.3.27 Tx Unicast Frame Counter

Short Name:TX_UC_CNT

Address:0x3F22F

Table 1247 **• Tx Unicast Frame Counter**

Bit	Name	Access	Description	Default
31:0	TX_UC_CNT	R/W	The number of unicast frames transmitted. Counter can be written by software.	0x00000000

2.16.3.28 Tx Multicast Frame Counter

Short Name:TX_MC_CNT

Address:0x3F230

Table 1248 **• Tx Multicast Frame Counter**

Bit	Name	Access	Description	Default
31:0	TX_MC_CNT	R/W	The number of multicast frames transmitted. Counter can be written by software.	0x00000000

2.16.3.29 Tx Broadcast Frame Counter

Short Name:TX_BC_CNT

Address:0x3F231

Table 1249 **• Tx Broadcast Frame Counter**

Bit	Name	Access	Description	Default
31:0	TX_BC_CNT	R/W	The number of broadcast frames transmitted. Counter can be written by software.	0x00000000

2.16.3.30 Tx 64 Byte Frame Counter

Short Name:TX_SIZE64_CNT

Address:0x3F232

Table 1250 **• Tx 64 Byte Frame Counter**

Bit	Name	Access	Description	Default
31:0	TX_SIZE64_CNT	R/W	The number of 64 bytes frames transmitted. Counter can be written by software.	0x00000000

2.16.3.31 Tx 65-127 Byte Frame Counter

Short Name:TX_SIZE65TO127_CNT

Address:0x3F233

Table 1251 **• Tx 65-127 Byte Frame Counter**

Bit	Name	Access	Description	Default
31:0	TX_SIZE65TO127_CNT	R/W	The number of 65 to 127 bytes frames transmitted. Counter can be written by software.	0x00000000

2.16.3.32 Tx 128-255 Byte Frame Counter

Short Name:TX_SIZE128TO255_CNT

Address:0x3F234

Table 1252 **• Tx 128-255 Byte Frame Counter**

Bit	Name	Access	Description	Default
31:0	TX_SIZE128TO255_CNT	R/W	The number of 128 to 255 bytes frames transmitted. Counter can be written by software.	0x00000000

2.16.3.33 Tx 256-511 Byte Frame Counter

Short Name:TX_SIZE256TO511_CNT

Address:0x3F235

Table 1253 **• Tx 256-511 Byte Frame Counter**

Bit	Name	Access	Description	Default
31:0	TX_SIZE256TO511_CNT	R/W	The number of 256 to 511 bytes frames transmitted. Counter can be written by software.	0x00000000

2.16.3.34 Tx 512-1023 Byte Frame Counter

Short Name:TX_SIZE512TO1023_CNT

Address:0x3F236

Table 1254 **• Tx 512-1023 byte frame counter**

Bit	Name	Access	Description	Default
31:0	TX_SIZE512TO1023_CNT	R/W	The number of 512 to 1023 bytes frames transmitted. Counter can be written by software.	0x00000000

2.16.3.35 Tx 1024-1518 Byte Frame Counter

Short Name:TX_SIZE1024TO1518_CNT

Address:0x3F237

***Table 1255* • Tx 1024-1518 byte frame counter**

Bit	Name	Access	Description	Default
31:0	TX_SIZE1024TO1518_CNT	R/W	The number of 1024 to 1518 bytes frames transmitted. Counter can be written by software.	0x00000000

2.16.3.36 Tx 1519 to Max Length Byte Frame Counter

Short Name:TX_SIZE1519TOMAX_CNT

Address:0x3F238

***Table 1256* • Tx 1519 to Max Length Byte Frame Counter**

Bit	Name	Access	Description	Default
31:0	TX_SIZE1519TOMAX_CNT	R/W	The number of frames transmitted that are longer than 1518 bytes but not longer than the maximum length register (maximum length register + 4 if the frame is VLAN tagged). Counter can be written by software.	0x00000000

Each MAC generates a statistics vector when receiving or transmitting a frame. This vector is used to generate the port statistics. All counters are 40 bits wide and are not reset when read. It is up to software to detect when a counter has wrapped around. When written, the counter assumes the written value.

2.16.3.37 Rx Bad Bytes Counter (LSB)

Short Name:RX_BAD_BYTES_CNT

Address:0x3F239

The number of received bytes in bad frames (LSBs only).

***Table 1257* • Rx Bad Bytes Counter (LSB)**

Bit	Name	Access	Description	Default
31:0	RX_BAD_BYTES_CNT	R/W	The number of received bytes in bad frames (LSBs only). Counter can be written by software.	0x00000000

2.16.3.38 Rx Bad Bytes Counter (MSB)

Short Name:RX_BAD_BYTES_MSB_CNT

Address:0x3F23A

The number of received bytes in bad frames (MSBs only).

***Table 1258* • Rx Bad Bytes Counter (MSB)**

Bit	Name	Access	Description	Default
7:0	RX_BAD_BYTES_MSB_CNT	R/W	The number of received bytes in bad frames (MSBs only). Counter can be written by software.	0x00

2.16.3.39 Rx OK Bytes Counter (LSB)

Short Name:RX_OK_BYTES_CNT

Address:0x3F23B

The number of received bytes in good frames (LSBs only).

***Table 1259* • Rx OK Bytes Counter (LSB)**

Bit	Name	Access	Description	Default
31:0	RX_OK_BYTES_CNT	R/W	The number of received bytes in good frames (LSBs only). Counter can be written by software.	0x00000000

2.16.3.40 Rx OK Bytes Counter (MSB)

Short Name:RX_OK_BYTES_MSB_CNT

Address:0x3F23C

The number of received bytes in good frames (MSBs only).

***Table 1260* • Rx OK Bytes Counter (MSB)**

Bit	Name	Access	Description	Default
7:0	RX_OK_BYTES_MSB_CNT	R/W	The number of received bytes in good frames (MSBs only). Counter can be written by software.	0x00

2.16.3.41 Rx Bytes Received Counter (LSB)

Short Name:RX_IN_BYTES_CNT

Address:0x3F23D

The number of good, bad, and framing bytes received (LSBs only).

***Table 1261* • Rx Bytes Received Counter (LSB)**

Bit	Name	Access	Description	Default
31:0	RX_IN_BYTES_CNT	R/W	The number of good, bad, and framing bytes received (LSBs only). Counter can be written by software.	0x00000000

2.16.3.42 Rx Bytes Received Counter (MSB)

Short Name:RX_IN_BYTES_MSB_CNT

Address:0x3F23E

The number of good, bad, and framing bytes received (MSBs only).

***Table 1262* • Rx Bytes Received Counter (MSB)**

Bit	Name	Access	Description	Default
7:0	RX_IN_BYTES_MSB_CNT	R/W	The number of good, bad, and framing bytes received (MSBs only). Counter can be written by software.	0x00

2.16.3.43 Tx OK Bytes Counter (LSB)

Short Name:TX_OK_BYTES_CNT

Address:0x3F23F

The number of bytes transmitted successfully (LSBs only).

***Table 1263* • Tx OK Bytes Counter (LSB)**

Bit	Name	Access	Description	Default
31:0	TX_OK_BYTES_CNT	R/W	The number of bytes transmitted successfully (LSBs only). Counter can be written by software.	0x00000000

2.16.3.44 Tx OK Bytes Counter (MSB)

Short Name:TX_OK_BYTES_MSB_CNT

Address:0x3F240

The number of bytes transmitted successfully (MSBs only).

***Table 1264* • Tx OK Bytes Counter (MSB)**

Bit	Name	Access	Description	Default
7:0	TX_OK_BYTES_MSB_CNT	R/W	The number of bytes transmitted successfully (MSBs only). Counter can be written by software.	0x00

2.16.3.45 Tx Bytes Transmitted Counter (LSB)

Short Name:TX_OUT_BYTES_CNT

Address:0x3F241

The number of good, bad, and framing bytes transmitted (LSBs only).

***Table 1265* • Tx Bytes Transmitted Counter (LSB)**

Bit	Name	Access	Description	Default
31:0	TX_OUT_BYTES_CNT	R/W	The number of good, bad, and framing bytes transmitted (LSBs only). Counter can be written by software.	0x00000000

2.16.3.46 Tx Bytes Transmitted Counter (MSB)

Short Name:TX_OUT_BYTES_MSB_CNT

Address:0x3F242

The number of good, bad, and framing bytes transmitted (MSBs only).

***Table 1266* • Tx Bytes Transmitted Counter (MSB)**

Bit	Name	Access	Description	Default
7:0	TX_OUT_BYTES_MSB_CNT	R/W	The number of good, bad, and framing bytes transmitted (MSBs only). Counter can be written by software.	0x00

2.17 FIFO_BIST (Device 0x4)

Table 1267 • **GEN_CFG**

Address	Short Description	Register Name	Details
0x4E900	Generator Configuration	GEN_CFG	Page 465

Table 1268 • **UPDATE**

Address	Short Description	Register Name	Details
0x4E901	Latch All Counters And Timestamps For Readback	UPDATE	Page 466

Table 1269 • **GEN_PKTLEN**

Address	Short Description	Register Name	Details
0x4E902	Packet Length	GEN_PKTLEN	Page 466

Table 1270 • **GEN_IPGLEN**

Address	Short Description	Register Name	Details
0x4E903	Lower 16 bits of 32-bit IPG Length	GEN_IPGLEN_LSW	Page 466
0x4E904	Upper 16 bits of 32-bit IPG Length	GEN_IPGLEN_MSW	Page 467

Table 1271 • **GEN_TIME**

Address	Short Description	Register Name	Details
0x4E905	PTP Timestamp	GEN_TIME	Page 467

Table 1272 • **GEN_ETYPE**

Address	Short Description	Register Name	Details
0x4E906	Ethernet type	GEN_ETYPE	Page 467

Table 1273 • **GEN_SA**

Address	Short Description	Register Name	Details
0x4E910	Lower 16 bits of 48-bit Source Address To Generate	GEN_SA0	Page 467
0x4E911	Middle 16 bits of 48-bit Source Address To Generate	GEN_SA1	Page 467
0x4E912	Upper 16 bits of 48-bit Source Address To Generate	GEN_SA2	Page 468

Table 1274 • **GEN_DA**

Address	Short Description	Register Name	Details
0x4E920	Lower 16 bits of 48-bit Destination Address To Generate	GEN_DA0	Page 468
0x4E921	Middle 16 bits of 48-bit Destination Address To Generate	GEN_DA1	Page 468
0x4E922	Upper 16 bits of 48-bit Destination Address To Generate	GEN_DA2	Page 468

Table 1275 • **GEN_SENT**

Address	Short Description	Register Name	Details
0x4E930	Lower 16 bits of 32-bit packets_sent Counter	GEN_SENT_LSW	Page 468
0x4E931	Upper 16 bits of 32-bit packets_sent Counter	GEN_SENT_MSW	Page 469

Table 1276 • **MON_CFG**

Address	Short Description	Register Name	Details
0x4E940	Monitor Configuration	MON_CFG	Page 469

Table 1277 • **MON_RST**

Address	Short Description	Register Name	Details
0x4E950	Self-clearing Monitor Counters Reset	MON_RST	Page 469

Table 1278 • **MON_GOODCRC**

Address	Short Description	Register Name	Details
0x4E960	Lower 16 bits of 32-bit Good_CRC Counter	MON_GOOD_LSW	Page 469
0x4E961	Upper 16 bits of 32-bit Good_CRC Counter	MON_GOOD_MSW	Page 470

Table 1279 • **MON_BADCRC**

Address	Short Description	Register Name	Details
0x4E970	Lower 16 bits of 32-bit Bad_CRC Counter	MON_BAD_LSW	Page 470
0x4E971	Upper 16 bits of 32-bit Bad_CRC Counter	MON_BAD_MSW	Page 470

Table 1280 • **MON_FRAG**

Address	Short Description	Register Name	Details
0x4E980	Lower 16 bits of 32-bit Packet_Fragment Counter	MON_FRAG_LSW	Page 470
0x4E981	Upper 16 bits of 32-bit Packet_Fragment Counter	MON_FRAG_MSW	Page 470

Table 1281 • **MON_LFAULT**

Address	Short Description	Register Name	Details
0x4E990	Lower 16 bits of 32-bit Local_Fault counter	MON_LFAULT_LSW	Page 470
0x4E991	Upper 16 bits of 32-bit Local_Fault counter	MON_LFAULT_MSW	Page 471

Table 1282 • **MON_BER**

Address	Short Description	Register Name	Details
0x4E9A0	Lower 16 bits of 32-bit BER Counter	MON_BER_LSW	Page 471
0x4E9A1	Upper 16 bits of 32-bit BER Counter	MON_BER_MSW	Page 471

Table 1283 • **MON_TSTAMP0**

Address	Short Description	Register Name	Details
0x4E9B0	PTP Timestamp0 (Oldest) bits 15-0	MON_TSTAMP0_0	Page 471
0x4E9B1	PTP Timestamp0 (Oldest) bits 31-16	MON_TSTAMP0_1	Page 471
0x4E9B2	PTP Timestamp0 (Oldest) bits 47-32	MON_TSTAMP0_2	Page 472
0x4E9B3	PTP Timestamp0 (Oldest) bits 63-48	MON_TSTAMP0_3	Page 472
0x4E9B4	PTP Timestamp0 (Oldest) bits 79-64	MON_TSTAMP0_4	Page 472

Table 1284 • **MON_TSTAMP1**

Address	Short Description	Register Name	Details
0x4E9C0	PTP Timestamp1 bits 15-0	MON_TSTAMP1_0	Page 472
0x4E9C1	PTP Timestamp1 bits 31-16	MON_TSTAMP1_1	Page 472
0x4E9C2	PTP Timestamp1 bits 47-32	MON_TSTAMP1_2	Page 473
0x4E9C3	PTP Timestamp1 bits 63-48	MON_TSTAMP1_3	Page 473
0x4E9C4	PTP Timestamp1 bits 79-64	MON_TSTAMP1_4	Page 473

Table 1285 • **MON_TSTAMP2**

Address	Short Description	Register Name	Details
0x4E9D0	PTP Timestamp2 bits 15-0	MON_TSTAMP2_0	Page 473
0x4E9D1	PTP Timestamp2 bits 31-16	MON_TSTAMP2_1	Page 473
0x4E9D2	PTP Timestamp2 bits 47-32	MON_TSTAMP2_2	Page 474
0x4E9D3	PTP Timestamp2 bits 63-48	MON_TSTAMP2_3	Page 474
0x4E9D4	PTP Timestamp2 bits 79-64	MON_TSTAMP2_4	Page 474

Table 1286 • **MON_TSTAMP3**

Address	Short Description	Register Name	Details
0x4E9E0	PTP Timestamp3 bits 15-0	MON_TSTAMP3_0	Page 474

Table 1286 • **MON_TSTAMP3** ***(continued)***

Address	Short Description	Register Name	Details
0x4E9E1	PTP Timestamp3 bits 31-16	MON_TSTAMP3_1	Page 474
0x4E9E2	PTP Timestamp3 bits 47-32	MON_TSTAMP3_2	Page 475
0x4E9E3	PTP Timestamp3 bits 63-48	MON_TSTAMP3_3	Page 475
0x4E9E4	PTP Timestamp3 bits 79-64	MON_TSTAMP3_4	Page 475

Table 1287 • **MON_TSTAMP4**

Address	Short Description	Register Name	Details
0x4E9F0	PTP Timestamp4 bits 15-0	MON_TSTAMP4_0	Page 475
0x4E9F1	PTP Timestamp4 bits 31-16	MON_TSTAMP4_1	Page 475
0x4E9F2	PTP Timestamp4 bits 47-32	MON_TSTAMP4_2	Page 476
0x4E9F3	PTP Timestamp4 bits 63-48	MON_TSTAMP4_3	Page 476
0x4E9F4	PTP Timestamp4 bits 79-64	MON_TSTAMP4_4	Page 476

Table 1288 • **MON_TSTAMP5**

Address	Short Description	Register Name	Details
0x4EA00	PTP Timestamp5 bits 15-0	MON_TSTAMP5_0	Page 476
0x4EA01	PTP Timestamp5 bits 31-16	MON_TSTAMP5_1	Page 476
0x4EA02	PTP Timestamp5 bits 47-32	MON_TSTAMP5_2	Page 477
0x4EA03	PTP Timestamp5 bits 63-48	MON_TSTAMP5_3	Page 477
0x4EA04	PTP Timestamp5 bits 79-64	MON_TSTAMP5_4	Page 477

Table 1289 • **MON_TSTAMP6**

Address	Short Description	Register Name	Details
0x4EA10	PTP Timestamp6 bits 15-0	MON_TSTAMP6_0	Page 477
0x4EA11	PTP Timestamp6 bits 31-16	MON_TSTAMP6_1	Page 477
0x4EA12	PTP Timestamp6 bits 47-32	MON_TSTAMP6_2	Page 478
0x4EA13	PTP Timestamp6 bits 63-48	MON_TSTAMP6_3	Page 478
0x4EA14	PTP Timestamp6 bits 79-64	MON_TSTAMP6_4	Page 478

Table 1290 • **MON_TSTAMP7**

Address	Short Description	Register Name	Details
0x4EA20	PTP Timestamp7 bits 15-0	MON_TSTAMP7_0	Page 478
0x4EA21	PTP Timestamp7 bits 31-16	MON_TSTAMP7_1	Page 478
0x4EA22	PTP Timestamp7 bits 47-32	MON_TSTAMP7_2	Page 479
0x4EA23	PTP Timestamp7 bits 63-48	MON_TSTAMP7_3	Page 479
0x4EA24	PTP Timestamp7 bits 79-64	MON_TSTAMP7_4	Page 479

Table 1291 • **MON_TSTAMP8**

Address	Short Description	Register Name	Details
0x4EA30	PTP Timestamp8 bits 15-0	MON_TSTAMP8_0	Page 479
0x4EA31	PTP Timestamp8 bits 31-16	MON_TSTAMP8_1	Page 479
0x4EA32	PTP Timestamp8 bits 47-32	MON_TSTAMP8_2	Page 480
0x4EA33	PTP Timestamp8 bits 63-48	MON_TSTAMP8_3	Page 480
0x4EA34	PTP Timestamp8 bits 79-64	MON_TSTAMP8_4	Page 480

Table 1292 • **MON_TSTAMP9**

Address	Short Description	Register Name	Details
0x4EA40	PTP Timestamp9 (Most Recent) bits 15-0	MON_TSTAMP9_0	Page 480
0x4EA41	PTP Timestamp9 (Most Recent) bits 31-16	MON_TSTAMP9_1	Page 480
0x4EA42	PTP Timestamp9 (Most Recent) bits 47-32	MON_TSTAMP9_2	Page 481
0x4EA43	PTP Timestamp9 (Most Recent) bits 63-48	MON_TSTAMP9_3	Page 481
0x4EA44	PTP Timestamp9 (Most Recent) bits 79-64	MON_TSTAMP9_4	Page 481

Table 1293 • **RATE_COMP_FIFO_STAT**

Address	Short Description	Register Name	Details
0x4EA50	Rate Compensation FIFO Mask	RATE_COMP_FIFO_MASK	Page 481
0x4EA51	Rate Compensation FIFO Status	RATE_COMP_FIFO_STAT	Page 482

Table 1294 • **RATE_COMP_FIFO_Idle_Counts**

Address	Short Description	Register Name	Details
0x4EA60	Tx FIFO Idle Add Count	Tx_FIFO_Idle_Add_Count	Page 483
0x4EA61	Tx FIFO Idle Drop Count	Tx_FIFO_Idle_Drop_Count	Page 483
0x4EA62	Rx FIFO Idle Add Count	Rx_FIFO_Idle_Add_Count	Page 483
0x4EA63	Rx FIFO Idle Drop Count	Rx_FIFO_Idle_Drop_Count	Page 484
0x4EA64	Tx FIFO2 Idle Add Count	Tx_FIFO2_Idle_Add_Count	Page 484
0x4EA65	Tx FIFO2 Idle Drop Count	Tx_FIFO2_Idle_Drop_Count	Page 484

Table 1295 • **Datapath_Control**

Address	Short Description	Register Name	Details
0x4EA70	Datapath_Control	Datapath_Control	Page 485

2.17.1 BIST Configuration

2.17.1.1 Generator Configuration

Short Name:GEN_CFG

Address:0x4E900

***Table 1296* • Generator Configuration**

Bit	Name	Access	Description	Default
14:12	lenofs	R/W	Decrease pktlen by lenofs	0x3
11:4	srate	R/W	Number of standard frames between PTP frames	0x00
3	single	One-shot	Generate a single packet during pktgen_idles	0x0
2	idles	R/W	Generate all Idles 0: Generate frames 1: Generate idles only	0x0
1	ptp_enable	R/W	Generate PTP frames 0: Generate standard frames 1: Generate PTP frames	0x0
0	enable	R/W	Enable packet generator 0: Generator is disabled 1: Generator is enabled Note: Pattern generator data can not simultaneously be inserted in the egress and ingress data paths. Insertion of pattern generator data into the paths is controlled by Datapath_Control.IGR_XGMII_PG_SEL and Datapath_Control.EGR_XGMII_PG_SEL.	0x0

2.17.1.2 Latch All Counters And Timestamps For Readback

Short Name:UPDATE

Address:0x4E901

***Table 1297* • Latch All Counters And Timestamps For Readback**

Bit	Name	Access	Description	Default
1	ts_hold	R/W	Freeze most recent 10 timestamps for readback 0 : timestamps are updating. Do not read. 1 : timestamps are not updating. Ok to read.	0x0
0	cntr_update	One-shot	Freeze all generator and monitor counters for readback	0x0

2.17.1.3 Packet Length

Short Name:GEN_PKTLEN

Address:0x4E902

***Table 1298* • Packet Length**

Bit	Name	Access	Description	Default
7:0	pktlen	R/W	Packet length 0: bytes = preamble + 64 + /T/ >0: bytes = 24 + pktlen*64 + (8-lenofs)	0x17

2.17.1.4 Lower 16 bits of 32-bit IPG Length

Short Name:GEN_IPGLEN_LSW

Address:0x4E903

***Table 1299* • Lower 16 bits of 32-bit IPG Length**

Bit	Name	Access	Description	Default
15:0	ipglen_lsw	R/W	IPG length: /I/ bytes = lenofs + ipglen*4	0x0001

2.17.1.5 Upper 16 bits of 32-bit IPG Length

Short Name:GEN_IPGLEN_MSW

Address:0x4E904

***Table 1300* • Upper 16 bits of 32-bit IPG Length**

Bit	Name	Access	Description	Default
15:0	ipglen_msw	R/W	IPG length: /I/ bytes = lenofs + ipglen*4	0x0000

2.17.1.6 PTP Timestamp

Short Name:GEN_TIME

Address:0x4E905

***Table 1301* • PTP Timestamp**

Bit	Name	Access	Description	Default
15:0	ptptime	R/W	PTP timestamp to generate: [15:8] is seconds, [7:0] is ns	0x0000

2.17.1.7 Ethernet Type

Short Name:GEN_ETYPE

Address:0x4E906

***Table 1302* • Ethernet Type**

Bit	Name	Access	Description	Default
15:0	etype	R/W	Etype field for standard frames	0x0000

2.17.1.8 Lower 16 bits of 48-bit Source Address To Generate

Short Name:GEN_SA0

Address:0x4E910

***Table 1303* • Lower 16 bits of 48-bit Source Address To Generate**

Bit	Name	Access	Description	Default
15:0	sa0	R/W	Generated source address [15:0]	0x0000

2.17.1.9 Middle 16 bits of 48-bit Source Address To Generate

Short Name:GEN_SA1

Address:0x4E911

Table 1304 **• Middle 16 bits of 48-bit Source Address To Generate**

Bit	Name	Access	Description	Default
15:0	sa1	R/W	Generated source address [31:16]	0x0000

2.17.1.10 Upper 16 bits of 48-bit Source Address To Generate

Short Name:GEN_SA2

Address:0x4E912

Table 1305 **• Upper 16 bits of 48-bit Source Address To Generate**

Bit	Name	Access	Description	Default
15:0	sa2	R/W	Generated source address [47:32]	0x0000

2.17.1.11 Lower 16 bits of 48-bit Destination Address To Generate

Short Name:GEN_DA0

Address:0x4E920

Table 1306 **• Lower 16 bits of 48-bit Destination Address To Generate**

Bit	Name	Access	Description	Default
15:0	da0	R/W	Generated destination address [15:0]	0x0000

2.17.1.12 Middle 16 bits of 48-bit Destination Address To Generate

Short Name:GEN_DA1

Address:0x4E921

Table 1307 **• Middle 16 bits of 48-bit Destination Address To Generate**

Bit	Name	Access	Description	Default
15:0	da1	R/W	Generated destination address [31:16]	0x0000

2.17.1.13 Upper 16 bits of 48-bit Destination Address To Generate

Short Name:GEN_DA2

Address:0x4E922

Table 1308 **• Upper 16 bits of 48-bit Destination Address To Generate**

Bit	Name	Access	Description	Default
15:0	da2	R/W	Generated destination address [47:32]	0x0000

2.17.1.14 Lower 16 bits of 32-bit packets_sent Counter

Short Name:GEN_SENT_LSW

Address:0x4E930

***Table 1309* • Lower 16 bits of 32-bit packets_sent Counter**

Bit	Name	Access	Description	Default
15:0	sent_lsw	R/O	LSW of number of packets generated	0x0000

2.17.1.15 Upper 16 bits of 32-bit packets_sent Counter

Short Name:GEN_SENT_MSW

Address:0x4E931

***Table 1310* • Upper 16 bits of 32-bit packets_sent Counter**

Bit	Name	Access	Description	Default
15:0	sent_msw	R/O	MSW of number of packets generated	0x0000

2.17.1.16 monitor configuration

Short Name:MON_CFG

Address:0x4E940

***Table 1311* • monitor configuration**

Bit	Name	Access	Description	Default
0	enable	R/W	Enable packet monitor 0: Monitor is disabled 1: Monitor is enabled	0x0

2.17.1.17 Self-Clearing Monitor Counters Reset

Short Name:MON_RST

Address:0x4E950

***Table 1312* • Self-Clearing Monitor Counters Reset**

Bit	Name	Access	Description	Default
5	ber_rst	One-shot	reset BER counter	0x0
4	lfault_rst	One-shot	reset Local_Fault counter	0x0
3	frag_rst	One-shot	reset Packet_Fragment counter	0x0
2	bad_rst	One-shot	reset Bad_CRC counter	0x0
1	good_rst	One-shot	reset Good_CRC counter	0x0
0	all_rst	One-shot	reset all counters	0x0

2.17.1.18 Lower 16 bits of 32-bit Good_CRC Counter

Short Name:MON_GOOD_LSW

Address:0x4E960

***Table 1313* • Lower 16 bits of 32-bit Good_CRC Counter**

Bit	Name	Access	Description	Default
15:0	good_lsw	R/O	LSW of Good_CRC counter	0x0000

2.17.1.19 Upper 16 bits of 32-bit Good_CRC Counter

Short Name:MON_GOOD_MSW

Address:0x4E961

Table 1314 **• Upper 16 bits of 32-bit Good_CRC Counter**

Bit	Name	Access	Description	Default
15:0	good_msw	R/O	MSW of Good_CRC counter	0x0000

2.17.1.20 Lower 16 bits of 32-bit Bad_CRC Counter

Short Name:MON_BAD_LSW

Address:0x4E970

Table 1315 **• Lower 16 bits of 32-bit Bad_CRC Counter**

Bit	Name	Access	Description	Default
15:0	bad_lsw	R/O	LSW of Bad_CRC counter	0x0000

2.17.1.21 Upper 16 bits of 32-bit Bad_CRC Counter

Short Name:MON_BAD_MSW

Address:0x4E971

Table 1316 **• Upper 16 bits of 32-bit Bad_CRC Counter**

Bit	Name	Access	Description	Default
15:0	bad_msw	R/O	MSW of Bad_CRC counter	0x0000

2.17.1.22 Lower 16 bits of 32-bit Packet_Fragment Counter

Short Name:MON_FRAG_LSW

Address:0x4E980

Table 1317 **• Lower 16 bits of 32-bit Packet_Fragment Counter**

Bit	Name	Access	Description	Default
15:0	frag_lsw	R/O	LSW of Packet_Fragment counter	0x0000

2.17.1.23 Upper 16 bits of 32-bit Packet_Fragment Counter

Short Name:MON_FRAG_MSW

Address:0x4E981

Table 1318 **• Upper 16 bits of 32-bit Packet_Fragment Counter**

Bit	Name	Access	Description	Default
15:0	frag_msw	R/O	MSW of Packet_Fragment counter	0x0000

2.17.1.24 Lower 16 bits of 32-bit Local_Fault Counter

Short Name:MON_LFAULT_LSW

Address:0x4E990

Table 1319 **• Lower 16 bits of 32-bit Local_Fault Counter**

Bit	Name	Access	Description	Default
15:0	lfault_lsw	R/O	LSW of Local_Fault counter	0x0000

2.17.1.25 Upper 16 bits of 32-bit Local_Fault Counter

Short Name:MON_LFAULT_MSW

Address:0x4E991

Table 1320 **• Upper 16 bits of 32-bit Local_Fault Counter**

Bit	Name	Access	Description	Default
15:0	lfault_msw	R/O	MSW of Local_Fault counter	0x0000

2.17.1.26 Lower 16 bits of 32-bit BER Counter

Short Name:MON_BER_LSW

Address:0x4E9A0

Table 1321 **• Lower 16 bits of 32-bit BER Counter**

Bit	Name	Access	Description	Default
15:0	ber_lsw	R/O	LSW of BER counter	0x0000

2.17.1.27 Upper 16 bits of 32-bit BER Counter

Short Name:MON_BER_MSW

Address:0x4E9A1

Table 1322 **• Upper 16 bits of 32-bit BER Counter**

Bit	Name	Access	Description	Default
15:0	ber_msw	R/O	MSW of BER counter	0x0000

2.17.1.28 PTP Timestamp0 (Oldest) bits 15-0

Short Name:MON_TSTAMP0_0

Address:0x4E9B0

Table 1323 **• PTP Timestamp0 (Oldest) bits 15-0**

Bit	Name	Access	Description	Default
15:0	tstamp0_0	R/O	PTP timestamp 0, bits [15:0]	0x0000

2.17.1.29 PTP Timestamp0 (Oldest) bits 31-16

Short Name:MON_TSTAMP0_1

Address:0x4E9B1

Table 1324 **• PTP Timestamp0 (Oldest) bits 31-16**

Bit	Name	Access	Description	Default
15:0	tstamp0_1	R/O	PTP timestamp 0, bits [31:16]	0x0000

2.17.1.30 PTP Timestamp0 (Oldest) bits 47-32

Short Name:MON_TSTAMP0_2

Address:0x4E9B2

Table 1325 **• PTP Timestamp0 (Oldest) bits 47-32**

Bit	Name	Access	Description	Default
15:0	tstamp0_2	R/O	PTP timestamp 0, bits [47:32]	0x0000

2.17.1.31 PTP Timestamp0 (Oldest) bits 63-48

Short Name:MON_TSTAMP0_3

Address:0x4E9B3

Table 1326 **• PTP Timestamp0 (Oldest) bits 63-48**

Bit	Name	Access	Description	Default
15:0	tstamp0_3	R/O	PTP timestamp 0, bits [63:48]	0x0000

2.17.1.32 PTP Timestamp0 (Oldest) bits 79-64

Short Name:MON_TSTAMP0_4

Address:0x4E9B4

Table 1327 **• PTP Timestamp0 (Oldest) bits 79-64**

Bit	Name	Access	Description	Default
15:0	tstamp0_4	R/O	PTP timestamp 0, bits [79:64]	0x0000

2.17.1.33 PTP Timestamp1 bits 15-0

Short Name:MON_TSTAMP1_0

Address:0x4E9C0

Table 1328 **• PTP Timestamp1 bits 15-0**

Bit	Name	Access	Description	Default
15:0	tstamp1_0	R/O	PTP timestamp 1, bits [15:0]	0x0000

2.17.1.34 PTP Timestamp1 bits 31-16

Short Name:MON_TSTAMP1_1

Address:0x4E9C1

***Table 1329* • PTP Timestamp1 bits 31-16**

Bit	Name	Access	Description	Default
15:0	tstamp1_1	R/O	PTP timestamp 1, bits [31:16]	0x0000

2.17.1.35 PTP Timestamp1 bits 47-32

Short Name:MON_TSTAMP1_2

Address:0x4E9C2

***Table 1330* • PTP Timestamp1 bits 47-32**

Bit	Name	Access	Description	Default
15:0	tstamp1_2	R/O	PTP timestamp 1, bits [47:32]	0x0000

2.17.1.36 PTP Timestamp1 bits 63-48

Short Name:MON_TSTAMP1_3

Address:0x4E9C3

***Table 1331* • PTP Timestamp1 bits 63-48**

Bit	Name	Access	Description	Default
15:0	tstamp1_3	R/O	PTP timestamp 1, bits [63:48]	0x0000

2.17.1.37 PTP Timestamp1 bits 79-64

Short Name:MON_TSTAMP1_4

Address:0x4E9C4

***Table 1332* • PTP Timestamp1 bits 79-64**

Bit	Name	Access	Description	Default
15:0	tstamp1_4	R/O	PTP timestamp 1, bits [79:64]	0x0000

2.17.1.38 PTP Timestamp2 bits 15-0

Short Name:MON_TSTAMP2_0

Address:0x4E9D0

***Table 1333* • PTP Timestamp2 bits 15-0**

Bit	Name	Access	Description	Default
15:0	tstamp2_0	R/O	PTP timestamp 2, bits [15:0]	0x0000

2.17.1.39 PTP Timestamp2 bits 31-16

Short Name:MON_TSTAMP2_1

Address:0x4E9D1

Table 1334 **• PTP Timestamp2 bits 31-16**

Bit	Name	Access	Description	Default
15:0	tstamp2_1	R/O	PTP timestamp 2, bits [31:16]	0x0000

2.17.1.40 PTP Timestamp2 bits 47-32

Short Name:MON_TSTAMP2_2

Address:0x4E9D2

Table 1335 **• PTP Timestamp2 bits 47-32**

Bit	Name	Access	Description	Default
15:0	tstamp2_2	R/O	PTP timestamp 2, bits [47:32]	0x0000

2.17.1.41 PTP Timestamp2 bits 63-48

Short Name:MON_TSTAMP2_3

Address:0x4E9D3

Table 1336 **• PTP Timestamp2 bits 63-48**

Bit	Name	Access	Description	Default
15:0	tstamp2_3	R/O	PTP timestamp 2, bits [63:48]	0x0000

2.17.1.42 PTP Timestamp2 bits 79-64

Short Name:MON_TSTAMP2_4

Address:0x4E9D4

Table 1337 **• PTP Timestamp2 bits 79-64**

Bit	Name	Access	Description	Default
15:0	tstamp2_4	R/O	PTP timestamp 2, bits [79:64]	0x0000

2.17.1.43 PTP Timestamp3 bits 15-0

Short Name:MON_TSTAMP3_0

Address:0x4E9E0

Table 1338 **• PTP Timestamp3 bits 15-0**

Bit	Name	Access	Description	Default
15:0	tstamp3_0	R/O	PTP timestamp 3, bits [15:0]	0x0000

2.17.1.44 PTP Timestamp3 bits 31-16

Short Name:MON_TSTAMP3_1

Address:0x4E9E1

***Table 1339* • PTP Timestamp3 bits 31-16**

Bit	Name	Access	Description	Default
15:0	tstamp3_1	R/O	PTP timestamp 3, bits [31:16]	0x0000

2.17.1.45 PTP Timestamp3 bits 47-32

Short Name:MON_TSTAMP3_2

Address:0x4E9E2

***Table 1340* • PTP Timestamp3 bits 47-32**

Bit	Name	Access	Description	Default
15:0	tstamp3_2	R/O	PTP timestamp 3, bits [47:32]	0x0000

2.17.1.46 PTP Timestamp3 bits 63-48

Short Name:MON_TSTAMP3_3

Address:0x4E9E3

***Table 1341* • PTP Timestamp3 bits 63-48**

Bit	Name	Access	Description	Default
15:0	tstamp3_3	R/O	PTP timestamp 3, bits [63:48]	0x0000

2.17.1.47 PTP Timestamp3 bits 79-64

Short Name:MON_TSTAMP3_4

Address:0x4E9E4

***Table 1342* • PTP Timestamp3 bits 79-64**

Bit	Name	Access	Description	Default
15:0	tstamp3_4	R/O	PTP timestamp 3, bits [79:64]	0x0000

2.17.1.48 PTP Timestamp4 bits 15-0

Short Name:MON_TSTAMP4_0

Address:0x4E9F0

***Table 1343* • PTP Timestamp4 bits 15-0**

Bit	Name	Access	Description	Default
15:0	tstamp4_0	R/O	PTP timestamp 4, bits [15:0]	0x0000

2.17.1.49 PTP Timestamp4 bits 31-16

Short Name:MON_TSTAMP4_1

Address:0x4E9F1

Table 1344 **• PTP Timestamp4 bits 31-16**

Bit	Name	Access	Description	Default
15:0	tstamp4_1	R/O	PTP timestamp 4, bits [31:16]	0x0000

2.17.1.50 PTP Timestamp4 bits 47-32

Short Name:MON_TSTAMP4_2

Address:0x4E9F2

Table 1345 **• PTP Timestamp4 bits 47-32**

Bit	Name	Access	Description	Default
15:0	tstamp4_2	R/O	PTP timestamp 4, bits [47:32]	0x0000

2.17.1.51 PTP Timestamp4 bits 63-48

Short Name:MON_TSTAMP4_3

Address:0x4E9F3

Table 1346 **• PTP Timestamp4 bits 63-48**

Bit	Name	Access	Description	Default
15:0	tstamp4_3	R/O	PTP timestamp 4, bits [63:48]	0x0000

2.17.1.52 PTP Timestamp4 bits 79-64

Short Name:MON_TSTAMP4_4

Address:0x4E9F4

Table 1347 **• PTP Timestamp4 bits 79-64**

Bit	Name	Access	Description	Default
15:0	tstamp4_4	R/O	PTP timestamp 4, bits [79:64]	0x0000

2.17.1.53 PTP Timestamp5 bits 15-0

Short Name:MON_TSTAMP5_0

Address:0x4EA00

Table 1348 **• PTP Timestamp5 bits 15-0**

Bit	Name	Access	Description	Default
15:0	tstamp5_0	R/O	PTP timestamp 5, bits [15:0]	0x0000

2.17.1.54 PTP Timestamp5 bits 31-16

Short Name:MON_TSTAMP5_1

Address:0x4EA01

***Table 1349* • PTP Timestamp5 bits 31-16**

Bit	Name	Access	Description	Default
15:0	tstamp5_1	R/O	PTP timestamp 5, bits [31:16]	0x0000

2.17.1.55 PTP Timestamp5 bits 47-32

Short Name:MON_TSTAMP5_2

Address:0x4EA02

***Table 1350* • PTP Timestamp5 bits 47-32**

Bit	Name	Access	Description	Default
15:0	tstamp5_2	R/O	PTP timestamp 5, bits [47:32]	0x0000

2.17.1.56 PTP Timestamp5 bits 63-48

Short Name:MON_TSTAMP5_3

Address:0x4EA03

***Table 1351* • PTP Timestamp5 bits 63-48**

Bit	Name	Access	Description	Default
15:0	tstamp5_3	R/O	PTP timestamp 5, bits [63:48]	0x0000

2.17.1.57 PTP Timestamp5 bits 79-64

Short Name:MON_TSTAMP5_4

Address:0x4EA04

***Table 1352* • PTP Timestamp5 bits 79-64**

Bit	Name	Access	Description	Default
15:0	tstamp5_4	R/O	PTP timestamp 5, bits [79:64]	0x0000

2.17.1.58 PTP Timestamp6 bits 15-0

Short Name:MON_TSTAMP6_0

Address:0x4EA10

***Table 1353* • PTP Timestamp6 bits 15-0**

Bit	Name	Access	Description	Default
15:0	tstamp6_0	R/O	PTP timestamp 6, bits [15:0]	0x0000

2.17.1.59 PTP Timestamp6 bits 31-16

Short Name:MON_TSTAMP6_1

Address:0x4EA11

Table 1354 **• PTP Timestamp6 bits 31-16**

Bit	Name	Access	Description	Default
15:0	tstamp6_1	R/O	PTP timestamp 6, bits [31:16]	0x0000

2.17.1.60 PTP Timestamp6 bits 47-32

Short Name:MON_TSTAMP6_2

Address:0x4EA12

Table 1355 **• PTP Timestamp6 bits 47-32**

Bit	Name	Access	Description	Default
15:0	tstamp6_2	R/O	PTP timestamp 6, bits [47:32]	0x0000

2.17.1.61 PTP Timestamp6 bits 63-48

Short Name:MON_TSTAMP6_3

Address:0x4EA13

Table 1356 **• PTP Timestamp6 bits 63-48**

Bit	Name	Access	Description	Default
15:0	tstamp6_3	R/O	PTP timestamp 6, bits [63:48]	0x0000

2.17.1.62 PTP Timestamp6 bits 79-64

Short Name:MON_TSTAMP6_4

Address:0x4EA14

Table 1357 **• PTP Timestamp6 bits 79-64**

Bit	Name	Access	Description	Default
15:0	tstamp6_4	R/O	PTP timestamp 6, bits [79:64]	0x0000

2.17.1.63 PTP Timestamp7 bits 15-0

Short Name:MON_TSTAMP7_0

Address:0x4EA20

Table 1358 **• PTP Timestamp7 bits 15-0**

Bit	Name	Access	Description	Default
15:0	tstamp7_0	R/O	PTP timestamp 7, bits [15:0]	0x0000

2.17.1.64 PTP Timestamp7 bits 31-16

Short Name:MON_TSTAMP7_1

Address:0x4EA21

***Table 1359* • PTP Timestamp7 bits 31-16**

Bit	Name	Access	Description	Default
15:0	tstamp7_1	R/O	PTP timestamp 7, bits [31:16]	0x0000

2.17.1.65 PTP Timestamp7 bits 47-32

Short Name:MON_TSTAMP7_2

Address:0x4EA22

***Table 1360* • PTP Timestamp7 bits 47-32**

Bit	Name	Access	Description	Default
15:0	tstamp7_2	R/O	PTP timestamp 7, bits [47:32]	0x0000

2.17.1.66 PTP Timestamp7 bits 63-48

Short Name:MON_TSTAMP7_3

Address:0x4EA23

***Table 1361* • PTP Timestamp7 bits 63-48**

Bit	Name	Access	Description	Default
15:0	tstamp7_3	R/O	PTP timestamp 7, bits [63:48]	0x0000

2.17.1.67 PTP Timestamp7 bits 79-64

Short Name:MON_TSTAMP7_4

Address:0x4EA24

***Table 1362* • PTP Timestamp7 bits 79-64**

Bit	Name	Access	Description	Default
15:0	tstamp7_4	R/O	PTP timestamp 7, bits [79:64]	0x0000

2.17.1.68 PTP Timestamp8 bits 15-0

Short Name:MON_TSTAMP8_0

Address:0x4EA30

***Table 1363* • PTP Timestamp8 bits 15-0**

Bit	Name	Access	Description	Default
15:0	tstamp8_0	R/O	PTP timestamp 8, bits [15:0]	0x0000

2.17.1.69 PTP Timestamp8 bits 31-16

Short Name:MON_TSTAMP8_1

Address:0x4EA31

Table 1364 **• PTP Timestamp8 bits 31-16**

Bit	Name	Access	Description	Default
15:0	tstamp8_1	R/O	PTP timestamp 8, bits [31:16]	0x0000

2.17.1.70 PTP Timestamp8 bits 47-32

Short Name:MON_TSTAMP8_2

Address:0x4EA32

Table 1365 **• PTP Timestamp8 bits 47-32**

Bit	Name	Access	Description	Default
15:0	tstamp8_2	R/O	PTP timestamp 8, bits [47:32]	0x0000

2.17.1.71 PTP Timestamp8 bits 63-48

Short Name:MON_TSTAMP8_3

Address:0x4EA33

Table 1366 **• PTP Timestamp8 bits 63-48**

Bit	Name	Access	Description	Default
15:0	tstamp8_3	R/O	PTP timestamp 8, bits [63:48]	0x0000

2.17.1.72 PTP Timestamp8 bits 79-64

Short Name:MON_TSTAMP8_4

Address:0x4EA34

Table 1367 **• PTP Timestamp8 bits 79-64**

Bit	Name	Access	Description	Default
15:0	tstamp8_4	R/O	PTP timestamp 8, bits [79:64]	0x0000

2.17.1.73 PTP Timestamp9 (Most Recent) bits 15-0

Short Name:MON_TSTAMP9_0

Address:0x4EA40

Table 1368 **• PTP Timestamp9 (Most Recent) bits 15-0**

Bit	Name	Access	Description	Default
15:0	tstamp9_0	R/O	PTP timestamp 9, bits [15:0]	0x0000

2.17.1.74 PTP Timestamp9 (Most Recent) bits 31-16

Short Name:MON_TSTAMP9_1

Address:0x4EA41

Table 1369 **• PTP Timestamp9 (Most Recent) bits 31-16**

Bit	Name	Access	Description	Default
15:0	tstamp9_1	R/O	PTP timestamp 9, bits [31:16]	0x0000

2.17.1.75 PTP Timestamp9 (Most Recent) bits 47-32

Short Name:MON_TSTAMP9_2

Address:0x4EA42

Table 1370 **• PTP Timestamp9 (Most Recent) bits 47-32**

Bit	Name	Access	Description	Default
15:0	tstamp9_2	R/O	PTP timestamp 9, bits [47:32]	0x0000

2.17.1.76 PTP Timestamp9 (Most Recent) bits 63-48

Short Name:MON_TSTAMP9_3

Address:0x4EA43

Table 1371 **• PTP Timestamp9 (Most Recent) bits 63-48**

Bit	Name	Access	Description	Default
15:0	tstamp9_3	R/O	PTP timestamp 9, bits [63:48]	0x0000

2.17.1.77 PTP Timestamp9 (Most Recent) bits 79-64

Short Name:MON_TSTAMP9_4

Address:0x4EA44

Table 1372 **• PTP Timestamp9 (Most Recent) bits 79-64**

Bit	Name	Access	Description	Default
15:0	tstamp9_4	R/O	PTP timestamp 9, bits [79:64]	0x0000

Overflow/underflow status for the rate compensating FIFOs is reported in this register. Tx FIFO2 in the chip's egress data path is active when the part is in 10G LAN or 10G WAN modes. An equivalent FIFO for 1G operation is embedded in the host side 1G PCS logic. The second egress FIFO and the ingress FIFO are used when the MACs are disabled. The flow control buffer connected to the host-side MAC is used for rate compensation when the MACs are enabled.

2.17.1.78 Rate Compensation FIFO Mask

Short Name:RATE_COMP_FIFO_MASK

Address:0x4EA50

Table 1373 **• Rate Compensation FIFO Mask**

Bit	Name	Access	Description	Default
5	TX_FIFO2_OVERFLOW_INTR_EN	R/W	Interrupt enable for Tx_FIFO2_overflow 0 = Tx_FIFO2_overflow will not propagate to interrupt 1 = Tx_FIFO2_overflow will propagate to interrupt	0x0

*Table 1373 • (continued)*Rate Compensation FIFO Mask

Bit	Name	Access	Description	Default
4	TX_FIFO2_UNDERFLOW_INTR_EN	R/W	Interrupt enable for Tx_FIFO2_underflow 0 = Tx_FIFO2_underflow will not propagate to interrupt1 = Tx_FIFO2_underflow will propagate to interrupt	0x0
3	RX_FIFO_OVERFLOW_INTR_EN	R/W	Interrupt enable for Rx_FIFO_overflow 0 = Rx_FIFO_overflow will not propagate to interrupt1 = Rx_FIFO_overflow will propagate to interrupt	0x0
2	RX_FIFO_UNDERFLOW_INTR_EN	R/W	Interrupt enable for Rx_FIFO_underflow 0 = Rx_FIFO_underflow will not propagate to interrupt1 = Rx_FIFO_underflow will propagate to interrupt	0x0
1	TX_FIFO_OVERFLOW_INTR_EN	R/W	Interrupt enable for Tx_FIFO_overflow 0 = Tx_FIFO_overflow will not propagate to interrupt1 = Tx_FIFO_overflow will propagate to interrupt	0x0
0	TX_FIFO_UNDERFLOW_INTR_EN	R/W	Interrupt enable for Tx_FIFO_underflow 0 = Tx_FIFO_underflow will not propagate to interrupt1 = Tx_FIFO_underflow will propagate to interrupt	0x0

2.17.1.79 Rate Compensation FIFO Status

Short Name:RATE_COMP_FIFO_STAT

Address:0x4EA51

Table 1374 • Rate Compensation FIFO Status

Bit	Name	Access	Description	Default
5	Tx_FIFO2_overflow	Sticky	Overflow status bit for the 10G host clock rate compensating FIFO in the chip's egress data path. Status: 0: No overflow 1: Overflow	0x0
4	Tx_FIFO2_underflow	Sticky	Underflow status bit for the 10G host clock rate compensating FIFO in the chip's egress data path. Status: 0: No underflow 1: Underflow	0x0
3	Rx_FIFO_overflow	Sticky	Overflow status bit for the rate compensating FIFO in the chip's ingress data path. The ingress FIFO is enabled when the MACs are disabled. Status: 0: No overflow 1: Overflow	0x0
2	Rx_FIFO_underflow	Sticky	Underflow status bit for the rate compensating FIFO in the chip's ingress data path. The ingress FIFO is enabled when the MACs are disabled. Status: 0: No underflow 1: Underflow	0x0

Table 1374 • **Rate Compensation FIFO Status *(continued)***

Bit	Name	Access	Description	Default
1	Tx_FIFO_overflow	Sticky	Overflow status bit for the second rate compensating FIFO in the chip's egress data path. The egress FIFO is enabled when the MACs are disabled. Status: 0: No overflow 1: Overflow	0x0
0	Tx_FIFO_underflow	Sticky	Underflow status bit for the second rate compensating FIFO in the chip's egress data path. The egress FIFO is enabled when the MACs are disabled. Status: 0: No underflow 1: Underflow	0x0

Reports the number of Idles added and dropped from the data streams.

2.17.1.80 Tx FIFO Idle Add Count

Short Name: Tx_FIFO_Idle_Add_Count

Address:0x4EA60

Table 1375 • **Tx FIFO Idle Add Count**

Bit	Name	Access	Description	Default
15:0	Tx_FIFO_idle_group_add_count	R/O	Idle group count added in Tx FIFO1 for line/host clock rate compensating in the chip's egress data path. The counter saturates when the maximum value is exceeded. The counter is cleared when the register is read.	0x0000

2.17.1.81 Tx FIFO Idle Drop Count

Short Name: Tx_FIFO_Idle_Drop_Count

Address:0x4EA61

Table 1376 • **Tx FIFO Idle Drop Count**

Bit	Name	Access	Description	Default
15:0	Tx_FIFO_idle_group_drop_count	R/O	Idle group count dropped in Tx FIFO1 for line/host clock rate compensating in the chip's egress data path. The counter saturates when the maximum value is exceeded. The counter is cleared when the register is read.	0x0000

2.17.1.82 Rx FIFO Idle Add Count

Short Name: Rx_FIFO_Idle_Add_Count

Address:0x4EA62

***Table 1377* • Rx FIFO Idle Add Count**

Bit	Name	Access	Description	Default
15:0	Rx_FIFO_idle_group_add_count	R/O	Idle group count added in the Rx FIFO for line/host clock rate compensating in the chip's ingress data path. The counter saturates when the maximum value is exceeded. The counter is cleared when the register is read.	0x0000

2.17.1.83 Rx FIFO Idle Drop Count

Short Name: Rx_FIFO_Idle_Drop_Count

Address:0x4EA63

***Table 1378* • Rx FIFO Idle Drop Count**

Bit	Name	Access	Description	Default
15:0	Rx_FIFO_idle_group_drop_count	R/O	Idle group count dropped in the Rx FIFO for line/host clock rate compensating in the chip's ingress data path. The counter saturates when the maximum value is exceeded. The counter is cleared when the register is read.	0x0000

2.17.1.84 Tx FIFO2 Idle Add Count

Short Name: Tx_FIFO2_Idle_Add_Count

Address:0x4EA64

***Table 1379* • Tx FIFO2 Idle Add Count**

Bit	Name	Access	Description	Default
15:0	Tx_FIFO2_idle_group_add_count	R/O	Idle group count added in Tx FIFO2 for 10G host clock rate compensating in the chip's egress data path. The counter saturates when the maximum value is exceeded. The counter is cleared when the register is read.	0x0000

2.17.1.85 Tx FIFO2 Idle Drop Count

Short Name: Tx_FIFO2_Idle_Drop_Count

Address:0x4EA65

***Table 1380* • Tx FIFO2 Idle Drop Count**

Bit	Name	Access	Description	Default
15:0	Tx_FIFO2_idle_group_drop_count	R/O	Idle group count dropped in Tx FIFO2 for 10G host clock rate compensating in the chip's egress data path. The counter saturates when the maximum value is exceeded. The counter is cleared when the register is read.	0x0000

2.17.2 Data Path Control

2.17.2.1 Data Path Control

Short Name: Datapath_Control

Address:0x4EA70

Table 1381 **• Data Path Control**

Bit	Name	Access	Description	Default
8	EGR_XGMII_PG_SEL	R/W	Selects source of data transmitted from PG_MUXA 0: Data is from client-side 1G/10G PCS 1: Data is from Pattern Generator	0x0
7	IGR_XGMII_PG_SEL	R/W	Selects source of data transmitted from PG_MUXB 0: Data is from PG_MUXC in the ingress data path 1: Data is from Pattern Generator	0x0
6	IGR_XGMII_PG_SEL2	R/W	Selects source of data transmitted from PG_MUXC. This mux is intended to be used to route data to the packet BIST monitor. This mux may not be used as a host-side loopback (i.e. Host-side data input looped back to host-side data output). 0: Data is from ingress data path 1: Data is from PG_MUXA in the egress data path	0x0
1	LOOP_L2C_ENA	R/W	Line-side/Network Loopback L2C Enable. Loopback L2C is: 0: Disabled 1: Enabled	0x0
0	LOOP_L2_ENA	R/W	Line-side/Network Loopback L2 Enable. Loopback L2 is: 0: Disabled 1: Enabled	0x0

2.18 LINE_KR_DEV7 (Device 0x7)

Table 1382 **• KR_7x0000**

Address	Short Description	Register Name	Details
0x70000	AN Control	KR_7x0000	Page 488

Table 1383 **• KR_7x0001**

Address	Short Description	Register Name	Details
0x70001	AN Status	KR_7x0001	Page 489

Table 1384 • **LD_adv**

Address	Short Description	Register Name	Details
0x70010	LD Advertised Abilities 15-0	KR_7x0010	Page 489
0x70011	LD Advertised Abilities 31-16	KR_7x0011	Page 489
0x70012	LD Advertised Abilities 47-32	KR_7x0012	Page 489

Table 1385 • **LP_base_page_0**

Address	Short Description	Register Name	Details
0x70013	LP Base Page Advertised Abilities 15-0	KR_7x0013	Page 490

Table 1386 • **LP_base_page_1**

Address	Short Description	Register Name	Details
0x70014	LP Base Page Advertised Abilities 31-16	KR_7x0014	Page 490

Table 1387 • **LP_base_page_2**

Address	Short Description	Register Name	Details
0x70015	LP Base Page Advertised Abilities 47-32	KR_7x0015	Page 490

Table 1388 • **LD_next_page**

Address	Short Description	Register Name	Details
0x70016	NxtPg Transmit 15-0	KR_7x0016	Page 490
0x70017	NxtPg Transmit 31-16	KR_7x0017	Page 490
0x70018	NxtPg Transmit 47-32	KR_7x0018	Page 491

Table 1389 • **LP_next_page**

Address	Short Description	Register Name	Details
0x70019	LP Next Page Ability 15-0	KR_7x0019	Page 491
0x7001A	LP Next Page Ability 31-16	KR_7x001A	Page 491
0x7001B	LP Next Page Ability 47-32	KR_7x001B	Page 491

Table 1390 • **KR_7x0030**

Address	Short Description	Register Name	Details
0x70030	Backplane Ethernet Status	KR_7x0030	Page 491

Table 1391 • **an_cfg0**

Address	Short Description	Register Name	Details
0x78000	VS AN Config 0	an_cfg0	Page 492

Table 1392 • **bl_tmr**

Address	Short Description	Register Name	Details
0x78010	VS AN break_link Timer LSW	bl_lsw	Page 492
0x78011	VS AN break_link Timer MSW	bl_msw	Page 492

Table 1393 • **aw_tmr**

Address	Short Description	Register Name	Details
0x78020	VS AN aneg_wait Timer LSW	aw_lsw	Page 493
0x78021	VS AN aneg_wait Timer MSW	aw_msw	Page 493

Table 1394 • **lflong_tmr**

Address	Short Description	Register Name	Details
0x78030	VS AN link_fail_inhibit Timer LSW	lflong_lsw	Page 493
0x78031	VS AN link_fail_inhibit_long Timer MSW	lflong_msw	Page 493

Table 1395 • **lfshort_tmr**

Address	Short Description	Register Name	Details
0x78040	VS AN link_fail_inhibit_short Timer LSW	lfshort_lsw	Page 493
0x78041	VS AN link_fail_inhibit_short Timer MSW	lfshort_msw	Page 493

Table 1396 • **lp_tmr**

Address	Short Description	Register Name	Details
0x78042	VS AN link_pass_inhibit Timer LSW	lp_lsw	Page 494
0x78043	VS AN link_pass_inhibit Timer MSW	lp_msw	Page 494

Table 1397 • **tr_tmr**

Address	Short Description	Register Name	Details
0x78044	VS AN Training State Timer LSW	tr_lsw	Page 494
0x78045	VS AN Training State Timer MSW	tr_msw	Page 494

Table 1398 • **pd_tmr**

Address	Short Description	Register Name	Details
0x78050	VS AN page_detect Timer LSW	pd_lsw	Page 494
0x78051	VS AN page_detect Timer MSW	pd_msw	Page 495

Table 1399 • **kr10g_tmr**

Address	Short Description	Register Name	Details
0x78060	VS AN rate_detect_10g Timer LSW	kr10g_lsw	Page 495
0x78061	VS AN rate_detect_10g Timer MSW	kr10g_msw	Page 495

Table 1400 • **kr3g_tmr**

Address	Short Description	Register Name	Details
0x78070	VS AN rate_detect_3g Timer LSW	kr3g_lsw	Page 495
0x78071	VS AN rate_detect_3g Timer MSW	kr3g_msw	Page 495

Table 1401 • **kr1g_tmr**

Address	Short Description	Register Name	Details
0x78080	VS AN rate_detect_1g Timer LSW	kr1g_lsw	Page 496
0x78081	VS AN rate_detect_1g Timer MSW	kr1g_msw	Page 496

Table 1402 • **an_hist**

Address	Short Description	Register Name	Details
0x78090	VS AN Arb State Mach History	an_hist	Page 496

Table 1403 • **an_sm**

Address	Short Description	Register Name	Details
0x780A0	VS AN arb state machine	an_sm	Page 496

Table 1404 • **an_sts0**

Address	Short Description	Register Name	Details
0x780B0	VS AN Status 0	an_sts0	Page 496

2.18.0.1 AN Control

Short Name:KR_7x0000

Address:0x70000

Table 1405 **• AN Control**

Bit	Name	Access	Description	Default
15	an_reset	R/W	AN reset (SC)	0x0
13	npctl	R/W	Extended next page control	0x0
12	an_enable	R/W	AN enable	0x0
9	an_restart	R/W	AN restart (SC)	0x0

2.18.0.2 AN Status

Short Name:KR_7x0001

Address:0x70001

Table 1406 **• AN Status**

Bit	Name	Access	Description	Default
9	pardetflt	R/O	Parallel detection fault (LH)	N/A
7	npstat	R/O	Extended next page status	N/A
6	pg_rcvd	R/O	Page received (LH)	N/A
5	an_complete	R/O	AN complete	N/A
4	rem_flt	R/O	Remote fault (LH)	N/A
3	an_able	R/O	AN ability	0x1
2	linkstat	R/O	Link status (LL)	N/A
0	an_lp_able	R/O	LP AN ability	N/A

2.18.0.3 LD Advertised Abilities 15-0

Short Name:KR_7x0010

Address:0x70010

Table 1407 **• LD Advertised Abilities 15-0**

Bit	Name	Access	Description	Default
15:0	adv0	R/W	Local advertised abilities D[15:0]	0x0000

2.18.0.4 LD Advertised Abilities 31-16

Short Name:KR_7x0011

Address:0x70011

Table 1408 **• LD Advertised Abilities 31-16**

Bit	Name	Access	Description	Default
15:0	adv1	R/W	Local advertised abilities D[31:16]	0x0000

2.18.0.5 LD Advertised Abilities 47-32

Short Name:KR_7x0012

Address:0x70012

Table 1409 **• LD advertised abilities 47-32**

Bit	Name	Access	Description	Default
15:0	adv2	R/W	Local advertised abilities D[47:32]	0x0000

2.18.0.6 LP Base Page Advertised Abilities 15-0

Short Name:KR_7x0013

Address:0x70013

Table 1410 **• LP Base Page Advertised Abilities 15-0**

Bit	Name	Access	Description	Default
15:0	lp_bp_adv0	R/O	LP advertised abilities D[15:0]	N/A

2.18.0.7 LP Base Page Advertised Abilities 31-16

Short Name:KR_7x0014

Address:0x70014

Table 1411 **• LP Base Page Advertised Abilities 31-16**

Bit	Name	Access	Description	Default
15:0	lp_bp_adv1	R/O	LP advertised abilities D[31:16]	N/A

2.18.0.8 LP Base Page Advertised Abilities 47-32

Short Name:KR_7x0015

Address:0x70015

Table 1412 **• LP Base Page Advertised Abilities 47-32**

Bit	Name	Access	Description	Default
15:0	lp_bp_adv2	R/O	LP advertised abilities D[47:32]	N/A

2.18.0.9 NxtPg Transmit 15-0

Short Name:KR_7x0016

Address:0x70016

Table 1413 **• NxtPg Transmit 15-0**

Bit	Name	Access	Description	Default
15:0	np_tx0	R/W	Next page to transmit D[15:0]	0x0000

2.18.0.10 NxtPg Transmit 31-16

Short Name:KR_7x0017

Address:0x70017

Table 1414 **• NxtPg Transmit 31-16**

Bit	Name	Access	Description	Default
15:0	np_tx1	R/W	Next page to transmit D[31:16]	0x0000

2.18.0.11 NxtPg Transmit 47-32

Short Name:KR_7x0018

Address:0x70018

Table 1415 **• NxtPg Transmit 47-32**

Bit	Name	Access	Description	Default
15:0	np_tx2	R/W	Next page to transmit D[47:32]	0x0000

2.18.0.12 LP Next Page Ability 15-0

Short Name:KR_7x0019

Address:0x70019

Table 1416 **• LP Next Page Ability 15-0**

Bit	Name	Access	Description	Default
15:0	lp_np_adv0	R/O	LP next page ability D[15:0]	N/A

2.18.0.13 LP Next Page Ability 31-16

Short Name:KR_7x001A

Address:0x7001A

Table 1417 **• LP Next Page Ability 31-16**

Bit	Name	Access	Description	Default
15:0	lp_np_adv1	R/O	LP next page ability D[31:16]	N/A

2.18.0.14 LP Next Page Ability 47-32

Short Name:KR_7x001B

Address:0x7001B

Table 1418 **• LP Next Page Ability 47-32**

Bit	Name	Access	Description	Default
15:0	lp_np_adv2	R/O	LP next page ability D[47:32]	N/A

2.18.0.15 Backplane Ethernet Status

Short Name:KR_7x0030

Address:0x70030

***Table 1419* • Backplane Ethernet Status**

Bit	Name	Access	Description	Default
8	an_neg_cr10	R/O	10G CR10 negotiated	0x0
6	an_neg_cr4	R/O	10G CR4 negotiated	0x0
5	an_neg_kr4	R/O	10G KR4 negotiated	0x0
4	an_neg_fec	R/O	10G KR FEC negotiated	0x0
3	an_neg_kr	R/O	10G KR negotiated	0x0
2	an_neg_kx4	R/O	10G KX4 negotiated	0x0
1	an_neg_kx	R/O	1G KX negotiated	0x0
0	an_bp_able	R/O	BP AN ability	0x1

2.18.0.16 VS AN Config 0

Short Name:an_cfg0

Address:0x78000

***Table 1420* • VS AN Config 0**

Bit	Name	Access	Description	Default
5	an_sm_hist_clr	R/W	Clear AN state machine history	0x0
4	clkg_disable	R/W	Disable clock gating	0x0
3	tr_disable	R/W	Bypass training if 10G negotiated	0x0
2	sync10g_sel	R/W	Select source of 10G sync signal 0: KR internal 1: External	0x0
1	sync8b10b_sel	R/W	Select source of 3G and 1G sync signal 0: KR internal 1: External	0x0

2.18.0.17 VS AN break_link Timer LSW

Short Name:bl_lsw

Address:0x78010

***Table 1421* • VS AN break_link Timer LSW**

Bit	Name	Access	Description	Default
15:0	bl_tmr_lsw	R/W	break_link_timer setting	0xD6AF

2.18.0.18 VS AN break_link Timer MSW

Short Name:bl_msw

Address:0x78011

***Table 1422* • VS AN break_link Timer MSW**

Bit	Name	Access	Description	Default
15:0	bl_tmr_msw	R/W	break_link_timer setting	0x0029

2.18.0.19 VS AN aneg_wait Timer LSW

Short Name:aw_lsw

Address:0x78020

***Table 1423* • VS AN aneg_wait Timer LSW**

Bit	Name	Access	Description	Default
15:0	aw_tmr_lsw	R/W	an_wait_timer setting	0xC3DF

2.18.0.20 VS AN aneg_wait Timer MSW

Short Name:aw_msw

Address:0x78021

***Table 1424* • VS AN aneg_wait Timer MSW**

Bit	Name	Access	Description	Default
15:0	aw_tmr_msw	R/W	an_wait_timer setting	0x0016

2.18.0.21 VS AN link_fail_inhibit Timer LSW

Short Name:lflong_lsw

Address:0x78030

***Table 1425* • VS AN link_fail_inhibit Timer LSW**

Bit	Name	Access	Description	Default
15:0	lflong_tmr_lsw	R/W	10g link_fail_inhibit_timer setting	0x00E2

2.18.0.22 VS AN link_fail_inhibit_long Timer MSW

Short Name:lflong_msw

Address:0x78031

***Table 1426* • VS AN link_fail_inhibit_long Timer MSW**

Bit	Name	Access	Description	Default
15:0	lflong_tmr_msw	R/W	10g link_fail_inhibit_timer setting	0x012D

2.18.0.23 VS AN link_fail_inhibit_short Timer LSW

Short Name:lfshort_lsw

Address:0x78040

***Table 1427* • VS AN link_fail_inhibit_short Timer LSW**

Bit	Name	Access	Description	Default
15:0	lfshort_tmr_lsw	R/W	1g link_fail_inhibit_timer setting	0xAFF4

2.18.0.24 VS AN link_fail_inhibit_short Timer MSW

Short Name:lfshort_msw

Address:0x78041

***Table 1428* • VS AN link_fail_inhibit_short Timer MSW**

Bit	Name	Access	Description	Default
15:0	lfshort_tmr_msw	R/W	1g link_fail_inhibit_timer setting	0x001B

2.18.0.25 VS AN link_pass_inhibit Timer LSW

Short Name:lp_lsw

Address:0x78042

***Table 1429* • VS AN link_pass_inhibit Timer LSW**

Bit	Name	Access	Description	Default
15:0	lp_tmr_lsw	R/W	link_pass_inhibit_timer setting	0x0000

2.18.0.26 VS AN link_pass_inhibit Timer MSW

Short Name:lp_msw

Address:0x78043

***Table 1430* • VS AN link_pass_inhibit Timer MSW**

Bit	Name	Access	Description	Default
15:0	lp_tmr_msw	R/W	link_pass_inhibit_timer setting	0x0000

2.18.0.27 VS AN training state Timer LSW

Short Name:tr_lsw

Address:0x78044

***Table 1431* • VS AN training state Timer LSW**

Bit	Name	Access	Description	Default
15:0	tr_tmr_lsw	R/W	training_state_timer setting	0x00E2

2.18.0.28 VS AN training state Timer MSW

Short Name:tr_msw

Address:0x78045

***Table 1432* • VS AN training state Timer MSW**

Bit	Name	Access	Description	Default
15:0	tr_tmr_msw	R/W	training_state_timer setting	0x012D

2.18.0.29 VS AN page_detect Timer LSW

Short Name:pd_lsw

Address:0x78050

***Table 1433* • VS AN page_detect Timer LSW**

Bit	Name	Access	Description	Default
15:0	pd_tmr_lsw	R/W	page_detect_timer setting	0x00E2

2.18.0.30 VS AN page_detect Timer MSW

Short Name:pd_msw

Address:0x78051

***Table 1434* • VS AN page_detect Timer MSW**

Bit	Name	Access	Description	Default
15:0	pd_tmr_msw	R/W	page_detect_timer setting	0x012D

2.18.0.31 VS AN rate_detect_10g Timer LSW

Short Name:kr10g_lsw

Address:0x78060

***Table 1435* • VS AN rate_detect_10g Timer LSW**

Bit	Name	Access	Description	Default
15:0	kr10g_tmr_lsw	R/W	rate_detect_10g_timer setting	0x1A80

2.18.0.32 VS AN rate_detect_10g Timer MSW

Short Name:kr10g_msw

Address:0x78061

***Table 1436* • VS AN rate_detect_10g Timer MSW**

Bit	Name	Access	Description	Default
15:0	kr10g_tmr_msw	R/W	rate_detect_10g_timer setting	0x0006

2.18.0.33 VS AN rate_detect_3g Timer LSW

Short Name:kr3g_lsw

Address:0x78070

***Table 1437* • VS AN rate_detect_3g Timer LSW**

Bit	Name	Access	Description	Default
15:0	kr3g_tmr_lsw	R/W	rate_detect_3g_timer setting	0x1A80

2.18.0.34 VS AN rate_detect_3g Timer MSW

Short Name:kr3g_msw

Address:0x78071

Table 1438 **• VS AN rate_detect_3g Timer MSW**

Bit	Name	Access	Description	Default
15:0	kr3g_tmr_msw	R/W	rate_detect_3g_timer setting	0x0006

2.18.0.35 VS AN rate_detect_1g Timer LSW

Short Name:kr1g_lsw

Address:0x78080

Table 1439 **• VS AN rate_detect_1g Timer LSW**

Bit	Name	Access	Description	Default
15:0	kr1g_tmr_lsw	R/W	rate_detect_1g_timer setting	0x1A80

2.18.0.36 VS AN rate_detect_1g Timer MSW

Short Name:kr1g_msw

Address:0x78081

Table 1440 **• VS AN rate_detect_1g Timer MSW**

Bit	Name	Access	Description	Default
15:0	kr1g_tmr_msw	R/W	rate_detect_1g_timer setting	0x0006

2.18.0.37 VS AN Arb State Mach History

Short Name:an_hist

Address:0x78090

Table 1441 **• VS AN Arb State Mach History**

Bit	Name	Access	Description	Default
14:0	an_sm_hist	R/O	AN state machine history	0x0000

2.18.0.38 VS AN Arb State Machine

Short Name:an_sm

Address:0x780A0

Table 1442 **• VS AN Arb State Machine**

Bit	Name	Access	Description	Default
3:0	an_sm	R/O	AN state machine	N/A

2.18.0.39 VS AN Status 0

Short Name:an_sts0

Address:0x780B0

Table 1443 **• VS AN Status 0**

Bit	Name	Access	Description	Default
10	sync8b10b	R/O	1G or 3G sync status of local detector	N/A
9	sync10g	R/O	10G sync status of local detector	N/A
8	nonce_match	R/O	Nonce match (LH)	N/A
7	incp_link	R/O	Incompatible link (LH)	N/A
6:4	link_hcd	R/O	Negotiated HCD 0: KX_1G 1: KX4_10G 2: KR_10G 3: KR4_40G 4: CR4_40G 5: CR10_100G	N/A
3:2	link_ctl	R/O	AN link_control variable 0: ENABLE 1: DISABLE 2: SCAN_FOR_CARRIER	N/A
1:0	line_rate	R/O	speed setting 0: 10G 1: 1G 2: 3G	N/A

2.19 HOST_KR_DEV7 (Device 0xF)

Table 1444 **• KR_7x0000**

Address	Short Description	Register Name	Details
0xF0000	AN Control	KR_7x0000	Page 500

Table 1445 **• KR_7x0001**

Address	Short Description	Register Name	Details
0xF0001	AN Status	KR_7x0001	Page 500

Table 1446 **• LD_adv**

Address	Short Description	Register Name	Details
0xF0010	LD Advertised Abilities 15-0	KR_7x0010	Page 501
0xF0011	LD Advertised Abilities 31-16	KR_7x0011	Page 501
0xF0012	LD Advertised Abilities 47-32	KR_7x0012	Page 501

Table 1447 • **LP_base_page_0**

Address	Short Description	Register Name	Details
0xF0013	LP Base Page Advertised Abilities 15-0	KR_7x0013	Page 501

Table 1448 • **LP_base_page_1**

Address	Short Description	Register Name	Details
0xF0014	LP Base Page Advertised Abilities 31-16	KR_7x0014	Page 501

Table 1449 • **LP_base_page_2**

Address	Short Description	Register Name	Details
0xF0015	LP Base Page Advertised Abilities 47-32	KR_7x0015	Page 502

Table 1450 • **LD_next_page**

Address	Short Description	Register Name	Details
0xF0016	NxtPg Transmit 15-0	KR_7x0016	Page 502
0xF0017	NxtPg Transmit 31-16	KR_7x0017	Page 502
0xF0018	NxtPg Transmit 47-32	KR_7x0018	Page 502

Table 1451 • **LP_next_page**

Address	Short Description	Register Name	Details
0xF0019	LP Next Page Ability 15-0	KR_7x0019	Page 502
0xF001A	LP Next Page Ability 31-16	KR_7x001A	Page 503
0xF001B	LP Next Page Ability 47-32	KR_7x001B	Page 503

Table 1452 • **KR_7x0030**

Address	Short Description	Register Name	Details
0xF0030	Backplane Ethernet Status	KR_7x0030	Page 503

Table 1453 • **an_cfg0**

Address	Short Description	Register Name	Details
0xF8000	VS AN Config 0	an_cfg0	Page 503

Table 1454 • **bl_tmr**

Address	Short Description	Register Name	Details
0xF8010	VS AN break_link Timer LSW	bl_lsw	Page 504
0xF8011	VS AN break_link Timer MSW	bl_msw	Page 504

Table 1455 • **aw_tmr**

Address	Short Description	Register Name	Details
0xF8020	VS AN aneg_wait Timer LSW	aw_lsw	Page 504
0xF8021	VS AN aneg_wait Timer MSW	aw_msw	Page 504

Table 1456 • **lflong_tmr**

Address	Short Description	Register Name	Details
0xF8030	VS AN link_fail_inhibit Timer LSW	lflong_lsw	Page 504
0xF8031	VS AN link_fail_inhibit_long Timer MSW	lflong_msw	Page 505

Table 1457 • **lfshort_tmr**

Address	Short Description	Register Name	Details
0xF8040	VS AN link_fail_inhibit_short Timer LSW	lfshort_lsw	Page 505
0xF8041	VS AN link_fail_inhibit_short Timer MSW	lfshort_msw	Page 505

Table 1458 • **lp_tmr**

Address	Short Description	Register Name	Details
0xF8042	VS AN link_pass_inhibit Timer LSW	lp_lsw	Page 505
0xF8043	VS AN link_pass_inhibit Timer MSW	lp_msw	Page 505

Table 1459 • **tr_tmr**

Address	Short Description	Register Name	Details
0xF8044	VS AN Training State Timer LSW	tr_lsw	Page 506
0xF8045	VS AN Training State Timer MSW	tr_msw	Page 506

Table 1460 • **pd_tmr**

Address	Short Description	Register Name	Details
0xF8050	VS AN page_detect Timer LSW	pd_lsw	Page 506
0xF8051	VS AN page_detect Timer MSW	pd_msw	Page 506

Table 1461 • **kr10g_tmr**

Address	Short Description	Register Name	Details
0xF8060	VS AN rate_detect_10g Timer LSW	kr10g_lsw	Page 506
0xF8061	VS AN rate_detect_10g Timer MSW	kr10g_msw	Page 507

Table 1462 • **kr3g_tmr**

Address	Short Description	Register Name	Details
0xF8070	VS AN rate_detect_3g Timer LSW	kr3g_lsw	Page 507
0xF8071	VS AN rate_detect_3g Timer MSW	kr3g_msw	Page 507

Table 1463 • **kr1g_tmr**

Address	Short Description	Register Name	Details
0xF8080	VS AN rate_detect_1g Timer LSW	kr1g_lsw	Page 507
0xF8081	VS AN rate_detect_1g Timer MSW	kr1g_msw	Page 507

Table 1464 • **an_hist**

Address	Short Description	Register Name	Details
0xF8090	VS AN Arb State Mach History	an_hist	Page 508

Table 1465 • **an_sm**

Address	Short Description	Register Name	Details
0xF80A0	VS AN Arb State Machine	an_sm	Page 508

Table 1466 • **an_sts0**

Address	Short Description	Register Name	Details
0xF80B0	VS AN Status 0	an_sts0	Page 508

2.19.0.1 AN Control

Short Name:KR_7x0000

Address:0xF0000

Table 1467 • **AN control**

Bit	Name	Access	Description	Default
15	an_reset	R/W	AN reset (SC)	0x0
13	npctl	R/W	Extended next page control	0x0
12	an_enable	R/W	AN enable	0x0
9	an_restart	R/W	AN restart (SC)	0x0

2.19.0.2 AN Status

Short Name:KR_7x0001

Address:0xF0001

Table 1468 • **AN Status**

Bit	Name	Access	Description	Default
9	pardetflt	R/O	Parallel detection fault (LH)	N/A

Table 1468 • **AN Status *(continued)***

Bit	Name	Access	Description	Default
7	npstat	R/O	Extended next page status	N/A
6	pg_rcvd	R/O	Page received (LH)	N/A
5	an_complete	R/O	AN complete	N/A
4	rem_flt	R/O	Remote fault (LH)	N/A
3	an_able	R/O	AN ability	0x1
2	linkstat	R/O	Link status (LL)	N/A
0	an_lp_able	R/O	LP AN ability	N/A

2.19.0.3 LD Advertised Abilities 15-0

Short Name:KR_7x0010

Address:0xF0010

Table 1469 • **LD Advertised Abilities 15-0**

Bit	Name	Access	Description	Default
15:0	adv0	R/W	Local advertised abilities D[15:0]	0x0000

2.19.0.4 LD Advertised Abilities 31-16

Short Name:KR_7x0011

Address:0xF0011

Table 1470 • **LD Advertised Abilities 31-16**

Bit	Name	Access	Description	Default
15:0	adv1	R/W	Local advertised abilities D[31:16]	0x0000

2.19.0.5 LD Advertised Abilities 47-32

Short Name:KR_7x0012

Address:0xF0012

Table 1471 • **LD Advertised Abilities 47-32**

Bit	Name	Access	Description	Default
15:0	adv2	R/W	Local advertised abilities D[47:32]	0x0000

2.19.0.6 LP Base Page Advertised Abilities 15-0

Short Name:KR_7x0013

Address:0xF0013

Table 1472 • **LP Base Page Advertised Abilities 15-0**

Bit	Name	Access	Description	Default
15:0	lp_bp_adv0	R/O	LP advertised abilities D[15:0]	N/A

2.19.0.7 LP Base Page Advertised Abilities 31-16

Short Name:KR_7x0014

Address:0xF0014

Table 1473 **• LP Base Page Advertised Abilities 31-16**

Bit	Name	Access	Description	Default
15:0	lp_bp_adv1	R/O	LP advertised abilities D[31:16]	N/A

2.19.0.8 LP Base Page Advertised Abilities 47-32

Short Name:KR_7x0015

Address:0xF0015

Table 1474 **• LP Base Page Advertised Abilities 47-32**

Bit	Name	Access	Description	Default
15:0	lp_bp_adv2	R/O	LP advertised abilities D[47:32]	N/A

2.19.0.9 NxtPg Transmit 15-0

Short Name:KR_7x0016

Address:0xF0016

Table 1475 **• NxtPg Transmit 15-0**

Bit	Name	Access	Description	Default
15:0	np_tx0	R/W	Next page to transmit D[15:0]	0x0000

2.19.0.10 NxtPg Transmit 31-16

Short Name:KR_7x0017

Address:0xF0017

Table 1476 **• NxtPg Transmit 31-16**

Bit	Name	Access	Description	Default
15:0	np_tx1	R/W	Next page to transmit D[31:16]	0x0000

2.19.0.11 NxtPg Transmit 47-32

Short Name:KR_7x0018

Address:0xF0018

Table 1477 **• NxtPg Transmit 47-32**

Bit	Name	Access	Description	Default
15:0	np_tx2	R/W	Next page to transmit D[47:32]	0x0000

2.19.0.12 LP Next Page Ability 15-0

Short Name:KR_7x0019

Address:0xF0019

Table 1478 **• LP Next Page Ability 15-0**

Bit	Name	Access	Description	Default
15:0	lp_np_adv0	R/O	LP next page ability D[15:0]	N/A

2.19.0.13 LP Next Page Ability 31-16

Short Name:KR_7x001A

Address:0xF001A

Table 1479 **• LP Next Page Ability 31-16**

Bit	Name	Access	Description	Default
15:0	lp_np_adv1	R/O	LP next page ability D[31:16]	N/A

2.19.0.14 LP Next Page Ability 47-32

Short Name:KR_7x001B

Address:0xF001B

Table 1480 **• LP Next Page Ability 47-32**

Bit	Name	Access	Description	Default
15:0	lp_np_adv2	R/O	LP next page ability D[47:32]	N/A

2.19.0.15 Backplane Ethernet Status

Short Name:KR_7x0030

Address:0xF0030

Table 1481 **• Backplane Ethernet Status**

Bit	Name	Access	Description	Default
8	an_neg_cr10	R/O	10G CR10 negotiated	0x0
6	an_neg_cr4	R/O	10G CR4 negotiated	0x0
5	an_neg_kr4	R/O	10G KR4 negotiated	0x0
4	an_neg_fec	R/O	10G KR FEC negotiated	0x0
3	an_neg_kr	R/O	10G KR negotiated	0x0
2	an_neg_kx4	R/O	10G KX4 negotiated	0x0
1	an_neg_kx	R/O	1G KX negotiated	0x0
0	an_bp_able	R/O	BP AN ability	0x1

2.19.0.16 VS AN Config 0

Short Name:an_cfg0

Address:0xF8000

Table 1482 **• VS AN Config 0**

Bit	Name	Access	Description	Default
5	an_sm_hist_clr	R/W	Clear AN state machine history	0x0

Table 1482 • **VS AN Config 0** ***(continued)***

Bit	Name	Access	Description	Default
4	clkg_disable	R/W	Disable clock gating	0x0
3	tr_disable	R/W	Bypass training if 10G negotiated	0x0
2	sync10g_sel	R/W	Select source of 10G sync signal 0: KR internal 1: External	0x0
1	sync8b10b_sel	R/W	Select source of 3G and 1G sync signal 0: KR internal 1: External	0x0

2.19.0.17 VS AN break_link Timer LSW

Short Name:bl_lsw

Address:0xF8010

Table 1483 • **VS AN break_link Timer LSW**

Bit	Name	Access	Description	Default
15:0	bl_tmr_lsw	R/W	break_link_timer setting	0xD6AF

2.19.0.18 VS AN break_link Timer MSW

Short Name:bl_msw

Address:0xF8011

Table 1484 • **VS AN break_link Timer MSW**

Bit	Name	Access	Description	Default
15:0	bl_tmr_msw	R/W	break_link_timer setting	0x0029

2.19.0.19 VS AN aneg_wait Timer LSW

Short Name:aw_lsw

Address:0xF8020

Table 1485 • **VS AN aneg_wait Timer LSW**

Bit	Name	Access	Description	Default
15:0	aw_tmr_lsw	R/W	an_wait_timer setting	0xC3DF

2.19.0.20 VS AN aneg_wait Timer MSW

Short Name:aw_msw

Address:0xF8021

Table 1486 • **VS AN aneg_wait Timer MSW**

Bit	Name	Access	Description	Default
15:0	aw_tmr_msw	R/W	an_wait_timer setting	0x0016

2.19.0.21 VS AN link_fail_inhibit Timer LSW

Short Name:lflong_lsw

Address:0xF8030

Table 1487 • **VS AN link_fail_inhibit Timer LSW**

Bit	Name	Access	Description	Default
15:0	lflong_tmr_lsw	R/W	10g link_fail_inhibit_timer setting	0x00E2

2.19.0.22 VS AN link_fail_inhibit_long Timer MSW

Short Name:lflong_msw

Address:0xF8031

Table 1488 • **VS AN link_fail_inhibit_long Timer MSW**

Bit	Name	Access	Description	Default
15:0	lflong_tmr_msw	R/W	10g link_fail_inhibit_timer setting	0x012D

2.19.0.23 VS AN link_fail_inhibit_short Timer LSW

Short Name:lfshort_lsw

Address:0xF8040

Table 1489 • **VS AN link_fail_inhibit_short Timer LSW**

Bit	Name	Access	Description	Default
15:0	lfshort_tmr_lsw	R/W	1g link_fail_inhibit_timer setting	0xAFF4

2.19.0.24 VS AN link_fail_inhibit_short Timer MSW

Short Name:lfshort_msw

Address:0xF8041

Table 1490 • **VS AN link_fail_inhibit_short Timer MSW**

Bit	Name	Access	Description	Default
15:0	lfshort_tmr_msw	R/W	1g link_fail_inhibit_timer setting	0x001B

2.19.0.25 VS AN link_pass_inhibit Timer LSW

Short Name:lp_lsw

Address:0xF8042

Table 1491 • **VS AN link_pass_inhibit Timer LSW**

Bit	Name	Access	Description	Default
15:0	lp_tmr_lsw	R/W	link_pass_inhibit_timer setting	0x0000

2.19.0.26 VS AN link_pass_inhibit Timer MSW

Short Name:lp_msw

Address:0xF8043

Table 1492 **• VS AN link_pass_inhibit Timer MSW**

Bit	Name	Access	Description	Default
15:0	lp_tmr_msw	R/W	link_pass_inhibit_timer setting	0x0000

2.19.0.27 VS AN training state Timer LSW

Short Name:tr_lsw

Address:0xF8044

Table 1493 **• VS AN training state Timer LSW**

Bit	Name	Access	Description	Default
15:0	tr_tmr_lsw	R/W	training_state_timer setting	0x00E2

2.19.0.28 VS AN training state Timer MSW

Short Name:tr_msw

Address:0xF8045

Table 1494 **• VS AN training state Timer MSW**

Bit	Name	Access	Description	Default
15:0	tr_tmr_msw	R/W	training_state_timer setting	0x012D

2.19.0.29 VS AN page_detect Timer LSW

Short Name:pd_lsw

Address:0xF8050

Table 1495 **• VS AN page_detect Timer LSW**

Bit	Name	Access	Description	Default
15:0	pd_tmr_lsw	R/W	page_detect_timer setting	0x00E2

2.19.0.30 VS AN page_detect Timer MSW

Short Name:pd_msw

Address:0xF8051

Table 1496 **• VS AN page_detect Timer MSW**

Bit	Name	Access	Description	Default
15:0	pd_tmr_msw	R/W	page_detect_timer setting	0x012D

2.19.0.31 VS AN rate_detect_10g Timer LSW

Short Name:kr10g_lsw

Address:0xF8060

***Table 1497* • VS AN rate_detect_10g Timer LSW**

Bit	Name	Access	Description	Default
15:0	kr10g_tmr_lsw	R/W	rate_detect_10g_timer setting	0x1A80

2.19.0.32 VS AN rate_detect_10g Timer MSW

Short Name:kr10g_msw

Address:0xF8061

***Table 1498* • VS AN rate_detect_10g Timer MSW**

Bit	Name	Access	Description	Default
15:0	kr10g_tmr_msw	R/W	rate_detect_10g_timer setting	0x0006

2.19.0.33 VS AN rate_detect_3g Timer LSW

Short Name:kr3g_lsw

Address:0xF8070

***Table 1499* • VS AN rate_detect_3g Timer LSW**

Bit	Name	Access	Description	Default
15:0	kr3g_tmr_lsw	R/W	rate_detect_3g_timer setting	0x1A80

2.19.0.34 VS AN rate_detect_3g Timer MSW

Short Name:kr3g_msw

Address:0xF8071

***Table 1500* • VS AN rate_detect_3g Timer MSW**

Bit	Name	Access	Description	Default
15:0	kr3g_tmr_msw	R/W	rate_detect_3g_timer setting	0x0006

2.19.0.35 VS AN rate_detect_1g Timer LSW

Short Name:kr1g_lsw

Address:0xF8080

***Table 1501* • VS AN rate_detect_1g Timer LSW**

Bit	Name	Access	Description	Default
15:0	kr1g_tmr_lsw	R/W	rate_detect_1g_timer setting	0x1A80

2.19.0.36 VS AN rate_detect_1g Timer MSW

Short Name:kr1g_msw

Address:0xF8081

***Table 1502* • VS AN rate_detect_1g Timer MSW**

Bit	Name	Access	Description	Default
15:0	kr1g_tmr_msw	R/W	rate_detect_1g_timer setting	0x0006

2.19.0.37 VS AN Arb State Mach History

Short Name:an_hist

Address:0xF8090

***Table 1503* • VS AN Arb State Mach History**

Bit	Name	Access	Description	Default
14:0	an_sm_hist	R/O	AN state machine history	0x0000

2.19.0.38 VS AN Arb State Machine

Short Name:an_sm

Address:0xF80A0

***Table 1504* • VS AN Arb State Machine**

Bit	Name	Access	Description	Default
3:0	an_sm	R/O	AN state machine	N/A

2.19.0.39 VS AN Status 0

Short Name:an_sts0

Address:0xF80B0

***Table 1505* • VS AN Status 0**

Bit	Name	Access	Description	Default
10	sync8b10b	R/O	1G or 3G sync status of local detector	N/A
9	sync10g	R/O	10G sync status of local detector	N/A
8	nonce_match	R/O	Nonce match (LH)	N/A
7	incp_link	R/O	Incompatible link (LH)	N/A
6:4	link_hcd	R/O	Negotiated HCD 0: KX_1G 1: KX4_10G 2: KR_10G 3: KR4_40G 4: CR4_40G 5: CR10_100G	N/A
3:2	link_ctl	R/O	AN link_control variable 0: ENABLE 1: DISABLE 2: SCAN_FOR_CARRIER	N/A
1:0	line_rate	R/O	speed setting 0: 10G 1: 1G 2: 3G	N/A

2.20 GLOBAL (Device 0x1E)

Table 1506 • **Device_Info**

Address	Short Description	Register Name	Details
0x1E0000	Device ID	Device_ID	Page 510
0x1E0001	Device Revision	Device_Revision	Page 510

Table 1507 • **Block_Level_Software_Reset**

Address	Short Description	Register Name	Details
0x1E0002	Block Level Software Reset	Block_Level_Software_Reset	Page 510

Table 1508 • **Pin_Status**

Address	Short Description	Register Name	Details
0x1E0004	Pin Status	Pin_Status	Page 511

Table 1509 • **Temp_Monitor**

Address	Short Description	Register Name	Details
0x1E01C0	Temperature Monitor Threshold Settings	Temp_Mon_Threshold	Page 512
0x1E01C1	Temperature Monitor Registers	Temp_Mon_Regs	Page 512

Table 1510 • **FEATURE_STAT**

Address	Short Description	Register Name	Details
0x1E02A0	Device Feature Status	FEATURE_STAT	Page 513

Table 1511 • **SPI_CTRL**

Address	Short Description	Register Name	Details
0x1E02B0	SPI Mode Control	SPI_CTRL	Page 513

Table 1512 • **RNG**

Address	Short Description	Register Name	Details
0x1E02D1	Random Number Generator	RNG_REG	Page 514

Table 1513 • **RCOMP_STATUS**

Address	Short Description	Register Name	Details
0x1E7010	RCOMP Status	RCOMP_STATUS	Page 514

2.20.1 Device ID and Revision

Device ID and Revision

2.20.1.1 Device ID

Short Name: Device_ID

Address:0x1E0000

Table 1514 • **Device ID**

Bit	Name	Access	Description	Default
15:0	Device_ID	R/O	This is the device ID register. The die design is used in multiple product SKUs. It is impossible to assign a default part number here to support all SKUs simultaneously.	0x0000

2.20.1.2 Device Revision

Short Name: Device_Revision

Address:0x1E0001

Table 1515 • **Device Revision**

Bit	Name	Access	Description	Default
3:0	Device_Revision	R/O	This is the revision number register.	0x0

2.20.1.3 Block Level Software Reset

Short Name: Block_Level_Software_Reset

Address:0x1E0002

Table 1516 • **Block Level Software Reset**

Bit	Name	Access	Description	Default
11	Software_Reset_Channel_3	One-shot	Reset the datapath and configuration registers in channel 3. 0: Normal Operation 1: Reset	0x0
10	Software_Reset_Channel_2	One-shot	Reset the datapath and configuration registers in channel 2. 0: Normal Operation 1: Reset	0x0
9	Software_Reset_Channel_1	One-shot	Reset the datapath and configuration registers in channel 1. 0: Normal Operation 1: Reset	0x0

Table 1516 • **Block Level Software Reset *(continued)***

Bit	Name	Access	Description	Default
8	Software_Reset_Channel_0	One-shot	Reset the datapath and configuration registers in channel 0. 0: Normal Operation 1: Reset	0x0
7	Software_Reset_DF2F	One-shot	Reset the F2DF logic. 0: Normal Operation 1: Reset	0x0
6	Software_Reset_F2DF	One-shot	Reset the F2DF logic. 0: Normal Operation 1: Reset	0x0
5	Software_Reset_TWS_Slave	One-shot	Reset the TWS-slave interface. 0: Normal Operation 1: Reset	0x0
3	Software_Reset_MDIO	One-shot	Reset the MDIO interface. 0: Normal Operation 1: Reset	0x0
2	Software_Reset_SPI	One-shot	Reset the SPI interface. This is the SPI interface available to read and write any register, not the push-out SPI interface dedicated to extracting 1588 timestamp data. 0: Normal Operation 1: Reset	0x0
0	Software_Reset_Chip	One-shot	Reset the datapath in all channels and all configuration registers except the GPIO configuration registers (1ExF200-1ExF27F) and global configuration registers (1Ex0000-1Ex71FF). GPIO functions are not modified when using this software reset since the GPIO configuration registers are not reset to default settings. The global configuration registers are used to program RCOMP, host side PLL and line side PLL logic blocks. 0: Normal Operation 1: Reset	0x0

2.20.1.4 Pin Status

Short Name: Pin_Status

Address:0x1E0004

Table 1517 • **Pin Status**

Bit	Name	Access	Description	Default
3	MODE3_Pin_State	R/O	State of MODE3 pin 0: Logic low 1: Logic high	0x0
2	MODE2_Pin_State	R/O	State of MODE2 pin 0: Logic low 1: Logic high	0x0

Table 1517 • **Pin Status** ***(continued)***

Bit	Name	Access	Description	Default
1	MODE1_Pin_State	R/O	State of MODE1 pin 0: Logic low 1: Logic high	0x0
0	MODE0_Pin_State	R/O	State of MODE0 pin 0: Logic low 1: Logic high	0x0

2.20.2 Temperature Monitor

Temperature monitor configuration and status registers

2.20.2.1 Temperature Monitor Threshold

Short Name: Temp_Mon_Threshold

Address:0x1E01C0

Temperature Monitor Threshold Settings

Table 1518 • **Temperature Monitor Threshold**

Bit	Name	Access	Description	Default
15:8	High_Temp_Threshold_Setting	R/W	Determines trigger for high temp alarm	0x00
7:0	Low_Temp_Threshold_Setting	R/W	Determines trigger for low temp alarm	0xFF

2.20.2.2 Temperature Monitor

Short Name: Temp_Mon_Regs

Address:0x1E01C1

Temperature Monitor Registers

Table 1519 • **Temperature Monitor**

Bit	Name	Access	Description	Default
12	Enable_Digital_Temp_Monitor	R/W	Enables the temperature monitor block 0: Temperature Monitor Disable 1: Temperature Monitor Enable	0x0
11	Temp_Monitor_Run	R/W	Initiates the temperature sampling process 0: Temperature Monitor idles 1: Temperature Monitor starts sampling	0x0
10	Temp_Monitor_Done_Status	R/O	Temp Monitor Done Status 0: Temperature Monitor is not done sampling 1: Temperature Monitor is done sampling, data in Temp_Monitor_Reading is ready	0x0

Table 1519 • **Temperature Monitor**

Bit	Name	Access	Description	Default
9	High_Temp_Alarm	R/O	High Temperature Alarm Sets when the Temp_Monitor_Reading is lower than the value set in High_Temp_Threshold_Setting. Temp_Monitor_Reading[7:0] value is inversely proportional to Temperature 0: Alarm is not set 1: Alarm is set	0x0
8	Low_Temp_Alarm	R/O	Low Temperature Alarm Sets when the Temp_Monitor_Reading is higher than the value set in Low_Temp_Threshold_Setting. Temp_Monitor_Reading[7:0] value is inversely proportional to Temperature 0: Alarm is not set 1: Alarm is set	0x0
7:0	Temp_Monitor_Reading	R/O	Temperature Monitor Reading This is the digital reading of the temperature monitor. Value is not valid unless Temp_Monitor_Done_Status = 1	0x09

2.20.3 Device Feature Status

2.20.3.1 Device Feature Status

Short Name:FEATURE_STAT

Address:0x1E02A0

Table 1520 • **Device Feature Status**

Bit	Name	Access	Description	Default
3	IP1588_STAT	R/O	Indicates the status of 1588 availability on the device 0: 1588 may be used 1: 1588 is permanently disabled	0x0
2	MACSEC_STAT	R/O	Indicates the status of MACsec availability on the device 0: MACsec block may be used 1: MACsec block is permanently disabled	0x0
1	TIMESTAMP_ACC_STAT	R/O	Indicates the 1588 timestamp accuracy 0: 4ns 1: 8ns	0x1
0	MACSEC_KEY_STAT	R/O	Indicates the MACsec encryption key capability 0: 128/256-bit 1: 128-bit	0x1

2.20.4 SPI Mode Control

2.20.4.1 SPI Mode Control

Short Name:SPI_CTRL

Address:0x1E02B0

***Table 1521* • SPI Mode Control**

Bit	Name	Access	Description	Default
0	FAST_MODE	R/W	Set the SPI interface mode 0: Normal mode 1: Fast mode	0x0

2.20.5 Random Number Generator

2.20.5.1 Rando_Num_Gen

Short Name:RNG_REG

Address:0x1E02D1

***Table 1522* •**

Bit	Name	Access	Description	Default
15:0	RNDNUM	R/O	Random number	0x0000

2.20.6 RCOMP Status

Status register set for RCOMP.

2.20.6.1 RCOMP Status

Short Name:RCOMP_STATUS

Address:0x1E7010

***Table 1523* • RCOMP Status**

Bit	Name	Access	Description	Default
12	BUSY	R/O	Resistor comparison activity 0: resistor measurement finished or inactive 1: resistor measurement in progress	0x0
7	DELTA_ALERT	R/O	Alarm signal if rcomp isn't best choice anymore 0: inactive 1: active	0x0
3:0	RCOMP	R/O	Measured resistor value 0: maximum resistance value 15: minimum resistance value	0x8

2.21 CLK_CFG (Device 0x1E)

***Table 1524* • LINE_OB_CFG**

Address	Short Description	Register Name	Details
0x1E7200	IDDQ enable for all line side clock output drivers	LINE_OB_IDDQ_CTRL	Page 515
0x1E7201	CKOUT3 Bias Control	CKOUT3_BIAS_CTRL	Page 516
0x1E7202	CKOUT3 Control	CKOUT3_CTRL	Page 516
0x1E7203	Squelch Control	CKOUT3_SQUELCH_CTRL	Page 517

Table 1524 • **LINE_OB_CFG *(continued)***

Address	Short Description	Register Name	Details
0x1E7204	CKOUT3 Data Selection	CKOUT3_DATA_SEL	Page 518
0x1E7205	CKOUT2 Bias Control	CKOUT2_BIAS_CTRL	Page 519
0x1E7206	CKOUT2 Control	CKOUT2_CTRL	Page 519
0x1E7207	Squelch Control	CKOUT2_SQUELCH_CTRL	Page 520
0x1E7208	CKOUT2 Data Selection	CKOUT2_DATA_SEL	Page 521
0x1E7209	CKOUT1 Bias Control	CKOUT1_BIAS_CTRL	Page 522
0x1E720A	CKOUT1 Control	CKOUT1_CTRL	Page 522
0x1E720B	Squelch Control	CKOUT1_SQUELCH_CTRL	Page 523
0x1E720C	CKOUT1 Data Selection	CKOUT1_DATA_SEL	Page 524
0x1E720D	CKOUT0 Bias Control	CKOUT0_BIAS_CTRL	Page 525
0x1E720E	CKOUT0 Control	CKOUT0_CTRL	Page 525
0x1E720F	Squelch Control	CKOUT0_SQUELCH_CTRL	Page 526
0x1E7210	CKOUT0 Data Selection	CKOUT0_DATA_SEL	Page 527

Table 1525 • **CS**

Address	Short Description	Register Name	Details
0x1E722B - 0x1E722E	Line Clock Select	LINE_CLK_SEL	Page 528
0x1E722F - 0x1E7232	Host Clock Select	HOST_CLK_SEL	Page 528
0x1E7233	SCKOut Clock Select	SCKOUT_CLK_SEL	Page 529
0x1E7234	Squelch Control	SCKOUT_SQUELCH_CTRL	Page 529
0x1E7235	FIFO Error Status	FIFO_ERR_STAT	Page 530
0x1E7236	FIFO Error Mask	FIFO_ERR_MASK	Page 531
0x1E7237	FIFO Error Interrupt	FIFO_ERR_INTR	Page 532

2.21.1 Line Side Clock Output Drivers

2.21.1.1 IDDQ Enable For All Line Side Clock Output Drivers

Short Name:LINE_OB_IDDQ_CTRL

Address:0x1E7200

Table 1526 • **IDDQ Enable For All Line Side Clock Output Drivers**

Bit	Name	Access	Description	Default
1	CKOUT23_IDDQN_CTRL	R/W	Put output buffers CKOUT2 and CKOUT3 into IDDQ mode 0 = IDDQ mode 1 = Normal operation	0x1

Table 1526 • **IDDQ Enable For All Line Side Clock Output Drivers *(continued)***

Bit	Name	Access	Description	Default
0	CKOUT01_IDDQN_CTRL	R/W	Put output buffers CKOUT0 and CKOUT1 into IDDQ mode 0 = IDDQ mode 1 = Normal operation	0x1

2.21.1.2 CKOUT3 Bias Control

Short Name:CKOUT3_BIAS_CTRL

Address:0x1E7201

CKOUT3 Bias Control

Table 1527 • **CKOUT3 Bias Control**

Bit	Name	Access	Description	Default
7:0	CKOUT3_BIAS_CTRL	R/W	CKOUT3 Bias Control [1:0]: sel_vref490m, fine tune of OBs internal 490mV reference voltage [3]: ena_data_cml2cmos, 1: enable feedback CMOS output (clock input directly fed back as CMOS signal, not used in malibu), 0: disable CMOS output [5:4]: sel_ena_abc, input mux, selects input source, 0: primary input, 1: sec. input (not used in malibu), 2: direct data path [7:6]: reserved	0x08

2.21.1.3 CKOUT3 Control

Short Name:CKOUT3_CTRL

Address:0x1E7202

CKOUT3 Control Registers

Table 1528 **• CKOUT3 Control**

Bit	Name	Access	Description	Default
15:0	CKOUT3_CTRL	R/W	CKOUT3 Control Registers [3:0]: rsel, resistor calibration input (large value: r-slow, small value: r-fast) [7:4]: reserved [8]: ena_cterm_drv, increases amplitude by 25% if OB is connected to a receiver whose common mode is terminated to VDDIO, 0: receivers common mode is terminated to VDDIO. 1: otherwise [9]: reserved [10]: enable_ob, 1: enable, 0: disable (powerdown) [11]: ena_1v2, selects if OB is supplied from 1V or 1.2V, 1: 1.2V, 0: 1.0V [15:12]: sel, selects drive amplitude. Max setting is limited in VDDOB = 1.0V mode, 0: lowest ampl. (300mV-400mV), 15: highest ampl. (550mV-700mV)	0x5064

2.21.1.4 Squelch Control

Short Name:CKOUT3_SQUELCH_CTRL

Address:0x1E7203

Table 1529 **• Squelch Control**

Bit	Name	Access	Description	Default
8	CKOUT3_SQUELCH_INV	R/W	0 = Use Squelch_src as is 1 = Invert Squelch_src	0x0

Table 1529 • **Squelch Control *(continued)***

Bit	Name	Access	Description	Default
5:0	CKOUT3_SQUELCH_SRC	R/W	Source of auto-squelch logic for CKOUT3 0 = from gpio 0 1 = from gpio 1 2 = from gpio 2 3 = from gpio 3 4 = from gpio 4 5 = from gpio 5 6 = from gpio 6 7 = from gpio 7 8 = 1g/10g link status from line 0 9 = 1g/10g link status from line 1 10 = 1g/10g link status from line 2 11 = 1g/10g link status from line 3 12 = 1g/10g link status from host 0 13 = 1g/10g link status from host 1 14 = 1g/10g link status from host 2 15 = 1g/10g link status from host 3 16 = serdes los from line 0 17 = serdes los from line 1 18 = serdes los from line 2 19 = serdes los from line 3 20 = serdes los from host 0 21 = serdes los from host 1 22 = serdes los from host 2 23 = serdes los from host 3 24 = 1g/10g link status from line 0 KR 25 = 1g/10g link status from line 1 KR 26 = 1g/10g link status from line 2 KR 27 = 1g/10g link status from line 3 KR 28 = 1g/10g link status from host 0 KR 29 = 1g/10g link status from host 1 KR 30 = 1g/10g link status from host 2 KR 31 = 1g/10g link status from host 3 KR 32-63 = No Squelch	0x3F

2.21.1.5 CKOUT3 Data Selection

Short Name:CKOUT3_DATA_SEL

Address:0x1E7204

Table 1530 • **CKOUT3 Data Selection**

Bit	Name	Access	Description	Default
8	CKOUT3_DIVIDE_BY_2	R/W	0 = Generate full-rate clock (i.e. LAN: 322.25MHz, WAN: 311.04MHz, 1G: 125MHz) 1 = Generate divide-by-2 version (i.e. LAN: 161.12MHz, etc)	0x0

Table 1530 • **CKOUT3 Data Selection** ***(continued)***

Bit	Name	Access	Description	Default
5:0	CKOUT3_DATA_SEL	R/W	Select data to be transmitted from CKOUT3 pin 0 = Line 0 Transmit Clock 1 = Line 1 Transmit Clock 2 = Line 2 Transmit Clock 3 = Line 3 Transmit Clock 4 = Host 0 Transmit Clock 5 = Host 1 Transmit Clock 6 = Host 2 Transmit Clock 7 = Host 3 Transmit Clock 8 = Line 0 Recovered Clock 9 = Line 1 Recovered Clock 10= Line 2 Recovered Clock 11= Line 3 Recovered Clock 12= Host 0 Recovered Clock 13= Host 1 Recovered Clock 14= Host 2 Recovered Clock 15= Host 3 Recovered Clock 16= Host Pll Clock 17= Line Pll Clock 18= CSR Clock 19= LTC Clock 20= Df2f clk 21= F2df clk 29= Debug 30= Debug 31= Oscillator output	0x3F

2.21.1.6 CKOUT2 Bias Control

Short Name:CKOUT2_BIAS_CTRL

Address:0x1E7205

CKOUT2 Bias Control

Table 1531 • **CKOUT2 Bias Control**

Bit	Name	Access	Description	Default
7:0	CKOUT2_BIAS_CTRL	R/W	CKOUT2 Bias Control [1:0]: sel_vref490m, fine tune of OBs internal 490mV reference voltage [3]: ena_data_cml2cmos, 1: enable feedback CMOS output (clock input directly fed back as CMOS signal, not used in malibu), 0: disable CMOS output [5:4]: sel_ena_abc, input mux, selects input source, 0: primary input, 1: sec. input (not used in malibu), 2: direct data path [7:6]: reserved	0x08

2.21.1.7 CKOUT2 Control

Short Name:CKOUT2_CTRL

Address:0x1E7206

CKOUT2 Control Registers

***Table 1532* • CKOUT2 Control**

Bit	Name	Access	Description	Default
15:0	CKOUT2_CTRL	R/W	CKOUT2 Control Registers [3:0]: rsel, resistor calibration input (large value: r-slow, small value: r-fast) [7:4]: reserved [8]: ena_cterm_drv, increases amplitude by 25% if OB is connected to a receiver whose common mode is terminated to VDDIO, 0: receivers common mode is terminated to VDDIO. 1: otherwise [9]: reserved [10]: enable_ob, 1: enable, 0: disable (powerdown) [11]: ena_1v2, selects if OB is supplied from 1V or 1.2V, 1: 1.2V, 0: 1.0V [15:12]: sel, selects drive amplitude. Max setting is limited in VDDOB = 1.0V mode, 0: lowest ampl. (300mV-400mV), 15: highest ampl. (550mV-700mV)	0x5064

2.21.1.8 Squelch Control

Short Name:CKOUT2_SQUELCH_CTRL

Address:0x1E7207

***Table 1533* • Squelch Control**

Bit	Name	Access	Description	Default
8	CKOUT2_SQUELCH_INV	R/W	0 = Use Squelch_src as is 1 = Invert Squelch_src	0x0

Table 1533 • **Squelch Control *(continued)***

Bit	Name	Access	Description	Default
5:0	CKOUT2_SQUELCH_SRC	R/W	Source of auto-squelch logic for CKOUT2 0 = from gpio 0 1 = from gpio 1 2 = from gpio 2 3 = from gpio 3 4 = from gpio 4 5 = from gpio 5 6 = from gpio 6 7 = from gpio 7 8 = 1g/10g link status from line 0 9 = 1g/10g link status from line 1 10 = 1g/10g link status from line 2 11 = 1g/10g link status from line 3 12 = 1g/10g link status from host 0 13 = 1g/10g link status from host 1 14 = 1g/10g link status from host 2 15 = 1g/10g link status from host 3 16 = serdes los from line 0 17 = serdes los from line 1 18 = serdes los from line 2 19 = serdes los from line 3 20 = serdes los from host 0 21 = serdes los from host 1 22 = serdes los from host 2 23 = serdes los from host 3 24 = 1g/10g link status from line 0 KR 25 = 1g/10g link status from line 1 KR 26 = 1g/10g link status from line 2 KR 27 = 1g/10g link status from line 3 KR 28 = 1g/10g link status from host 0 KR 29 = 1g/10g link status from host 1 KR 30 = 1g/10g link status from host 2 KR 31 = 1g/10g link status from host 3 KR 32-63 = No Squelch	0x3F

2.21.1.9 CKOUT2 Data Selection

Short Name:CKOUT2_DATA_SEL

Address:0x1E7208

Table 1534 • **CKOUT2 Data Selection**

Bit	Name	Access	Description	Default
8	CKOUT2_DIVIDE_BY_2	R/W	0 = Generate full-rate clock (i.e. LAN: 322.25MHz, WAN: 311.04MHz, 1G: 125MHz) 1 = Generate divide-by-2 version (i.e. LAN: 161.12MHz, etc)	0x0

Table 1534 • **CKOUT2 Data Selection *(continued)***

Bit	Name	Access	Description	Default
5:0	CKOUT2_DATA_SEL	R/W	Select data to be transmitted from CKOUT2 pin 0 = Line 0 Transmit Clock 1 = Line 1 Transmit Clock 2 = Line 2 Transmit Clock 3 = Line 3 Transmit Clock 4 = Host 0 Transmit Clock 5 = Host 1 Transmit Clock 6 = Host 2 Transmit Clock 7 = Host 3 Transmit Clock 8 = Line 0 Recovered Clock 9 = Line 1 Recovered Clock 10= Line 2 Recovered Clock 11= Line 3 Recovered Clock 12= Host 0 Recovered Clock 13= Host 1 Recovered Clock 14= Host 2 Recovered Clock 15= Host 3 Recovered Clock 16= Host Pll Clock 17= Line Pll Clock 18= CSR Clock 19= LTC Clock 20= Df2f clk 21= F2df clk 29= Debug 30= Debug 31= Oscillator output	0x3F

2.21.1.10 CKOUT1 Bias Control

Short Name:CKOUT1_BIAS_CTRL

Address:0x1E7209

CKOUT1 Bias Control

Table 1535 • **CKOUT1 Bias Control**

Bit	Name	Access	Description	Default
7:0	CKOUT1_BIAS_CTRL	R/W	CKOUT1 Bias Control [1:0]: sel_vref490m, fine tune of OBs internal 490mV reference voltage [3]: ena_data_cml2cmos, 1: enable feedback CMOS output (clock input directly fed back as CMOS signal, not used in malibu), 0: disable CMOS output [5:4]: sel_ena_abc, input mux, selects input source, 0: primary input, 1: sec. input (not used in malibu), 2: direct data path [7:6]: reserved	0x08

2.21.1.11 CKOUT1 Control

Short Name:CKOUT1_CTRL

Address:0x1E720A

CKOUT1 Control Registers

***Table 1536* • CKOUT1 Control**

Bit	Name	Access	Description	Default
15:0	CKOUT1_CTRL	R/W	CKOUT1 Control Registers [3:0]: rsel, resistor calibration input (large value: r-slow, small value: r-fast) [7:4]: reserved [8]: ena_cterm_drv, increases amplitude by 25% if OB is connected to a receiver whose common mode is terminated to VDDIO, 0: receivers common mode is terminated to VDDIO. 1: otherwise [9]: reserved [10]: enable_ob, 1: enable, 0: disable (powerdown) [11]: ena_1v2, selects if OB is supplied from 1V or 1.2V, 1: 1.2V, 0: 1.0V [15:12]: sel, selects drive amplitude. Max setting is limited in VDDOB = 1.0V mode, 0: lowest ampl. (300mV-400mV), 15: highest ampl. (550mV-700mV)	0x5064

2.21.1.12 Squelch Control

Short Name:CKOUT1_SQUELCH_CTRL

Address:0x1E720B

***Table 1537* • Squelch Control**

Bit	Name	Access	Description	Default
8	CKOUT1_SQUELCH_INV	R/W	0 = Use Squelch_src as is 1 = Invert Squelch_src	0x0

Table 1537 • **Squelch Control *(continued)***

Bit	Name	Access	Description	Default
5:0	CKOUT1_SQUELCH_SRC	R/W	Source of auto-squelch logic for CKOUT1 0 = from gpio 0 1 = from gpio 1 2 = from gpio 2 3 = from gpio 3 4 = from gpio 4 5 = from gpio 5 6 = from gpio 6 7 = from gpio 7 8 = 1g/10g link status from line 0 9 = 1g/10g link status from line 1 10 = 1g/10g link status from line 2 11 = 1g/10g link status from line 3 12 = 1g/10g link status from host 0 13 = 1g/10g link status from host 1 14 = 1g/10g link status from host 2 15 = 1g/10g link status from host 3 16 = serdes los from line 0 17 = serdes los from line 1 18 = serdes los from line 2 19 = serdes los from line 3 20 = serdes los from host 0 21 = serdes los from host 1 22 = serdes los from host 2 23 = serdes los from host 3 24 = 1g/10g link status from line 0 KR 25 = 1g/10g link status from line 1 KR 26 = 1g/10g link status from line 2 KR 27 = 1g/10g link status from line 3 KR 28 = 1g/10g link status from host 0 KR 29 = 1g/10g link status from host 1 KR 30 = 1g/10g link status from host 2 KR 31 = 1g/10g link status from host 3 KR 32-63 = No Squelch	0x3F

2.21.1.13 CKOUT1 Data Selection

Short Name:CKOUT1_DATA_SEL

Address:0x1E720C

Table 1538 • **CKOUT1 Data Selection**

Bit	Name	Access	Description	Default
8	CKOUT1_DIVIDE_BY_2	R/W	0 = Generate full-rate clock (i.e. LAN: 322.25MHz, WAN: 311.04MHz, 1G: 125MHz) 1 = Generate divide-by-2 version (i.e. LAN: 161.12MHz, etc)	0x0

Table 1538 • **CKOUT1 Data Selection *(continued)***

Bit	Name	Access	Description	Default
5:0	CKOUT1_DATA_SEL	R/W	Select data to be transmitted from CKOUT1 pin 0 = Line 0 Transmit Clock 1 = Line 1 Transmit Clock 2 = Line 2 Transmit Clock 3 = Line 3 Transmit Clock 4 = Host 0 Transmit Clock 5 = Host 1 Transmit Clock 6 = Host 2 Transmit Clock 7 = Host 3 Transmit Clock 8 = Line 0 Recovered Clock 9 = Line 1 Recovered Clock 10= Line 2 Recovered Clock 11= Line 3 Recovered Clock 12= Host 0 Recovered Clock 13= Host 1 Recovered Clock 14= Host 2 Recovered Clock 15= Host 3 Recovered Clock 16= Host Pll Clock 17= Line Pll Clock 18= CSR Clock 19= LTC Clock 20= Df2f clk 21= F2df clk 29= Debug 30= Debug 31= Oscillator output	0x3F

2.21.1.14 CKOUT0 Bias Control

Short Name:CKOUT0_BIAS_CTRL

Address:0x1E720D

CKOUT0 Bias Control

Table 1539 • **CKOUT0 Bias Control**

Bit	Name	Access	Description	Default
7:0	CKOUT0_BIAS_CTRL	R/W	CKOUT0 Bias Control [1:0]: sel_vref490m, fine tune of OBs internal 490mV reference voltage [3]: ena_data_cml2cmos, 1: enable feedback CMOS output (clock input directly fed back as CMOS signal, not used in malibu), 0: disable CMOS output [5:4]: sel_ena_abc, input mux, selects input source, 0: primary input, 1: sec. input (not used in malibu), 2: direct data path [7:6]: reserved	0x08

2.21.1.15 CKOUT0 Control

Short Name:CKOUT0_CTRL

Address:0x1E720E

CKOUT0 Control Registers

***Table 1540* • CKOUT0 Control**

Bit	Name	Access	Description	Default
15:0	CKOUT0_CTRL	R/W	CKOUT0 Control Registers [3:0]: rsel, resistor calibration input (large value: r-slow, small value: r-fast) [7:4]: reserved [8]: ena_cterm_drv, increases amplitude by 25% if OB is connected to a receiver whose common mode is terminated to VDDIO, 0: receivers common mode is terminated to VDDIO. 1: otherwise [9]: reserved [10]: enable_ob, 1: enable, 0: disable (powerdown) [11]: ena_1v2, selects if OB is supplied from 1V or 1.2V, 1: 1.2V, 0: 1.0V [15:12]: sel, selects drive amplitude. Max setting is limited in VDDOB = 1.0V mode, 0: lowest ampl. (300mV-400mV), 15: highest ampl. (550mV-700mV)	0x5064

2.21.1.16 Squelch Control

Short Name:CKOUT0_SQUELCH_CTRL

Address:0x1E720F

***Table 1541* • Squelch Control**

Bit	Name	Access	Description	Default
8	CKOUT0_SQUELCH_INV	R/W	0 = Use Squelch_src as is 1 = Invert Squelch_src	0x0

Table 1541 • **Squelch Control *(continued)***

Bit	Name	Access	Description	Default
5:0	CKOUT0_SQUELCH_SRC	R/W	Source of auto-squelch logic for CKOUT0 0 = from gpio 0 1 = from gpio 1 2 = from gpio 2 3 = from gpio 3 4 = from gpio 4 5 = from gpio 5 6 = from gpio 6 7 = from gpio 7 8 = 1g/10g link status from line 0 9 = 1g/10g link status from line 1 10 = 1g/10g link status from line 2 11 = 1g/10g link status from line 3 12 = 1g/10g link status from host 0 13 = 1g/10g link status from host 1 14 = 1g/10g link status from host 2 15 = 1g/10g link status from host 3 16 = serdes los from line 0 17 = serdes los from line 1 18 = serdes los from line 2 19 = serdes los from line 3 20 = serdes los from host 0 21 = serdes los from host 1 22 = serdes los from host 2 23 = serdes los from host 3 24 = 1g/10g link status from line 0 KR 25 = 1g/10g link status from line 1 KR 26 = 1g/10g link status from line 2 KR 27 = 1g/10g link status from line 3 KR 28 = 1g/10g link status from host 0 KR 29 = 1g/10g link status from host 1 KR 30 = 1g/10g link status from host 2 KR 31 = 1g/10g link status from host 3 KR 32-63 = No Squelch	0x3F

2.21.1.17 CKOUT0 Data Selection

Short Name:CKOUT0_DATA_SEL

Address:0x1E7210

Table 1542 • **CKOUT0 Data Selection**

Bit	Name	Access	Description	Default
8	CKOUT0_DIVIDE_BY_2	R/W	0 = Generate full-rate clock (i.e. LAN: 322.25MHz, WAN: 311.04MHz, 1G: 125MHz) 1 = Generate divide-by-2 version (i.e. LAN: 161.12MHz, etc)	0x0

Table 1542 • **CKOUT0 Data Selection *(continued)***

Bit	Name	Access	Description	Default
5:0	CKOUT0_DATA_SEL	R/W	Select data to be transmitted from CKOUT0 pin 0 = Line 0 Transmit Clock 1 = Line 1 Transmit Clock 2 = Line 2 Transmit Clock 3 = Line 3 Transmit Clock 4 = Host 0 Transmit Clock 5 = Host 1 Transmit Clock 6 = Host 2 Transmit Clock 7 = Host 3 Transmit Clock 8 = Line 0 Recovered Clock 9 = Line 1 Recovered Clock 10= Line 2 Recovered Clock 11= Line 3 Recovered Clock 12= Host 0 Recovered Clock 13= Host 1 Recovered Clock 14= Host 2 Recovered Clock 15= Host 3 Recovered Clock 16= Host Pll Clock 17= Line Pll Clock 18= CSR Clock 19= LTC Clock 20= Df2f clk 21= F2df clk 29= Debug 30= Debug 31= Oscillator output	0x3F

2.21.1.18 Line Clock Select

Short Name:LINE_CLK_SEL

Addresses:0x1E722B - 0x1E722E

Table 1543 • **Line Clock Select**

Bit	Name	Access	Description	Default
3:0	LINE_CLK_SEL	R/W	Selects the source to which the given line transmit clock will be synchronized 0 = Line 0 recovered clock 1 = Line 1 recovered clock 2 = Line 2 recovered clock 3 = Line 3 recovered clock 4 = Host 0 recovered clock 5 = Host 1 recovered clock 6 = Host 2 recovered clock 7 = Host 3 recovered clock 8 = SREFCK 9-15 = Synchronization disabled	0xF

2.21.1.19 Host Clock Select

Short Name:HOST_CLK_SEL

Addresses:0x1E722F - 0x1E7232

Table 1544 • **Host Clock Select**

Bit	Name	Access	Description	Default
3:0	HOST_CLK_SEL	R/W	Selects the source to which the given host transmit clock will be synchronized 0 = Line 0 recovered clock 1 = Line 1 recovered clock 2 = Line 2 recovered clock 3 = Line 3 recovered clock 4 = Host 0 recovered clock 5 = Host 1 recovered clock 6 = Host 2 recovered clock 7 = Host 3 recovered clock 8 = SREFCK 9-15 = Synchronization disabled	0xF

2.21.1.20 SCKOUT Clock Select

Short Name:SCKOUT_CLK_SEL

Address:0x1E7233

Table 1545 • **SCKOut Clock Select**

Bit	Name	Access	Description	Default
3:0	SCKOUT_CLK_SEL	R/W	Selects the source to which the SCKOUT transmit clock will be synchronized 0 = Line 0 recovered clock 1 = Line 1 recovered clock 2 = Line 2 recovered clock 3 = Line 3 recovered clock 4 = Host 0 recovered clock 5 = Host 1 recovered clock 6 = Host 2 recovered clock 7 = Host 3 recovered clock 8 = SREFCK 9-15 = Synchronization disabled	0xF

2.21.1.21 Squelch Control

Short Name:SCKOUT_SQUELCH_CTRL

Address:0x1E7234

Table 1546 • **Squelch Control**

Bit	Name	Access	Description	Default
8	SCKOUT_SQUELCH_INV	R/W	0 = Use Squelch_src as is 1 = Invert Squelch_src	0x0

Table 1546 • **Squelch Control *(continued)***

Bit	Name	Access	Description	Default
5:0	SCKOUT_SQUELCH_SRC	R/W	Source of auto-squelch logic for SCKOUT 0 = from gpio 0 1 = from gpio 1 2 = from gpio 2 3 = from gpio 3 4 = from gpio 4 5 = from gpio 5 6 = from gpio 6 7 = from gpio 7 8 = 1g/10g link status from line 0 9 = 1g/10g link status from line 1 10 = 1g/10g link status from line 2 11 = 1g/10g link status from line 3 12 = 1g/10g link status from host 0 13 = 1g/10g link status from host 1 14 = 1g/10g link status from host 2 15 = 1g/10g link status from host 3 16 = serdes los from line 0 17 = serdes los from line 1 18 = serdes los from line 2 19 = serdes los from line 3 20 = serdes los from host 0 21 = serdes los from host 1 22 = serdes los from host 2 23 = serdes los from host 3 24 = 1g/10g link status from line 0 KR 25 = 1g/10g link status from line 1 KR 26 = 1g/10g link status from line 2 KR 27 = 1g/10g link status from line 3 KR 28 = 1g/10g link status from host 0 KR 29 = 1g/10g link status from host 1 KR 30 = 1g/10g link status from host 2 KR 31 = 1g/10g link status from host 3 KR 32-63 = No Squelch	0x3F

2.21.1.22 FIFO Error Status

Short Name:FIFO_ERR_STAT

Address:0x1E7235

Table 1547 • **FIFO Error Status**

Bit	Name	Access	Description	Default
8	DF2F_FIFO_ERR_STAT	R/O	Current DF2F lane sync fifo error status 0 = No Error 1 = FIFO Error	0x0
7	HOST3_FIFO_ERR_STAT	R/O	Current host 3 lane sync fifo error status 0 = No Error 1 = FIFO Error	0x0
6	HOST2_FIFO_ERR_STAT	R/O	Current host 2 lane sync fifo error status 0 = No Error 1 = FIFO Error	0x0

Table 1547 • **FIFO Error Status** ***(continued)***

Bit	Name	Access	Description	Default
5	HOST1_FIFO_ERR_STAT	R/O	Current host 1 lane sync fifo error status 0 = No Error 1 = FIFO Error	0x0
4	HOST0_FIFO_ERR_STAT	R/O	Current host 0 lane sync fifo error status 0 = No Error 1 = FIFO Error	0x0
3	LINE3_FIFO_ERR_STAT	R/O	Current line 3 lane sync fifo error status 0 = No Error 1 = FIFO Error	0x0
2	LINE2_FIFO_ERR_STAT	R/O	Current line 2 lane sync fifo error status 0 = No Error 1 = FIFO Error	0x0
1	LINE1_FIFO_ERR_STAT	R/O	Current line 1 lane sync fifo error status 0 = No Error 1 = FIFO Error	0x0
0	LINE0_FIFO_ERR_STAT	R/O	Current line 0 lane sync fifo error status 0 = No Error 1 = FIFO Error	0x0

2.21.1.23 FIFO Error Mask

Short Name:FIFO_ERR_MASK

Address:0x1E7236

Table 1548 • **FIFO Error Mask**

Bit	Name	Access	Description	Default
8	DF2F_FIFO_ERR_INTR_EN	R/W	Interrupt enable for line 0 lane sync fifo 0 = DF2F_FIFO_ERR_STICKY will not propagate to interrupt 1 = DF2F_FIFO_ERR_STICKY will propagate to interrupt	0x0
7	HOST3_FIFO_ERR_INTR_EN	R/W	Interrupt enable for line 0 lane sync fifo 0 = HOST3_FIFO_ERR_STICKY will not propagate to interrupt 1 = HOST3_FIFO_ERR_STICKY will propagate to interrupt	0x0
6	HOST2_FIFO_ERR_INTR_EN	R/W	Interrupt enable for line 0 lane sync fifo 0 = HOST2_FIFO_ERR_STICKY will not propagate to interrupt 1 = HOST2_FIFO_ERR_STICKY will propagate to interrupt	0x0
5	HOST1_FIFO_ERR_INTR_EN	R/W	Interrupt enable for line 0 lane sync fifo 0 = HOST1_FIFO_ERR_STICKY will not propagate to interrupt 1 = HOST1_FIFO_ERR_STICKY will propagate to interrupt	0x0

Table 1548 • **FIFO Error Mask** ***(continued)***

Bit	Name	Access	Description	Default
4	HOST0_FIFO_ERR_INTR_EN	R/W	Interrupt enable for line 0 lane sync fifo 0 = HOST0_FIFO_ERR_STICKY will not propagate to interrupt 1 = HOST0_FIFO_ERR_STICKY will propagate to interrupt	0x0
3	LINE3_FIFO_ERR_INTR_EN	R/W	Interrupt enable for line 0 lane sync fifo 0 = LINE3_FIFO_ERR_STICKY will not propagate to interrupt 1 = LINE3_FIFO_ERR_STICKY will propagate to interrupt	0x0
2	LINE2_FIFO_ERR_INTR_EN	R/W	Interrupt enable for line 0 lane sync fifo 0 = LINE2_FIFO_ERR_STICKY will not propagate to interrupt 1 = LINE2_FIFO_ERR_STICKY will propagate to interrupt	0x0
1	LINE1_FIFO_ERR_INTR_EN	R/W	Interrupt enable for line 0 lane sync fifo 0 = LINE1_FIFO_ERR_STICKY will not propagate to interrupt 1 = LINE1_FIFO_ERR_STICKY will propagate to interrupt	0x0
0	LINE0_FIFO_ERR_INTR_EN	R/W	Interrupt enable for line 0 lane sync fifo 0 = LINE0_FIFO_ERR_STICKY will not propagate to interrupt 1 = LINE0_FIFO_ERR_STICKY will propagate to interrupt	0x0

2.21.1.24 FIFO Error Interrupt

Short Name:FIFO_ERR_INTR

Address:0x1E7237

Table 1549 • **FIFO Error Interrupt**

Bit	Name	Access	Description	Default
8	DF2F_FIFO_ERR_STICKY	Sticky	0 = FIFO error not detected since last cleared 1 = FIFO error detected since last cleared	0x0
7	HOST3_FIFO_ERR_STICKY	Sticky	0 = FIFO error not detected since last cleared 1 = FIFO error detected since last cleared	0x0
6	HOST2_FIFO_ERR_STICKY	Sticky	0 = FIFO error not detected since last cleared 1 = FIFO error detected since last cleared	0x0
5	HOST1_FIFO_ERR_STICKY	Sticky	0 = FIFO error not detected since last cleared 1 = FIFO error detected since last cleared	0x0
4	HOST0_FIFO_ERR_STICKY	Sticky	0 = FIFO error not detected since last cleared 1 = FIFO error detected since last cleared	0x0
3	LINE3_FIFO_ERR_STICKY	Sticky	0 = FIFO error not detected since last cleared 1 = FIFO error detected since last cleared	0x0
2	LINE2_FIFO_ERR_STICKY	Sticky	0 = FIFO error not detected since last cleared 1 = FIFO error detected since last cleared	0x0
1	LINE1_FIFO_ERR_STICKY	Sticky	0 = FIFO error not detected since last cleared 1 = FIFO error detected since last cleared	0x0

*Table 1549 • (continued)*FIFO Error Interrupt

Bit	Name	Access	Description	Default
0	LINE0_FIFO_ERR_STICKY	Sticky	0 = FIFO error not detected since last cleared 1 = FIFO error detected since last cleared	0x0

2.22 GLOBAL_RESET (Device 0x1E)

Table 1550 • FAST_ACCESS_RESET

Address	Short Description	Register Name	Details
0x1E8000	Fast Reset for Non-CSR Ring	GLOBAL_FAST_RESET	Page 533

2.22.1 Fast Reset for Non-CSR Ring

Short Name:GLOBAL_FAST_RESET

Address:0x1E8000

Fast access reset registers are not on a CSR ring

Table 1551 • Fast Reset for Non-CSR Ring

Bit	Name	Access	Description	Default
13	CSR_RING_5_FAST_RESET	One-shot	Self-clearing software reset register 0: Normal operation 1: Reset CSR ring 2	0x0
12	CSR_RING_4_FAST_RESET	One-shot	Self-clearing software reset register 0: Normal operation 1: Reset CSR ring 2	0x0
11	CSR_RING_3_FAST_RESET	One-shot	Self-clearing software reset register 0: Normal operation 1: Reset CSR ring 2	0x0
10	CSR_RING_2_FAST_RESET	One-shot	Self-clearing software reset register 0: Normal operation 1: Reset CSR ring 2	0x0
9	CSR_RING_1_FAST_RESET	One-shot	Self-clearing software reset register 0: Normal operation 1: Reset CSR ring 1	0x0
8	CSR_RING_0_FAST_RESET	One-shot	Self-clearing software reset register 0: Normal operation 1: Reset CSR ring 0	0x0
7	CHANNEL_3_FAST_RESET	One-shot	Self-clearing software reset register 0: Normal operation 1: Reset channel 1 and CSR ring 1	0x0
6	CHANNEL_2_FAST_RESET	One-shot	Self-clearing software reset register 0: Normal operation 1: Reset channel 1 and CSR ring 1	0x0
5	CHANNEL_1_FAST_RESET	One-shot	Self-clearing software reset register 0: Normal operation 1: Reset channel 1 and CSR ring 1	0x0

Table 1551 • **Fast Reset for Non-CSR Ring *(continued)***

Bit	Name	Access	Description	Default
4	CHANNEL_0_FAST_RESET	One-shot	Self-clearing software reset register 0: Normal operation 1: Reset channel 0 and CSR ring 0	0x0
0	CHIP_FAST_RESET	One-shot	Reset the datapath in both channels and all configuration registers except those used for global configuration. 0: Normal operation 1: Reset	0x0

2.23 HOST_PLL5G (Device 0x1E)

Table 1552 • **H_PLL5G**

Address	Short Description	Register Name	Details
0x1E8100	H_PLL5G Configuration 0A	H_PLL5G_CFG0A	Page 534
0x1E8101	H_PLL5G Configuration 0B	H_PLL5G_CFG0B	Page 535
0x1E8102	H_PLL5G Configuration 1A	H_PLL5G_CFG1A	Page 536
0x1E8103	H_PLL5G Configuration 1B	H_PLL5G_CFG1B	Page 536
0x1E8104	H_PLL5G Configuration 2A	H_PLL5G_CFG2A	Page 537
0x1E8105	H_PLL5G Configuration 2B	H_PLL5G_CFG2B	Page 537
0x1E8106	H_PLL5G Configuration 3A	H_PLL5G_CFG3A	Page 538
0x1E8107	H_PLL5G Configuration 3B	H_PLL5G_CFG3B	Page 539
0x1E810C	H_PLL5G Configuration 6	H_PLL5G_CFG6A	Page 539
0x1E810D	H_PLL5G Configuration 6B	H_PLL5G_CFG6B	Page 539
0x1E810E	H_PLL5G Status 0	H_PLL5G_STATUS0	Page 539
0x1E8111	H_PLL5G Interrupts	H_PLL5G_INTR	Page 540
0x1E8112	H_PLL5G Interrupt Masks	H_PLL5G_INTR_MASK	Page 540

2.23.1 H_PLL5G Configuration

Configuration register set for H_PLL5G (host side PLL5G).

2.23.1.1 H_PLL5G Configuration 0A

Short Name:H_PLL5G_CFG0A

Address:0x1E8100

Configuration register 0A for H_PLL5G

Table 1553 **• H_PLL5G Configuration 0A**

Bit	Name	Access	Description	Default
5:0	CORE_CLK_DIV	R/W	Setting for core clock divider 0: 625 MHz, 1: 312.5 MHz 2: 500 MHz 3: 277.77 MHz 4: 500 MHz 5: 250 MHz 6: 416.66 MHz 7: 227.27 MHz 8: 416.66 MHz 9: 208.33 MHz 10: 357.14 MHz 11: 192.3 MHz 12: 357.14 MHz 13: 178.57 MHz 14: 312.5 MHz 15: 166.66 MHz 17: 156,25 MHz	0x11
11:6	CPU_CLK_DIV	R/W	Setting for CPU clock divider 2: 500 MHz 5: 250 MHz 6: 416.66 MHz 14: 312.5 MHz 15: 166.66 MHz Others: Reserved	0x05
12	ENA_BIAS	R/W	enable BIAS circuitry incl. Bandgap, voltage regulators, etc.	0x1
13	ENA_VCO_BUF	R/W	enable BIAS for LCPLL VCO output buffer	0x1
14	ENA_CP1	R/W	enable current mode charge pump, normal mode	0x1
15	ENA_VCO_CONTRH	R/W	enable fine VCO operating point regulator	0x1

2.23.1.2 H_PLL5G Configuration 0B

Short Name:H_PLL5G_CFG0B

Address:0x1E8101

Configuration register 0B for H_PLL5G

Table 1554 **• H_PLL5G Configuration 0B**

Bit	Name	Access	Description	Default
1:0	SELCPI	R/W	setting for charge pump current 0: lowest current 3: highest current	0x2
6:2	LOOP_BW_RES	R/W	setting for filter resistor value 0: biggest resistance 31: lowest resistance	0x0D
10:7	SELBGV820	R/W	fine tune of bandgap voltage distribution 0: lowest voltage 15: highest voltage	0x7

Table 1554 • **H_PLL5G Configuration 0B *(continued)***

Bit	Name	Access	Description	Default
11	ENA_LOCK_FINE	R/W	enable fine locking, last stage in startup locking sequence	0x0
12	DIV4	R/W	RCPLL feedback divider setting	0x1
13	ENA_CLKTREE	R/W	RCPLL enable BIAS for clocktree buffer (active low) 0: enable BIAS 1: disable BIAS	0x1
14	ENA_LANE	R/W	RCPLL Global enable for serdes lane.	0x1
15	ENA_ROT	R/W	RCPLL feedback divider setting	0x0

2.23.1.3 H_PLL5G Configuration 1A

Short Name:H_PLL5G_CFG1A

Address:0x1E8102

Configuration register 1A for H_PLL5G

Table 1555 • **H_PLL5G Configuration 1A**

Bit	Name	Access	Description	Default
0	FORCE_SET_ENA	R/W	RCPLL When set to '1' the value at sx_pll_fsm_ctrl_data_I is not taken as reference value for the FSM, but is directly applied to the PLL as frequency range setting.	0x0
1	HALF_RATE	R/W	RCPLL Enable for half rate mode	0x0
2	OUT_OF_RANGE_RECAL_ENA	R/W	RCPLL Enable recalibration of PLL when out of range is detected	0x0
3	PWD_RX	R/W	RCPLL Power down for the Rx-path	0x0
4	PWD_TX	R/W	RCPLL Power down for the Tx-path	0x0
5	QUARTER_RATE	R/W	RCPLL Enable for quarter rate mode	0x1
13:6	RC_CTRL_DATA	R/W	RCPLL Control input for startup FSM	0x78
14	RC_ENABLE	R/W	RCPLL Enable for startup FSM	0x1
15	READBACK_DATA_SEL	R/W	RCPLL Selects whether (when set to '1') the frequency range setting from the FSM can be read back at sx_pll_rb_data_o or (when cleared to 0) the measured period.	0x0

2.23.1.4 H_PLL5G Configuration 1B

Short Name:H_PLL5G_CFG1B

Address:0x1E8103

Configuration register 1B for H_PLL5G

Table 1556 • **H_PLL5G Configuration 1B**

Bit	Name	Access	Description	Default
0	ROT_DIR	R/W	RCPLL feedback divider setting	0x0
1	ROT_SPEED	R/W	RCPLL feedback divider setting	0x0

Table 1556 • **H_PLL5G Configuration 1B *(continued)***

Bit	Name	Access	Description	Default
2	ENA_DIRECT	R/W	enable for direct data mode (ATPG/JTAG) reference clock input buffer and test output buffer	0x0

2.23.1.5 H_PLL5G Configuration 2A

Short Name:H_PLL5G_CFG2A

Address:0x1E8104

Configuration register 2A for H_PLL5G

Table 1557 • **H_PLL5G Configuration 2A**

Bit	Name	Access	Description	Default
0	ENA_GAIN_TEST	R/W	enable static VCO frequency stepping	0x0
1	DISABLE_FSM	R/W	disable automatic FSM startup frequency stepping	0x0
2	EN_RESET_FRQ_DET	R/W	enable FSM frequency deviation detection	0x1
3	EN_RESET_LIM_DET	R/W	enable FSM limiter detection	0x0
4	EN_RESET_OVERRUN	R/W	enable FSM frequency deviation overrun	0x1
9:5	GAIN_TEST	R/W	setting for static VCO frequency stepping 0: lowest frequency 31: highest frequency	0x00
10	DISABLE_FSM_POR	R/W	disables the startup FSM to start ramp up the frequency from POR 0: normal 1: disable	0x0
11	FRC_FSM_POR	R/W	forces the startup FSM to start ramp up the frequency by POR 0: no force 1: force	0x0
12	ENA_AMP_CTRL_FORCE	R/W	enable static VCO amplitude control	0x0
13	ENA_AMPCTRL	R/W	enable automatic VCO amplitude control	0x1
14	PWD_AMPCTRL_N	R/W	force VCO amplitude control output to low (no VCO current) 0:force 1: no force	0x1
15	ENA_CLK_BYPASS	R/W	enable clock bypass for all output clocks to come from ref clock pad	0x0

2.23.1.6 H_PLL5G Configuration 2B

Short Name:H_PLL5G_CFG2B

Address:0x1E8105

Configuration register 2B for H_PLL5G

Table 1558 **• H_PLL5G Configuration 2B**

Bit	Name	Access	Description	Default
7:0	AMPC_SEL	R/W	static VCO amplitude control, active w/ ena_amp_ctrl_force 0: lowest current, 255: highest current	0x10
8	ENA_CLK_BYPASS1	R/W	enable clock bypass for all output clocks to come from extra dividers (125MHz, 250MHz, 312.5MHz)	0x0
9	ENA_CP2	R/W	enable resistor mode chargepump, test mode	0x0
10	ENA_RCPLL	R/W	enable RCPLL clock buffer in LCPLL VCO (sx_ena_vco_buf_i must be set to 0)	0x0
11	ENA_FBTESTOUT	R/W	enable feedback divider output to test output buffer	0x0
12	ENA_VCO_NREF_TESTOUT	R/W	enable VCO frequency control output	0x0
13	ENA_PFD_IN_FLIP	R/W	enable flip of refclk and fbclk at PFD, used for 2nd chargepump	0x0
14	ENA_TEST_MODE	R/W	enables test modes, e.g. fbdivsel	0x0

2.23.1.7 H_PLL5G Configuration 3A

Short Name:H_PLL5G_CFG3A

Address:0x1E8106

Configuration register 3A for H_PLL5G

Table 1559 **• H_PLL5G Configuration 3A**

Bit	Name	Access	Description	Default
7:0	FBDIVSEL	R/W	setting for feedback divider, divide by 12..255	0x28
8	FBDIVSEL_TST_ENA	R/W	enable feedback divider testmode	0x0
9	FORCE_CP	R/W	force chargepump output to nominal VCO operating point	0x0
10	FORCE_ENA	R/W	enable force VCO frequency high/low (force_hi/lo)	0x0
11	FORCE_HI	R/W	force chargepump output to high, gives highest VCO frequency	0x0
12	FORCE_LO	R/W	force chargepump output to low, gives lowest VCO frequency	0x0
13	FORCE_VCO_CONTRH	R/W	force vco contrh input to mid level (mid CML level)	0x0
14	RST_FB_N	R/W	reset for feedback divider, active low 0: reset 1:no reset	0x1
15	SEL_CML_CMOS_PFD	R/W	select CML or CMOS phase/frequency detector 0: CML 1: CMOS	0x0

2.23.1.8 H_PLL5G Configuration 3B

Short Name:H_PLL5G_CFG3B

Address:0x1E8107

Configuration register 3B for H_PLL5G

***Table 1560* • H_PLL5G Configuration 3B**

Bit	Name	Access	Description	Default
0	SEL_FBDCLK	R/W	enable symmetric feedback divider clock output 0: fbclk/2 1: fbclk	0x0
1	ENA_TEST_OUT	R/W	enable differential test output	0x1
2	ENA_ANA_TEST_OUT	R/W	enable analog test output	0x0
5:3	TESTOUT_SEL	R/W	select test output buffer input signal	0x4
7:6	TEST_ANA_OUT_SEL	R/W	select analog test output input signal	0x0

2.23.1.9 H_PLL5G Configuration 6

Short Name:H_PLL5G_CFG6A

Address:0x1E810C

Configuration register 6 for H_PLL5G

***Table 1561* • H_PLL5G Configuration 6**

Bit	Name	Access	Description	Default
5:0	DDR_CLK_DIV	R/W	Setting for DDR clock divider (see core_clk_div)	0x0E
6	ENA_FBCLKC2	R/W	enable feedback divider CMOS 1/2 clock (for FSM)	0x1
7	ENA_REFCLKC2	R/W	enable reference CMOS 1/2 clock	0x1
15:8	DIV125REF_SEL	R/W	select reference CML clock divider (8,9,10,12 to 255)	0x14

2.23.1.10 H_PLL5G Configuration 6B

Short Name:H_PLL5G_CFG6B

Address:0x1E810D

Configuration register 6B for L_PLL5G

***Table 1562* • H_PLL5G Configuration 6B**

Bit	Name	Access	Description	Default
1:0	POR_DEL_SEL	R/W	enable reference CMOS 1/2 clock (dummy)	0x0

2.23.1.11 H_PLL5G Status 0

Short Name:H_PLL5G_STATUS0

Address:0x1E810E

Status register 0 for the H_PLL5G

Table 1563 **• H_PLL5G Status 0**

Bit	Name	Access	Description	Default
0	LOCK_STATUS	R/O	PLL lock status 0: not locked 1: locked	0x0
8:1	READBACK_DATA	R/O	RCPLL Interface to read back internal data of the FSM.	0x00
9	CALIBRATION_DONE	R/O	RCPLL Flag that indicates that the calibration procedure has finished.	0x0
10	CALIBRATION_ERR	R/O	RCPLL Flag that indicates errors that may occur during the calibration procedure.	0x0
11	OUT_OF_RANGE_ERR	R/O	RCPLL Flag that indicates a out of range condition while NOT in calibration mode.	0x0
12	RANGE_LIM	R/O	RCPLL Flag range limiter signaling	0x0

2.23.1.12 H_PLL5G Interrupts

Short Name:H_PLL5G_INTR

Address:0x1E8111

Interrupt registers for H_PLL5G

Table 1564 **• H_PLL5G Interrupts**

Bit	Name	Access	Description	Default
0	LOCK_STATUS_INTR	Sticky	PLL LOCK_STATUS Interrupt Register 1: H_PLL5G_STATUS0::LOCK_STATUS has changed state since the last time this interrupt bit was cleared. 0: H_PLL5G_STATUS0::LOCK_STATUS has not changed state since the last time this interrupt bit was cleared.	0x0

2.23.1.13 H_PLL5G Interrupt Masks

Short Name:H_PLL5G_INTR_MASK

Address:0x1E8112

Interrupt masks for H_PLL5G

Table 1565 **• H_PLL5G Interrupt Masks**

Bit	Name	Access	Description	Default
0	LOCK_STATUS_INTR_MASK	R/W	Interrupt mask for PLL LOCK_STATUS. H_PLL5G_INTR::LOCK_STATUS_INTR contributes to the chip's interrupt output pin when enabled. 1: Interrupt enabled 0: Interrupt disabled	0x0

2.24 LINE_PLL5G (Device 0x1E)

Table 1566 **• L_PLL5G**

Address	Short Description	Register Name	Details
0x1E8200	L_PLL5G Configuration 0A	L_PLL5G_CFG0A	Page 541
0x1E8201	L_PLL5G Configuration 0B	L_PLL5G_CFG0B	Page 542
0x1E8202	L_PLL5G Configuration 1A	L_PLL5G_CFG1A	Page 543
0x1E8203	L_PLL5G Configuration 1B	L_PLL5G_CFG1B	Page 543
0x1E8204	L_PLL5G Configuration 2A	L_PLL5G_CFG2A	Page 544
0x1E8205	L_PLL5G Configuration 2B	L_PLL5G_CFG2B	Page 544
0x1E8206	L_PLL5G Configuration 3A	L_PLL5G_CFG3A	Page 545
0x1E8207	L_PLL5G Configuration 3B	L_PLL5G_CFG3B	Page 546
0x1E8208	L_PLL5G Configuration 4A	L_PLL5G_CFG4A	Page 546
0x1E8209	L_PLL5G Configuration 4B	L_PLL5G_CFG4B	Page 547
0x1E820A	L_PLL5G Configuration 5A	L_PLL5G_CFG5A	Page 547
0x1E820B	L_PLL5G Configuration 5B	L_PLL5G_CFG5B	Page 548
0x1E820C	L_PLL5G Configuration 6A	L_PLL5G_CFG6A	Page 549
0x1E820D	L_PLL5G Configuration 6B	L_PLL5G_CFG6B	Page 549
0x1E820E	L_PLL5G Status 0	L_PLL5G_STATUS0	Page 549
0x1E8211	L_PLL5G Interrupts	L_PLL5G_INTR	Page 550
0x1E8212	L_PLL5G Interrupt Masks	L_PLL5G_INTR_MASK	Page 550

2.24.1 L_PLL5G Configuration

Configuration and Status register set for PLL5G_LSIDE.

2.24.1.1 L_PLL5G Configuration 0A

Short Name:L_PLL5G_CFG0A

Address:0x1E8200

Configuration register 0A for L_PLL5G

Table 1567 **• L_PLL5G Configuration 0A**

Bit	Name	Access	Description	Default
5:0	CORE_CLK_DIV	R/W	setting for core clock divider, division factors for [5:4] 0: 2 1: 4 2: 1 3: 3 for [3:0] 0: 4 1: 8 2: 5 3: 9 4: 5 5: 10 6: 6 7: 11 8: 6 9: 12 10: 7 11: 13 12: 7 13: 14 14: 8 15: 15	0x05
11:6	CPU_CLK_DIV	R/W	setting for CPU clock divider (see core_clk_div)	0x05
12	ENA_BIAS	R/W	enable BIAS circuitry incl. Bandgap, voltage regulators, etc.	0x1
13	ENA_VCO_BUF	R/W	enable BIAS for LCPLL VCO output buffer	0x1
14	ENA_CP1	R/W	enable current mode charge pump, mission mode	0x1
15	ENA_VCO_CONTRH	R/W	enable fine VCO operating point regulator	0x1

2.24.1.2 L_PLL5G Configuration 0B

Short Name:L_PLL5G_CFG0B

Address:0x1E8201

Configuration register 0B for L_PLL5G

Table 1568 **• L_PLL5G Configuration 0B**

Bit	Name	Access	Description	Default
1:0	SELCPI	R/W	setting for charge pump current, 0: lowest current 3: highest current	0x2
6:2	LOOP_BW_RES	R/W	setting for filter resistor value, 0: biggest resistance 31: lowest resistance	0x0D
10:7	SELBGV820	R/W	fine tune of bandgap voltage distribution, 0: highest voltage, 15: lowest voltage	0x7

Table 1568 • **L_PLL5G Configuration 0B *(continued)***

Bit	Name	Access	Description	Default
11	ENA_LOCK_FINE	R/W	enable fine locking, last stage in startup locking sequence	0x0
12	DIV4	R/W	RCPLL feedback divider setting	0x1
13	ENA_CLKTREE	R/W	RCPLL enable BIAS for clocktree buffer (active low) 0: enable BIAS 1: disable BIAS	0x1
14	ENA_LANE	R/W	RCPLL Global enable for serdes lane.	0x1
15	ENA_ROT	R/W	RCPLL feedback divider setting	0x0

2.24.1.3 L_PLL5G Configuration 1A

Short Name:L_PLL5G_CFG1A

Address:0x1E8202

Configuration register 1A for L_PLL5G

Table 1569 • **L_PLL5G Configuration 1A**

Bit	Name	Access	Description	Default
0	FORCE_SET_ENA	R/W	RCPLL When set to 1 the value at sx_pll_fsm_ctrl_data_i is not taken as reference value for the FSM, but is directly applied to the PLL as frequency range setting.	0x0
1	HALF_RATE	R/W	RCPLL Enable for half rate mode	0x0
2	OUT_OF_RANGE_RECAL_ENA	R/W	RCPLL Enable recalibration of PLL when out of range is detected	0x0
3	PWD_RX	R/W	RCPLL Power down for the Rx-path	0x0
4	PWD_TX	R/W	RCPLL Power down for the Tx-path	0x0
5	QUARTER_RATE	R/W	RCPLL Enable for quarter rate mode	0x1
13:6	RC_CTRL_DATA	R/W	RCPLL Control input for startup FSM	0x78
14	RC_ENABLE	R/W	RCPLL Enable for startup FSM	0x1
15	READBACK_DATA_SEL	R/W	RCPLL Selects whether (when set to 1) the frequency range setting from the FSM can be read back at sx_pll_rb_data_o or (when cleared to 0) the measured period.	0x0

2.24.1.4 L_PLL5G Configuration 1B

Short Name:L_PLL5G_CFG1B

Address:0x1E8203

Configuration register 1B for L_PLL5G

Table 1570 • **L_PLL5G Configuration 1B**

Bit	Name	Access	Description	Default
0	ROT_DIR	R/W	RCPLL feedback divider setting	0x0
1	ROT_SPEED	R/W	RCPLL feedback divider setting	0x0

Table 1570 • **L_PLL5G Configuration 1B *(continued)***

Bit	Name	Access	Description	Default
2	ENA_DIRECT	R/W	enable for direct data mode (ATPG/JTAG) reference clock input buffer and test output buffer	0x0

2.24.1.5 L_PLL5G Configuration 2A

Short Name:L_PLL5G_CFG2A

Address:0x1E8204

Configuration register 2A for L_PLL5G

Table 1571 • **L_PLL5G Configuration 2A**

Bit	Name	Access	Description	Default
0	ENA_GAIN_TEST	R/W	enable static VCO frequency stepping	0x0
1	DISABLE_FSM	R/W	disable automatic FSM startup frequency stepping	0x0
2	EN_RESET_FRQ_DET	R/W	enable FSM frequency deviation detection	0x1
3	EN_RESET_LIM_DET	R/W	enable FSM limiter detection	0x0
4	EN_RESET_OVERRUN	R/W	enable FSM frequency deviation overrun	0x1
9:5	GAIN_TEST	R/W	setting for static VCO frequency stepping, 0: lowest frequency 31: highest frequency	0x00
10	DISABLE_FSM_POR	R/W	disables the startup FSM to start ramp up the frequency from POR, 0: normal 1: disable	0x0
11	FRC_FSM_POR	R/W	forces the startup FSM to start ramp up the frequency by POR, 0: no force 1: force	0x0
12	ENA_AMP_CTRL_FORCE	R/W	enable static VCO amplitude control	0x0
13	ENA_AMPCTRL	R/W	enable automatic VCO amplitude control	0x1
14	PWD_AMPCTRL_N	R/W	force VCO amplitude control output to low (no VCO current), 0: force 1: no force	0x1
15	ENA_CLK_BYPASS	R/W	enable clock bypass for all output clocks to come from ref clock pad	0x0

2.24.1.6 L_PLL5G Configuration 2B

Short Name:L_PLL5G_CFG2B

Address:0x1E8205

Configuration register 2B for L_PLL5G

Table 1572 **• L_PLL5G Configuration 2B**

Bit	Name	Access	Description	Default
7:0	AMPC_SEL	R/W	static VCO amplitude control, active w/ ena_amp_ctrl_force, 0: lowest current 255: highest current	0x10
8	ENA_CLK_BYPASS1	R/W	enable clock bypass for all output clocks to come from extra dividers (125MHz, 250MHz, 312.5MHz)	0x0
9	ENA_CP2	R/W	enable resistor mode chargepump, test mode	0x0
10	ENA_RCPLL	R/W	enable RCPLL clock buffer in LCPLL VCO (sx_ena_vco_buf_i must be set to 0)	0x0
11	ENA_FBTESTOUT	R/W	enable feedback divider output to test output buffer	0x0
12	ENA_VCO_NREF_TESTOUT	R/W	enable VCO frequency control output	0x0
13	ENA_PFD_IN_FLIP	R/W	enable flip of refclk and fbclk at PFD, used for 2nd chargepump	0x0
14	ENA_TEST_MODE	R/W	enables test modes, e.g. fbdivsel	0x0

2.24.1.7 L_PLL5G Configuration 3A

Short Name:L_PLL5G_CFG3A

Address:0x1E8206

Configuration register 3A for L_PLL5G

Table 1573 **• L_PLL5G Configuration 3A**

Bit	Name	Access	Description	Default
7:0	FBDIVSEL	R/W	setting for feedback divider, divide by 8,10,12..255	0x28
8	FBDIVSEL_TST_ENA	R/W	enable feedback divider testmode	0x0
9	FORCE_CP	R/W	force chargepump output to nominal VCO operating point	0x0
10	FORCE_ENA	R/W	enable force VCO frequency high/low (force_hi/lo)	0x0
11	FORCE_HI	R/W	force chargepump output to high, gives highest VCO frequency	0x0
12	FORCE_LO	R/W	force chargepump output to low, gives lowest VCO frequency	0x0
13	FORCE_VCO_CONTRH	R/W	force vco contrh input to mid level (mid CML level)	0x0
14	RST_FB_N	R/W	reset for feedback divider, active low, 0: reset 1:no reset	0x1

Table 1573 • **L_PLL5G Configuration 3A *(continued)***

Bit	Name	Access	Description	Default
15	SEL_CML_CMOS_PFD	R/W	select CML or CMOS phase/frequency detector, 0: CML 1: CMOS	0x0

2.24.1.8 L_PLL5G Configuration 3B

Short Name:L_PLL5G_CFG3B

Address:0x1E8207

Configuration register 3B for L_PLL5G

Table 1574 • **L_PLL5G Configuration 3B**

Bit	Name	Access	Description	Default
0	SEL_FBDCLK	R/W	enable symmetric feedback divider clock output, 0: fbclk/2 1: fbclk	0x0
1	ENA_TEST_OUT	R/W	enable differential test output	0x1
2	ENA_ANA_TEST_OUT	R/W	enable analog test output	0x0
5:3	TESTOUT_SEL	R/W	select test output buffer input signal, 0: feedback clock 1: pad reference clock 2: core clock 3: CPU clock 4: lock toggle 5: DDR clock 6: reference clock / 2 7: ext. test input	0x4
7:6	TEST_ANA_OUT_SEL	R/W	select analog test output input signal	0x0

2.24.1.9 L_PLL5G Configuration 4A

Short Name:L_PLL5G_CFG4A

Address:0x1E8208

Configuration register 4A for L_PLL5G

Table 1575 **• L_PLL5G Configuration 4A**

Bit	Name	Access	Description	Default
15:0	IB_CTRL	R/W	Settings for LREFCK reference clock input buffer. [1:0] = select value for adjustable reference voltage from bandgap voltage: 0: 490mV 1: 508mV 2: 487mV 3: 478mV [8:2] = reserved [9] = enable common mode voltage termination to VDD: 1: enable 0: disable [10] = enable_ib 1: enable 0: disable [11] = reserved [15:12] = value for resistor calibration (RCOMP): 15: lowest value 0: highest value	0x7EE0

2.24.1.10 L_PLL5G Configuration 4B

Short Name:L_PLL5G_CFG4B

Address:0x1E8209

Configuration register 4B for L_PLL5G

Table 1576 **• L_PLL5G Configuration 4B**

Bit	Name	Access	Description	Default
7:0	IB_BIAS_CTRL	R/W	Settings for LREFCK reference clock input buffer BIAS. [0] = enable single rail input from P branch: 1: enable 0: disable [1] = enable single rail input from N branch: 1: enable 0: disable [2] = reserved [3] = enable input termination: 1: enable 0: disable [7:4] = reserved	0x08

2.24.1.11 L_PLL5G Configuration 5A

Short Name:L_PLL5G_CFG5A

Address:0x1E820A

Configuration register 5A for L_PLL5G

Table 1577 **• L_PLL5G Configuration 5A**

Bit	Name	Access	Description	Default
15:0	OB_CTRL	R/W	Settings for test output buffer. [3:0] = value for resistor calibration (RCOMP). 15: lowest value 0: highest value [7:4] = Adjustment for Common Mode Voltage, 0: off --> results in a value around 500mV: 1: 440mV 2: 480mV 3: 460mV 4: 530mV 6: 500mV 8: 570mV 12: 550mV [8] = disable VCM control: 1: disable 0: enable [9] = enable VREG measure: 1: enable 0: disable [10] = enable output buffer: 1: enable 0: disable (powerdown) [11] = reserved [15:12] = select output level: 400mVppd (0) to 1100mVppd (15) in 50mVppd steps	0x5064

2.24.1.12 L_PLL5G Configuration 5B

Short Name:L_PLL5G_CFG5B

Address:0x1E820B

Configuration register 5B for L_PLL5G

Table 1578 **• L_PLL5G Configuration 5B**

Bit	Name	Access	Description	Default
7:0	OB_BIAS_CTRL	R/W	Settings for test output buffer BIAS. [2:0] = Sets the class AB bias current in the common mode control circuit. 0.5 mA is expected to give sufficient performance (default 0x2) and is default. Other settings are for debug. Current range is 0 to 1.75 mA in 0.25mA steps [3] = enable internal CML to CMOS converter for input to test output path [5:4] = reserved [7:6] = slope/slew rate control: 0: 45ps 1: 85ps 2: 105ps 3: 115ps rise/fall time (all values are typical)	0x08

2.24.1.13 L_PLL5G Configuration 6A

Short Name:L_PLL5G_CFG6A

Address:0x1E820C

Configuration register 6A for L_PLL5G

Table 1579 **• L_PLL5G Configuration 6A**

Bit	Name	Access	Description	Default
5:0	DDR_CLK_DIV	R/W	Setting for DDR clock divider (see core_clk_div)	0x0E
6	ENA_FBCLKC2	R/W	enable feedback divider CMOS 1/2 clock (for FSM)	0x1
7	ENA_REFCLKC2	R/W	enable reference CMOS 1/2 clock	0x1
15:8	DIV125REF_SEL	R/W	select reference CML clock divider (8,9,10,12 to 255)	0x14

2.24.1.14 L_PLL5G Configuration 6B

Short Name:L_PLL5G_CFG6B

Address:0x1E820D

Configuration register 6B for L_PLL5G

Table 1580 **• L_PLL5G Configuration 6B**

Bit	Name	Access	Description	Default
1:0	POR_DEL_SEL	R/W	enable reference CMOS 1/2 clock (dummy)	0x0

2.24.1.15 L_PLL5G Status 0

Short Name:L_PLL5G_STATUS0

Address:0x1E820E

Status register 0 for the L_PLL5G

Table 1581 **• L_PLL5G Status 0**

Bit	Name	Access	Description	Default
0	LOCK_STATUS	R/O	PLL lock status, 0: not locked 1: locked	0x0
8:1	READBACK_DATA	R/O	RCPLL Interface to read back internal data of the FSM.	0x00
9	CALIBRATION_DONE	R/O	RCPLL Flag that indicates that the calibration procedure has finished.	0x0
10	CALIBRATION_ERR	R/O	RCPLL Flag that indicates errors that may occur during the calibration procedure.	0x0
11	OUT_OF_RANGE_ERR	R/O	RCPLL Flag that indicates a out of range condition while NOT in calibration mode.	0x0
12	RANGE_LIM	R/O	RCPLL Flag range limiter signaling	0x0

2.24.1.16 L_PLL5G Interrupts

Short Name:L_PLL5G_INTR

Address:0x1E8211

Interrupt registers for L_PLL5G

Table 1582 **• L_PLL5G Interrupts**

Bit	Name	Access	Description	Default
0	LOCK_STATUS_INTR	Sticky	PLL LOCK_STATUS Interrupt Register 1: L_PLL5G_STATUS0::LOCK_STATUS has changed state since the last time this interrupt bit was cleared. 0: L_PLL5G_STATUS0::LOCK_STATUS has not changed state since the last time this interrupt bit was cleared.	0x0

2.24.1.17 L_PLL5G Interrupt Masks

Short Name:L_PLL5G_INTR_MASK

Address:0x1E8212

Interrupt masks for L_PLL5G

Table 1583 **• L_PLL5G Interrupt Masks**

Bit	Name	Access	Description	Default
0	LOCK_STATUS_INTR_MASK	R/W	Interrupt mask for PLL LOCK_STATUS. L_PLL5G_INTR::LOCK_STATUS_INTR contributes to the chip's interrupt output pin when enabled. 1: Interrupt enabled 0: Interrupt disabled	0x0

2.25 F2DF_DF2F_16BIT Global (Device 0x1E)

Table 1584 • **F2DF_DF2F_STAT**

Address	Short Description	Register Name	Details
0x1EEE40	Status	F2DF_DF2F_STAT1	Page 554

Table 1585 • **SD10G65_DFT**

Address	Short Description	Register Name	Details
0x1EEE50	SD10G65 DFT Main Configuration 1	DFT_RX_CFG_1	Page 554
0x1EEE51	SD10G65 DFT Main Configuration 2	DFT_RX_CFG_2	Page 555
0x1EEE52	SD10G65 DFT Pattern Mask Configuration 1	DFT_RX_MASK_CFG_1	Page 556
0x1EEE53	SD10G65 DFT Pattern Mask Configuration 2	DFT_RX_MASK_CFG_2	Page 556
0x1EEE54	SD10G65 DFT Pattern Checker Configuration 1	DFT_RX_PAT_CFG_1	Page 556
0x1EEE55	SD10G65 DFT Pattern Checker Configuration 2	DFT_RX_PAT_CFG_2	Page 557
0x1EEE56	SD10G65 DFT BIST Configuration 0A	DFT_BIST_CFG0A	Page 557
0x1EEE57	SD10G65 DFT BIST Configuration 0B	DFT_BIST_CFG0B	Page 557
0x1EEE58	SD10G65 DFT BIST Configuration 1A	DFT_BIST_CFG1A	Page 557
0x1EEE59	SD10G65 DFT BIST Configuration 1B	DFT_BIST_CFG1B	Page 557
0x1EEE5A	SD10G65 DFT BIST Configuration 2A	DFT_BIST_CFG2A	Page 558
0x1EEE5B	SD10G65 DFT BIST Configuration 2B	DFT_BIST_CFG2B	Page 558
0x1EEE5C	SD10G65 DFT BIST Configuration 3A	DFT_BIST_CFG3A	Page 558
0x1EEE5D	SD10G65 DFT BIST Configuration 3B	DFT_BIST_CFG3B	Page 558
0x1EEE5E	SD10G65 DFT Error Status 1	DFT_ERR_STAT_1	Page 559
0x1EEE5F	SD10G65 DFT Error Status 2	DFT_ERR_STAT_2	Page 559
0x1EEE60	SD10G65 DFT PRBS Status 1	DFT_PRBS_STAT_1	Page 559
0x1EEE61	SD10G65 DFT PRBS Status 2	DFT_PRBS_STAT_2	Page 559
0x1EEE62	SD10G65 DFT Miscellaneous Status 1	DFT_MAIN_STAT_1	Page 559
0x1EEE63	SD10G65 DFT Miscellaneous Status 2	DFT_MAIN_STAT_2	Page 560
0x1EEE64	SD10G65 DFT Main Configuration	DFT_TX_CFG	Page 560
0x1EEE65	SD10G65 DFT Tx Constant Pattern Configuration 1	DFT_TX_PAT_CFG_1	Page 561
0x1EEE66	SD10G65 DFT Tx Constant Pattern Configuration 2	DFT_TX_PAT_CFG_2	Page 561
0x1EEE67	SD10G65 DFT Tx Constant Pattern Status	DFT_TX_CMP_DAT_STAT	Page 561
0x1EEE68	DFT clock compare Config	DFT_CLK_CMP_CFG	Page 562
0x1EEE69	DFT Clock Compare Timer A	DFT_CLK_CMP_TIMERA	Page 562
0x1EEE6A	DFT Clock Compare Timer B	DFT_CLK_CMP_TIMERB	Page 563
0x1EEE6B	DFT Clock Comparison Value A	DFT_CLK_CMP_VALUEA	Page 563
0x1EEE6C	DFT Clock Comparison Value B	DFT_CLK_CMP_VALUEB	Page 563

Table 1585 • **SD10G65_DFT *(continued)***

Address	Short Description	Register Name	Details
0x1EEE6D	DFT Clock Comparison Maximum Value A	DFT_CLK_CMP_MAXVALA	Page 563
0x1EEE6E	DFT Clock Comparison Maximum Value B	DFT_CLK_CMP_MAXVALB	Page 564
0x1EEE6F	DFT Tx Error Insertion Configuration 1	DFT_TX_ERR_INSERT_CFG_1	Page 564
0x1EEE70	DFT Tx Error Insertion Configuration 2	DFT_TX_ERR_INSERT_CFG_2	Page 564
0x1EEE71	DFT Clock Generator Configuration 1	DFT_CLK_GEN_CFG_1	Page 565
0x1EEE72	DFT Clock Generator Configuration 2	DFT_CLK_GEN_CFG_2	Page 565
0x1EEE73	DFT Clock Generator Configuration 3	DFT_CLK_GEN_CFG_3	Page 566

2.25.1 F2DF and DF2F Logic Configuration

2.25.1.1 SCKOUT Output C

Short Name:DF2F_DOUT_C

Address:0x1EEE30

Table 1586 • **SCKOUT Output C**

Bit	Name	Access	Description	Default
7:0	DF2F_DOUT_C	R/W	A repeating parallel data word up to 40 bits long is serialized and transmitted from the SCKOUT output. This register contains bits [39:32] of the parallel data word. Clock frequency transmitted from the pin depends upon both the parallel data word setting and the serializer configuration.	0xF0

2.25.1.2 SCKOUT Output B

Short Name:DF2F_DOUT_B

Address:0x1EEE31

Table 1587 • **SCKOUT Output B**

Bit	Name	Access	Description	Default
15:0	DF2F_DOUT_B	R/W	A repeating parallel data word up to 40 bits long is serialized and transmitted from the SCKOUT output. his register contains bits [31:16] of the parallel data word. Clock frequency transmitted from the pin depends upon both the parallel data word setting and the serializer configuration.	0xF0F0

2.25.1.3 SCKOUT Output A

Short Name:DF2F_DOUT_A

Address:0x1EEE32

Table 1588 • **SCKOUT Output A**

Bit	Name	Access	Description	Default
15:0	DF2F_DOUT_A	R/W	A repeating parallel data word up to 40 bits long is serialized and transmitted from the SCKOUT output. This register contains bits [15:0] of the parallel data word. Clock frequency transmitted from the pin depends upon both the parallel data word setting and the serializer configuration.	0xF0F0

2.25.1.4 SD10G65 Spread Spectrum Clocking

Short Name:SD10G65_SSC_SYNC

Address:0x1EEE33

SD10G65 Spread Spectrum Clocking

Table 1589 • **SD10G65 Spread Spectrum Clocking**

Bit	Name	Access	Description	Default
4	SSC_SYNC_STAT	R/O	Spread Spectrum Clocking Output	0x0
0	SSC_SYNC_CFG	R/W	Spread Spectrum Clocking Input	0x0

2.25.1.5 SD10G65 Smooth Clocking Update

Short Name:SD10G65_SMOOTH_UPDATE

Address:0x1EEE34

SD10G65 Smooth Clocking Update

Table 1590 • **SD10G65 Smooth Clocking Update**

Bit	Name	Access	Description	Default
0	SMOOTH_UPDATE	R/W	Smooth Update	0x0

2.25.1.6 SD10G65 Smooth Clocking Value MSB

Short Name:SD10G65_SMOOTH_VALUE_MSB

Address:0x1EEE35

SD10G65 Smooth Clocking Value MSB

Table 1591 • **SD10G65 Smooth Clocking Value MSB**

Bit	Name	Access	Description	Default
6:0	SMOOTH_VALUE_MSB	R/W	Smooth Clocking Value MSB bit [22:16]	0x00

2.25.1.7 SD10G65 Smooth Clocking Value LSB

Short Name:SD10G65_SMOOTH_VALUE_LSB

Address:0x1EEE36

SD10G65 Smooth Clocking Value LSB

Table 1592 **• SD10G65 Smooth Clocking Value LSB**

Bit	Name	Access	Description	Default
15:0	SMOOTH_VALUE_LSB	R/W	Smooth Clocking Value LSB bit [15:0]	0x0000

2.25.2 F2DF and DF2F Logic Status

2.25.2.1 Status

Short Name:F2DF_DF2F_STAT1

Address:0x1EEE40

Table 1593 **• Status**

Bit	Name	Access	Description	Default
4	PLL_LOCK_TX	R/O	Indicates PLL lock status for the DF2F serializer. 1 = Locked 0 = Not locked	0x0
1	F2DF_SIG_DET	R/O	Signal detect status from the F2DF deserializer. 1 = Signal detected 0 = Signal not detected	0x0
0	PLL_LOCK_RX	R/O	Indicates PLL lock status for the F2DF deserializer. 1 = Locked 0 = Not locked	0x0

2.25.3 DFT Configuration and Status

Configuration and status register set for SD10G65 DFT

2.25.3.1 SD10G65 DFT Main Configuration 1

Short Name:DFT_RX_CFG_1

Address:0x1EEE50

Main configuration register 1 for SD10G65 DFT.

Table 1594 **• SD10G65 DFT Main Configuration 1**

Bit	Name	Access	Description	Default
12	STUCK_AT_PAR_MASK_CFG	R/W	Disables error generation based on stuck_at_par errors, 0: stuck_at_par error generates 63 errors per clock cycle (in PRBS mode only) 1: stuck_at_par error does not generate errors	0x1
11	STUCK_AT_01_MASK_CFG	R/W	Disables error generation based on stuck_at_01 errors, 0: stuck_at_01 error generates 63 errors per clock cycle (in PRBS mode only) 1: stuck_at_01 error does not generate errors	0x0
10	DIRECT_THROUGH_ENA_CFG	R/W	Enables data through from gearbox to gearbox	0x0
9	ERR_CNT_CAPT_CFG	R/W	Captures data from error counter to allow reading of stable data	0x0

Table 1594 • **SD10G65 DFT Main Configuration 1** ***(continued)***

Bit	Name	Access	Description	Default
8:7	RX_DATA_SRC_SEL	R/W	Data source selection 0: main path 1: vscope high path 2: vscope low path	0x0
6:5	BIST_CNT_CFG	R/W	States in which error counting is enabled 3:all but IDLE; 2:check 1:stable+check 0:wait_stable+stable+check	0x0
4	FREEZE_PATTERN_CFG	R/W	Disable change of stored patterns (e.g. to avoid changes during read-out)	0x0
3	CHK_MODE_CFG	R/W	Selects pattern to check 0: PRBS pattern 1: constant pattern	0x0
2:0	RX_WID_SEL_CFG	R/W	Selects DES interface width 0:8 1:10 2:16 3:20 4:32 5:40 (default)	0x4

2.25.3.2 SD10G65 DFT Main Configuration 2

Short Name:DFT_RX_CFG_2

Address:0x1EEE51

Main configuration register 2 for SD10G65 DFT.

Table 1595 • **SD10G65 DFT Main Configuration 2**

Bit	Name	Access	Description	Default
14	RX_WORD_MODE_CFG	R/W	Pattern generator: 0:bytes mode; 1:10-bits word mode	0x0
13:11	RX_PRBS_SEL_CFG	R/W	Selects PRBS check 0: prbs7 1: prbs15 2: prbs23 3: prbs11 4: prbs31 (default) 5: prbs9	0x4
10	INV_ENA_CFG	R/W	Enables PRBS checker input inversion	0x0
9	CMP_MODE_CFG	R/W	Selects compare mode 0: compare mode possible 1 learn mode is forced	0x0
8:6	LRN_CNT_CFG	R/W	Number of consecutive errors/non-errors before transitioning to respective state value = num-40-bits-words + 1	0x0
5	CNT_RST	R/W	SW reset of error counter; rising edge activates reset	0x0

Table 1595 • **SD10G65 DFT Main Configuration 2** ***(continued)***

Bit	Name	Access	Description	Default
4:3	CNT_CFG	R/W	Selects modes in which error counter is active 0:learn and compare mode 1:transition between modes 2:learn mode 3:compare mode	0x0
2:1	BIST_MODE_CFG	R/W	BIST mode 0: off 1: BIST 2: BER 3:CONT (infinite mode)	0x3
0	DFT_RX_ENA	R/W	Enable Rx DFT capability 0: Disable DFT 1: Enable DFT	0x0

2.25.3.3 SD10G65 DFT Pattern Mask Configuration 1

Short Name:DFT_RX_MASK_CFG_1

Address:0x1EEE52

Configuration register 1 for SD10G65 DFT to mask data bits preventing error counting for these bits.

Table 1596 • **SD10G65 DFT Pattern Mask Configuration 1**

Bit	Name	Access	Description	Default
15:0	LSB_MASK_CFG_1	R/W	Mask out (active high) errors in 16 bit MSB data bits [31:16]	0x0000

2.25.3.4 SD10G65 DFT Pattern Mask Configuration 2

Short Name:DFT_RX_MASK_CFG_2

Address:0x1EEE53

Configuration register 2 for SD10G65 DFT to mask data bits preventing error counting for these bits.

Table 1597 • **SD10G65 DFT Pattern Mask Configuration 2**

Bit	Name	Access	Description	Default
15:0	LSB_MASK_CFG_2	R/W	Mask out (active high) errors in 16 LSB data bits [15:0]	0x0000

2.25.3.5 SD10G65 DFT Pattern Checker Configuration 1

Short Name:DFT_RX_PAT_CFG_1

Address:0x1EEE54

Pattern checker configuration register 1 for SD10G65 DFT.

Table 1598 • **SD10G65 DFT Pattern Checker Configuration 1**

Bit	Name	Access	Description	Default
15:8	MSB_MASK_CFG	R/W	Mask out (active high) errors in 8 MSB data bits	0x00
0	PAT_READ_CFG	R/W	Pattern read enable	0x0

2.25.3.6 SD10G65 DFT Pattern Checker Configuration 2

Short Name:DFT_RX_PAT_CFG_2

Address:0x1EEE55

Pattern checker configuration register 2 for SD10G65 DFT.

***Table 1599* • SD10G65 DFT Pattern Checker Configuration 2**

Bit	Name	Access	Description	Default
11:8	MAX_ADDR_CHK_CFG	R/W	Maximum address in Checker (before continuing with address 0)	0x0
3:0	READ_ADDR_CFG	R/W	Address to read patterns from used by SW	0x0

2.25.3.7 SD10G65 DFT BIST Configuration A

Short Name:DFT_BIST_CFG0A

Address:0x1EEE56

BIST configuration register A for SD10G65 DFT controlling 'check and wait-stable' mode.

***Table 1600* • SD10G65 DFT BIST Configuration A**

Bit	Name	Access	Description	Default
15:0	WAKEUP_DLY_CFG	R/W	BIST FSM: threshold to leave DOZE state	0x0000

2.25.3.8 SD10G65 DFT BIST Configuration B

Short Name:DFT_BIST_CFG0B

Address:0x1EEE57

BIST configuration register B for SD10G65 DFT controlling 'check and wait-stable' mode.

***Table 1601* • SD10G65 DFT BIST Configuration B**

Bit	Name	Access	Description	Default
15:0	MAX_BIST_FRAMES_CFG	R/W	BIST FSM: threshold to enter FINISHED state	0x0000

2.25.3.9 SD10G65 DFT BIST Configuration A

Short Name:DFT_BIST_CFG1A

Address:0x1EEE58

BIST configuration register A for SD10G65 DFT controlling 'stable' mode.

***Table 1602* • SD10G65 DFT BIST Configuration A**

Bit	Name	Access	Description	Default
15:0	MAX_UNSTABLE_CYC_CFG	R/W	BIST FSM: threshold to iterate counter for max_stable_attempts	0x0000

2.25.3.10 SD10G65 DFT BIST Configuration B

Short Name:DFT_BIST_CFG1B

Address:0x1EEE59

BIST configuration register B for SD10G65 DFT controlling 'stable' mode.

Table 1603 **• SD10G65 DFT BIST Configuration B**

Bit	Name	Access	Description	Default
15:0	STABLE_THRES_CFG	R/W	BIST FSM: threshold to enter CHECK state	0x0000

2.25.3.11 SD10G65 DFT BIST Configuration A

Short Name:DFT_BIST_CFG2A

Address:0x1EEE5A

BIST configuration register B for SD10G65 DFT controlling frame length in 'check' mode.

Table 1604 **• SD10G65 DFT BIST Configuration A**

Bit	Name	Access	Description	Default
15:0	FRAME_LEN_CFG_MSB	R/W	BIST FSM: threshold to iterate counter for max_bist_frames [31:16]	0x0000

2.25.3.12 SD10G65 DFT BIST Configuration B

Short Name:DFT_BIST_CFG2B

Address:0x1EEE5B

BIST configuration register B for SD10G65 DFT controlling frame length in 'check' mode.

Table 1605 **• SD10G65 DFT BIST Configuration B**

Bit	Name	Access	Description	Default
15:0	FRAME_LEN_CFG_LSB	R/W	BIST FSM: threshold to iterate counter for max_bist_frames [15:0]	0x0000

2.25.3.13 SD10G65 DFT BIST Configuration A

Short Name:DFT_BIST_CFG3A

Address:0x1EEE5C

BIST configuration register A for SD10G65 DFT controlling stable attempts in ' wait-stable' mode.

Table 1606 **• SD10G65 DFT BIST Configuration A**

Bit	Name	Access	Description	Default
15:0	MAX_STABLE_ATTEMPTS_CFG_MSB	R/W	BIST FSM: threshold to enter SYNC_ERR state [31:16]	0x0000

2.25.3.14 SD10G65 DFT BIST Configuration B

Short Name:DFT_BIST_CFG3B

Address:0x1EEE5D

BIST configuration register B for SD10G65 DFT controlling stable attempts in ' wait-stable' mode.

Table 1607 **• SD10G65 DFT BIST Configuration B**

Bit	Name	Access	Description	Default
15:0	MAX_STABLE_ATTEMPTS_CFG_LSB	R/W	BIST FSM: threshold to enter SYNC_ERR state [15:0]	0x0000

2.25.3.15 SD10G65 DFT Error Status 1

Short Name:DFT_ERR_STAT_1

Address:0x1EEE5E

Status register 1 for SD10G65 DFT containing the error counter value

Table 1608 **• SD10G65 DFT Error Status 1**

Bit	Name	Access	Description	Default
15:0	ERR_CNT_MSB	R/O	Counter output depending on cnt_cfg [31:16]	0x0000

2.25.3.16 SD10G65 DFT Error Status 2

Short Name:DFT_ERR_STAT_2

Address:0x1EEE5F

Status register B2 for SD10G65 DFT containing the error counter value

Table 1609 **• SD10G65 DFT Error Status 2**

Bit	Name	Access	Description	Default
15:0	ERR_CNT_LSB	R/O	Counter output depending on cnt_cfg [15:0]	0x0000

2.25.3.17 SD10G65 DFT PRBS Status 1

Short Name:DFT_PRBS_STAT_1

Address:0x1EEE60

Status register 1 for SD10G65 DFT containing the PRBS data related to 1st sync lost event

Table 1610 **• SD10G65 DFT PRBS status 1**

Bit	Name	Access	Description	Default
15:0	PRBS_DATA_STAT_MSB	R/O	PRBS data after first sync lost [31:16]	0x0000

2.25.3.18 SD10G65 DFT PRBS Status 2

Short Name:DFT_PRBS_STAT_2

Address:0x1EEE61

Status register 2 for SD10G65 DFT containing the PRBS data related to 1st sync lost event

Table 1611 **• SD10G65 DFT PRBS Status 2**

Bit	Name	Access	Description	Default
15:0	PRBS_DATA_STAT_LSB	R/O	PRBS data after first sync lost [15:0]	0x0000

2.25.3.19 SD10G65 DFT Miscellaneous Status 1

Short Name:DFT_MAIN_STAT_1

Address:0x1EEE62

Status register 1 for SD10G65 DFT

Table 1612 **• SD10G65 DFT Miscellaneous Status 1**

Bit	Name	Access	Description	Default
9:0	CMP_DATA_STAT	R/O	10 bits data word at address 'read_addr_cfg' used for further observation by SW	0x000

2.25.3.20 SD10G65 DFT Miscellaneous Status 2

Short Name:DFT_MAIN_STAT_2

Address:0x1EEE63

Status register 2 for SD10G65 DFT

Table 1613 **• SD10G65 DFT Miscellaneous Status 2**

Bit	Name	Access	Description	Default
5	STUCK_AT_PAR	R/O	Data input is unchanged for all 40 parallel bits for at least 7 clock cycles (defined by c_STCK_CNT_THRES)	0x0
4	STUCK_AT_01	R/O	Data input is constantly 0 or constantly 1 for all 40 parallel bits for at least 7 clock cycles (defined by c_STCK_CNT_THRES)	0x0
3	NO_SYNC	R/O	BIST: no sync found since BIST enabled	0x0
2	INSTABLE	R/O	BIST: input data not stable	0x0
1	INCOMPLETE	R/O	BIST not complete (i.e. not reached stable state or following)	0x0
0	ACTIVE	R/O	BIST is active (i.e. left DOZE but did not enter a final state)	0x0

2.25.3.21 SD10G65 DFT Main Configuration

Short Name:DFT_TX_CFG

Address:0x1EEE64

Main configuration register for SD10G65 DFT.

Table 1614 **• SD10G65 DFT Main Configuration**

Bit	Name	Access	Description	Default
12	RST_ON_STUCK_AT_CFG	R/W	Enables (1) reset of PRBS generator in case of unchanged data ('stuck-at') for at least 511 clock cycles. Can be disabled (0) e.g. in scrambler mode to avoid the very rare case that input patterns allow to keep the generator's shift register filled with a constant value.	0x1
11:9	TX_WID_SEL_CFG	R/W	Selects SER interface width 0:8 1:10 2:16 3:20 4:32 5:40 (default)	0x4

Table 1614 • **SD10G65 DFT Main Configuration** ***(continued)***

Bit	Name	Access	Description	Default
8:6	TX_PRBS_SEL_CFG	R/W	Selects PRBS generator 0: prbs7 1: prbs15 2: prbs23 3: prbs11 4: prbs31 (default) 5: prbs9	0x4
5	SCRAM_INV_CFG	R/W	Inverts the scrambler output	0x0
4	IPATH_CFG	R/W	Selects PRBS generator input 0:pat-gen 1:core	0x0
3:2	OPATH_CFG	R/W	Selects DFT-Tx output 0:PRBS/scrambler (default) 1:bypass	0x0
1	TX_WORD_MODE_CFG	R/W	Word width of constant pattern generator 0:bytes mode; 1:10-bits word mode	0x0
0	DFT_TX_ENA	R/W	Enable Tx DFT capability 0: Disable DFT 1: Enable DFT	0x0

2.25.3.22 SD10G65 DFT Tx Constant Pattern Configuration 1

Short Name:DFT_TX_PAT_CFG_1

Address:0x1EEE65

Tx Constant MSB pattern configuration register 1 for SD10G65 DFT.

Table 1615 • **SD10G65 DFT Tx Constant Pattern Configuration 1**

Bit	Name	Access	Description	Default
4	PAT_VLD_CFG	R/W	Constant patterns are valid to store	0x0
3:0	MAX_ADDR_GEN_CFG	R/W	Maximum address in generator (before continuing with address 0)	0x0

2.25.3.23 SD10G65 DFT Tx Constant Pattern Configuration 2

Short Name:DFT_TX_PAT_CFG_2

Address:0x1EEE66

Tx Constant MSB pattern configuration register 2 for SD10G65 DFT.

Table 1616 • **SD10G65 DFT Tx Constant Pattern Configuration 2**

Bit	Name	Access	Description	Default
13:10	STORE_ADDR_CFG	R/W	Current storage address for patterns in generator	0x0
9:0	PATTERN_CFG	R/W	10 bits word of constant patterns for transmission	0x000

2.25.3.24 SD10G65 DFT Tx Constant Pattern Status

Short Name:DFT_TX_CMP_DAT_STAT

Address:0x1EEE67

Status register for SD10G65 DFT containing the constant patterns used for comparison (last in LEARN mode)

Table 1617 **• SD10G65 DFT Tx Constant Pattern Status**

Bit	Name	Access	Description	Default
12	TX_STUCK_AT_STICKY	Sticky	Scrambler/PRBS generator output unchanged for at least 511 clock cycles. The high state is cleared by writing a 1 to the bit.	0x0
9:0	PAT_STAT	R/O	10 bits data word at address 'store_addr_cfg' used for further observation by SW	0x000

2.25.3.25 DFT Clock Compare Config

Short Name:DFT_CLK_CMP_CFG

Address:0x1EEE68

Configuration register for Clock Compare logic. Compared clocks are always divided by 4 before any further processing. A clock edge on tx_clk increments the counter, a clock edge on rx_clk decrements the counter. If only one clock is selected for clock comparison, the number of clock cycles within a given time can be measured.

Table 1618 **• DFT Clock Compare Config**

Bit	Name	Access	Description	Default
12	CLK_CMP_UPDTOG	R/O	Clock compare value updated toggle bit. Toggles on each update of CLK_CMP_VALUE	0x0
8	CLK_CMP_WRAP_ENA	R/W	Enable clock comparison counter wrap 0: counter saturates 1: counter wraps	0x0
7:6	CLK_CMP_DIV_TX	R/W	Clock compare divider for Tx clock 0: tx clk 1: tx_clk/2 2: tx_clk/4 3: tx_clk/8	0x3
5:4	CLK_CMP_DIV_RX	R/W	Clock compare divider for Rx clock 0: rx clk 1: rx_clk/2 2: rx_clk/4 3: rx_clk/8	0x3
3:2	CLK_CMP_SEL	R/W	Clock compare selection 0: rx_clk vs. tx_clk 1: rx_clk 2: tx_clk 3: Reserved	0x0
1	CLK_CMP_MODE	R/W	Clock comparison mode 0: single shot 1: continuous	0x0
0	CLK_CMP_ENA	R/W	Enable clock comparison (enabling automatically clears comparison counter)	0x0

2.25.3.26 DFT Clock Compare Timer A

Short Name:DFT_CLK_CMP_TIMERA

Address:0x1EEE69

Upper half of clock comparison timer. After timer has expired, current clock comparison value is stored. The timer is clocked at 156.25 MHz.

Table 1619 **• DFT Clock Compare Timer**

Bit	Name	Access	Description	Default
15:0	CLK_CMP_TIMER_MSB	R/W	Clock comparison timer, bits [31:16]. Counter interval is N + 1 clock cycles where the clock frequency is 156.25 MHz.	0x0950

2.25.3.27 DFT Clock Compare Timer B

Short Name:DFT_CLK_CMP_TIMERB

Address:0x1EEE6A

Lower half of clock comparison timer. After timer has expired, current clock comparison value is stored. The timer is clocked at 156.25 MHz.

Table 1620 **• DFT Clock Compare Timer B**

Bit	Name	Access	Description	Default
15:0	CLK_CMP_TIMER_LSB	R/W	Clock comparison timer, bits [15:0]. Counter interval is N + 1 clock cycles where the clock frequency is 156.25 MHz.	0x2F8F

2.25.3.28 DFT Clock Comparison Value A

Short Name:DFT_CLK_CMP_VALUEA

Address:0x1EEE6B

Upper half of clock comparison result. This register is updated after clock comparison timer has expired. In continuous mode this register is periodically updated.

Table 1621 **• DFT Clock Comparison Value A**

Bit	Name	Access	Description	Default
15:0	CLK_CMP_VALUE_MSB	R/O	Clock comparison value (difference between clk0 and clk1), bits [31:16]	0x0000

2.25.3.29 DFT Clock Comparison Value B

Short Name:DFT_CLK_CMP_VALUEB

Address:0x1EEE6C

Lower half of clock comparison result. This register is updated after clock comparison timer has expired. In continuous mode this register is periodically updated.

Table 1622 **• DFT Clock Comparison Value B**

Bit	Name	Access	Description	Default
15:0	CLK_CMP_VALUE_LSB	R/O	Clock comparison value (difference between clk0 and clk1), bits [15:0]	0x0000

2.25.3.30 DFT Clock Comparison Maximum Value A

Short Name:DFT_CLK_CMP_MAXVALA

Address:0x1EEE6D

Upper half of clock comparison max result. Can be used to judge e.g. SSC clock deviation. This register is updated after clock comparison timer has expired. In continuous mode this register is periodically updated.

Table 1623 **• DFT Clock Comparison Maximum Value A**

Bit	Name	Access	Description	Default
15:0	CLK_CMP_MAXVAL_MSB	R/O	Clock comparison max value (maximum measured difference between clk0 and clk1), bits [31:16]	0x0000

2.25.3.31 DFT Clock Comparison Maximum Value B

Short Name:DFT_CLK_CMP_MAXVALB

Address:0x1EEE6E

Lower half of clock comparison max result. Can be used to judge e.g. SSC clock deviation. This register is updated after clock comparison timer has expired. In continuous mode this register is periodically updated.

Table 1624 **• DFT Clock Comparison Maximum Value B**

Bit	Name	Access	Description	Default
15:0	CLK_CMP_MAXVAL_LSB	R/O	Clock comparison max value (maximum measured difference between clk0 and clk1), bits [15:0]	0x0000

2.25.3.32 DFT Tx Error Insertion Configuration 1

Short Name:DFT_TX_ERR_INSERT_CFG_1

Address:0x1EEE6F

Configuration register for explicit error insertion into DFT driven data stream. Allows to insert expected errors to check e.g. Tx/Rx connectivity

Table 1625 **• DFT Tx Error Insertion Configuration 1**

Bit	Name	Access	Description	Default
15:6	CG_TIMER_CFG	R/W	Preload value for clock generator timer	0x000
4	ERR_TRIG_ONESHOT_CFG	R/W	Trigger a single error or a burst of errors (refer to num_err_cfg) 0 to 1 (edge) activates this function	0x0
3:0	ERR_FREQ_CFG	R/W	Frequency of continuous/limited error insertion in steps of 40 bits 0: disable continuous insertion 1-15: step between 2 errors = 2^(err_freq_cfg + 5) 40 bit words (refer also to err_posit_offs_cfg)	0x0

2.25.3.33 DFT Tx Error Insertion Configuration

Short Name:DFT_TX_ERR_INSERT_CFG_2

Address:0x1EEE70

Configuration register for explicit error insertion into DFT driven data stream. Allows to insert expected errors to check e.g. Tx/Rx connectivity

Table 1626 **• DFT Tx Error Insertion Configuration**

Bit	Name	Access	Description	Default
15:10	ERR_POSIT_CFG	R/W	Position within 40 bit word where an error is inserted by inverting the bit value 0: LSB 39: MSB 40-63: reserved	0x00
9:4	ERR_POSIT_OFFS_CFG	R/W	Offset of bit position increased per inserted error; allows 'walking' error. Offset is reset when continuous/limited error insertion is disabled or burst mode is enabled and burst insertion is finished or err_posit_offs_cfg = 0 0: disabled 1: move 1 bit (from LSB to MSB) ... 39: move 39 bit (from LSB to MSB) 40-63: reserved	0x00
3:0	NUM_ERR_CFG	R/W	limited error insertion: burst mode (err_freq_cfg must be > 0) 0: burst mode is disabled 1-15: number of errors after each error triggering = 2^(num_err_cfg + 5)	0x0

2.25.3.34 DFT Clock Generator Configuration 1

Short Name:DFT_CLK_GEN_CFG_1

Address:0x1EEE71

Configuration register for clock generator to build a low speed clock signal of variable length and variable duty cycle provided on all data bits simultaneously

Table 1627 **• DFT Clock Generator Configuration 1**

Bit	Name	Access	Description	Default
9:0	CG_PER_CFG	R/W	(Half) clock period cfg in normal mode: high period = cg_per_cfg + cg_dcd_cfg, low period = cg_per_cfg - cg_dcd_cfg	0x000

2.25.3.35 DFT Clock Generator Configuration 2

Short Name:DFT_CLK_GEN_CFG_2

Address:0x1EEE72

Configuration register for clock generator to build a low speed clock signal of variable length and variable duty cycle provided on all data bits simultaneously

Table 1628 **• DFT Clock Generator Configuration 2**

Bit	Name	Access	Description	Default
9:0	CG_PER_JUMP_CFG	R/W	(Half) clock period cfg in jump mode: high period = cg_per_cfg + cg_dcd_cfg, low period = cg_per_cfg - cg_dcd_cfg	0x000

2.25.3.36 DFT Clock Generator Configuration 3

Short Name:DFT_CLK_GEN_CFG_3

Address:0x1EEE73

Configuration register for clock generator to build a low speed clock signal of variable length and variable duty cycle provided on all data bits simultaneously

Table 1629 **• DFT Clock Generator Configuration 3**

Bit	Name	Access	Description	Default
11:2	CG_DCD_CFG	R/W	Duty cycle distortion: high period = cg_per_cfg + cg_dcd_cfg, low period = cg_per_cfg - cg_dcd_cfg	0x000
1:0	CG_MODE_CFG	R/W	clock generator mode 0: normal operation cg_per_cfg controls period; 0->1 transition: after current period has finished (only) the next period is controlled by cg_per_jump_cfg afterwards normal operation; 2: every N'th period the high value is replaced by a low value N is defined by cg_timer_cfg; 3: every N'th period the low value is replaced by a high value N is defined by cg_timer_cfg	0x0

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Table 1630 **• SD10G65_ACC**

Address	Short Description	Register Name	Details
0x1EEF00	APC top control configuration	APC_TOP_CTRL_CFG	Page 568
0x1EEF01	APC common configuration 0	APC_COMMON_CFG0	Page 568
0x1EEF02	APC FLEXCTRL read counter	APC_FLEXCTRL_CNT_STATUS	Page 569
0x1EEF03	APC level detect calibration configuration	APC_LD_CAL_CFG	Page 570
0x1EEF04	APC sampling stage calibration configuration 0	APC_IS_CAL_CFG0	Page 570
0x1EEF05	APC sampling stage calibration configuration 1	APC_IS_CAL_CFG1	Page 571

Table 1631 **• SD10G65_DES**

Address	Short Description	Register Name	Details
0x1EF000	SD10G65 DES Configuration 0	SD10G65_DES_CFG0	Page 571
0x1EF001	SD10G65 MOEBDIV Configuration 0	SD10G65_MOEBDIV_CFG0	Page 572

Table 1632 **• SD10G65_OB**

Address	Short Description	Register Name	Details
0x1EF010	SD10G65 OB Configuration 0	SD10G65_OB_CFG0	Page 572
0x1EF011	SD10G65 OB Configuration 1	SD10G65_OB_CFG1	Page 573
0x1EF012	SD10G65 OB Configuration 2	SD10G65_OB_CFG2	Page 574

Table 1632 • **SD10G65_OB *(continued)***

Address	Short Description	Register Name	Details
0x1EF013	SD10G65 OB Configuration 3	SD10G65_OB_CFG3	Page 575

Table 1633 • **SD10G65_IB**

Address	Short Description	Register Name	Details
0x1EF020	SD10G65 IB Configuration 0	SD10G65_IB_CFG0	Page 575
0x1EF021	SD10G65 IB Configuration 1	SD10G65_IB_CFG1	Page 577
0x1EF022	SD10G65 IB Configuration 2	SD10G65_IB_CFG2	Page 578
0x1EF023	SD10G65 IB Configuration 3	SD10G65_IB_CFG3	Page 578
0x1EF024	SD10G65 IB Configuration 4	SD10G65_IB_CFG4	Page 580
0x1EF025	SD10G65 IB Configuration 5	SD10G65_IB_CFG5	Page 580
0x1EF026	SD10G65 IB Configuration 6	SD10G65_IB_CFG6	Page 582
0x1EF027	SD10G65 IB Configuration 7	SD10G65_IB_CFG7	Page 583
0x1EF028	SD10G65 IB Configuration 8	SD10G65_IB_CFG8	Page 583
0x1EF029	SD10G65 IB Configuration 9	SD10G65_IB_CFG9	Page 584
0x1EF02A	SD10G65 IB Configuration 10	SD10G65_IB_CFG10	Page 584
0x1EF02B	SD10G65 IB Configuration 11	SD10G65_IB_CFG11	Page 585
0x1EF02C	SD10G65 SBUS Rx CFG Service-Bus related setting	SD10G65_SBUS_RX_CFG	Page 586

Table 1634 • **SD10G65_RX_RCPLL**

Address	Short Description	Register Name	Details
0x1EF030	SD10G65 Rx RCPLL Configuration 0	SD10G65_RX_RCPLL_CFG0	Page 587
0x1EF031	SD10G65 Rx RCPLL Configuration 1	SD10G65_RX_RCPLL_CFG1	Page 587
0x1EF032	SD10G65 Rx RCPLL Configuration 2	SD10G65_RX_RCPLL_CFG2	Page 588
0x1EF033	SD10G65 Rx RCPLL Status 0	SD10G65_RX_RCPLL_STAT0	Page 588

Table 1635 • **SD10G65_RX_SYNTH**

Address	Short Description	Register Name	Details
0x1EF040	SD10G65 Rx Synthesizer Configuration 0	SD10G65_RX_SYNTH_CFG0	Page 589
0x1EF041	SD10G65 Rx Synthesizer Configuration 1	SD10G65_RX_SYNTH_CFG1	Page 589
0x1EF042	SD10G65 Rx Synthesizer Configuration 2	SD10G65_RX_SYNTH_CFG2	Page 589
0x1EF043	SD10G65 Rx Synthesizer Configuration 3	SD10G65_RX_SYNTH_CFG3	Page 590
0x1EF044	SD10G65 Rx Synthesizer Configuration 4	SD10G65_RX_SYNTH_CFG4	Page 590
0x1EF045	SD10G65 Rx Synthesizer Register CDR loopfilter Control	SD10G65_RX_SYNTH_CDRLF	Page 591
0x1EF046	SD10G65 Rx Synthesizer Register 0 for qualifier access	SD10G65_RX_SYNTH_QUALIFIER0	Page 591

Table 1635 • **SD10G65_RX_SYNTH *(continued)***

Address	Short Description	Register Name	Details
0x1EF047	SD10G65 Rx Synthesizer Register 1 for Qualifier Access	SD10G65_RX_SYNTH_QUALIFIER1	Page 592
0x1EF048	SD10G65 Rx Synthesizer Register for Sync Control Data	SD10G65_RX_SYNTH_SYNC_CTRL	Page 592
0x1EF049	F2DF Configuration / Status	F2DF_CFG_STAT	Page 592

Table 1636 • **SD10G65_TX_SYNTH**

Address	Short Description	Register Name	Details
0x1EF050	SD10G65 Tx Synthesizer Configuration 0	SD10G65_TX_SYNTH_CFG0	Page 593
0x1EF051	SD10G65 Tx Synthesizer Configuration 1	SD10G65_TX_SYNTH_CFG1	Page 593
0x1EF052	SD10G65 Tx Synthesizer Configuration 3	SD10G65_TX_SYNTH_CFG3	Page 594
0x1EF053	SD10G65 Tx Synthesizer Configuration 4	SD10G65_TX_SYNTH_CFG4	Page 594
0x1EF054	SD10G65 SSC Generator Configuration 0	SD10G65_SSC_CFG0	Page 594
0x1EF055	SD10G65 SSC Generator Configuration 1	SD10G65_SSC_CFG1	Page 594

Table 1637 • **SD10G65_TX_RCPLL**

Address	Short Description	Register Name	Details
0x1EF060	SD10G65 Tx RCPLL Configuration 0	SD10G65_TX_RCPLL_CFG0	Page 595
0x1EF061	SD10G65 Tx RCPLL Configuration 1	SD10G65_TX_RCPLL_CFG1	Page 595
0x1EF062	SD10G65 Tx RCPLL Configuration 2	SD10G65_TX_RCPLL_CFG2	Page 596
0x1EF063	SD10G65 Tx RCPLL Status 0	SD10G65_TX_RCPLL_STAT0	Page 597

2.26.1 SD10G65 ACC Configuration and Status

Configuration and status register set for SD10G65 ACC (Automatic Calibration Control)

2.26.1.1 APC Top Control Configuration

Short Name:APC_TOP_CTRL_CFG

Address:0x1EEF00

Configuration register for top control logic

Table 1638 • **APC Top Control Configuration**

Bit	Name	Access	Description	Default
31:24	PWR_UP_TIME	R/W	Delay time required to power up auxiliary channels	0x0F
23:16	PWR_DN_TIME	R/W	Delay time required to power down auxiliary channels	0x05

2.26.1.2 APC Common Configuration 0

Short Name:APC_COMMON_CFG0

Address:0x1EEF01

Common configurations 0 for APC logic.

Table 1639 **• APC Common Configuration 0**

Bit	Name	Access	Description	Default
19:16	TOP_CTRL_STATE	R/O	Current state of APC top control state machine	0x0
15:12	BLOCK_READ_SEL	R/W	Select flexctrl block in order to read internal counters. Counter values readable from APC_FLEXCTRL_CNT_STATUS. 0: Offset-ctrl 1: L-ctrl 2: C-ctrl 3: AGC-ctrl 4: DFE1-ctrl 5: DFE2-ctrl 6: DFE3-ctrl 7: DFE4-ctrl 8: SAM_Offset-cal 9: Level-cal 10: HML sampling errors	0x0
11	RESET_APC	R/W	Reset APC core logic (configuration registers are not reset) 1: Reset APC 0: Normal operation (mission mode)	0x0
8:6	IF_WIDTH	R/W	Interface bit-width 0: 8-bit 1: 10-bit 2: 16-bit 3: 20-bit 4: 32-bit 5: 40-bit	0x4
3	APC_DIRECT_ENA	R/W	Enable APC direct connections instead of local IB configuration registers.	0x0
2:0	APC_MODE	R/W	APC operation mode 0: Off 1: Manual mode 2: Perform calibrarion and run FSM1 3: Perform calibration and run FSM2 4: Perform calibration and run FSM1 and FSM2 in ping-pong operation 5: Perform calibration and then enter manual mode	0x0

2.26.1.3 APC FLEXCTRL Read Counter

Short Name:APC_FLEXCTRL_CNT_STATUS

Address:0x1EEF02

Observation register for multiple counters. The selection is done via APC_COMMON_CFG.BLOCK_READ_SEL (select flexctrl block to be read) and APC_XXX_CTRL.XXX_READ_CNT_SEL (counter within flexctrl block XXX) or

APC_COMMON_CFG.OFFSCAL_READ_CNT_SEL. Note that the EQZ and DFE counters hit_cnt and err_cnt make only sense in DISCRETE control mode.

Table 1640 • **APC FLEXCTRL Read Counter**

Bit	Name	Access	Description	Default
31:0	APC_CTRL_CNTVAL	R/O	Current counter value	0x00000000

2.26.1.4 APC Level Detect Calibration Configuration

Short Name:APC_LD_CAL_CFG

Address:0x1EEF03

Configuration register for APC level detect calibrations logic

Table 1641 • **APC Level Detect Calibration Configuration**

Bit	Name	Access	Description	Default
30:28	CAL_CLK_DIV	R/W	Calibration clock divider. Clock used in calibration blocks is divided by 2^(2*CAL_CLK_DIV) 0: No clock division 1: Clock is divided by 4 2: Clock is divided by 16 ... 7: Clock is divided by 16384	0x2
19	DETLEV_CAL_DONE	R/O	Detect level calibration state 1: finished	0x0
12	SKIP_SDET_CAL	R/W	Skip signal detect calibration	0x0
11	SKIP_LD_CAL	R/W	Skip level detect calibration	0x0
10:5	IE_SDET_LEVEL	R/W	Level for IE signal detect (when controlled by APC) 0: 20mV	0x02
4:1	DETLVL_TIMER	R/W	Timer for calibration process 14: Use for 400MHz rx_clk	0xE
0	START_DETLVL_CAL	R/W	Start signal and level detect calibration process (sampling stage; only in manual mode, see apc_mode)	0x0

2.26.1.5 APC Sampling Stage Calibration Configuration 0

Short Name:APC_IS_CAL_CFG0

Address:0x1EEF04

Configuration register 0 for APC sampling stage calibrations logic

Table 1642 • **APC Sampling Stage Calibration Configuration 0**

Bit	Name	Access	Description	Default
25:20	IB_DFE_GAIN_ADJ	R/W	Gain adjustment for DFE amplifier	0x24
19:14	CPMD_THRES_INIT	R/W	Initial value for CP/MD FF threshold calibration.	0x00
13:8	VSC_THRES_INIT	R/W	Initial value for VScope FF threshold calibration.	0x00
7	SKIP_OBSERVE_INIT	R/W	Skip observe block initialization	0x0

Table 1642 • **APC Sampling Stage Calibration Configuration 0** ***(continued)***

Bit	Name	Access	Description	Default
6	SKIP_OFFSET_INIT	R/W	Skip sample FF offset initialization	0x0
5	SKIP_THRESHOLD_INIT	R/W	Skip sample FF threshold initialization	0x0
4	SKIP_DFE_BUFFER_INIT	R/W	Skip DFE buffer 0db initialization	0x0
3	SKIP_OBSERVE_CAL	R/W	Skip observe block calibration	0x0
2	SKIP_OFFSET_CAL	R/W	Skip sample FF offset calibration	0x0
1	SKIP_THRESHOLD_CAL	R/W	Skip sample FF threshold calibration	0x0
0	SKIP_DFE_BUFFER_CAL	R/W	Skip DFE buffer 0db calibration	0x0

2.26.1.6 APC Sampling Stage Calibration Configuration 1

Short Name:APC_IS_CAL_CFG1

Address:0x1EEF05

Configuration register 1 for APC sampling stage calibrations logic

Table 1643 • **APC Sampling Stage Calibration Configuration 1**

Bit	Name	Access	Description	Default
19:16	CAL_NUM_ITERATIONS	R/W	Controls number of calibrations iterations to settle values that depend on each other (offset vs threshold). Coding number of iterations = cal_num_iterations + 1.	0xF
13:9	PAR_DATA_NUM_ONES_THRES	R/W	Selects the number of ones threshold when using parallel data. Value for rising ramp from zero to one. The value for the falling ramp (one -> zero) is half the interface width minus par_data_num_ones_thres.	0x10
8	PAR_DATA_SEL	R/W	Controls whether the parallel data from the deserializer or the signal from the observe multiplexer in the sample stage is used. Coding: 0: observe multiplexer, 1: parallel data.	0x1
7:3	OFFSCAL_READ_CNT_SEL	R/W	Select offset calibration result to be read (BLOCK_READ_SEL = 8 required)	0x00
2	OFFSCAL_DIS_SWAP	R/W	Swaps disp with disn used during calibration	0x0
1	OFFSCAL_DONE	R/O	Offset calibration state 1: finished	0x0
0	START_OFFSCAL	R/W	Start offset calibration process (sampling stage; only in manual mode, see apc_mode)	0x0

2.26.2 SD10G65 DES Configuration and Status

Configuration and status register set for SD10G65 DES

2.26.2.1 SD10G65 DES Configuration 0

Short Name:SD10G65_DES_CFG0

Address:0x1EF000

Configuration register 0 for SD10G65 DES.

Table 1644 **• SD10G65 DES Configuration 0**

Bit	Name	Access	Description	Default
7	DES_INV_H	R/W	Invert output of high auxiliary deserializer	0x0
6	DES_INV_L	R/W	Invert output of low auxiliary deserializer	0x0
5	DES_INV_M	R/W	Invert output of main deserializer	0x0
4:2	DES_IF_MODE_SEL	R/W	Interface width 0: 8 1: 10 2: 16 (energy efficient) 3: 20 (energy efficient) 4: 32 5: 40 6: 16 bit (fast) 7: 20 bit (fast)	0x4
1	DES_VSC_DIS	R/W	Auxiliary deserializer channels disable.	0x1
0	DES_DIS	R/W	Deserializer disable.	0x0

2.26.2.2 SD10G65 MOEBDIV Configuration 0

Short Name:SD10G65_MOEBDIV_CFG0

Address:0x1EF001

Configuration register 0 for SD10G65 MoebiusDivider

Table 1645 **• SD10G65 MOEBDIV Configuration 0**

Bit	Name	Access	Description	Default
11:9	MOEBDIV_BW_CDR_SEL_A	R/W	Bandwidth selection for cp/md of cdr loop when core NOT flags valid data detected	0x3
8:6	MOEBDIV_BW_CDR_SEL_B	R/W	Bandwidth selection for cp/md of cdr loop when core flags valid data detected	0x3
5:3	MOEBDIV_BW_CORE_SEL	R/W	Bandwidth selection for cp/md signals towards core	0x0
2	MOEBDIV_CPMD_SWAP	R/W	CP/MD swapping	0x0
1	MOEBDIV_DIV32_ENA	R/W	MD divider enable	0x0
0	MOEBDIV_DIS	R/W	Divider disable	0x0

2.26.3 SD10G65 OB Configuration and Status

Configuration and status register set for SD10G65 OB

2.26.3.1 SD10G65 OB Configuration 0

Short Name:SD10G65_OB_CFG0

Address:0x1EF010

Configuration register 0 for SD10G65 OB.

Table 1646 **• SD10G65 OB Configuration 0**

Bit	Name	Access	Description	Default
23	SER_INV	R/W	Invert input to serializer	0x0
22:21	CLK_BUF_CMV	R/W	Control of common mode voltage of clock buffer between synthesizer and OB.	0x0
17	RST	R/W	Set digital part into pseudo reset	0x0
16	EN_PAD_LOOP	R/W	Enable pad loop	0x0
15	EN_INP_LOOP	R/W	Enable input loop	0x0
14	EN_DIRECT	R/W	Enable direct path	0x0
13	EN_OB	R/W	Enable output buffer and serializer	0x0
8	INCR_LEVN	R/W	Selects amplitude range controlled via levn. See description of levn.	0x1
7:5	SEL_IFW	R/W	Interface width 0: 8 1: 10 2: 16 3: 20 4: 32 5: 40 6-7: Reserved	0x4
4:0	LEVN	R/W	Amplitude control value. Step size is 25 mVpp, decreasing amplitude with increasing control value. Range depends on incr_levn. Coding for incr_levn=0: 31: 500mVpp, 30: 525mVpp, 29: 550mVpp, ..., 0: 1275mVpp. Coding for incr_levn=1: 31: 300mVpp, 30: 325mVpp, 29: 350mVpp, .., 0: 1075mVpp. (Note: maximum achievable amplitude depends on the supply voltage)	0x07

2.26.3.2 SD10G65 OB Configuration 1

Short Name:SD10G65_OB_CFG1

Address:0x1EF011

Configuration register 1 for SD10G65 OB.

Table 1647 **• SD10G65 OB Configuration 1**

Bit	Name	Access	Description	Default
26	AB_COMP_EN	R/W	Enable amplitude compensation of AB bleed current	0x1
25:23	DIODE_CUR	R/W	Bleed current for class AB operation of driver 0: 1% 1: 0.5% 2: 2% 3: reserved	0x0

Table 1647 • **SD10G65 OB Configuration 1** ***(continued)***

Bit	Name	Access	Description	Default
22:21	LEV_SHFT	R/W	Level shift ctrl of class AB bias generator 0: 50mV 1: 100mV 2:150mV 3: 200mV	0x1
19:18	PREDRV_R_CTRL	R/W	Slew rate ctrl of OB (R), encoding see PREDRV_C_CTRL	0x3
17:16	PREDRV_C_CTRL	R/W	Slew rate ctrl of OB (C) C=3 R=3: 25ps C=3 R=0: 35ps C=0 R=3: 55ps C=1 R=0: 70ps C=0 R=0: 120 ps	0x3
15:10	VTAIL	R/W	Tail voltage driver settings 0: reserved 1: 75mV 2: 100mV 4: 125mV 8: 150mV 16: 175mV 32: 200mV Intermediate values possible when setting two bits	0x02
9:5	VCAS	R/W	Ctrl of cascade volt in drv stage 0: reserved 1: 0 2: 1/12 4: 2/12 8: 3/12 16: 4/12 Intermediate values possible when setting two bits	0x01
4	R_COR	R/W	Additional resistor calibration trim	0x0
3:0	R_I	R/W	Offset resistance adjustment for CML cells (two-complement) 1000: -8 1111: -1 0000: 0 0111: 7	0x0

2.26.3.3 SD10G65 OB Configuration 2

Short Name:SD10G65_OB_CFG2

Address:0x1EF012

Configuration register 2 for SD10G65 OB. D_filter contains four 6-bit precalculated DA input values. Please note the differences in programming for various interface (IF) bit widths. For calculation details see documentation of OB10G.

Table 1648 **• SD10G65 OB Configuration 2**

Bit	Name	Access	Description	Default
23:0	D_FILTER	R/W	Transmit filter coefficients for FIR taps. Suggested start value (no emphasis, max amplitude) 0x820820: for I/F width 8/10 bits 0x7DF820: for I/F width 16/20/32/40 bits	0x7DF820

2.26.3.4 SD10G65 OB Configuration 3

Short Name:SD10G65_OB_CFG3

Address:0x1EF013

Configuration register 3 for SD10G65 OB.

Table 1649 **• SD10G65 OB Configuration 3**

Bit	Name	Access	Description	Default
18	REC_DET_DONE	R/O	Indicates a completed receiver detect measurement. Should be one few us after rec_det_start is set.	0x0
17	REC_DET_START	R/W	Rising edge starts receiver detect measurement. Has to be kept set until rec_det_value has been read.	0x0
16	REC_DET_ENABLE	R/W	Enable reciver detect function. MUST be disabled for normal operation!	0x0
15:12	RESERVED	R/W	Must be set to its default.	0x2
11:0	REC_DET_VALUE	R/O	Holds the time between the start and the flag of the receiver detect measurement. Time [ns +/- 4 ns] = 8 * value - 12	0x000

2.26.4 SD10G65 IB Configuration and Status

Configuration and status register set for SD10G65 IB

2.26.4.1 SD10G65 IB Configuration 0

Short Name:SD10G65_IB_CFG0

Address:0x1EF020

Configuration register 0 for SD10G65 IB. Note: Configuration bit-grp IB_CLKDIV_ENA was named IB_VSCOPE_CLK_ENA in an early revision of the input buffer.

Table 1650 **• SD10G65 IB Configuration 0**

Bit	Name	Access	Description	Default
30:27	IB_RCML_ADJ	R/W	Offset resistance adjustment for CML cells (two-complement) 1000: -8 1111: -1 0000: 0 0111: 7	0x0

Table 1650 • **SD10G65 IB Configuration 0** ***(continued)***

Bit	Name	Access	Description	Default
26:23	IB_TERM_V_SEL	R/W	Select termination voltage	0x8
22	IB_TERM_VDD_ENA	R/W	Enable common mode termination 0: no common mode termination (only AC-common mode termination) 1: termination to VDDI	0x0
21	IB_RIB_SHIFT	R/W	Shifts resistance adjustment value ib_rib_adj by +1	0x0
20:17	IB_RIB_ADJ	R/W	Offset resistance adjustment for termination (two-complement) 1000: -8 1111: -1 0000: 0 0111: 7	0x0
14	IB_DFE_ENA	R/W	Enable DFE stage (gates IB_ISEL_DFE) 0: Disable 1: Enable	0x0
13:12	IB_SIG_SEL	R/W	Select input buffer input signal 0: normal operation 1: -6dB input 2: OB->IB data loop or test signal 3: RESERVED	0x0
11	IB_VBULK_SEL	R/W	Controls Bulk Voltage of High Speed Cells 0: High 1: Low (mission mode)	0x1
10	IB_IA_ENA	R/W	Enable for IA including ACJtag 0: Disable 1: Enable	0x1
9	IB_IA_SDET_ENA	R/W	Enable for IA signal detect circuit (IB_SDET_SEL = 0 required) 0: Disable 1: Enable	0x0
8	IB_IE_SDET_ENA	R/W	Enable for IA signal detect circuit (IB_SDET_SEL = 1 required) 0: Disable 1: Enable	0x0
7	IB_LD_ENA	R/W	Enable for level detect circuit 0: Disable 1: Enable	0x0
6	IB_1V_ENA	R/W	Enable for 1V mode 0: VDDI=1.2V 1: VDDI=1.0V	0x0
5	IB_CLKDIV_ENA	R/W	Enable clock dividers in sampling stag 0: Disable (use in double rate mode) 1: Enable (use in full rate mode)	0x0
3	IB_VSCOPE_ENA	R/W	Enable VScope Path of Sampling-Stage 0: Disable 1: Enable	0x0

Table 1650 • **SD10G65 IB Configuration 0** ***(continued)***

Bit	Name	Access	Description	Default
2	IB_SAM_ENA	R/W	Enable SAMpling stage 0: Disable 1: Enable (mission mode)	0x0
1	IB_EQZ_ENA	R/W	Enable EQualiZation stage 0: Disable 1: Enable (mission mode)	0x0

2.26.4.2 SD10G65 IB Configuration 1

Short Name:SD10G65_IB_CFG1

Address:0x1EF021

Configuration register 1 for SD10G65 IB.

Table 1651 • **SD10G65 IB Configuration 1**

Bit	Name	Access	Description	Default
31:28	IB_AMP_L	R/W	Inductor peaking of 1. stage Input buffer 0: no peaking 15: max. peaking max. peaking > 3db at 8GHz	0x8
27:24	IB_EQZ_L0	R/W	Inductor peaking of EQ-Buffer0 (over all 2. stage) 0: no peaking 15: max. peaking max. peaking > 3db at 8GHz	0x8
23:20	IB_EQZ_L1	R/W	Inductor peaking of EQ-Buffer1 (over all 3. stage) 0: no peaking 15: max. peaking max. peaking > 3dB at 8GHz	0x8
19:16	IB_EQZ_L2	R/W	Inductor peaking of EQ-Buffer2 (over all 4. stage) 0: no peaking 15: max. peaking max. peaking > 3dB at 8GHz	0x8
15:12	IB_AGC_L	R/W	Inductor peaking of EQ-Buffer3 (over all 5. stage) 0: no peaking 15: max. peaking max. peaking > 3dB at 8GHz	0x8
11:9	IB_AMP_C	R/W	C-gain peaking for IB-stage 0: no peaking 7: max. peaking corner frequency adjustment with ib_eqz_c_adj_ib	0x4
8:6	IB_EQZ_C0	R/W	C-gain peaking for EQ-stage0 0: no peaking 7: max. peaking corner frequency adjustment with ib_eqz_c_adj_es0	0x4

Table 1651 • **SD10G65 IB Configuration 1** ***(continued)***

Bit	Name	Access	Description	Default
5:3	IB_EQZ_C1	R/W	C-gain peaking for EQ-stage1 0: no peaking 7: max. peaking corner frequency adjustment with ib_eqz_c_adj_es1	0x4
2:0	IB_EQZ_C2	R/W	C-gain peaking for EQ-stage2 0: no peaking 7: max. peaking corner frequency adjustment with ib_eqz_c_adj_es2	0x4

2.26.4.3 SD10G65 IB Configuration 2

Short Name:SD10G65_IB_CFG2

Address:0x1EF022

Configuration register 2 for SD10G65 IB.

Table 1652 • **SD10G65 IB Configuration 2**

Bit	Name	Access	Description	Default
27:18	IB_EQZ_GAIN	R/W	Gain of Input Buffer 0-511 gain adjustment only in first stage > 511 gain in first stage at max. 512-639 gain in 2.stage increased from 1 to 2 > 639 gain = 2 640-767 gain in 3.stage increased from 1 to 2 > 767 gain = 2 768-895 gain in 4.stage increased from 1 to 2 >895 gain at max.	0x040
17:10	IB_EQZ_AGC	R/W	Amplification (gain) of AGC in Input Buffer (normal operation) after gain calibration 0: gain = 0.3 255: gain = 1.5 if disp/disn is active dac function for dfe gain calibration	0x80
9:0	IB_EQZ_OFFSET	R/W	Offset value for IB-stage of Input Buffer 512: neutral > 512: positive < 512: negative range +/- 600mV (low gain) to +/-30mV (high gain) gain dependent offset sensitivity required for Base line wander compensation not supported in test chip	0x200

2.26.4.4 SD10G65 IB Configuration 3

Short Name:SD10G65_IB_CFG3

Address:0x1EF023

Configuration register 1 for SD10G65 IB. Note: the behavior of IB_EQ_LD1_OFFSET changes when APC is disabled. In this case IB_EQ_LD1_OFFSET directly controls the level for Level-Detect circuitry 1. Coding: 0: 20mV, 1: 25mV, ... 63: 340mV.

Table 1653 **• SD10G65 IB Configuration 3**

Bit	Name	Access	Description	Default
31:30	IB_LDSD_DIVSEL	R/W	Dividing factor for SDET and LD circuits of IE. 0: 128 1: 32 2: 8 3: 4	0x1
29:27	IB_SDET_CLK_DIV	R/W	Clock dividing factor for Signal Detect circuit of IA 0: 2 ... 7: 256	0x5
26	IB_SET_SDET	R/W	Force Signal-Detect output to high level 0: Normal operation 1: Force sigdet high	0x0
24	IB_SDET_SEL	R/W	Selects source of signal detect (ib_X_sdet_ena must be enabled accordingly) 0: IA 1: IE	0x0
23	IB_DIRECT_SEL	R/W	Selects source of direct data path to core 0: IE 1: IA	0x0
22:17	IB_EQ_LD1_OFFSET	R/W	With APC enabled level offset (6bit-signed) compared to IB_EQ_LD0_LEVEL for Level-Detect circuitry 1. Saturating between 20mV and 340mV. See also note in register description. 0: no offset 1: +5mV 31: +155mV 63(= -1): -5mV 32(= -32): -160mV.	0x00
16:11	IB_EQ_LD0_LEVEL	R/W	Level for Level-Detect circuitry 0. 0: 20mV 1: 25mV ... 40: 220mV ... 63: 340mV	0x28
10:5	IB_IE_SDET_LEVEL	R/W	Threshold value for IE Signal-Detect. 0: 20mV 1: 25mV 2: 30mV ... 63: 340mV	0x02
4:0	IB_IA_SDET_LEVEL	R/W	Threshold value for IA Signal-Detect. 0: 0mV ... 8: 80mV ... 31: 310mV	0x08

2.26.4.5 SD10G65 IB Configuration 4

Short Name:SD10G65_IB_CFG4

Address:0x1EF024

Configuration register 4 for SD10G65 IB.

***Table 1654* • SD10G65 IB Configuration 4**

Bit	Name	Access	Description	Default
31:30	IB_EQZ_C_ADJ_IB	R/W	corner frequency selection for c-gain peaking 1.stage 0: lowest corner frequency 3: highest corner frequency	0x2
29:28	IB_EQZ_C_ADJ_ES2	R/W	corner frequency selection for c-gain peaking 2.stage 0: lowest corner frequency 3: highest corner frequency	0x2
27:26	IB_EQZ_C_ADJ_ES1	R/W	corner frequency selection for c-gain peaking 3.stage 0: lowest corner frequency 3: highest corner frequency	0x2
25:24	IB_EQZ_C_ADJ_ES0	R/W	corner frequency selection for c-gain peaking 4.stage 0: lowest corner frequency 3: highest corner frequency	0x2
23:21	IB_EQZ_L_MODE	R/W	Coder mode: APC L value to IE inductance 0: equ. distributed (double step 3->4) 1: equ. distributed (no change 6+7) 2: 1st buffer max - 2nd buffer max - ...	0x0
20:18	IB_EQZ_C_MODE	R/W	Coder mode: APC C value to IE capacitance 0: equ. distributed 2: 1st buffer max - 2nd buffer max - ...	0x0
17:12	IB_VSCOPE_H_THRES	R/W	Threshold value (offset) for vscope-high sampling path 0: -max 31: -0 32: +0 63: +max (depending on calibration)	0x30
11:6	IB_VSCOPE_L_THRES	R/W	Threshold value (offset) for vscope-low sampling path 0: -max 31: -0 32: +0 63: +max (depending on calibration)	0x0F
5:0	IB_MAIN_THRES	R/W	Threshold value (offset) for main sampling path 0: -max 31: -0 32: +0 63: +max (depending on calibration)	0x20

2.26.4.6 SD10G65 IB Configuration 5

Short Name:SD10G65_IB_CFG5

Address:0x1EF025

Configuration register 5 for SD10G65 IB.

Table 1655 **• SD10G65 IB Configuration 5**

Bit	Name	Access	Description	Default
31:28	IB_TSTGEN_AMPL	R/W	Test generator amplitude setting 0: 0mV ... 15: 150mV	0x0
27	IB_TSTGEN_ENA	R/W	Test generator enable but data path selected with 'ib_sig_sel' (disable input loop if testgenerator is used) 0: inactive 1: active	0x0
26	IB_TSTGEN_DATA	R/W	Test generator data 0: low 1: high	0x0
25	IB_TSTGEN_TOGGLE_ENA	R/W	Test generator data toggle enable 0: inactive 1: active	0x0
22	IB_JUMPH_ENA	R/W	Enable jump to opposite half of h-channel 0: Post main sampler 1: Pre main sampler	0x0
21	IB_JUMPL_ENA	R/W	Enable jump to opposite half of l-channel 0: Post main sampler 1: Pre main sampler	0x0
20:19	IB_DFE_DIS	R/W	DFE output disable required to calibrate IS 0: mission mode 3: Vout = 0V 1: Vout= xx*ampldfe/64 2: Vout=-xx*ampldfe/64 ampldfe=196mV if ena1V = '1' (1V mode) ampldfe=260mV if ena1V = '0' (1.2V mode) xx= TBD	0x0
18:17	IB_AGC_DIS	R/W	AGC output disable required to calibrate DFE-gain 0: mission mode 3: Vout = 0V 1: Vout= xx*ampldfe/64 2: Vout=-xx*ampldfe/64 ampldfe=270mV if ena1V = '1' (1V mode) ampldfe=360mV if ena1V = '0' (1.2V mode) xx=	0x0
16	IB_EQ_LD_CAL_ENA	R/W	Selects EQ Level Detect for calibration	0x0
15	IB_THRES_CAL_ENA	R/W	Selects IS threshold circuit for calibration	0x0
14	IB_IS_OFFS_CAL_ENA	R/W	Selects IS offset circuit for calibration	0x0
13	IB_IA_OFFS_CAL_ENA	R/W	Selects IA offset circuit for calibration	0x0
12	IB_IE_SDET_CAL_ENA	R/W	Selects IE Signal Detect for calibration	0x0

Table 1655 • **SD10G65 IB Configuration 5** ***(continued)***

Bit	Name	Access	Description	Default
11	IB_HYS_CAL_ENA	R/W	Enable calibration in order to eliminate hysteresis 1: Enable 0: Disable	0x0
10	IB_CALMUX_ENA	R/W	Enables IS MUX in detblk1	0x1
9:6	IB_OFFS_BLKSEL	R/W	Selects calibration target (sample stage threshold, sample stage offset, aux.-stage offset), dependend on calibration group, see encoding. When ib_thres_cal_ena = 1 0: MD0 threshold 1: MD1 threshold 2: CP0 threshold 3: CP1 threshold 4: VH0 threshold 5: VH1 threshold 6: VL0 threshold 7: VL1 threshold When ib_is_offs_cal_ena = 1 0: MD0 offset 1: MD1 offset 2: CP0 offset 3: CP1 offset 4: VH0 offset 5: VH1 offset 6: VL0 offset 7: VL1 offset When ib_ia_offs_cal_ena = 1 0: Observe0 offset 1: Observe1 offset 2: Observe0 threshold 3: Observe1 threshold (MSB not used)	0x0
5:0	IB_OFFS_VALUE	R/W	Calibration value for IA/IS. Values for threshold calibration get inverted for negative threshold voltages (ib_vscope_h_thres, ib_vscope_l_thres or ib_main_thres). For offset calibration 0: -max_offset * 32/32 31: -max_offset * 1/32 32: +max_offset * 1/32 63: +max_offset * 32/32 For threshold calibration 0: min_threshold 63: max_threshold	0x1F

2.26.4.7 SD10G65 IB Configuration 6

Short Name:SD10G65_IB_CFG6

Address:0x1EF026

Configuration register 6 for SD10G65 IB.

Table 1656 **• SD10G65 IB Configuration 6**

Bit	Name	Access	Description	Default
22:16	IB_EQZ_GAIN_ADJ	R/W	0dB Gain adjustment for EQZ-stages of Input Buffer level at LD0 = LD1 -> 0dB level range 160mV-220mV	0x2A
12	IB_AUTO_AGC_ADJ	R/W	Enable automatic AGC adjustment 1: AGC is adjusted automatically (IB_EQZ_AGC_ADJ value is not used) 0: AGC is adjusted with value stored in IB_EQZ_AGC_ADJ	0x0
11:5	IB_EQZ_AGC_ADJ	R/W	Gain adjustment of AGC-amplifier Bitgroup should be set to 2*IB_DFE_GAIN_ADJ	0x3E
4:0	IB_SAM_OFFS_ADJ	R/W	Range for offset calibration of all sampling paths 0: 0mV 32: 80mV	0x10

2.26.4.8 SD10G65 IB Configuration 7

Short Name:SD10G65_IB_CFG7

Address:0x1EF027

Configuration register 7 for SD10G65 IB.

Table 1657 **• SD10G65 IB Configuration 7**

Bit	Name	Access	Description	Default
28:23	IB_MAIN_THRES_CAL	R/W	Initial value for calibration of main sampling path	0x30
22	IB_DFE_OFFSET_H_L	R/W	Selects higher or lower DFE offset for IS calibration 0: ib_dfe_offset_l 1: ib_dfe_offset_h	0x0
21:16	IB_DFE_GAIN_ADJ	R/W	Gain adjustment of DFEamplifier DFE Gain 1 Volt mode = 0dB 1.2 Volt mode 1dB measurement with int. DAC and VScope Channels	0x24
11:6	IB_DFE_OFFSET_H	R/W	Higher threshold offset of DFE buffer for IS calibration 0: 0mv 63: 200mV	0x17
5:0	IB_DFE_OFFSET_L	R/W	Lower sample offset of DFE buffer for IS calibration 0: 0mv 63: 200mV	0x06

2.26.4.9 SD10G65 IB Configuration 8

Short Name:SD10G65_IB_CFG8

Address:0x1EF028

Configuration register 8 for SD10G65 IB.

Table 1658 **• SD10G65 IB Configuration 8**

Bit	Name	Access	Description	Default
20	IB_SEL_VCLK	R/W	Use separate Vscope clock for Vscope-channels	0x0
19	IB_BIAS_MODE	R/W	Bias regulation mode 0: constant resistor 1: constant current	0x1
18	IB_LAT_NEUTRAL	R/W	Enables neutral setting of latches 1: Reset to mid values 0: Normal operation	0x0
14	RESERVED	R/W	Must be set to its default.	0x1
12:10	IB_CML_AMPL	R/W	Amplitude of cml stages inside IS 0: 200mVppd 7: 240mVppd	0x4
9:4	IB_BIAS_ADJ	R/W	Gain of cml stages inside IS 0: 3dB 31: 6dB 63: 9dB	0x1F
3:0	IB_CML_CURR	R/W	Current through CML Cells 0: 150% 5: 100% 15: 50%	0x5

2.26.4.10 SD10G65 IB Configuration 9

Short Name:SD10G65_IB_CFG9

Address:0x1EF029

Configuration register 9 for SD10G65 IB.

Table 1659 **• SD10G65 IB Configuration 9**

Bit	Name	Access	Description	Default
28:24	IB_DFE_COEF4	R/W	Weighting for fourth DFE coefficient	0x10
20:16	IB_DFE_COEF3	R/W	Weighting for third DFE coefficient	0x10
13:8	IB_DFE_COEF2	R/W	Weighting for second DFE coefficient	0x20
6:0	IB_DFE_COEF1	R/W	Weighting for first DFE coefficient	0x40

2.26.4.11 SD10G65 IB Configuration 10

Short Name:SD10G65_IB_CFG10

Address:0x1EF02A

Configuration register 10 for SD10G65 IB.

Table 1660 **• SD10G65 IB Configuration 10**

Bit	Name	Access	Description	Default
31	IB_IA_DOFFS_CAL	R/O	Data offset calibration result IA stage	0x0
30	IB_IS_DOFFS_CAL	R/O	Data offset calibration result IS stage	0x0
29	IB_IE_SDET_PEDGE	R/O	Detection of toggling signal at PADP and PADN	0x0

Table 1660 • **SD10G65 IB Configuration 10** ***(continued)***

Bit	Name	Access	Description	Default
28	IB_IE_SDET_NEDGE	R/O	Detection of toggling signal at PADP and PADN	0x0
27	IB_IE_SDET	R/O	Result signal detect of IE stage	0x0
26	IB_IA_SDET	R/O	Result signal detect of IA stage	0x0
25	IB_EQZ_LD1_PEDGE	R/O	Result of Level-Detect1 (after ES2-stage of EQZ) circuitry 1: Input level above threshold defined by IB_EQ_LD_LEV	0x0
24	IB_EQZ_LD1_NEDGE	R/O	Result of Level-Detect1 (after ES2-stage of EQZ) circuitry 1: Input level above threshold defined by IB_EQ_LD_LEV	0x0
23	IB_EQZ_LD0_PEDGE	R/O	Result of Level-Detect0 (after IB-stage of EQZ) circuitry 1: Input level above threshold defined by IB_EQ_LD_LEV	0x0
22	IB_EQZ_LD0_NEDGE	R/O	Result of Level-Detect0 (after IB-stage of EQZ) circuitry 1: Input level above threshold defined by IB_EQ_LD_LEV	0x0
21	IB_IE_DIRECT_DATA	R/O	Direct Data output from IE block	0x0
20	IB_IA_DIRECT_DATA	R/O	Direct Data output from IA block	0x0
17	IB_LOOP_REC	R/W	Receive enable for BiDi loop (a.k.a. PAD loop o. Tx->Rx loop). Is or'ed with primary input: ib_pad_loop_ena_i. Disable testgenerator 'ib_tstgen_ena' if input loop is used	0x0
16	IB_LOOP_DRV	R/W	Drive enable for BiDi loop (a.k.a. Input loop o. Rx->Tx loop). Is or'ed with primary input: ib_inp_loop_ena_i. Is overruled by PAD loop.	0x0
10	IB_JTAG_OUT_P	R/O	JTAG debug p-output	0x0
9	IB_JTAG_OUT_N	R/O	JTAG debug n-output	0x0
8:4	IB_JTAG_THRES	R/W	JTAG debug threshold 0: 0mV 1: 10mV 31: 310mV	0x08
3	IB_JTAG_IN_P	R/W	JTAG debug p-input	0x0
2	IB_JTAG_IN_N	R/W	JTAG debug n-input	0x0
1	IB_JTAG_CLK	R/W	JTAG debug clk	0x0
0	IB_JTAG_ENA	R/W	JTAG debug enable	0x0

2.26.4.12 SD10G65 IB Configuration 11

Short Name:SD10G65_IB_CFG11

Address:0x1EF02B

Configuration register 11 for SD10G65 IB.

Table 1661 **• SD10G65 IB Configuration 11**

Bit	Name	Access	Description	Default
15:12	IB_DFE_ISEL	R/W	DFE Bias current settings (bit-group is gated with IB_DFE_ENA) 0: DFE disabled 1: Minimum current 15: Maximum current	0x7
11	IB_ENA_400_INP	R/W	Increase current in first stage (only available in 1.2 Volt mode)	0x0
10:6	IB_TC_DFE	R/W	Gain temperature coefficient for DFE stage	0x0C
5:1	IB_TC_EQ	R/W	Gain temperature coefficient for AGC stage	0x0C

2.26.4.13 SD10G65 SBUS Rx CFG Service-Bus Related Setting

Short Name:SD10G65_SBUS_RX_CFG

Address:0x1EF02C

Configuration register for Service-Bus related setting. Note: SBUS configuration applies for Rx/Tx aggregates only, any configuration applied to SBUS_TX_CFG (output buffer cfg space) will be ignored.

Table 1662 **• SD10G65 SBUS Rx CFG Service-Bus Related Setting**

Bit	Name	Access	Description	Default
12	SBUS_LOOPDRV_ENA	R/W	Enable BiDi loop driver for F2DF testing	0x0
11:8	SBUS_ANAOUT_SEL	R/W	Analog test output 0: l0_ctrlspeed[0] 1: vbulk 2: nref 3: vref820m 4: vddfilt 5: vddfilt 6: ie_aout 7: ib_aout 8: ob_aout2 9: pll_frange 10: pll_srange 11: pll_vreg820m_tx 12: pll_vreg820m_rx 13: ob_aout_n 14: ob_aout_p 15: vddfilt	0x0
7	SBUS_ANAOUT_EN	R/W	Enable analog test output multiplexer	0x0
6:3	SBUS_RCOMP	R/W	Offset value for BIAS resistor calibration (2-complement) 1000: -8 1111: -1 0000: 0 0111: 7	0x0

Table 1662 • **SD10G65 SBUS Rx CFG Service-Bus Related Setting *(continued)***

Bit	Name	Access	Description	Default
2:1	SBUS_BIAS_SPEED_SEL	R/W	Bias speed selection 0: Below 4Gbps 1: 4Gbps to 6Gbps 2: 6Gbps to 9Gbps 3: Above 9Gbps	0x3
0	SBUS_BIAS_EN	R/W	Bias enable 1: Enable 0: Disable	0x0

2.26.5 SD10G65 Rx RCPLL Configuration and Status

Configuration and status register set for SD10G65 Rx RCPLL

2.26.5.1 SD10G65 Rx RCPLL Configuration 0

Short Name:SD10G65_RX_RCPLL_CFG0

Address:0x1EF030

Configuration register 0 for SD10G65 Rx RCPLL.

Table 1663 • **SD10G65 Rx RCPLL Configuration 0**

Bit	Name	Access	Description	Default
25:16	PLLF_START_CNT	R/W	Preload value of the ramp up counter, reduces ramp up time for higher frequencies	0x002
9:7	PLLF_RAMP_MODE_SEL	R/W	Sets the ramp characteristic of the FSM, higher values give faster ramp up but less accuracy, 0: normal (default) ramping 1: faster ramping 2: fastest ramping 3: slow ramping uses all possible values of r_ctrl	0x0
5	RESERVED	R/W	Must be set to its default.	0x1
4	RESERVED	R/W	Must be set to its default.	0x1
0	PLLF_ENA	R/W	Enable RCPLL FSM	0x0

2.26.5.2 SD10G65 Rx RCPLL Configuration 1

Short Name:SD10G65_RX_RCPLL_CFG1

Address:0x1EF031

Configuration register 1 for SD10G65 Rx RCPLL.

Table 1664 • **SD10G65 Rx RCPLL Configuration 1**

Bit	Name	Access	Description	Default
31:16	PLLF_REF_CNT_END	R/W	Target value: 1/vco_frq * par.bit.width * 512 * ref_clk_frq	0x00C6
13:4	RESERVED	R/W	Must be set to its default.	0x002
1:0	RESERVED	R/W	Must be set to its default.	0x1

2.26.5.3 SD10G65 Rx RCPLL Configuration 2

Short Name:SD10G65_RX_RCPLL_CFG2

Address:0x1EF032

Configuration register 2 for SD10G65 Rx RCPLL.

***Table 1665* • SD10G65 Rx RCPLL Configuration 2**

Bit	Name	Access	Description	Default
23:20	RESERVED	R/W	Must be set to its default.	0x3
16	RESERVED	R/W	Must be set to its default.	0x1
15	RESERVED	R/W	Must be set to its default.	0x1
14	RESERVED	R/W	Must be set to its default.	0x1
13	RESERVED	R/W	Must be set to its default.	0x1
12:11	PLL_LPF_CUR	R/W	Select chargepump current, 0: 50uA 1: 100uA 2: 150uA 3: 200uA	0x3
10:7	PLL_LPF_RES	R/W	Select loop filter resistor value, 0: not allowed 1: 2400 2: 1600 3: 960 4: 1200 5: 800 6: 685 7: 533 8: 800 9: 600 10: 533 11: 436 12: 480 13: 400 14: 369 15: 320	0xA
6:2	RESERVED	R/W	Must be set to its default.	0x1F
0	PLL_ENA	R/W	Enable analog RCPLL part	0x0

2.26.5.4 SD10G65 Rx RCPLL Status 0

Short Name:SD10G65_RX_RCPLL_STAT0

Address:0x1EF033

Status register 0 for SD10G65 Rx RCPLL.

***Table 1666* • SD10G65 Rx RCPLL Status 0**

Bit	Name	Access	Description	Default
31	PLLF_LOCK_STAT	R/O	PLL lock status, 0: not locked 1: locked	0x0

2.26.6 SD10G65 Rx SYNTH Configuration and Status

Configuration and status register set for SD10G65 Rx SYNTH

2.26.6.1 SD10G65 Rx Synthesizer Configuration 0

Short Name:SD10G65_RX_SYNTH_CFG0

Address:0x1EF040

Configuration register 0 for SD10G65 Rx SYNTH.

***Table 1667* • SD10G65 Rx Synthesizer Configuration 0**

Bit	Name	Access	Description	Default
21:18	RESERVED	R/W	Must be set to its default.	0xF
17:16	SYNTH_FBDIV_SEL	R/W	selects feedback divider setting. 0: divide by 1 1: divide by 2 2: divide by 4 3: reserved	0x1
15:14	SYNTH_FB_STEP	R/W	selects step width for sync output	0x0
12:11	SYNTH_I2_STEP	R/W	selects step width for integrator2	0x0
9	SYNTH_I2_ENA	R/W	enable contribution of integral2 part	0x1
8	SYNTH_I1_STEP	R/W	selects step width for integrator1	0x0
6	SYNTH_P_STEP	R/W	selects step width for proportional	0x0
4	SYNTH_SPEED_SEL	R/W	Selects circuit speed. 0: for settings with synth_fbdiv_sel = 2 1: for setting with synth_fbdiv_sel less than 2	0x1
3	SYNTH_HRATE_ENA	R/W	enables half rate mode	0x0
1	RESERVED	R/W	Must be set to its default.	0x1
0	SYNTH_ENA	R/W	synthesizer enable	0x0

2.26.6.2 SD10G65 Rx Synthesizer Configuration 1

Short Name:SD10G65_RX_SYNTH_CFG1

Address:0x1EF041

Configuration register 1 for SD10G65 Rx SYNTH.

***Table 1668* • SD10G65 Rx Synthesizer Configuration 1**

Bit	Name	Access	Description	Default
25:22	RESERVED	R/W	Must be set to its default.	0x4
21:8	SYNTH_FREQ_MULT	R/W	frequency multiplier	0x2100
7:4	SYNTH_FREQM_1	R/W	frequency m setting bits 35:32	0x0
3:0	SYNTH_FREQN_1	R/W	frequency n setting bits 35:32	0x8

2.26.6.3 SD10G65 Rx Synthesizer Configuration 2

Short Name:SD10G65_RX_SYNTH_CFG2

Address:0x1EF042

Configuration register 2 for SD10G65 Rx SYNTH.

Table 1669 **• SD10G65 Rx Synthesizer Configuration 2**

Bit	Name	Access	Description	Default
31	SYNTH_SKIP_BIT_FWD	R/W	Rising edge triggers bit skip forward in serial data stream. Used to align data to parallel interface boundaries.	0x0
30	SYNTH_SKIP_BIT_REV	R/W	Rising edge triggers bit skip reverse in serial data stream. Used to align data to parallel interface boundaries.	0x0
27:26	SYNTH_DV_CTRL_I2E	R/W	Controls the data valid behavior for the CDRLF I2 enable function: b0 = 0 => external signal controls, 1 => b1 controls	0x0
25:24	SYNTH_DV_CTRL_I1M	R/W	Controls the data valid behavior for the CDRLF I1 max function: b0 = 0 => external signal controls, 1 => b1 controls	0x0
23:22	SYNTH_DV_CTRL_I1E	R/W	Controls the data valid behavior for the CDRLF I1 enable function: b0 = 0 => external signal controls, 1 => b1 controls	0x0
21:20	SYNTH_DV_CTRL_MD	R/W	Controls the data valid behavior for the moebdiv select function: b0 = 0 => external signal controls, 1 => b1 controls	0x0
18	SYNTH_CPMD_DIG_SEL	R/W	Cp/md dig select. Coding 0: select Bit 0/5 as cp/md (FX100 mode); 1: use cp/md from core	0x0
17	SYNTH_CPMD_DIG_ENA	R/W	uses cp/md selected via synth_cpmd_dig_sel instead of cp/md from sample stage	0x0
16	SYNTH_AUX_ENA	R/W	enables clock for VScope / APC auxiliary data channels	0x1
14:8	SYNTH_PHASE_DATA	R/W	relationship phase center/edge	0x08
6:0	SYNTH_PHASE_AUX	R/W	relationship phase center/aux	0x08

2.26.6.4 SD10G65 Rx Synthesizer Configuration 3

Short Name:SD10G65_RX_SYNTH_CFG3

Address:0x1EF043

Configuration register 3 for SD10G65 Rx SYNTH.

Table 1670 **• SD10G65 Rx Synthesizer Configuration 3**

Bit	Name	Access	Description	Default
31:0	SYNTH_FREQM_0	R/W	frequency m setting bits 31:0	0x00000000

2.26.6.5 SD10G65 Rx Synthesizer Configuration 4

Short Name:SD10G65_RX_SYNTH_CFG4

Address:0x1EF044

Configuration register 4 for SD10G65 Rx SYNTH.

***Table 1671* • SD10G65 Rx Synthesizer Configuration 4**

Bit	Name	Access	Description	Default
31:0	SYNTH_FREQN_0	R/W	frequency n setting bits 31:0	0x00000000

2.26.6.6 SD10G65 Rx Synthesizer CDR Loop Filter Control

Short Name:SD10G65_RX_SYNTH_CDRLF

Address:0x1EF045

Register for CDR loopfilter control for SD10G65 Rx SYNTH.

***Table 1672* • SD10G65 Rx Synthesizer CDR Loop Filter Control**

Bit	Name	Access	Description	Default
31	SYNTH_INTEG3_ENA	R/W	Enables integrator 3	0x0
30:26	SYNTH_INTEG3_DSEL	R/W	Select filter damping / gain peaking when integrator 3 is enabled. The control value is interpreted as signed value. Positive values increase the damping, i.e. lowering the gain peaking; negative values decease the damping, i.e. raising the gain peaking. The allowed programming range depends on the SYNTH_INTEG2_FSEL setting: 0 <= (SYNTH_INTEG2_FSEL - SYNTH_INTEG3_DSEL) <= 53. SYNTH_INTEG2_FSEL - SYNTH_INTEG3_DSEL = 0 and SYNTH_INTEG2_FSEL - SYNTH_INTEG3_DSEL = 1 gives the same damping.	0x00
25:21	SYNTH_INTEG1_MAX1	R/W	max value of integrator 1 during normal operation	0x02
20:16	SYNTH_INTEG1_MAX0	R/W	max value of integrator 1 during init phase	0x00
15:11	SYNTH_INTEG1_LIM	R/W	limit of integrator 1	0x02
10:6	SYNTH_INTEG1_FSEL	R/W	frequency select of integrator 1	0x02
5:0	SYNTH_INTEG2_FSEL	R/W	frequency select of integrator 2	0x31

2.26.6.7 SD10G65 Rx Synthesizer 0 for Qualifier Access

Short Name:SD10G65_RX_SYNTH_QUALIFIER0

Address:0x1EF046

Register 0 for qualifier access for SD10G65 Rx SYNTH.

***Table 1673* • SD10G65 Rx Synthesizer 0 for Qualifier Access**

Bit	Name	Access	Description	Default
20	SYNTH_CAPTURE_QUAL	R/W	Rising edge captures qualifier for readback	0x0
19:16	SYNTH_QUAL_I2_MSB	R/O	MS Bits of captured integrator 2	0x0
15:0	SYNTH_QUAL_I1	R/O	Captured integrator 1 value	0x0000

2.26.6.8 SD10G65 Rx Synthesizer 1 for Qualifier Access

Short Name:SD10G65_RX_SYNTH_QUALIFIER1

Address:0x1EF047

Register 1 for qualifier access for SD10G65 Rx SYNTH.

***Table 1674* • SD10G65 Rx Synthesizer 1 for Qualifier Access**

Bit	Name	Access	Description	Default
31:0	SYNTH_QUAL_I2_LSB	R/O	LS Bits of captured integrator 2	0x00000000

2.26.6.9 SD10G65 Rx Synthesizer for Sync Control Data

Short Name:SD10G65_RX_SYNTH_SYNC_CTRL

Address:0x1EF048

Register 0 for sync control data for SD10G65 Rx SYNTH.

***Table 1675* • SD10G65 Rx Synthesizer for Sync Control Data**

Bit	Name	Access	Description	Default
3:0	SYNTH_SC_SYNC_TIMER_SEL	R/W	Selects the synchronization period for the I2 value via sync control bus. Must be disabled (0) when sync control test generator is used. Coding in 312.5MHz clock cycles: 0: disabled, 1: 2^6, 2: 2^7, .., 15: 2^20.	0xF

2.26.6.10 F2DF Configuration and Status

Short Name:F2DF_CFG_STAT

Address:0x1EF049

Configuration / status register for the F2DF control logic.

***Table 1676* • F2DF Configuration and Status**

Bit	Name	Access	Description	Default
27:25	F2DF_SAMPLE_DIV	R/W	Sampling divider: sample every 2^f2df_sample_div parallel data word.	0x0
21:17	F2DF_SIDE_DET_BIT_SEL	R/W	Select bit from input data used for side detection. Debug feature: '31' select constant zero, '30' select constant one.	0x00
16:14	F2DF_SIDE_DET_ONES_WEIGHT	R/W	Sample '1' => increment 8bit filter saturating counter by 2**n. Cnt >= 0xC0 => ProperSide detected.	0x0
13:11	F2DF_SIDE_DET_ZEROS_WEIGHT	R/W	Sample '0' => decrement 8bit filter saturating counter by 2**n. Cnt < 0x40 => WrongSide detected.	0x0
9:4	F2DF_TOG_DET_CNT	R/W	Determines the number of samples that have to show at least one toggle.	0x00
3	F2DF_DATA_VALID_PROPPER_SIDE	R/W	Data valid value in "PropperSide" state. '0': data valid flaged only in "Lock" state; '1' data valid also flaged in "PropperSide" state.	0x0

Table 1676 • **F2DF Configuration and Status** *(continued)*

Bit	Name	Access	Description	Default
0	F2DF_ENABLE	R/W	F2df enable. Enabling the f2df circuit automatically switches the input of the CDR-loop to the f2df control block (overrules synth_cpmd_dig_sel and synth_cpmd_dig_ena) and replaces the data valid signal from the core logic by the data valid signal generated by the f2df control logic.	0x0

2.26.7 SD10G65 Tx SYNTH Configuration and Status

Configuration and status register set for SD10G65 Tx SYNTH

2.26.7.1 SD10G65 Tx Synthesizer Configuration 0

Short Name:SD10G65_TX_SYNTH_CFG0

Address:0x1EF050

Configuration register 0 for SD10G65 Tx SYNTH.

Table 1677 • **SD10G65 Tx Synthesizer Configuration 0**

Bit	Name	Access	Description	Default
25:23	RESERVED	R/W	Must be set to its default.	0x3
22:18	RESERVED	R/W	Must be set to its default.	0x17
17:16	SYNTH_FBDIV_SEL	R/W	selects feedback divider setting	0x2
13:11	SYNTH_CS_SPEED	R/W	comon sync speed	0x0
10	SYNTH_LS_SPEED	R/W	lane sync speed	0x0
8	SYNTH_LS_ENA	R/W	lane sync enable	0x1
7	SYNTH_DS_SPEED	R/W	dig. sync speed	0x0
5	SYNTH_DS_ENA	R/W	dig. sync enable	0x0
4	SYNTH_SPEED_SEL	R/W	Selects circuit speed. Coding: 0 for settings with synth_fbdiv_sel = 2; 1 for setting with synth_fbdiv_sel smaller than 2.	0x0
3	SYNTH_HRATE_ENA	R/W	half rate enable	0x0
2	RESERVED	R/W	Must be set to its default.	0x1
1	RESERVED	R/W	Must be set to its default.	0x1
0	SYNTH_ENA	R/W	synthesizer enable	0x0

2.26.7.2 SD10G65 Tx Synthesizer Configuration 1

Short Name:SD10G65_TX_SYNTH_CFG1

Address:0x1EF051

Configuration register 1 for SD10G65 Tx SYNTH.

Table 1678 • **SD10G65 Tx Synthesizer Configuration 1**

Bit	Name	Access	Description	Default
25:22	RESERVED	R/W	Must be set to its default.	0x4
21:8	SYNTH_FREQ_MULT	R/W	frequency multiplier	0x2100

Table 1678 • **SD10G65 Tx Synthesizer Configuration 1 *(continued)***

Bit	Name	Access	Description	Default
7:4	SYNTH_FREQM_1	R/W	frequency m setting bits 35:32	0x0
3:0	SYNTH_FREQN_1	R/W	frequency n setting bits 35:32	0x8

2.26.7.3 SD10G65 Tx Synthesizer Configuration 3

Short Name:SD10G65_TX_SYNTH_CFG3

Address:0x1EF052

Configuration register 3 for SD10G65 Tx SYNTH.

Table 1679 • **SD10G65 Tx Synthesizer Configuration 3**

Bit	Name	Access	Description	Default
31:0	SYNTH_FREQM_0	R/W	frequency m setting bits 31:0	0x00000000

2.26.7.4 SD10G65 Tx Synthesizer Configuration 4

Short Name:SD10G65_TX_SYNTH_CFG4

Address:0x1EF053

Configuration register 4 for SD10G65 Tx SYNTH.

Table 1680 • **SD10G65 Tx Synthesizer Configuration 4**

Bit	Name	Access	Description	Default
31:0	SYNTH_FREQN_0	R/W	frequency n setting bits 31:0	0x00000000

2.26.7.5 SD10G65 SSC Generator Configuration 0

Short Name:SD10G65_SSC_CFG0

Address:0x1EF054

Configuration register 0 for SD10G65 SSC generator.

Table 1681 • **SD10G65 SSC Generator Configuration 0**

Bit	Name	Access	Description	Default
31:19	SSC_MOD_LIM	R/W	SSC modulation amplitude limiter	0x0000
18:7	SSC_MOD_PERIOD	R/W	SSC modulation period / amplitude.	0x000
6:1	SSC_MOD_FREQ	R/W	SSC modulation frequency fine tuning control	0x00
0	SSC_ENA	R/W	SSC generator enable.	0x0

2.26.7.6 SD10G65 SSC Generator Configuration 1

Short Name:SD10G65_SSC_CFG1

Address:0x1EF055

Configuration register 1 for SD10G65 SSC generator.

Table 1682 **• SD10G65 SSC Generator Configuration 1**

Bit	Name	Access	Description	Default
29	MLD_SYNC_SRC_SEL	R/W	Select between the internal and external MLD phase detector: 0: internal; 1: external	0x0
28:25	MLD_SYNC_CTRL	R/W	Control of the internal MLD phase detector: b0: enable; b1: enable hyst. b2: enable window function; b3: select window size	0x0
24:23	MLD_SYNC_CLK_SEL	R/W	Select the MLD clock source for the internal MLD phase detector	0x0
22	SYNC_CTRL_WRAP_INHIBIT	R/W	Controls integrator 2 replica behavior: '0': wrapping; '1': saturating.	0x0
21:16	SYNC_CTRL_FSEL	R/W	Frequency select of integrator 2 replica used for lane sync.	0x31
10	SMOOTH_ENA	R/W	Enables Smooth generator	0x0
9:5	SSC_SD_GAIN	R/W	SSC sigma delta gain.	0x00
4:3	SSC_SYNC_POS	R/W	SSC modulation start position on synchronization trigger	0x0
2:0	SSC_MOD_MUL	R/W	SSC modulation period multiplier encoded 2**n: 0 => 1; 1 => 2; 2 => 4, 3 => 8 ...	0x0

2.26.8 SD10G65 Tx RCPLL Configuration and Status

Configuration and status register set for SD10G65 Tx RCPLL

2.26.8.1 SD10G65 Tx RCPLL Configuration 0

Short Name:SD10G65_TX_RCPLL_CFG0

Address:0x1EF060

Configuration register 0 for SD10G65 Tx RCPLL.

Table 1683 **• SD10G65 Tx RCPLL Configuration 0**

Bit	Name	Access	Description	Default
25:16	PLLF_START_CNT	R/W	Preload value of the ramp up counter, reduces ramp up time for higher frequencies	0x002
9:7	PLLF_RAMP_MODE_SEL	R/W	Sets the ramp characteristic of the FSM, higher values give faster ramp up but less accuracy, 0: normal (default) ramping 1: faster ramping 2: fastest ramping 3: slow ramping uses all possible values of r_ctrl	0x0
5	RESERVED	R/W	Must be set to its default.	0x1
4	RESERVED	R/W	Must be set to its default.	0x1
0	PLLF_ENA	R/W	Enable RCPLL FSM	0x0

2.26.8.2 SD10G65 Tx RCPLL Configuration 1

Short Name:SD10G65_TX_RCPLL_CFG1

Address:0x1EF061

Configuration register 1 for SD10G65 Tx RCPLL.

Table 1684 **• SD10G65 Tx RCPLL Configuration 1**

Bit	Name	Access	Description	Default
31:16	PLLF_REF_CNT_END	R/W	Target value: 1/vco_frq * par.bit.width * 512 * ref_clk_frq	0x00C6
13:4	RESERVED	R/W	Must be set to its default.	0x002
1:0	RESERVED	R/W	Must be set to its default.	0x1

2.26.8.3 SD10G65 Tx RCPLL Configuration 2

Short Name:SD10G65_TX_RCPLL_CFG2

Address:0x1EF062

Configuration register 2 for SD10G65 Tx RCPLL.

Table 1685 **• SD10G65 Tx RCPLL Configuration 2**

Bit	Name	Access	Description	Default
23:20	RESERVED	R/W	Must be set to its default.	0x3
16	RESERVED	R/W	Must be set to its default.	0x1
15	RESERVED	R/W	Must be set to its default.	0x1
14	RESERVED	R/W	Must be set to its default.	0x1
13	RESERVED	R/W	Must be set to its default.	0x1
12:11	PLL_LPF_CUR	R/W	Select chargepump current, 0: 50uA 1: 100uA 2: 150uA 3: 200uA	0x3
10:7	PLL_LPF_RES	R/W	Select loop filter resistor value, 0: not allowed 1: 2400 2: 1600 3: 960 4: 1200 5: 800 6: 685 7: 533 8: 800 9: 600 10: 533 11: 436 12: 480 13: 400 14: 369 15: 320	0xA
6:2	RESERVED	R/W	Must be set to its default.	0x1F
0	PLL_ENA	R/W	Enable analog RCPLL part	0x0

2.26.8.4 SD10G65 Tx RCPLL Status 0

Short Name:SD10G65_TX_RCPLL_STAT0

Address:0x1EF063

Status register 0 for SD10G65 Tx RCPLL.

***Table 1686* • SD10G65 Tx RCPLL Status 0**

Bit	Name	Access	Description	Default
31	PLLF_LOCK_STAT	R/O	PLL lock status, 0: not locked 1: locked	0x0

2.27 EXP Global (Device 0x1E)

***Table 1687* • EXP_CFG**

Address	Short Description	Register Name	Details
0x1EF100	EXP Bypass and Resets	CFG1	Page 598
0x1EF101	EXP Invert Configuration	COND_CFG	Page 599

***Table 1688* • EXP_STATUS**

Address	Short Description	Register Name	Details
0x1EF102	EXP Select Status	STAT1	Page 599
0x1EF103	EXP Interrupt Mask	INTR_EN	Page 600
0x1EF104	EXP Sticky	INTR	Page 601

***Table 1689* • HOST0_CFG**

Address	Short Description	Register Name	Details
0x1EF105	H0 Source Select	H0_SRC_SEL	Page 602
0x1EF106	H0 Filter	H0_FILTER	Page 603

***Table 1690* • HOST1_CFG**

Address	Short Description	Register Name	Details
0x1EF107	H1 Source Select	H1_SRC_SEL	Page 604
0x1EF108	H1 Filter	H1_FILTER	Page 605

***Table 1691* • HOST2_CFG**

Address	Short Description	Register Name	Details
0x1EF109	H2 Source Select	H2_SRC_SEL	Page 606
0x1EF10A	H2 Filter	H2_FILTER	Page 607

Table 1692 • **HOST3_CFG**

Address	Short Description	Register Name	Details
0x1EF10B	H3 Source Select	H3_SRC_SEL	Page 608
0x1EF10C	H3 Filter	H3_FILTER	Page 609

Table 1693 • **LINE0_CFG**

Address	Short Description	Register Name	Details
0x1EF10D	L0 Source Select	L0_SRC_SEL	Page 610
0x1EF10E	L0 Filter	L0_FILTER	Page 611

Table 1694 • **LINE1_CFG**

Address	Short Description	Register Name	Details
0x1EF10F	L1 Source Select	L1_SRC_SEL	Page 612
0x1EF110	L1 Filter	L1_FILTER	Page 613

Table 1695 • **LINE2_CFG**

Address	Short Description	Register Name	Details
0x1EF111	L2 Source Select	L2_SRC_SEL	Page 614
0x1EF112	L2 Filter	L2_FILTER	Page 615

Table 1696 • **LINE3_CFG**

Address	Short Description	Register Name	Details
0x1EF113	L3 Source Select	L3_SRC_SEL	Page 616
0x1EF114	L3 Filter	L3_FILTER	Page 617

2.27.1 Global Configuration

2.27.1.1 EXP Bypass and Resets

Short Name:CFG1

Address:0x1EF100

Table 1697 • **EXP Bypass and Resets**

Bit	Name	Access	Description	Default
31	L3_RESET	One-shot	Reset the FIFO read port on Line 3	0x0
30	L2_RESET	One-shot	Reset the FIFO read port on Line 2	0x0
29	L1_RESET	One-shot	Reset the FIFO read port on Line 1	0x0
28	L0_RESET	One-shot	Reset the FIFO read port on Line 0	0x0
27	H3_RESET	One-shot	Reset the FIFO read port on Host 3	0x0

*Table 1697 • (continued)*EXP Bypass and Resets

Bit	Name	Access	Description	Default
26	H2_RESET	One-shot	Reset the FIFO read port on Host 2	0x0
25	H1_RESET	One-shot	Reset the FIFO read port on Host 1	0x0
24	H0_RESET	One-shot	Reset the FIFO read port on Host 0	0x0
19:16	RESERVED	R/W	Must be set to its default.	0x7
0	BYPASS	R/W	Bypass cross-connect functionality and pass data directly through Note condition logic is still active in bypass mode 0: Enable Cross-connect 1: Bypass Cross-connect	0x1

2.27.1.2 EXP Invert Configuration

Short Name:COND_CFG

Address:0x1EF101

Table 1698 • EXP Invert Configuration

Bit	Name	Access	Description	Default
15:8	INVERT_GPIO	R/W	Invert corresponding GPIO input when used as a switch condition; One bit for each external input to the cross connect control function.	0x00
3	INVERT_LOF	R/W	Invert EWIS LOF indicator when used as a switch condition	0x0
2	INVERT_LOS	R/W	Invert PMA LOS indicator when used as a switch condition	0x0
1	INVERT_LINK_STATUS	R/W	Invert 1000Base-X PCS link_status indication when used as a switch condition	0x0

2.27.1.3 EXP Select Status

Short Name:STAT1

Address:0x1EF102

Table 1699 • EXP Select Status

Bit	Name	Access	Description	Default
15:14	L3_SEL	R/O		0x3
13:12	L2_SEL	R/O		0x2
11:10	L1_SEL	R/O		0x1
9:8	L0_SEL	R/O		0x0
7:6	H3_SEL	R/O		0x3
5:4	H2_SEL	R/O		0x2
3:2	H1_SEL	R/O		0x1
1:0	H0_SEL	R/O		0x0

2.27.1.4 EXP Interrupt Mask

Short Name:INTR_EN

Address:0x1EF103

Table 1700 • **EXP Interrupt Mask**

Bit	Name	Access	Description	Default
23	L3_COND_ALT_UNF_DET_INTR_EN	R/W	Allow L3_COND_ALT_UNF_DET_STICKY to propagate to INTR	0x0
22	L2_COND_ALT_UNF_DET_INTR_EN	R/W	Allow L2_COND_ALT_UNF_DET_STICKY to propagate to INTR	0x0
21	L1_COND_ALT_UNF_DET_INTR_EN	R/W	Allow L1_COND_ALT_UNF_DET_STICKY to propagate to INTR	0x0
20	L0_COND_ALT_UNF_DET_INTR_EN	R/W	Allow L0_COND_ALT_UNF_DET_STICKY to propagate to INTR	0x0
19	H3_COND_ALT_UNF_DET_INTR_EN	R/W	Allow H3_COND_ALT_UNF_DET_STICKY to propagate to INTR	0x0
18	H2_COND_ALT_UNF_DET_INTR_EN	R/W	Allow H2_COND_ALT_UNF_DET_STICKY to propagate to INTR	0x0
17	H1_COND_ALT_UNF_DET_INTR_EN	R/W	Allow H1_COND_ALT_UNF_DET_STICKY to propagate to INTR	0x0
16	H0_COND_ALT_UNF_DET_INTR_EN	R/W	Allow H0_COND_ALT_UNF_DET_STICKY to propagate to INTR	0x0
15	L3_COND_ALT_DET_INTR_EN	R/W	Allow L3_COND_ALT_DET_STICKY to propagate to INTR	0x0
14	L2_COND_ALT_DET_INTR_EN	R/W	Allow L2_COND_ALT_DET_STICKY to propagate to INTR	0x0
13	L1_COND_ALT_DET_INTR_EN	R/W	Allow L1_COND_ALT_DET_STICKY to propagate to INTR	0x0
12	L0_COND_ALT_DET_INTR_EN	R/W	Allow L0_COND_ALT_DET_STICKY to propagate to INTR	0x0
11	H3_COND_ALT_DET_INTR_EN	R/W	Allow H3_COND_ALT_DET_STICKY to propagate to INTR	0x0
10	H2_COND_ALT_DET_INTR_EN	R/W	Allow H2_COND_ALT_DET_STICKY to propagate to INTR	0x0
9	H1_COND_ALT_DET_INTR_EN	R/W	Allow H1_COND_ALT_DET_STICKY to propagate to INTR	0x0
8	H0_COND_ALT_DET_INTR_EN	R/W	Allow H0_COND_ALT_DET_STICKY to propagate to INTR	0x0
7	L3_SWITCH_INTR_EN	R/W	Enable L3_SWITCH_STICKY to propagate to INTR	0x0
6	L2_SWITCH_INTR_EN	R/W	Enable L2_SWITCH_STICKY to propagate to INTR	0x0
5	L1_SWITCH_INTR_EN	R/W	Enable L1_SWITCH_STICKY to propagate to INTR	0x0
4	L0_SWITCH_INTR_EN	R/W	Enable L0_SWITCH_STICKY to propagate to INTR	0x0

*Table 1700 • (continued)*EXP Interrupt Mask

Bit	Name	Access	Description	Default
3	H3_SWITCH_INTR_EN	R/W	Enable H3_SWITCH_STICKY to propagate to INTR	0x0
2	H2_SWITCH_INTR_EN	R/W	Enable H2_SWITCH_STICKY to propagate to INTR	0x0
1	H1_SWITCH_INTR_EN	R/W	Enable H1_SWITCH_STICKY to propagate to INTR	0x0
0	H0_SWITCH_INTR_EN	R/W	Enable H0_SWITCH_STICKY to propagate to INTR	0x0

2.27.1.5 EXP Sticky

Short Name:INTR

Address:0x1EF104

Table 1701 • EXP Sticky

Bit	Name	Access	Description	Default
23	L3_COND_ALT_UNF_DET_STICKY	Sticky	L3 COND_ALT (unfiltered) change detected	0x0
22	L2_COND_ALT_UNF_DET_STICKY	Sticky	L2 COND_ALT (unfiltered) change detected	0x0
21	L1_COND_ALT_UNF_DET_STICKY	Sticky	L1 COND_ALT (unfiltered) change detected	0x0
20	L0_COND_ALT_UNF_DET_STICKY	Sticky	L0 COND_ALT (unfiltered) change detected	0x0
19	H3_COND_ALT_UNF_DET_STICKY	Sticky	H3 COND_ALT (unfiltered) change detected	0x0
18	H2_COND_ALT_UNF_DET_STICKY	Sticky	H2 COND_ALT (unfiltered) change detected	0x0
17	H1_COND_ALT_UNF_DET_STICKY	Sticky	H1 COND_ALT (unfiltered) change detected	0x0
16	H0_COND_ALT_UNF_DET_STICKY	Sticky	H0 COND_ALT (unfiltered) change detected	0x0
15	L3_COND_ALT_DET_STICKY	Sticky	L3 filtered COND_ALT change detected	0x0
14	L2_COND_ALT_DET_STICKY	Sticky	L2 filtered COND_ALT change detected	0x0
13	L1_COND_ALT_DET_STICKY	Sticky	L1 filtered COND_ALT change detected	0x0
12	L0_COND_ALT_DET_STICKY	Sticky	L0 filtered COND_ALT change detected	0x0
11	H3_COND_ALT_DET_STICKY	Sticky	H3 filtered COND_ALT change detected	0x0
10	H2_COND_ALT_DET_STICKY	Sticky	H2 filtered COND_ALT change detected	0x0
9	H1_COND_ALT_DET_STICKY	Sticky	H1 filtered COND_ALT change detected	0x0

*Table 1701 • (continued)*EXP Sticky

Bit	Name	Access	Description	Default
8	H0_COND_ALT_DET_STICKY	Sticky	H0 filtered COND_ALT change detected	0x0
7	L3_SWITCH_STICKY	Sticky	L3 source selection has changed	0x0
6	L2_SWITCH_STICKY	Sticky	L2 source selection has changed	0x0
5	L1_SWITCH_STICKY	Sticky	L1 source selection has changed	0x0
4	L0_SWITCH_STICKY	Sticky	L0 source selection has changed	0x0
3	H3_SWITCH_STICKY	Sticky	H3 source selection has changed	0x0
2	H2_SWITCH_STICKY	Sticky	H2 source selection has changed	0x0
1	H1_SWITCH_STICKY	Sticky	H1 source selection has changed	0x0
0	H0_SWITCH_STICKY	Sticky	H0 source selection has changed	0x0

2.27.1.6 H0 Source Select

Short Name:H0_SRC_SEL

Address:0x1EF105

Table 1702 • **H0 Source Select**

Bit	Name	Access	Description	Default
12:8	ALT_SRC	R/W	Event source used to trigger a switch to ALT_CH 0 = GPIO0 1 = GPIO1 2 = GPIO2 3 = GPIO3 4 = GPIO4 5 = GPIO5 6 = GPIO6 7 = GPIO7 8 = Always false 9 = Always false 10 = Always false 11 = Always false 12 = Line 0 link status 13 = Line 1 link status 14 = Line 2 link status 15 = Line 3 link status 16 = Line 0 serdes los 17 = Line 1 serdes los 18 = Line 2 serdes los 19 = Line 3 serdes los 20 = Line 0 10g wis lof 21 = Line 1 10g wis lof 22 = Line 2 10g wis lof 23 = Line 3 10g wis lof 24 = Always false 25 = Always false 26 = Always false 27 = Always false 28 = Always false 29 = Always false 30 = Always false 31 = Always true	0x1E
5	FILTER_EN	R/W	Enable filtering of condition source 0 = No filtering (assertion of selected condition source causes immediate switch to ALT_CH) 1 = Filtering enabled	0x0
4	ALT_EN	R/W	Enable conditional switching to ALTernate channel 0 = Force default channel 1 = Allow switching to ALTernate channel based on source selection and filtering	0x0
3:2	ALT_CH	R/W	Alternate line rx from which host tx receives traffic	0x1
1:0	DEFAULT_CH	R/W	Default line rx from which host tx receives traffic	0x0

2.27.1.7 H0 Filter

Short Name:H0_FILTER

Address:0x1EF106

Table 1703 • **H0 Filter**

Bit	Name	Access	Description	Default
31:24	COUNTB2316	R/W	COUNTB is the number of CSR clock cycles needed for selected condition to be continuously false before event can be cleared. COUNTB2316 is the upper 8 bits of this 24 bit threshold.	0x00
23:16	COUNTB70	R/W	COUNTB is the number of CSR clock cycles needed for selected condition to be continuously false before event can be cleared. COUNTB70 is the lower 8 bits of this 24 bit threshold.	0x00
15:8	COUNTA2316	R/W	COUNTA is the number of CSR clock cycles needed for selected condition to be continuously true before event can be set. COUNTA2316 is the upper 8 bits of this 24 bit threshold.	0x00
7:0	COUNTA70	R/W	COUNTA is the number of CSR clock cycles needed for selected condition to be continuously true before event can be set. COUNTA70 is the lower 8 bits of this 24 bit threshold.	0x00

2.27.1.8 H1 Source Select

Short Name:H1_SRC_SEL

Address:0x1EF107

Table 1704 • **H1 Source Select**

Bit	Name	Access	Description	Default
12:8	ALT_SRC	R/W	Event source used to trigger a switch to ALT_CH 0 = GPIO0 1 = GPIO1 2 = GPIO2 3 = GPIO3 4 = GPIO4 5 = GPIO5 6 = GPIO6 7 = GPIO7 8 = Always false 9 = Always false 10 = Always false 11 = Always false 12 = Line 0 link status 13 = Line 1 link status 14 = Line 2 link status 15 = Line 3 link status 16 = Line 0 serdes los 17 = Line 1 serdes los 18 = Line 2 serdes los 19 = Line 3 serdes los 20 = Line 0 10g wis lof 21 = Line 1 10g wis lof 22 = Line 2 10g wis lof 23 = Line 3 10g wis lof 24 = Always false 25 = Always false 26 = Always false 27 = Always false 28 = Always false 29 = Always false 30 = Always false 31 = Always true	0x1E
5	FILTER_EN	R/W	Enable filtering of condition source 0 = No filtering (assertion of selected condition source causes immediate switch to ALT_CH) 1 = Filtering enabled	0x0
4	ALT_EN	R/W	Enable conditional switching to ALTernate channel 0 = Force default channel 1 = Allow switching to ALTernate channel based on source selection and filtering	0x0
3:2	ALT_CH	R/W	Alternate line rx from which host tx receives traffic	0x0
1:0	DEFAULT_CH	R/W	Default line rx from which host tx receives traffic	0x1

2.27.1.9 H1 Filter

Short Name:H1_FILTER

Address:0x1EF108

Table 1705 • **H1 Filter**

Bit	Name	Access	Description	Default
31:24	COUNTB2316	R/W	COUNTB is the number of CSR clock cycles needed for selected condition to be continuously false before event can be cleared. COUNTB2316 is the upper 8 bits of this 24 bit threshold.	0x00
23:16	COUNTB70	R/W	COUNTB is the number of CSR clock cycles needed for selected condition to be continuously false before event can be cleared. COUNTB70 is the lower 8 bits of this 24 bit threshold.	0x00
15:8	COUNTA2316	R/W	COUNTA is the number of CSR clock cycles needed for selected condition to be continuously true before event can be set. COUNTA2316 is the upper 8 bits of this 24 bit threshold.	0x00
7:0	COUNTA70	R/W	COUNTA is the number of CSR clock cycles needed for selected condition to be continuously true before event can be set. COUNTA70 is the lower 8 bits of this 24 bit threshold.	0x00

2.27.1.10 H2 Source Select

Short Name:H2_SRC_SEL

Address:0x1EF109

Table 1706 • **H2 Source Select**

Bit	Name	Access	Description	Default
12:8	ALT_SRC	R/W	Event source used to trigger a switch to ALT_CH 0 = GPIO0 1 = GPIO1 2 = GPIO2 3 = GPIO3 4 = GPIO4 5 = GPIO5 6 = GPIO6 7 = GPIO7 8 = Always false 9 = Always false 10 = Always false 11 = Always false 12 = Line 0 link status 13 = Line 1 link status 14 = Line 2 link status 15 = Line 3 link status 16 = Line 0 serdes los 17 = Line 1 serdes los 18 = Line 2 serdes los 19 = Line 3 serdes los 20 = Line 0 10g wis lof 21 = Line 1 10g wis lof 22 = Line 2 10g wis lof 23 = Line 3 10g wis lof 24 = Always false 25 = Always false 26 = Always false 27 = Always false 28 = Always false 29 = Always false 30 = Always false 31 = Always true	0x1E
5	FILTER_EN	R/W	Enable filtering of condition source 0 = No filtering (assertion of selected condition source causes immediate switch to ALT_CH) 1 = Filtering enabled	0x0
4	ALT_EN	R/W	Enable conditional switching to ALTernate channel 0 = Force default channel 1 = Allow switching to ALTernate channel based on source selection and filtering	0x0
3:2	ALT_CH	R/W	Alternate line rx from which host tx receives traffic	0x2
1:0	DEFAULT_CH	R/W	Default line rx from which host tx receives traffic	0x2

2.27.1.11 H2 Filter

Short Name:H2_FILTER

Address:0x1EF10A

Table 1707 • **H2 Filter**

Bit	Name	Access	Description	Default
31:24	COUNTB2316	R/W	COUNTB is the number of CSR clock cycles needed for selected condition to be continuously false before event can be cleared. COUNTB2316 is the upper 8 bits of this 24 bit threshold.	0x00
23:16	COUNTB70	R/W	COUNTB is the number of CSR clock cycles needed for selected condition to be continuously false before event can be cleared. COUNTB70 is the lower 8 bits of this 24 bit threshold.	0x00
15:8	COUNTA2316	R/W	COUNTA is the number of CSR clock cycles needed for selected condition to be continuously true before event can be set. COUNTA2316 is the upper 8 bits of this 24 bit threshold.	0x00
7:0	COUNTA70	R/W	COUNTA is the number of CSR clock cycles needed for selected condition to be continuously true before event can be set. COUNTA70 is the lower 8 bits of this 24 bit threshold.	0x00

2.27.1.12 H3 Source Select

Short Name:H3_SRC_SEL

Address:0x1EF10B

Table 1708 • **H3 Source Select**

Bit	Name	Access	Description	Default
12:8	ALT_SRC	R/W	Event source used to trigger a switch to ALT_CH 0 = GPIO0 1 = GPIO1 2 = GPIO2 3 = GPIO3 4 = GPIO4 5 = GPIO5 6 = GPIO6 7 = GPIO7 8 = Always false 9 = Always false 10 = Always false 11 = Always false 12 = Line 0 link status 13 = Line 1 link status 14 = Line 2 link status 15 = Line 3 link status 16 = Line 0 serdes los 17 = Line 1 serdes los 18 = Line 2 serdes los 19 = Line 3 serdes los 20 = Line 0 10g wis lof 21 = Line 1 10g wis lof 22 = Line 2 10g wis lof 23 = Line 3 10g wis lof 24 = Always false 25 = Always false 26 = Always false 27 = Always false 28 = Always false 29 = Always false 30 = Always false 31 = Always true	0x1E
5	FILTER_EN	R/W	Enable filtering of condition source 0 = No filtering (assertion of selected condition source causes immediate switch to ALT_CH) 1 = Filtering enabled	0x0
4	ALT_EN	R/W	Enable conditional switching to ALTernate channel 0 = Force default channel 1 = Allow switching to ALTernate channel based on source selection and filtering	0x0
3:2	ALT_CH	R/W	Alternate line rx from which host tx receives traffic	0x1
1:0	DEFAULT_CH	R/W	Default line rx from which host tx receives traffic	0x3

2.27.1.13 H3 Filter

Short Name:H3_FILTER

Address:0x1EF10C

Table 1709 • **H3 Filter**

Bit	Name	Access	Description	Default
31:24	COUNTB2316	R/W	COUNTB is the number of CSR clock cycles needed for selected condition to be continuously false before event can be cleared. COUNTB2316 is the upper 8 bits of this 24 bit threshold.	0x00
23:16	COUNTB70	R/W	COUNTB is the number of CSR clock cycles needed for selected condition to be continuously false before event can be cleared. COUNTB70 is the lower 8 bits of this 24 bit threshold.	0x00
15:8	COUNTA2316	R/W	COUNTA is the number of CSR clock cycles needed for selected condition to be continuously true before event can be set. COUNTA2316 is the upper 8 bits of this 24 bit threshold.	0x00
7:0	COUNTA70	R/W	COUNTA is the number of CSR clock cycles needed for selected condition to be continuously true before event can be set. COUNTA70 is the lower 8 bits of this 24 bit threshold.	0x00

2.27.1.14 L0 Source Select

Short Name:L0_SRC_SEL

Address:0x1EF10D

Table 1710 • **L0 Source Select**

Bit	Name	Access	Description	Default
12:8	ALT_SRC	R/W	Event source used to trigger a switch to ALT_CH 0 = GPIO0 1 = GPIO1 2 = GPIO2 3 = GPIO3 4 = GPIO4 5 = GPIO5 6 = GPIO6 7 = GPIO7 8 = Always false 9 = Always false 10 = Always false 11 = Always false 12 = Host 0 link status 13 = Host 1 link status 14 = Host 2 link status 15 = Host 3 link status 16 = Host 0 serdes los 17 = Host 1 serdes los 18 = Host 2 serdes los 19 = Host 3 serdes los 20 = Always false 21 = Always false 22 = Always false 23 = Always false 24 = Always false 25 = Always false 26 = Always false 27 = Always false 28 = Always false 29 = Always false 30 = Always false 31 = Always true	0x1E
5	FILTER_EN	R/W	Enable filtering of condition source 0 = No filtering (assertion of selected condition source causes immediate switch to ALT_CH) 1 = Filtering enabled	0x0
4	ALT_EN	R/W	Enable conditional switching to ALTernate channel 0 = Force default channel 1 = Allow switching to ALTernate channel based on source selection and filtering	0x0
3:2	ALT_CH	R/W	Alternate host rx from which line tx receives traffic	0x1
1:0	DEFAULT_CH	R/W	Default host rx from which line tx receives traffic	0x0

2.27.1.15 L0 Filter

Short Name:L0_FILTER

Address:0x1EF10E

Table 1711 • **L0 Filter**

Bit	Name	Access	Description	Default
31:24	COUNTB2316	R/W	COUNTB is the number of CSR clock cycles needed for selected condition to be continuously false before event can be cleared. COUNTB2316 is the upper 8 bits of this 24 bit threshold.	0x00
23:16	COUNTB70	R/W	COUNTB is the number of CSR clock cycles needed for selected condition to be continuously false before event can be cleared. COUNTB70 is the lower 8 bits of this 24 bit threshold.	0x00
15:8	COUNTA2316	R/W	COUNTA is the number of CSR clock cycles needed for selected condition to be continuously true before event can be set. COUNTA2316 is the upper 8 bits of this 24 bit threshold.	0x00
7:0	COUNTA70	R/W	COUNTA is the number of CSR clock cycles needed for selected condition to be continuously true before event can be set. COUNTA70 is the lower 8 bits of this 24 bit threshold.	0x00

2.27.1.16 L1 Source Select

Short Name:L1_SRC_SEL

Address:0x1EF10F

Table 1712 • **L1 Source Select**

Bit	Name	Access	Description	Default
12:8	ALT_SRC	R/W	Event source used to trigger a switch to ALT_CH 0 = GPIO0 1 = GPIO1 2 = GPIO2 3 = GPIO3 4 = GPIO4 5 = GPIO5 6 = GPIO6 7 = GPIO7 8 = Always false 9 = Always false 10 = Always false 11 = Always false 12 = Host 0 link status 13 = Host 1 link status 14 = Host 2 link status 15 = Host 3 link status 16 = Host 0 serdes los 17 = Host 1 serdes los 18 = Host 2 serdes los 19 = Host 3 serdes los 20 = Always false 21 = Always false 22 = Always false 23 = Always false 24 = Always false 25 = Always false 26 = Always false 27 = Always false 28 = Always false 29 = Always false 30 = Always false 31 = Always true	0x1E
5	FILTER_EN	R/W	Enable filtering of condition source 0 = No filtering (assertion of selected condition source causes immediate switch to ALT_CH) 1 = Filtering enabled	0x0
4	ALT_EN	R/W	Enable conditional switching to ALTernate channel 0 = Force default channel 1 = Allow switching to ALTernate channel based on source selection and filtering	0x0
3:2	ALT_CH	R/W	Alternate host rx from which line tx receives traffic	0x0
1:0	DEFAULT_CH	R/W	Default host rx from which line tx receives traffic	0x1

2.27.1.17 L1 Filter

Short Name:L1_FILTER

Address:0x1EF110

Table 1713 • **L1 Filter**

Bit	Name	Access	Description	Default
31:24	COUNTB2316	R/W	COUNTB is the number of CSR clock cycles needed for selected condition to be continuously false before event can be cleared. COUNTB2316 is the upper 8 bits of this 24 bit threshold.	0x00
23:16	COUNTB70	R/W	COUNTB is the number of CSR clock cycles needed for selected condition to be continuously false before event can be cleared. COUNTB70 is the lower 8 bits of this 24 bit threshold.	0x00
15:8	COUNTA2316	R/W	COUNTA is the number of CSR clock cycles needed for selected condition to be continuously true before event can be set. COUNTA2316 is the upper 8 bits of this 24 bit threshold.	0x00
7:0	COUNTA70	R/W	COUNTA is the number of CSR clock cycles needed for selected condition to be continuously true before event can be set. COUNTA70 is the lower 8 bits of this 24 bit threshold.	0x00

2.27.1.18 L2 Source Select

Short Name:L2_SRC_SEL

Address:0x1EF111

Table 1714 • **L2 Source Select**

Bit	Name	Access	Description	Default
12:8	ALT_SRC	R/W	Event source used to trigger a switch to ALT_CH 0 = GPIO0 1 = GPIO1 2 = GPIO2 3 = GPIO3 4 = GPIO4 5 = GPIO5 6 = GPIO6 7 = GPIO7 8 = Always false 9 = Always false 10 = Always false 11 = Always false 12 = Host 0 link status 13 = Host 1 link status 14 = Host 2 link status 15 = Host 3 link status 16 = Host 0 serdes los 17 = Host 1 serdes los 18 = Host 2 serdes los 19 = Host 3 serdes los 20 = Always false 21 = Always false 22 = Always false 23 = Always false 24 = Always false 25 = Always false 26 = Always false 27 = Always false 28 = Always false 29 = Always false 30 = Always false 31 = Always true	0x1E
5	FILTER_EN	R/W	Enable filtering of condition source 0 = No filtering (assertion of selected condition source causes immediate switch to ALT_CH) 1 = Filtering enabled	0x0
4	ALT_EN	R/W	Enable conditional switching to ALTernate channel 0 = Force default channel 1 = Allow switching to ALTernate channel based on source selection and filtering	0x0
3:2	ALT_CH	R/W	Alternate host rx from which line tx receives traffic	0x3
1:0	DEFAULT_CH	R/W	Default host rx from which line tx receives traffic	0x2

2.27.1.19 L2 Filter

Short Name:L2_FILTER

Address:0x1EF112

Table 1715 • **L2 Filter**

Bit	Name	Access	Description	Default
31:24	COUNTB2316	R/W	COUNTB is the number of CSR clock cycles needed for selected condition to be continuously false before event can be cleared. COUNTB2316 is the upper 8 bits of this 24 bit threshold.	0x00
23:16	COUNTB70	R/W	COUNTB is the number of CSR clock cycles needed for selected condition to be continuously false before event can be cleared. COUNTB70 is the lower 8 bits of this 24 bit threshold.	0x00
15:8	COUNTA2316	R/W	COUNTA is the number of CSR clock cycles needed for selected condition to be continuously true before event can be set. COUNTA2316 is the upper 8 bits of this 24 bit threshold.	0x00
7:0	COUNTA70	R/W	COUNTA is the number of CSR clock cycles needed for selected condition to be continuously true before event can be set. COUNTA70 is the lower 8 bits of this 24 bit threshold.	0x00

2.27.1.20 L3 Source Select

Short Name:L3_SRC_SEL

Address:0x1EF113

Table 1716 • **L3 Source Select**

Bit	Name	Access	Description	Default
12:8	ALT_SRC	R/W	Event source used to trigger a switch to ALT_CH 0 = GPIO0 1 = GPIO1 2 = GPIO2 3 = GPIO3 4 = GPIO4 5 = GPIO5 6 = GPIO6 7 = GPIO7 8 = Always false 9 = Always false 10 = Always false 11 = Always false 12 = Host 0 link status 13 = Host 1 link status 14 = Host 2 link status 15 = Host 3 link status 16 = Host 0 serdes los 17 = Host 1 serdes los 18 = Host 2 serdes los 19 = Host 3 serdes los 20 = Always false 21 = Always false 22 = Always false 23 = Always false 24 = Always false 25 = Always false 26 = Always false 27 = Always false 28 = Always false 29 = Always false 30 = Always false 31 = Always true	0x1E
5	FILTER_EN	R/W	Enable filtering of condition source 0 = No filtering (assertion of selected condition source causes immediate switch to ALT_CH) 1 = Filtering enabled	0x0
4	ALT_EN	R/W	Enable conditional switching to ALTernate channel 0 = Force default channel 1 = Allow switching to ALTernate channel based on source selection and filtering	0x0
3:2	ALT_CH	R/W	Alternate host rx from which line tx receives traffic	0x2
1:0	DEFAULT_CH	R/W	Default host rx from which line tx receives traffic	0x3

2.27.1.21 L3 Filter

Short Name:L3_FILTER

Address:0x1EF114

Table 1717 • **L3 Filter**

Bit	Name	Access	Description	Default
31:24	COUNTB2316	R/W	COUNTB is the number of CSR clock cycles needed for selected condition to be continuously false before event can be cleared. COUNTB2316 is the upper 8 bits of this 24 bit threshold.	0x00
23:16	COUNTB70	R/W	COUNTB is the number of CSR clock cycles needed for selected condition to be continuously false before event can be cleared. COUNTB70 is the lower 8 bits of this 24 bit threshold.	0x00
15:8	COUNTA2316	R/W	COUNTA is the number of CSR clock cycles needed for selected condition to be continuously true before event can be set. COUNTA2316 is the upper 8 bits of this 24 bit threshold.	0x00
7:0	COUNTA70	R/W	COUNTA is the number of CSR clock cycles needed for selected condition to be continuously true before event can be set. COUNTA70 is the lower 8 bits of this 24 bit threshold.	0x00

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Table 1718 • **GPIO_CFG_STAT**

Address	Short Description	Register Name	Details
0x1EF200	GPIO Output Enable Config 1	GPIO_CFG1	Page 620
0x1EF201	GPIO Output Enable Config 0	GPIO_CFG0	Page 621
0x1EF202	GPIO Output Invert Config 1	GPIO_OUT_INV_CFG1	Page 621
0x1EF203	GPIO Output Invert Config 0	GPIO_OUT_INV_CFG0	Page 621
0x1EF204	Current Status of GPIO Inputs	GPIO_STAT1	Page 622
0x1EF205	Current Status of GPIO Inputs	GPIO_STAT0	Page 622
0x1EF206	Current Status of GPIO Outputs	GPIO_OUT_STAT1	Page 622
0x1EF207	Current Status of GPIO Outputs	GPIO_OUT_STAT0	Page 622
0x1EF208	GPIO State Change 1	GPIO_CHANGE1	Page 622
0x1EF209	GPIO State Chang 0	GPIO_CHANGE0	Page 623
0x1EF20A	GPIO Interrupt Mask 1	GPIO_MASK1	Page 623
0x1EF20B	GPIO Interrupt Mask 0	GPIO_MASK0	Page 623
0x1EF20C	GPIO Output Configuration 0	GPIO_OUT_CFG_0	Page 623
0x1EF20D	GPIO Output Configuration 1	GPIO_OUT_CFG_1	Page 625
0x1EF20E	GPIO Output Configuration 2	GPIO_OUT_CFG_2	Page 627
0x1EF20F	GPIO Output Configuration 3	GPIO_OUT_CFG_3	Page 629
0x1EF210	GPIO Output Configuration 4	GPIO_OUT_CFG_4	Page 631
0x1EF211	GPIO Output Configuration 5	GPIO_OUT_CFG_5	Page 633
0x1EF212	GPIO Output Configuration 6	GPIO_OUT_CFG_6	Page 635

Table 1718 • **GPIO_CFG_STAT** *(continued)*

Address	Short Description	Register Name	Details
0x1EF213	GPIO Output Configuration 7	GPIO_OUT_CFG_7	Page 637
0x1EF214	GPIO Output Configuration 8	GPIO_OUT_CFG_8	Page 639
0x1EF215	GPIO Output Configuration 9	GPIO_OUT_CFG_9	Page 641
0x1EF216	GPIO Output Configuration 10	GPIO_OUT_CFG_10	Page 643
0x1EF217	GPIO Output Configuration 11	GPIO_OUT_CFG_11	Page 645
0x1EF218	GPIO Output Configuration 12	GPIO_OUT_CFG_12	Page 647
0x1EF219	GPIO Output Configuration 13	GPIO_OUT_CFG_13	Page 649
0x1EF21A	GPIO Output Configuration 14	GPIO_OUT_CFG_14	Page 651
0x1EF21B	GPIO Output Configuration 15	GPIO_OUT_CFG_15	Page 653
0x1EF21C	GPIO Output Configuration 16	GPIO_OUT_CFG_16	Page 655
0x1EF21D	GPIO Output Configuration 17	GPIO_OUT_CFG_17	Page 657
0x1EF21E	GPIO Output Configuration 18	GPIO_OUT_CFG_18	Page 659
0x1EF21F	GPIO Output Configuration 19	GPIO_OUT_CFG_19	Page 661
0x1EF220	GPIO Output Configuration 20	GPIO_OUT_CFG_20	Page 663
0x1EF221	GPIO Output Configuration 21	GPIO_OUT_CFG_21	Page 665
0x1EF222	GPIO Output Configuration 22	GPIO_OUT_CFG_22	Page 667
0x1EF223	GPIO Output Configuration 23	GPIO_OUT_CFG_23	Page 669
0x1EF224	GPIO Output Configuration 24	GPIO_OUT_CFG_24	Page 671
0x1EF225	GPIO Output Configuration 25	GPIO_OUT_CFG_25	Page 673
0x1EF226	GPIO Output Configuration 26	GPIO_OUT_CFG_26	Page 675
0x1EF227	GPIO Output Configuration 27	GPIO_OUT_CFG_27	Page 677
0x1EF228	GPIO Output Configuration 28	GPIO_OUT_CFG_28	Page 679
0x1EF229	GPIO Output Configuration 29	GPIO_OUT_CFG_29	Page 681
0x1EF22A	GPIO Output Configuration 30	GPIO_OUT_CFG_30	Page 683
0x1EF22B	GPIO Output Configuration 31	GPIO_OUT_CFG_31	Page 685
0x1EF22C	GPIO Output Configuration 32	GPIO_OUT_CFG_32	Page 687
0x1EF22D	GPIO Output Configuration 33	GPIO_OUT_CFG_33	Page 689
0x1EF22E	GPIO Output Configuration 34	GPIO_OUT_CFG_34	Page 691
0x1EF22F	GPIO Output Configuration 35	GPIO_OUT_CFG_35	Page 693
0x1EF230	GPIO Output Configuration 36	GPIO_OUT_CFG_36	Page 695
0x1EF231	GPIO Output Configuration 37	GPIO_OUT_CFG_37	Page 697
0x1EF232	GPIO Output Configuration 38	GPIO_OUT_CFG_38	Page 699
0x1EF233	GPIO Output Configuration 39	GPIO_OUT_CFG_39	Page 701
0x1EF234	Channel 0 Line LOPC Configuration	CH0_LINE_LOPC_CFG	Page 703
0x1EF235	Channel 1 Line LOPC Configuration	CH1_LINE_LOPC_CFG	Page 704
0x1EF236	Channel 2 Line LOPC Configuration	CH2_LINE_LOPC_CFG	Page 704
0x1EF237	Channel 3 Line LOPC Configuration	CH3_LINE_LOPC_CFG	Page 704
0x1EF238	Channel 0 Host LOPC Configuration	CH0_HOST_LOPC_CFG	Page 705

Table 1718 • **GPIO_CFG_STAT** ***(continued)***

Address	Short Description	Register Name	Details
0x1EF239	Channel 1 Host LOPC Configuration	CH1_HOST_LOPC_CFG	Page 705
0x1EF23A	Channel 2 Host LOPC Configuration	CH2_HOST_LOPC_CFG	Page 705
0x1EF23B	Channel 3 Host LOPC Configuration	CH3_HOST_LOPC_CFG	Page 705
0x1EF23C	Channel 0 TOSI Configuration	CH0_TOSI_SDAT_CFG	Page 706
0x1EF23D	Channel 1 TOSI Configuration	CH1_TOSI_SDAT_CFG	Page 706
0x1EF23E	Channel 2 TOSI Configuration	CH2_TOSI_SDAT_CFG	Page 706
0x1EF23F	Channel 3 TOSI Configuration	CH3_TOSI_SDAT_CFG	Page 707
0x1EF240	Channel 0 I2C Master Data Configuration	CH0_I2C_MST_DATA_IN_CFG	Page 707
0x1EF241	Channel 1 I2C Master Data Configuration	CH1_I2C_MST_DATA_IN_CFG	Page 707
0x1EF242	Channel 2 I2C Master Data Configuration	CH2_I2C_MST_DATA_IN_CFG	Page 708
0x1EF243	Channel 3 I2C Master Data Configuration	CH3_I2C_MST_DATA_IN_CFG	Page 708
0x1EF244	Channel 0 I2C Master Clock Configuration	CH0_I2C_MST_CLK_IN_CFG	Page 708
0x1EF245	Channel 1 I2C Master Clock Configuration	CH1_I2C_MST_CLK_IN_CFG	Page 709
0x1EF246	Channel 2 I2C Master Clock Configuration	CH2_I2C_MST_CLK_IN_CFG	Page 709
0x1EF247	Channel 3 I2C Master Clock Configuration	CH3_I2C_MST_CLK_IN_CFG	Page 709
0x1EF248 - 0x1EF24F	EXP4 External Configuration	EXP4_EXT_IN_CFG	Page 710
0x1EF250 - 0x1EF257	AS External Configuration	AS_EXT_IN_CFG	Page 710
0x1EF258	I2C CLK Configuration	I2C_CLKIN_CFG	Page 710
0x1EF259	I2C Data Configuration	I2C_DATAIN_CFG	Page 710
0x1EF25A	PMTICK Configuration	PMTICK_CFG	Page 711
0x1EF25B	Blink Configuration	BLINK_CFG	Page 711

Table 1719 • **INTR_CFG_STAT**

Address	Short Description	Register Name	Details
0x1EF25C - 0x1EF25F	Interrupt Source	INTR_SRC_EN	Page 711
0x1EF260 - 0x1EF263	Interrupt Status	INTR_STAT	Page 712

2.28.1 GPIO Configuration and Status

2.28.1.1 GPIO Output Enable Config 1

Short Name:GPIO_CFG1

Address:0x1EF200

Table 1720 • **GPIO Output Enable Config 1**

Bit	Name	Access	Description	Default
7:0	GPIO_OUT1_EN	R/W	Output enable mask for GPIO[39:32]. Each bit corresponds to the output enable of that GPIO. e.g. bit 1 -> GPIO[33] 0 = Output is not enabled (output buffer is tri-stated) 1 = Output is enabled (output is either pull low or is tri-stated depending on what is driving it)	0x01

2.28.1.2 GPIO Output Enable Config 0

Short Name:GPIO_CFG0

Address:0x1EF201

Table 1721 • **GPIO Output Enable Config 0**

Bit	Name	Access	Description	Default
31:0	GPIO_OUT_EN	R/W	Output enable mask. Each bit corresponds to the output enable of that GPIO. e.g. bit 7 -> GPIO[7] 0 = Output is not enabled (output buffer is tri-stated) 1 = Output is enabled (output is either pull low or is tri-stated depending on what is driving it)	0x00000000

2.28.1.3 GPIO Output Invert Config 1

Short Name:GPIO_OUT_INV_CFG1

Address:0x1EF202

Table 1722 • **GPIO Output Invert Config 1**

Bit	Name	Access	Description	Default
7:0	GPIO_OUT1_INV	R/W	Output invert for GPIO[39:32]. Each bit corresponds to the output invert of that GPIO. e.g. bit 1 -> GPIO[33] 0 = Output is not inverted (output reflects state of selected source) 1 = Output is inverted	0x00

2.28.1.4 GPIO Output Invert Config 0

Short Name:GPIO_OUT_INV_CFG0

Address:0x1EF203

Table 1723 • **GPIO Output Invert Config 0**

Bit	Name	Access	Description	Default
31:0	GPIO_OUT_INV	R/W	Output invert. Each bit corresponds to the output enable of that GPIO. e.g. bit 7 -> GPIO[7] 0 = Output is not inverted (output reflects state of selected source) 1 = Output is inverted	0x00000000

2.28.1.5 Current Status of GPIO Inputs 1

Short Name:GPIO_STAT1

Address:0x1EF204

Table 1724 • **Current Status of GPIO Inputs 1**

Bit	Name	Access	Description	Default
7:0	GPIO_IN1_STAT	R/O	Input state of each GPIO input [39:32]	0x00

2.28.1.6 Current Status of GPIO Inputs 0

Short Name:GPIO_STAT0

Address:0x1EF205

Table 1725 • **Current Status of GPIO Inputs 0**

Bit	Name	Access	Description	Default
31:0	GPIO_IN_STAT	R/O	Input state of each GPIO input	0x00000000

2.28.1.7 Current Status of GPIO Outputs 1

Short Name:GPIO_OUT_STAT1

Address:0x1EF206

Table 1726 • **Current Status of GPIO Outputs 1**

Bit	Name	Access	Description	Default
7:0	GPIO_OUT1_STAT	R/O	Input state of each GPIO output [39:32]	0x00

2.28.1.8 Current Status of GPIO Outputs 0

Short Name:GPIO_OUT_STAT0

Address:0x1EF207

Table 1727 • **Current Status of GPIO Outputs 0**

Bit	Name	Access	Description	Default
31:0	GPIO_OUT_STAT	R/O	Input state of each GPIO output	0x00000000

2.28.1.9 GPIO State Change 1

Short Name:GPIO_CHANGE1

Address:0x1EF208

Table 1728 • **GPIO State Change 1**

Bit	Name	Access	Description	Default
7:0	GPIO_IN1_CHG_STICKY	Sticky	GPIO input state change detection for each GPIO[39:32]	0x00

2.28.1.10 GPIO State Change 0

Short Name:GPIO_CHANGE0

Address:0x1EF209

Table 1729 • **GPIO State Change 0**

Bit	Name	Access	Description	Default
31:0	GPIO_IN_CHG_STICKY	Sticky	GPIO input state change detection for each GPIO[31:0]	0x00000000

2.28.1.11 GPIO Interrupt Mask 1

Short Name:GPIO_MASK1

Address:0x1EF20A

Table 1730 • **GPIO Interrupt Mask 1**

Bit	Name	Access	Description	Default
7:0	GPIO_IN1_INTR_EN	R/W	0 = Corresponding GPIO_IN1_CHG_STICKY will not propagate to INTR 1 = Corresponding GPIO_IN1_CHG_STICKY will propagate to INTR	0x00

2.28.1.12 GPIO Interrupt Mask 0

Short Name:GPIO_MASK0

Address:0x1EF20B

Table 1731 • **GPIO Interrupt Mask 0**

Bit	Name	Access	Description	Default
31:0	GPIO_IN_INTR_EN	R/W	Interrupt enable mask 0 = Corresponding GPIO_IN_CHG_STICKY will not propagate to INTR 1 = Corresponding GPIO_IN_CHG_STICKY will propagate to INTR	0x00000000

2.28.1.13 GPIO Output Configuration 0

Short Name:GPIO_OUT_CFG_0

Address:0x1EF20C

Table 1732 **• GPIO Output Configuration 0**

Bit	Name	Access	Description	Default
6:0	GPIO_0_SEL	R/W	Selects the source for GPIO_0 output 0 = GPIO output 0 from channel 0 1 = GPIO output 1 from channel 0 2 = GPIO output 2 from channel 0 3 = GPIO output 3 from channel 0 4 = GPIO output 4 from channel 0 5 = GPIO output 5 from channel 0 6 = GPIO output 6 from channel 0 7 = GPIO output 7 from channel 0 8 = GPIO output 0 from channel 1 9 = GPIO output 1 from channel 1 10 = GPIO output 2 from channel 1 11 = GPIO output 3 from channel 1 12 = GPIO output 4 from channel 1 13 = GPIO output 5 from channel 1 14 = GPIO output 6 from channel 1 15 = GPIO output 7 from channel 1 16 = GPIO output 0 from channel 2 17 = GPIO output 1 from channel 2 18 = GPIO output 2 from channel 2 19 = GPIO output 3 from channel 2 20 = GPIO output 4 from channel 2 21 = GPIO output 5 from channel 2 22 = GPIO output 6 from channel 2 23 = GPIO output 7 from channel 2 24 = GPIO output 0 from channel 3 25 = GPIO output 1 from channel 3 26 = GPIO output 2 from channel 3 27 = GPIO output 3 from channel 3 28 = GPIO output 4 from channel 3 29 = GPIO output 5 from channel 3 30 = GPIO output 6 from channel 3 31 = GPIO output 7 from channel 3 32 = Tx Enable for channel 0 33 = Tx Enable for channel 1 34 = Tx Enable for channel 2 35 = Tx Enable for channel 3	0x00

Table 1732 • **GPIO Output Configuration 0** ***(continued)***

Bit	Name	Access	Description	Default
6:0	GPIO_0_SEL	R/W	*(continued)* Selects the source for GPIO_0 output 36 = PPS_0 from ip1588 37 = PPS_1 from ip1588 38 = PPS_2 from ip1588 39 = PPS_3 from ip1588 40 = PLL5G Lock status from Line PLL 41 = PLL5G Lock status from Host PLL 42 = RCOMP Busy 43 = N/A 44 = N/A 45 = N/A 46 = N/A 47 = N/A 48 = Channel interrupt 0 from channel 0 49 = Channel interrupt 1 from channel 0 50 = Channel interrupt 0 from channel 1 51 = Channel interrupt 1 from channel 1 52 = Channel interrupt 0 from channel 2 53 = Channel interrupt 1 from channel 2 54 = Channel interrupt 0 from channel 3 55 = Channel interrupt 1 from channel 3 56 = Interrupt from ip1588 channel 0 57 = Interrupt from ip1588 channel 1 58 = Interrupt from ip1588 channel 2 59 = Interrupt from ip1588 channel 3 60 = Timestamp FIFO !empty from ip1588 channel 0 61 = Timestamp FIFO !empty from ip1588 channel 1 62 = Timestamp FIFO !empty from ip1588 channel 2 63 = Timestamp FIFO !empty from ip1588 channel 3 64 = Aggregated interrupt 0 65 = Aggregated interrupt 1 66 = Aggregated interrupt 2 67 = Aggregated interrupt 3 68 = Interrupt from pll 0 69 = Interrupt from pll 1 70 = I2C Slave SDA 71 = Cross connect interrupt 72 = LED Blinker 73-127 = Drive low (or high by also setting output INV bit)	0x00

2.28.1.14 GPIO Output Configuration 1

Short Name:GPIO_OUT_CFG_1

Address:0x1EF20D

Table 1733 **• GPIO Output Configuration 1**

Bit	Name	Access	Description	Default
6:0	GPIO_1_SEL	R/W	Selects the source for GPIO_1 output 0 = GPIO output 0 from channel 0 1 = GPIO output 1 from channel 0 2 = GPIO output 2 from channel 0 3 = GPIO output 3 from channel 0 4 = GPIO output 4 from channel 0 5 = GPIO output 5 from channel 0 6 = GPIO output 6 from channel 0 7 = GPIO output 7 from channel 0 8 = GPIO output 0 from channel 1 9 = GPIO output 1 from channel 1 10 = GPIO output 2 from channel 1 11 = GPIO output 3 from channel 1 12 = GPIO output 4 from channel 1 13 = GPIO output 5 from channel 1 14 = GPIO output 6 from channel 1 15 = GPIO output 7 from channel 1 16 = GPIO output 0 from channel 2 17 = GPIO output 1 from channel 2 18 = GPIO output 2 from channel 2 19 = GPIO output 3 from channel 2 20 = GPIO output 4 from channel 2 21 = GPIO output 5 from channel 2 22 = GPIO output 6 from channel 2 23 = GPIO output 7 from channel 2 24 = GPIO output 0 from channel 3 25 = GPIO output 1 from channel 3 26 = GPIO output 2 from channel 3 27 = GPIO output 3 from channel 3 28 = GPIO output 4 from channel 3 29 = GPIO output 5 from channel 3 30 = GPIO output 6 from channel 3 31 = GPIO output 7 from channel 3 32 = Tx Enable for channel 0 33 = Tx Enable for channel 1 34 = Tx Enable for channel 2 35 = Tx Enable for channel 3	0x00

Table 1733 • **GPIO Output Configuration 1** ***(continued)***

Bit	Name	Access	Description	Default
6:0	GPIO_1_SEL	R/W	*(continued)* Selects the source for GPIO_1 output 36 = PPS_0 from ip1588 37 = PPS_1 from ip1588 38 = PPS_2 from ip1588 39 = PPS_3 from ip1588 40 = PLL5G Lock status from Line PLL 41 = PLL5G Lock status from Host PLL 42 = RCOMP Busy 43 = N/A 44 = N/A 45 = N/A 46 = N/A 47 = N/A 48 = Channel interrupt 0 from channel 0 49 = Channel interrupt 1 from channel 0 50 = Channel interrupt 0 from channel 1 51 = Channel interrupt 1 from channel 1 52 = Channel interrupt 0 from channel 2 53 = Channel interrupt 1 from channel 2 54 = Channel interrupt 0 from channel 3 55 = Channel interrupt 1 from channel 3 56 = Interrupt from ip1588 channel 0 57 = Interrupt from ip1588 channel 1 58 = Interrupt from ip1588 channel 2 59 = Interrupt from ip1588 channel 3 60 = Timestamp FIFO !empty from ip1588 channel 0 61 = Timestamp FIFO !empty from ip1588 channel 1 62 = Timestamp FIFO !empty from ip1588 channel 2 63 = Timestamp FIFO !empty from ip1588 channel 3 64 = Aggregated interrupt 0 65 = Aggregated interrupt 1 66 = Aggregated interrupt 2 67 = Aggregated interrupt 3 68 = Interrupt from pll 0 69 = Interrupt from pll 1 70 = I2C Slave SDA 71 = Cross connect interrupt 72 = LED Blinker 73-127 = Drive low (or high by also setting output INV bit)	0x00

2.28.1.15 GPIO Output Configuration 2

Short Name:GPIO_OUT_CFG_2

Address:0x1EF20E

Table 1734 **• GPIO Output Configuration 2**

Bit	Name	Access	Description	Default
6:0	GPIO_2_SEL	R/W	Selects the source for GPIO_2 output 0 = GPIO output 0 from channel 0 1 = GPIO output 1 from channel 0 2 = GPIO output 2 from channel 0 3 = GPIO output 3 from channel 0 4 = GPIO output 4 from channel 0 5 = GPIO output 5 from channel 0 6 = GPIO output 6 from channel 0 7 = GPIO output 7 from channel 0 8 = GPIO output 0 from channel 1 9 = GPIO output 1 from channel 1 10 = GPIO output 2 from channel 1 11 = GPIO output 3 from channel 1 12 = GPIO output 4 from channel 1 13 = GPIO output 5 from channel 1 14 = GPIO output 6 from channel 1 15 = GPIO output 7 from channel 1 16 = GPIO output 0 from channel 2 17 = GPIO output 1 from channel 2 18 = GPIO output 2 from channel 2 19 = GPIO output 3 from channel 2 20 = GPIO output 4 from channel 2 21 = GPIO output 5 from channel 2 22 = GPIO output 6 from channel 2 23 = GPIO output 7 from channel 2 24 = GPIO output 0 from channel 3 25 = GPIO output 1 from channel 3 26 = GPIO output 2 from channel 3 27 = GPIO output 3 from channel 3 28 = GPIO output 4 from channel 3 29 = GPIO output 5 from channel 3 30 = GPIO output 6 from channel 3 31 = GPIO output 7 from channel 3 32 = Tx Enable for channel 0 33 = Tx Enable for channel 1 34 = Tx Enable for channel 2 35 = Tx Enable for channel 3	0x00

Table 1734 • **GPIO Output Configuration 2** ***(continued)***

Bit	Name	Access	Description	Default
6:0	GPIO_2_SEL	R/W	*(continued)* Selects the source for GPIO_2 output 36 = PPS_0 from ip1588 37 = PPS_1 from ip1588 38 = PPS_2 from ip1588 39 = PPS_3 from ip1588 40 = PLL5G Lock status from Line PLL 41 = PLL5G Lock status from Host PLL 42 = RCOMP Busy 43 = N/A 44 = N/A 45 = N/A 46 = N/A 47 = N/A 48 = Channel interrupt 0 from channel 0 49 = Channel interrupt 1 from channel 0 50 = Channel interrupt 0 from channel 1 51 = Channel interrupt 1 from channel 1 52 = Channel interrupt 0 from channel 2 53 = Channel interrupt 1 from channel 2 54 = Channel interrupt 0 from channel 3 55 = Channel interrupt 1 from channel 3 56 = Interrupt from ip1588 channel 0 57 = Interrupt from ip1588 channel 1 58 = Interrupt from ip1588 channel 2 59 = Interrupt from ip1588 channel 3 60 = Timestamp FIFO !empty from ip1588 channel 0 61 = Timestamp FIFO !empty from ip1588 channel 1 62 = Timestamp FIFO !empty from ip1588 channel 2 63 = Timestamp FIFO !empty from ip1588 channel 3 64 = Aggregated interrupt 0 65 = Aggregated interrupt 1 66 = Aggregated interrupt 2 67 = Aggregated interrupt 3 68 = Interrupt from pll 0 69 = Interrupt from pll 1 70 = I2C Slave SDA 71 = Cross connect interrupt 72 = LED Blinker 73-127 = Drive low (or high by also setting output INV bit)	0x00

2.28.1.16 GPIO Output Configuration 3

Short Name:GPIO_OUT_CFG_3

Address:0x1EF20F

Table 1735 **• GPIO Output Configuration 3**

Bit	Name	Access	Description	Default
6:0	GPIO_3_SEL	R/W	Selects the source for GPIO_3 output 0 = GPIO output 0 from channel 0 1 = GPIO output 1 from channel 0 2 = GPIO output 2 from channel 0 3 = GPIO output 3 from channel 0 4 = GPIO output 4 from channel 0 5 = GPIO output 5 from channel 0 6 = GPIO output 6 from channel 0 7 = GPIO output 7 from channel 0 8 = GPIO output 0 from channel 1 9 = GPIO output 1 from channel 1 10 = GPIO output 2 from channel 1 11 = GPIO output 3 from channel 1 12 = GPIO output 4 from channel 1 13 = GPIO output 5 from channel 1 14 = GPIO output 6 from channel 1 15 = GPIO output 7 from channel 1 16 = GPIO output 0 from channel 2 17 = GPIO output 1 from channel 2 18 = GPIO output 2 from channel 2 19 = GPIO output 3 from channel 2 20 = GPIO output 4 from channel 2 21 = GPIO output 5 from channel 2 22 = GPIO output 6 from channel 2 23 = GPIO output 7 from channel 2 24 = GPIO output 0 from channel 3 25 = GPIO output 1 from channel 3 26 = GPIO output 2 from channel 3 27 = GPIO output 3 from channel 3 28 = GPIO output 4 from channel 3 29 = GPIO output 5 from channel 3 30 = GPIO output 6 from channel 3 31 = GPIO output 7 from channel 3 32 = Tx Enable for channel 0 33 = Tx Enable for channel 1 34 = Tx Enable for channel 2 35 = Tx Enable for channel 3	0x00

Table 1735 • **GPIO Output Configuration 3** ***(continued)***

Bit	Name	Access	Description	Default
6:0	GPIO_3_SEL	R/W	*(continued)* Selects the source for GPIO_3 output 36 = PPS_0 from ip1588 37 = PPS_1 from ip1588 38 = PPS_2 from ip1588 39 = PPS_3 from ip1588 40 = PLL5G Lock status from Line PLL 41 = PLL5G Lock status from Host PLL 42 = RCOMP Busy 43 = N/A 44 = N/A 45 = N/A 46 = N/A 47 = N/A 48 = Channel interrupt 0 from channel 0 49 = Channel interrupt 1 from channel 0 50 = Channel interrupt 0 from channel 1 51 = Channel interrupt 1 from channel 1 52 = Channel interrupt 0 from channel 2 53 = Channel interrupt 1 from channel 2 54 = Channel interrupt 0 from channel 3 55 = Channel interrupt 1 from channel 3 56 = Interrupt from ip1588 channel 0 57 = Interrupt from ip1588 channel 1 58 = Interrupt from ip1588 channel 2 59 = Interrupt from ip1588 channel 3 60 = Timestamp FIFO !empty from ip1588 channel 0 61 = Timestamp FIFO !empty from ip1588 channel 1 62 = Timestamp FIFO !empty from ip1588 channel 2 63 = Timestamp FIFO !empty from ip1588 channel 3 64 = Aggregated interrupt 0 65 = Aggregated interrupt 1 66 = Aggregated interrupt 2 67 = Aggregated interrupt 3 68 = Interrupt from pll 0 69 = Interrupt from pll 1 70 = I2C Slave SDA 71 = Cross connect interrupt 72 = LED Blinker 73-127 = Drive low (or high by also setting output INV bit)	0x00

2.28.1.17 GPIO Output Configuration 4

Short Name:GPIO_OUT_CFG_4

Address:0x1EF210

Table 1736 **• GPIO Output Configuration 4**

Bit	Name	Access	Description	Default
6:0	GPIO_4_SEL	R/W	Selects the source for GPIO_4 output 0 = GPIO output 0 from channel 0 1 = GPIO output 1 from channel 0 2 = GPIO output 2 from channel 0 3 = GPIO output 3 from channel 0 4 = GPIO output 4 from channel 0 5 = GPIO output 5 from channel 0 6 = GPIO output 6 from channel 0 7 = GPIO output 7 from channel 0 8 = GPIO output 0 from channel 1 9 = GPIO output 1 from channel 1 10 = GPIO output 2 from channel 1 11 = GPIO output 3 from channel 1 12 = GPIO output 4 from channel 1 13 = GPIO output 5 from channel 1 14 = GPIO output 6 from channel 1 15 = GPIO output 7 from channel 1 16 = GPIO output 0 from channel 2 17 = GPIO output 1 from channel 2 18 = GPIO output 2 from channel 2 19 = GPIO output 3 from channel 2 20 = GPIO output 4 from channel 2 21 = GPIO output 5 from channel 2 22 = GPIO output 6 from channel 2 23 = GPIO output 7 from channel 2 24 = GPIO output 0 from channel 3 25 = GPIO output 1 from channel 3 26 = GPIO output 2 from channel 3 27 = GPIO output 3 from channel 3 28 = GPIO output 4 from channel 3 29 = GPIO output 5 from channel 3 30 = GPIO output 6 from channel 3 31 = GPIO output 7 from channel 3 32 = Tx Enable for channel 0 33 = Tx Enable for channel 1 34 = Tx Enable for channel 2 35 = Tx Enable for channel 3	0x00

Table 1736 • **GPIO Output Configuration 4** ***(continued)***

Bit	Name	Access	Description	Default
6:0	GPIO_4_SEL	R/W	*(continued)* Selects the source for GPIO_4 output 36 = PPS_0 from ip1588 37 = PPS_1 from ip1588 38 = PPS_2 from ip1588 39 = PPS_3 from ip1588 40 = PLL5G Lock status from Line PLL 41 = PLL5G Lock status from Host PLL 42 = RCOMP Busy 43 = N/A 44 = N/A 45 = N/A 46 = N/A 47 = N/A 48 = Channel interrupt 0 from channel 0 49 = Channel interrupt 1 from channel 0 50 = Channel interrupt 0 from channel 1 51 = Channel interrupt 1 from channel 1 52 = Channel interrupt 0 from channel 2 53 = Channel interrupt 1 from channel 2 54 = Channel interrupt 0 from channel 3 55 = Channel interrupt 1 from channel 3 56 = Interrupt from ip1588 channel 0 57 = Interrupt from ip1588 channel 1 58 = Interrupt from ip1588 channel 2 59 = Interrupt from ip1588 channel 3 60 = Timestamp FIFO !empty from ip1588 channel 0 61 = Timestamp FIFO !empty from ip1588 channel 1 62 = Timestamp FIFO !empty from ip1588 channel 2 63 = Timestamp FIFO !empty from ip1588 channel 3 64 = Aggregated interrupt 0 65 = Aggregated interrupt 1 66 = Aggregated interrupt 2 67 = Aggregated interrupt 3 68 = Interrupt from pll 0 69 = Interrupt from pll 1 70 = I2C Slave SDA 71 = Cross connect interrupt 72 = LED Blinker 73-127 = Drive low (or high by also setting output INV bit)	0x00

2.28.1.18 GPIO Output Configuration 5

Short Name:GPIO_OUT_CFG_5

Address:0x1EF211

Table 1737 **• GPIO Output Configuration 5**

Bit	Name	Access	Description	Default
6:0	GPIO_5_SEL	R/W	Selects the source for GPIO_5 output 0 = GPIO output 0 from channel 0 1 = GPIO output 1 from channel 0 2 = GPIO output 2 from channel 0 3 = GPIO output 3 from channel 0 4 = GPIO output 4 from channel 0 5 = GPIO output 5 from channel 0 6 = GPIO output 6 from channel 0 7 = GPIO output 7 from channel 0 8 = GPIO output 0 from channel 1 9 = GPIO output 1 from channel 1 10 = GPIO output 2 from channel 1 11 = GPIO output 3 from channel 1 12 = GPIO output 4 from channel 1 13 = GPIO output 5 from channel 1 14 = GPIO output 6 from channel 1 15 = GPIO output 7 from channel 1 16 = GPIO output 0 from channel 2 17 = GPIO output 1 from channel 2 18 = GPIO output 2 from channel 2 19 = GPIO output 3 from channel 2 20 = GPIO output 4 from channel 2 21 = GPIO output 5 from channel 2 22 = GPIO output 6 from channel 2 23 = GPIO output 7 from channel 2 24 = GPIO output 0 from channel 3 25 = GPIO output 1 from channel 3 26 = GPIO output 2 from channel 3 27 = GPIO output 3 from channel 3 28 = GPIO output 4 from channel 3 29 = GPIO output 5 from channel 3 30 = GPIO output 6 from channel 3 31 = GPIO output 7 from channel 3 32 = Tx Enable for channel 0 33 = Tx Enable for channel 1 34 = Tx Enable for channel 2 35 = Tx Enable for channel 3	0x00

Table 1737 • **GPIO Output Configuration 5** ***(continued)***

Bit	Name	Access	Description	Default
6:0	GPIO_5_SEL	R/W	*(continued)* Selects the source for GPIO_5 output 36 = PPS_0 from ip1588 37 = PPS_1 from ip1588 38 = PPS_2 from ip1588 39 = PPS_3 from ip1588 40 = PLL5G Lock status from Line PLL 41 = PLL5G Lock status from Host PLL 42 = RCOMP Busy 43 = N/A 44 = N/A 45 = N/A 46 = N/A 47 = N/A 48 = Channel interrupt 0 from channel 0 49 = Channel interrupt 1 from channel 0 50 = Channel interrupt 0 from channel 1 51 = Channel interrupt 1 from channel 1 52 = Channel interrupt 0 from channel 2 53 = Channel interrupt 1 from channel 2 54 = Channel interrupt 0 from channel 3 55 = Channel interrupt 1 from channel 3 56 = Interrupt from ip1588 channel 0 57 = Interrupt from ip1588 channel 1 58 = Interrupt from ip1588 channel 2 59 = Interrupt from ip1588 channel 3 60 = Timestamp FIFO !empty from ip1588 channel 0 61 = Timestamp FIFO !empty from ip1588 channel 1 62 = Timestamp FIFO !empty from ip1588 channel 2 63 = Timestamp FIFO !empty from ip1588 channel 3 64 = Aggregated interrupt 0 65 = Aggregated interrupt 1 66 = Aggregated interrupt 2 67 = Aggregated interrupt 3 68 = Interrupt from pll 0 69 = Interrupt from pll 1 70 = I2C Slave SDA 71 = Cross connect interrupt 72 = LED Blinker 73-127 = Drive low (or high by also setting output INV bit)	0x00

2.28.1.19 GPIO Output Configuration 6

Short Name:GPIO_OUT_CFG_6

Address:0x1EF212

Table 1738 **• GPIO Output Configuration 6**

Bit	Name	Access	Description	Default
6:0	GPIO_6_SEL	R/W	Selects the source for GPIO_6 output 0 = GPIO output 0 from channel 0 1 = GPIO output 1 from channel 0 2 = GPIO output 2 from channel 0 3 = GPIO output 3 from channel 0 4 = GPIO output 4 from channel 0 5 = GPIO output 5 from channel 0 6 = GPIO output 6 from channel 0 7 = GPIO output 7 from channel 0 8 = GPIO output 0 from channel 1 9 = GPIO output 1 from channel 1 10 = GPIO output 2 from channel 1 11 = GPIO output 3 from channel 1 12 = GPIO output 4 from channel 1 13 = GPIO output 5 from channel 1 14 = GPIO output 6 from channel 1 15 = GPIO output 7 from channel 1 16 = GPIO output 0 from channel 2 17 = GPIO output 1 from channel 2 18 = GPIO output 2 from channel 2 19 = GPIO output 3 from channel 2 20 = GPIO output 4 from channel 2 21 = GPIO output 5 from channel 2 22 = GPIO output 6 from channel 2 23 = GPIO output 7 from channel 2 24 = GPIO output 0 from channel 3 25 = GPIO output 1 from channel 3 26 = GPIO output 2 from channel 3 27 = GPIO output 3 from channel 3 28 = GPIO output 4 from channel 3 29 = GPIO output 5 from channel 3 30 = GPIO output 6 from channel 3 31 = GPIO output 7 from channel 3 32 = Tx Enable for channel 0 33 = Tx Enable for channel 1 34 = Tx Enable for channel 2 35 = Tx Enable for channel 3	0x00

Table 1738 • **GPIO Output Configuration 6** ***(continued)***

Bit	Name	Access	Description	Default
6:0	GPIO_6_SEL	R/W	*(continued)* Selects the source for GPIO_6 output 36 = PPS_0 from ip1588 37 = PPS_1 from ip1588 38 = PPS_2 from ip1588 39 = PPS_3 from ip1588 40 = PLL5G Lock status from Line PLL 41 = PLL5G Lock status from Host PLL 42 = RCOMP Busy 43 = N/A 44 = N/A 45 = N/A 46 = N/A 47 = N/A 48 = Channel interrupt 0 from channel 0 49 = Channel interrupt 1 from channel 0 50 = Channel interrupt 0 from channel 1 51 = Channel interrupt 1 from channel 1 52 = Channel interrupt 0 from channel 2 53 = Channel interrupt 1 from channel 2 54 = Channel interrupt 0 from channel 3 55 = Channel interrupt 1 from channel 3 56 = Interrupt from ip1588 channel 0 57 = Interrupt from ip1588 channel 1 58 = Interrupt from ip1588 channel 2 59 = Interrupt from ip1588 channel 3 60 = Timestamp FIFO !empty from ip1588 channel 0 61 = Timestamp FIFO !empty from ip1588 channel 1 62 = Timestamp FIFO !empty from ip1588 channel 2 63 = Timestamp FIFO !empty from ip1588 channel 3 64 = Aggregated interrupt 0 65 = Aggregated interrupt 1 66 = Aggregated interrupt 2 67 = Aggregated interrupt 3 68 = Interrupt from pll 0 69 = Interrupt from pll 1 70 = I2C Slave SDA 71 = Cross connect interrupt 72 = LED Blinker 73-127 = Drive low (or high by also setting output INV bit)	0x00

2.28.1.20 GPIO Output Configuration 7

Short Name:GPIO_OUT_CFG_7

Address:0x1EF213

***Table 1739* • GPIO Output Configuration 7**

Bit	Name	Access	Description	Default
6:0	GPIO_7_SEL	R/W	Selects the source for GPIO_7 output 0 = GPIO output 0 from channel 0 1 = GPIO output 1 from channel 0 2 = GPIO output 2 from channel 0 3 = GPIO output 3 from channel 0 4 = GPIO output 4 from channel 0 5 = GPIO output 5 from channel 0 6 = GPIO output 6 from channel 0 7 = GPIO output 7 from channel 0 8 = GPIO output 0 from channel 1 9 = GPIO output 1 from channel 1 10 = GPIO output 2 from channel 1 11 = GPIO output 3 from channel 1 12 = GPIO output 4 from channel 1 13 = GPIO output 5 from channel 1 14 = GPIO output 6 from channel 1 15 = GPIO output 7 from channel 1 16 = GPIO output 0 from channel 2 17 = GPIO output 1 from channel 2 18 = GPIO output 2 from channel 2 19 = GPIO output 3 from channel 2 20 = GPIO output 4 from channel 2 21 = GPIO output 5 from channel 2 22 = GPIO output 6 from channel 2 23 = GPIO output 7 from channel 2 24 = GPIO output 0 from channel 3 25 = GPIO output 1 from channel 3 26 = GPIO output 2 from channel 3 27 = GPIO output 3 from channel 3 28 = GPIO output 4 from channel 3 29 = GPIO output 5 from channel 3 30 = GPIO output 6 from channel 3 31 = GPIO output 7 from channel 3 32 = Tx Enable for channel 0 33 = Tx Enable for channel 1 34 = Tx Enable for channel 2 35 = Tx Enable for channel 3	0x00

Table 1739 • **GPIO Output Configuration 7** ***(continued)***

Bit	Name	Access	Description	Default
6:0	GPIO_7_SEL	R/W	*(continued)* Selects the source for GPIO_7 output 36 = PPS_0 from ip1588 37 = PPS_1 from ip1588 38 = PPS_2 from ip1588 39 = PPS_3 from ip1588 40 = PLL5G Lock status from Line PLL 41 = PLL5G Lock status from Host PLL 42 = RCOMP Busy 43 = N/A 44 = N/A 45 = N/A 46 = N/A 47 = N/A 48 = Channel interrupt 0 from channel 0 49 = Channel interrupt 1 from channel 0 50 = Channel interrupt 0 from channel 1 51 = Channel interrupt 1 from channel 1 52 = Channel interrupt 0 from channel 2 53 = Channel interrupt 1 from channel 2 54 = Channel interrupt 0 from channel 3 55 = Channel interrupt 1 from channel 3 56 = Interrupt from ip1588 channel 0 57 = Interrupt from ip1588 channel 1 58 = Interrupt from ip1588 channel 2 59 = Interrupt from ip1588 channel 3 60 = Timestamp FIFO !empty from ip1588 channel 0 61 = Timestamp FIFO !empty from ip1588 channel 1 62 = Timestamp FIFO !empty from ip1588 channel 2 63 = Timestamp FIFO !empty from ip1588 channel 3 64 = Aggregated interrupt 0 65 = Aggregated interrupt 1 66 = Aggregated interrupt 2 67 = Aggregated interrupt 3 68 = Interrupt from pll 0 69 = Interrupt from pll 1 70 = I2C Slave SDA 71 = Cross connect interrupt 72 = LED Blinker 73-127 = Drive low (or high by also setting output INV bit)	0x00

2.28.1.21 GPIO Output Configuration 8

Short Name:GPIO_OUT_CFG_8

Address:0x1EF214

Table 1740 **• GPIO Output Configuration 8**

Bit	Name	Access	Description	Default
6:0	GPIO_8_SEL	R/W	Selects the source for GPIO_8 output 0 = GPIO output 0 from channel 0 1 = GPIO output 1 from channel 0 2 = GPIO output 2 from channel 0 3 = GPIO output 3 from channel 0 4 = GPIO output 4 from channel 0 5 = GPIO output 5 from channel 0 6 = GPIO output 6 from channel 0 7 = GPIO output 7 from channel 0 8 = GPIO output 0 from channel 1 9 = GPIO output 1 from channel 1 10 = GPIO output 2 from channel 1 11 = GPIO output 3 from channel 1 12 = GPIO output 4 from channel 1 13 = GPIO output 5 from channel 1 14 = GPIO output 6 from channel 1 15 = GPIO output 7 from channel 1 16 = GPIO output 0 from channel 2 17 = GPIO output 1 from channel 2 18 = GPIO output 2 from channel 2 19 = GPIO output 3 from channel 2 20 = GPIO output 4 from channel 2 21 = GPIO output 5 from channel 2 22 = GPIO output 6 from channel 2 23 = GPIO output 7 from channel 2 24 = GPIO output 0 from channel 3 25 = GPIO output 1 from channel 3 26 = GPIO output 2 from channel 3 27 = GPIO output 3 from channel 3 28 = GPIO output 4 from channel 3 29 = GPIO output 5 from channel 3 30 = GPIO output 6 from channel 3 31 = GPIO output 7 from channel 3 32 = Tx Enable for channel 0 33 = Tx Enable for channel 1 34 = Tx Enable for channel 2 35 = Tx Enable for channel 3	0x00

Table 1740 • **GPIO Output Configuration 8** ***(continued)***

Bit	Name	Access	Description	Default
6:0	GPIO_8_SEL	R/W	*(continued)* Selects the source for GPIO_8 output 36 = PPS_0 from ip1588 37 = PPS_1 from ip1588 38 = PPS_2 from ip1588 39 = PPS_3 from ip1588 40 = PLL5G Lock status from Line PLL 41 = PLL5G Lock status from Host PLL 42 = RCOMP Busy 43 = N/A 44 = N/A 45 = N/A 46 = N/A 47 = N/A 48 = Channel interrupt 0 from channel 0 49 = Channel interrupt 1 from channel 0 50 = Channel interrupt 0 from channel 1 51 = Channel interrupt 1 from channel 1 52 = Channel interrupt 0 from channel 2 53 = Channel interrupt 1 from channel 2 54 = Channel interrupt 0 from channel 3 55 = Channel interrupt 1 from channel 3 56 = Interrupt from ip1588 channel 0 57 = Interrupt from ip1588 channel 1 58 = Interrupt from ip1588 channel 2 59 = Interrupt from ip1588 channel 3 60 = Timestamp FIFO !empty from ip1588 channel 0 61 = Timestamp FIFO !empty from ip1588 channel 1 62 = Timestamp FIFO !empty from ip1588 channel 2 63 = Timestamp FIFO !empty from ip1588 channel 3 64 = Aggregated interrupt 0 65 = Aggregated interrupt 1 66 = Aggregated interrupt 2 67 = Aggregated interrupt 3 68 = Interrupt from pll 0 69 = Interrupt from pll 1 70 = I2C Slave SDA 71 = Cross connect interrupt 72 = LED Blinker 73-127 = Drive low (or high by also setting output INV bit)	0x00

2.28.1.22 GPIO Output Configuration 9

Short Name:GPIO_OUT_CFG_9

Address:0x1EF215

Table 1741 **• GPIO Output Configuration 9**

Bit	Name	Access	Description	Default
6:0	GPIO_9_SEL	R/W	Selects the source for GPIO_9 output 0 = GPIO output 0 from channel 0 1 = GPIO output 1 from channel 0 2 = GPIO output 2 from channel 0 3 = GPIO output 3 from channel 0 4 = GPIO output 4 from channel 0 5 = GPIO output 5 from channel 0 6 = GPIO output 6 from channel 0 7 = GPIO output 7 from channel 0 8 = GPIO output 0 from channel 1 9 = GPIO output 1 from channel 1 10 = GPIO output 2 from channel 1 11 = GPIO output 3 from channel 1 12 = GPIO output 4 from channel 1 13 = GPIO output 5 from channel 1 14 = GPIO output 6 from channel 1 15 = GPIO output 7 from channel 1 16 = GPIO output 0 from channel 2 17 = GPIO output 1 from channel 2 18 = GPIO output 2 from channel 2 19 = GPIO output 3 from channel 2 20 = GPIO output 4 from channel 2 21 = GPIO output 5 from channel 2 22 = GPIO output 6 from channel 2 23 = GPIO output 7 from channel 2 24 = GPIO output 0 from channel 3 25 = GPIO output 1 from channel 3 26 = GPIO output 2 from channel 3 27 = GPIO output 3 from channel 3 28 = GPIO output 4 from channel 3 29 = GPIO output 5 from channel 3 30 = GPIO output 6 from channel 3 31 = GPIO output 7 from channel 3 32 = Tx Enable for channel 0 33 = Tx Enable for channel 1 34 = Tx Enable for channel 2 35 = Tx Enable for channel 3	0x00

Table 1741 • **GPIO Output Configuration 9** ***(continued)***

Bit	Name	Access	Description	Default
6:0	GPIO_9_SEL	R/W	*(continued)* Selects the source for GPIO_9 output 36 = PPS_0 from ip1588 37 = PPS_1 from ip1588 38 = PPS_2 from ip1588 39 = PPS_3 from ip1588 40 = PLL5G Lock status from Line PLL 41 = PLL5G Lock status from Host PLL 42 = RCOMP Busy 43 = N/A 44 = N/A 45 = N/A 46 = N/A 47 = N/A 48 = Channel interrupt 0 from channel 0 49 = Channel interrupt 1 from channel 0 50 = Channel interrupt 0 from channel 1 51 = Channel interrupt 1 from channel 1 52 = Channel interrupt 0 from channel 2 53 = Channel interrupt 1 from channel 2 54 = Channel interrupt 0 from channel 3 55 = Channel interrupt 1 from channel 3 56 = Interrupt from ip1588 channel 0 57 = Interrupt from ip1588 channel 1 58 = Interrupt from ip1588 channel 2 59 = Interrupt from ip1588 channel 3 60 = Timestamp FIFO !empty from ip1588 channel 0 61 = Timestamp FIFO !empty from ip1588 channel 1 62 = Timestamp FIFO !empty from ip1588 channel 2 63 = Timestamp FIFO !empty from ip1588 channel 3 64 = Aggregated interrupt 0 65 = Aggregated interrupt 1 66 = Aggregated interrupt 2 67 = Aggregated interrupt 3 68 = Interrupt from pll 0 69 = Interrupt from pll 1 70 = I2C Slave SDA 71 = Cross connect interrupt 72 = LED Blinker 73-127 = Drive low (or high by also setting output INV bit)	0x00

2.28.1.23 GPIO Output Configuration 10

Short Name:GPIO_OUT_CFG_10

Address:0x1EF216

Table 1742 **• GPIO Output Configuration 10**

Bit	Name	Access	Description	Default
6:0	GPIO_10_SEL	R/W	Selects the source for GPIO_10 output 0 = GPIO output 0 from channel 0 1 = GPIO output 1 from channel 0 2 = GPIO output 2 from channel 0 3 = GPIO output 3 from channel 0 4 = GPIO output 4 from channel 0 5 = GPIO output 5 from channel 0 6 = GPIO output 6 from channel 0 7 = GPIO output 7 from channel 0 8 = GPIO output 0 from channel 1 9 = GPIO output 1 from channel 1 10 = GPIO output 2 from channel 1 11 = GPIO output 3 from channel 1 12 = GPIO output 4 from channel 1 13 = GPIO output 5 from channel 1 14 = GPIO output 6 from channel 1 15 = GPIO output 7 from channel 1 16 = GPIO output 0 from channel 2 17 = GPIO output 1 from channel 2 18 = GPIO output 2 from channel 2 19 = GPIO output 3 from channel 2 20 = GPIO output 4 from channel 2 21 = GPIO output 5 from channel 2 22 = GPIO output 6 from channel 2 23 = GPIO output 7 from channel 2 24 = GPIO output 0 from channel 3 25 = GPIO output 1 from channel 3 26 = GPIO output 2 from channel 3 27 = GPIO output 3 from channel 3 28 = GPIO output 4 from channel 3 29 = GPIO output 5 from channel 3 30 = GPIO output 6 from channel 3 31 = GPIO output 7 from channel 3 32 = Tx Enable for channel 0 33 = Tx Enable for channel 1 34 = Tx Enable for channel 2 35 = Tx Enable for channel 3	0x00

Table 1742 • **GPIO Output Configuration 10** ***(continued)***

Bit	Name	Access	Description	Default
6:0	GPIO_10_SEL	R/W	*(continued)* Selects the source for GPIO_10 output 36 = PPS_0 from ip1588 37 = PPS_1 from ip1588 38 = PPS_2 from ip1588 39 = PPS_3 from ip1588 40 = PLL5G Lock status from Line PLL 41 = PLL5G Lock status from Host PLL 42 = RCOMP Busy 43 = N/A 44 = N/A 45 = N/A 46 = N/A 47 = N/A 48 = Channel interrupt 0 from channel 0 49 = Channel interrupt 1 from channel 0 50 = Channel interrupt 0 from channel 1 51 = Channel interrupt 1 from channel 1 52 = Channel interrupt 0 from channel 2 53 = Channel interrupt 1 from channel 2 54 = Channel interrupt 0 from channel 3 55 = Channel interrupt 1 from channel 3 56 = Interrupt from ip1588 channel 0 57 = Interrupt from ip1588 channel 1 58 = Interrupt from ip1588 channel 2 59 = Interrupt from ip1588 channel 3 60 = Timestamp FIFO !empty from ip1588 channel 0 61 = Timestamp FIFO !empty from ip1588 channel 1 62 = Timestamp FIFO !empty from ip1588 channel 2 63 = Timestamp FIFO !empty from ip1588 channel 3 64 = Aggregated interrupt 0 65 = Aggregated interrupt 1 66 = Aggregated interrupt 2 67 = Aggregated interrupt 3 68 = Interrupt from pll 0 69 = Interrupt from pll 1 70 = I2C Slave SDA 71 = Cross connect interrupt 72 = LED Blinker 73-127 = Drive low (or high by also setting output INV bit)	0x00

2.28.1.24 GPIO Output Configuration 11

Short Name:GPIO_OUT_CFG_11

Address:0x1EF217

Table 1743 **• GPIO Output Configuration 11**

Bit	Name	Access	Description	Default
6:0	GPIO_11_SEL	R/W	Selects the source for GPIO_11 output 0 = GPIO output 0 from channel 0 1 = GPIO output 1 from channel 0 2 = GPIO output 2 from channel 0 3 = GPIO output 3 from channel 0 4 = GPIO output 4 from channel 0 5 = GPIO output 5 from channel 0 6 = GPIO output 6 from channel 0 7 = GPIO output 7 from channel 0 8 = GPIO output 0 from channel 1 9 = GPIO output 1 from channel 1 10 = GPIO output 2 from channel 1 11 = GPIO output 3 from channel 1 12 = GPIO output 4 from channel 1 13 = GPIO output 5 from channel 1 14 = GPIO output 6 from channel 1 15 = GPIO output 7 from channel 1 16 = GPIO output 0 from channel 2 17 = GPIO output 1 from channel 2 18 = GPIO output 2 from channel 2 19 = GPIO output 3 from channel 2 20 = GPIO output 4 from channel 2 21 = GPIO output 5 from channel 2 22 = GPIO output 6 from channel 2 23 = GPIO output 7 from channel 2 24 = GPIO output 0 from channel 3 25 = GPIO output 1 from channel 3 26 = GPIO output 2 from channel 3 27 = GPIO output 3 from channel 3 28 = GPIO output 4 from channel 3 29 = GPIO output 5 from channel 3 30 = GPIO output 6 from channel 3 31 = GPIO output 7 from channel 3 32 = Tx Enable for channel 0 33 = Tx Enable for channel 1 34 = Tx Enable for channel 2 35 = Tx Enable for channel 3	0x00

Table 1743 • **GPIO Output Configuration 11** ***(continued)***

Bit	Name	Access	Description	Default
6:0	GPIO_11_SEL	R/W	*(continued)* Selects the source for GPIO_11 output 36 = PPS_0 from ip1588 37 = PPS_1 from ip1588 38 = PPS_2 from ip1588 39 = PPS_3 from ip1588 40 = PLL5G Lock status from Line PLL 41 = PLL5G Lock status from Host PLL 42 = RCOMP Busy 43 = N/A 44 = N/A 45 = N/A 46 = N/A 47 = N/A 48 = Channel interrupt 0 from channel 0 49 = Channel interrupt 1 from channel 0 50 = Channel interrupt 0 from channel 1 51 = Channel interrupt 1 from channel 1 52 = Channel interrupt 0 from channel 2 53 = Channel interrupt 1 from channel 2 54 = Channel interrupt 0 from channel 3 55 = Channel interrupt 1 from channel 3 56 = Interrupt from ip1588 channel 0 57 = Interrupt from ip1588 channel 1 58 = Interrupt from ip1588 channel 2 59 = Interrupt from ip1588 channel 3 60 = Timestamp FIFO !empty from ip1588 channel 0 61 = Timestamp FIFO !empty from ip1588 channel 1 62 = Timestamp FIFO !empty from ip1588 channel 2 63 = Timestamp FIFO !empty from ip1588 channel 3 64 = Aggregated interrupt 0 65 = Aggregated interrupt 1 66 = Aggregated interrupt 2 67 = Aggregated interrupt 3 68 = Interrupt from pll 0 69 = Interrupt from pll 1 70 = I2C Slave SDA 71 = Cross connect interrupt 72 = LED Blinker 73-127 = Drive low (or high by also setting output INV bit)	0x00

2.28.1.25 GPIO Output Configuration 12

Short Name:GPIO_OUT_CFG_12

Address:0x1EF218

Table 1744 **• GPIO Output Configuration 12**

Bit	Name	Access	Description	Default
6:0	GPIO_12_SEL	R/W	Selects the source for GPIO_12 output 0 = GPIO output 0 from channel 0 1 = GPIO output 1 from channel 0 2 = GPIO output 2 from channel 0 3 = GPIO output 3 from channel 0 4 = GPIO output 4 from channel 0 5 = GPIO output 5 from channel 0 6 = GPIO output 6 from channel 0 7 = GPIO output 7 from channel 0 8 = GPIO output 0 from channel 1 9 = GPIO output 1 from channel 1 10 = GPIO output 2 from channel 1 11 = GPIO output 3 from channel 1 12 = GPIO output 4 from channel 1 13 = GPIO output 5 from channel 1 14 = GPIO output 6 from channel 1 15 = GPIO output 7 from channel 1 16 = GPIO output 0 from channel 2 17 = GPIO output 1 from channel 2 18 = GPIO output 2 from channel 2 19 = GPIO output 3 from channel 2 20 = GPIO output 4 from channel 2 21 = GPIO output 5 from channel 2 22 = GPIO output 6 from channel 2 23 = GPIO output 7 from channel 2 24 = GPIO output 0 from channel 3 25 = GPIO output 1 from channel 3 26 = GPIO output 2 from channel 3 27 = GPIO output 3 from channel 3 28 = GPIO output 4 from channel 3 29 = GPIO output 5 from channel 3 30 = GPIO output 6 from channel 3 31 = GPIO output 7 from channel 3 32 = Tx Enable for channel 0 33 = Tx Enable for channel 1 34 = Tx Enable for channel 2 35 = Tx Enable for channel 3	0x00

Table 1744 • **GPIO Output Configuration 12** ***(continued)***

Bit	Name	Access	Description	Default
6:0	GPIO_12_SEL	R/W	*(continued)* Selects the source for GPIO_12 output 36 = PPS_0 from ip1588 37 = PPS_1 from ip1588 38 = PPS_2 from ip1588 39 = PPS_3 from ip1588 40 = PLL5G Lock status from Line PLL 41 = PLL5G Lock status from Host PLL 42 = RCOMP Busy 43 = N/A 44 = N/A 45 = N/A 46 = N/A 47 = N/A 48 = Channel interrupt 0 from channel 0 49 = Channel interrupt 1 from channel 0 50 = Channel interrupt 0 from channel 1 51 = Channel interrupt 1 from channel 1 52 = Channel interrupt 0 from channel 2 53 = Channel interrupt 1 from channel 2 54 = Channel interrupt 0 from channel 3 55 = Channel interrupt 1 from channel 3 56 = Interrupt from ip1588 channel 0 57 = Interrupt from ip1588 channel 1 58 = Interrupt from ip1588 channel 2 59 = Interrupt from ip1588 channel 3 60 = Timestamp FIFO !empty from ip1588 channel 0 61 = Timestamp FIFO !empty from ip1588 channel 1 62 = Timestamp FIFO !empty from ip1588 channel 2 63 = Timestamp FIFO !empty from ip1588 channel 3 64 = Aggregated interrupt 0 65 = Aggregated interrupt 1 66 = Aggregated interrupt 2 67 = Aggregated interrupt 3 68 = Interrupt from pll 0 69 = Interrupt from pll 1 70 = I2C Slave SDA 71 = Cross connect interrupt 72 = LED Blinker 73-127 = Drive low (or high by also setting output INV bit)	0x00

2.28.1.26 GPIO Output Configuration 13

Short Name:GPIO_OUT_CFG_13

Address:0x1EF219

***Table 1745* • GPIO Output Configuration 13**

Bit	Name	Access	Description	Default
6:0	GPIO_13_SEL	R/W	Selects the source for GPIO_13 output 0 = GPIO output 0 from channel 0 1 = GPIO output 1 from channel 0 2 = GPIO output 2 from channel 0 3 = GPIO output 3 from channel 0 4 = GPIO output 4 from channel 0 5 = GPIO output 5 from channel 0 6 = GPIO output 6 from channel 0 7 = GPIO output 7 from channel 0 8 = GPIO output 0 from channel 1 9 = GPIO output 1 from channel 1 10 = GPIO output 2 from channel 1 11 = GPIO output 3 from channel 1 12 = GPIO output 4 from channel 1 13 = GPIO output 5 from channel 1 14 = GPIO output 6 from channel 1 15 = GPIO output 7 from channel 1 16 = GPIO output 0 from channel 2 17 = GPIO output 1 from channel 2 18 = GPIO output 2 from channel 2 19 = GPIO output 3 from channel 2 20 = GPIO output 4 from channel 2 21 = GPIO output 5 from channel 2 22 = GPIO output 6 from channel 2 23 = GPIO output 7 from channel 2 24 = GPIO output 0 from channel 3 25 = GPIO output 1 from channel 3 26 = GPIO output 2 from channel 3 27 = GPIO output 3 from channel 3 28 = GPIO output 4 from channel 3 29 = GPIO output 5 from channel 3 30 = GPIO output 6 from channel 3 31 = GPIO output 7 from channel 3 32 = Tx Enable for channel 0 33 = Tx Enable for channel 1 34 = Tx Enable for channel 2 35 = Tx Enable for channel 3	0x00

Table 1745 • **GPIO Output Configuration 13** ***(continued)***

Bit	Name	Access	Description	Default
6:0	GPIO_13_SEL	R/W	*(continued)* Selects the source for GPIO_13 output 36 = PPS_0 from ip1588 37 = PPS_1 from ip1588 38 = PPS_2 from ip1588 39 = PPS_3 from ip1588 40 = PLL5G Lock status from Line PLL 41 = PLL5G Lock status from Host PLL 42 = RCOMP Busy 43 = N/A 44 = N/A 45 = N/A 46 = N/A 47 = N/A 48 = Channel interrupt 0 from channel 0 49 = Channel interrupt 1 from channel 0 50 = Channel interrupt 0 from channel 1 51 = Channel interrupt 1 from channel 1 52 = Channel interrupt 0 from channel 2 53 = Channel interrupt 1 from channel 2 54 = Channel interrupt 0 from channel 3 55 = Channel interrupt 1 from channel 3 56 = Interrupt from ip1588 channel 0 57 = Interrupt from ip1588 channel 1 58 = Interrupt from ip1588 channel 2 59 = Interrupt from ip1588 channel 3 60 = Timestamp FIFO !empty from ip1588 channel 0 61 = Timestamp FIFO !empty from ip1588 channel 1 62 = Timestamp FIFO !empty from ip1588 channel 2 63 = Timestamp FIFO !empty from ip1588 channel 3 64 = Aggregated interrupt 0 65 = Aggregated interrupt 1 66 = Aggregated interrupt 2 67 = Aggregated interrupt 3 68 = Interrupt from pll 0 69 = Interrupt from pll 1 70 = I2C Slave SDA 71 = Cross connect interrupt 72 = LED Blinker 73-127 = Drive low (or high by also setting output INV bit)	0x00

2.28.1.27 GPIO Output Configuration 14

Short Name:GPIO_OUT_CFG_14

Address:0x1EF21A

Table 1746 **• GPIO Output Configuration 14**

Bit	Name	Access	Description	Default
6:0	GPIO_14_SEL	R/W	Selects the source for GPIO_14 output 0 = GPIO output 0 from channel 0 1 = GPIO output 1 from channel 0 2 = GPIO output 2 from channel 0 3 = GPIO output 3 from channel 0 4 = GPIO output 4 from channel 0 5 = GPIO output 5 from channel 0 6 = GPIO output 6 from channel 0 7 = GPIO output 7 from channel 0 8 = GPIO output 0 from channel 1 9 = GPIO output 1 from channel 1 10 = GPIO output 2 from channel 1 11 = GPIO output 3 from channel 1 12 = GPIO output 4 from channel 1 13 = GPIO output 5 from channel 1 14 = GPIO output 6 from channel 1 15 = GPIO output 7 from channel 1 16 = GPIO output 0 from channel 2 17 = GPIO output 1 from channel 2 18 = GPIO output 2 from channel 2 19 = GPIO output 3 from channel 2 20 = GPIO output 4 from channel 2 21 = GPIO output 5 from channel 2 22 = GPIO output 6 from channel 2 23 = GPIO output 7 from channel 2 24 = GPIO output 0 from channel 3 25 = GPIO output 1 from channel 3 26 = GPIO output 2 from channel 3 27 = GPIO output 3 from channel 3 28 = GPIO output 4 from channel 3 29 = GPIO output 5 from channel 3 30 = GPIO output 6 from channel 3 31 = GPIO output 7 from channel 3 32 = Tx Enable for channel 0 33 = Tx Enable for channel 1 34 = Tx Enable for channel 2 35 = Tx Enable for channel 3	0x00

Table 1746 • **GPIO Output Configuration 14** ***(continued)***

Bit	Name	Access	Description	Default
6:0	GPIO_14_SEL	R/W	*(continued)* Selects the source for GPIO_14 output 36 = PPS_0 from ip1588 37 = PPS_1 from ip1588 38 = PPS_2 from ip1588 39 = PPS_3 from ip1588 40 = PLL5G Lock status from Line PLL 41 = PLL5G Lock status from Host PLL 42 = RCOMP Busy 43 = N/A 44 = N/A 45 = N/A 46 = N/A 47 = N/A 48 = Channel interrupt 0 from channel 0 49 = Channel interrupt 1 from channel 0 50 = Channel interrupt 0 from channel 1 51 = Channel interrupt 1 from channel 1 52 = Channel interrupt 0 from channel 2 53 = Channel interrupt 1 from channel 2 54 = Channel interrupt 0 from channel 3 55 = Channel interrupt 1 from channel 3 56 = Interrupt from ip1588 channel 0 57 = Interrupt from ip1588 channel 1 58 = Interrupt from ip1588 channel 2 59 = Interrupt from ip1588 channel 3 60 = Timestamp FIFO !empty from ip1588 channel 0 61 = Timestamp FIFO !empty from ip1588 channel 1 62 = Timestamp FIFO !empty from ip1588 channel 2 63 = Timestamp FIFO !empty from ip1588 channel 3 64 = Aggregated interrupt 0 65 = Aggregated interrupt 1 66 = Aggregated interrupt 2 67 = Aggregated interrupt 3 68 = Interrupt from pll 0 69 = Interrupt from pll 1 70 = I2C Slave SDA 71 = Cross connect interrupt 72 = LED Blinker 73-127 = Drive low (or high by also setting output INV bit)	0x00

2.28.1.28 GPIO Output Configuration 15

Short Name:GPIO_OUT_CFG_15

Address:0x1EF21B

Table 1747 **• GPIO Output Configuration 15**

Bit	Name	Access	Description	Default
6:0	GPIO_15_SEL	R/W	Selects the source for GPIO_15 output 0 = GPIO output 0 from channel 0 1 = GPIO output 1 from channel 0 2 = GPIO output 2 from channel 0 3 = GPIO output 3 from channel 0 4 = GPIO output 4 from channel 0 5 = GPIO output 5 from channel 0 6 = GPIO output 6 from channel 0 7 = GPIO output 7 from channel 0 8 = GPIO output 0 from channel 1 9 = GPIO output 1 from channel 1 10 = GPIO output 2 from channel 1 11 = GPIO output 3 from channel 1 12 = GPIO output 4 from channel 1 13 = GPIO output 5 from channel 1 14 = GPIO output 6 from channel 1 15 = GPIO output 7 from channel 1 16 = GPIO output 0 from channel 2 17 = GPIO output 1 from channel 2 18 = GPIO output 2 from channel 2 19 = GPIO output 3 from channel 2 20 = GPIO output 4 from channel 2 21 = GPIO output 5 from channel 2 22 = GPIO output 6 from channel 2 23 = GPIO output 7 from channel 2 24 = GPIO output 0 from channel 3 25 = GPIO output 1 from channel 3 26 = GPIO output 2 from channel 3 27 = GPIO output 3 from channel 3 28 = GPIO output 4 from channel 3 29 = GPIO output 5 from channel 3 30 = GPIO output 6 from channel 3 31 = GPIO output 7 from channel 3 32 = Tx Enable for channel 0 33 = Tx Enable for channel 1 34 = Tx Enable for channel 2 35 = Tx Enable for channel 3	0x00

Table 1747 • **GPIO Output Configuration 15** ***(continued)***

Bit	Name	Access	Description	Default
6:0	GPIO_15_SEL	R/W	*(continued)* Selects the source for GPIO_15 output 36 = PPS_0 from ip1588 37 = PPS_1 from ip1588 38 = PPS_2 from ip1588 39 = PPS_3 from ip1588 40 = PLL5G Lock status from Line PLL 41 = PLL5G Lock status from Host PLL 42 = RCOMP Busy 43 = N/A 44 = N/A 45 = N/A 46 = N/A 47 = N/A 48 = Channel interrupt 0 from channel 0 49 = Channel interrupt 1 from channel 0 50 = Channel interrupt 0 from channel 1 51 = Channel interrupt 1 from channel 1 52 = Channel interrupt 0 from channel 2 53 = Channel interrupt 1 from channel 2 54 = Channel interrupt 0 from channel 3 55 = Channel interrupt 1 from channel 3 56 = Interrupt from ip1588 channel 0 57 = Interrupt from ip1588 channel 1 58 = Interrupt from ip1588 channel 2 59 = Interrupt from ip1588 channel 3 60 = Timestamp FIFO !empty from ip1588 channel 0 61 = Timestamp FIFO !empty from ip1588 channel 1 62 = Timestamp FIFO !empty from ip1588 channel 2 63 = Timestamp FIFO !empty from ip1588 channel 3 64 = Aggregated interrupt 0 65 = Aggregated interrupt 1 66 = Aggregated interrupt 2 67 = Aggregated interrupt 3 68 = Interrupt from pll 0 69 = Interrupt from pll 1 70 = I2C Slave SDA 71 = Cross connect interrupt 72 = LED Blinker 73-127 = Drive low (or high by also setting output INV bit)	0x00

2.28.1.29 GPIO Output Configuration 16

Short Name:GPIO_OUT_CFG_16

Address:0x1EF21C

Table 1748 **• GPIO Output Configuration 16**

Bit	Name	Access	Description	Default
6:0	GPIO_16_SEL	R/W	Selects the source for GPIO_16 output 0 = GPIO output 0 from channel 0 1 = GPIO output 1 from channel 0 2 = GPIO output 2 from channel 0 3 = GPIO output 3 from channel 0 4 = GPIO output 4 from channel 0 5 = GPIO output 5 from channel 0 6 = GPIO output 6 from channel 0 7 = GPIO output 7 from channel 0 8 = GPIO output 0 from channel 1 9 = GPIO output 1 from channel 1 10 = GPIO output 2 from channel 1 11 = GPIO output 3 from channel 1 12 = GPIO output 4 from channel 1 13 = GPIO output 5 from channel 1 14 = GPIO output 6 from channel 1 15 = GPIO output 7 from channel 1 16 = GPIO output 0 from channel 2 17 = GPIO output 1 from channel 2 18 = GPIO output 2 from channel 2 19 = GPIO output 3 from channel 2 20 = GPIO output 4 from channel 2 21 = GPIO output 5 from channel 2 22 = GPIO output 6 from channel 2 23 = GPIO output 7 from channel 2 24 = GPIO output 0 from channel 3 25 = GPIO output 1 from channel 3 26 = GPIO output 2 from channel 3 27 = GPIO output 3 from channel 3 28 = GPIO output 4 from channel 3 29 = GPIO output 5 from channel 3 30 = GPIO output 6 from channel 3 31 = GPIO output 7 from channel 3 32 = Tx Enable for channel 0 33 = Tx Enable for channel 1 34 = Tx Enable for channel 2 35 = Tx Enable for channel 3	0x00

Table 1748 • **GPIO Output Configuration 16** ***(continued)***

Bit	Name	Access	Description	Default
6:0	GPIO_16_SEL	R/W	*(continued)* Selects the source for GPIO_16 output 36 = PPS_0 from ip1588 37 = PPS_1 from ip1588 38 = PPS_2 from ip1588 39 = PPS_3 from ip1588 40 = PLL5G Lock status from Line PLL 41 = PLL5G Lock status from Host PLL 42 = RCOMP Busy 43 = N/A 44 = N/A 45 = N/A 46 = N/A 47 = N/A 48 = Channel interrupt 0 from channel 0 49 = Channel interrupt 1 from channel 0 50 = Channel interrupt 0 from channel 1 51 = Channel interrupt 1 from channel 1 52 = Channel interrupt 0 from channel 2 53 = Channel interrupt 1 from channel 2 54 = Channel interrupt 0 from channel 3 55 = Channel interrupt 1 from channel 3 56 = Interrupt from ip1588 channel 0 57 = Interrupt from ip1588 channel 1 58 = Interrupt from ip1588 channel 2 59 = Interrupt from ip1588 channel 3 60 = Timestamp FIFO !empty from ip1588 channel 0 61 = Timestamp FIFO !empty from ip1588 channel 1 62 = Timestamp FIFO !empty from ip1588 channel 2 63 = Timestamp FIFO !empty from ip1588 channel 3 64 = Aggregated interrupt 0 65 = Aggregated interrupt 1 66 = Aggregated interrupt 2 67 = Aggregated interrupt 3 68 = Interrupt from pll 0 69 = Interrupt from pll 1 70 = I2C Slave SDA 71 = Cross connect interrupt 72 = LED Blinker 73-127 = Drive low (or high by also setting output INV bit)	0x00

2.28.1.30 GPIO Output Configuration 17

Short Name:GPIO_OUT_CFG_17

Address:0x1EF21D

Table 1749 **• GPIO Output Configuration 17**

Bit	Name	Access	Description	Default
6:0	GPIO_17_SEL	R/W	Selects the source for GPIO_17 output 0 = GPIO output 0 from channel 0 1 = GPIO output 1 from channel 0 2 = GPIO output 2 from channel 0 3 = GPIO output 3 from channel 0 4 = GPIO output 4 from channel 0 5 = GPIO output 5 from channel 0 6 = GPIO output 6 from channel 0 7 = GPIO output 7 from channel 0 8 = GPIO output 0 from channel 1 9 = GPIO output 1 from channel 1 10 = GPIO output 2 from channel 1 11 = GPIO output 3 from channel 1 12 = GPIO output 4 from channel 1 13 = GPIO output 5 from channel 1 14 = GPIO output 6 from channel 1 15 = GPIO output 7 from channel 1 16 = GPIO output 0 from channel 2 17 = GPIO output 1 from channel 2 18 = GPIO output 2 from channel 2 19 = GPIO output 3 from channel 2 20 = GPIO output 4 from channel 2 21 = GPIO output 5 from channel 2 22 = GPIO output 6 from channel 2 23 = GPIO output 7 from channel 2 24 = GPIO output 0 from channel 3 25 = GPIO output 1 from channel 3 26 = GPIO output 2 from channel 3 27 = GPIO output 3 from channel 3 28 = GPIO output 4 from channel 3 29 = GPIO output 5 from channel 3 30 = GPIO output 6 from channel 3 31 = GPIO output 7 from channel 3 32 = Tx Enable for channel 0 33 = Tx Enable for channel 1 34 = Tx Enable for channel 2 35 = Tx Enable for channel 3	0x00

Table 1749 • **GPIO Output Configuration 17** ***(continued)***

Bit	Name	Access	Description	Default
6:0	GPIO_17_SEL	R/W	*(continued)* Selects the source for GPIO_17 output 36 = PPS_0 from ip1588 37 = PPS_1 from ip1588 38 = PPS_2 from ip1588 39 = PPS_3 from ip1588 40 = PLL5G Lock status from Line PLL 41 = PLL5G Lock status from Host PLL 42 = RCOMP Busy 43 = N/A 44 = N/A 45 = N/A 46 = N/A 47 = N/A 48 = Channel interrupt 0 from channel 0 49 = Channel interrupt 1 from channel 0 50 = Channel interrupt 0 from channel 1 51 = Channel interrupt 1 from channel 1 52 = Channel interrupt 0 from channel 2 53 = Channel interrupt 1 from channel 2 54 = Channel interrupt 0 from channel 3 55 = Channel interrupt 1 from channel 3 56 = Interrupt from ip1588 channel 0 57 = Interrupt from ip1588 channel 1 58 = Interrupt from ip1588 channel 2 59 = Interrupt from ip1588 channel 3 60 = Timestamp FIFO !empty from ip1588 channel 0 61 = Timestamp FIFO !empty from ip1588 channel 1 62 = Timestamp FIFO !empty from ip1588 channel 2 63 = Timestamp FIFO !empty from ip1588 channel 3 64 = Aggregated interrupt 0 65 = Aggregated interrupt 1 66 = Aggregated interrupt 2 67 = Aggregated interrupt 3 68 = Interrupt from pll 0 69 = Interrupt from pll 1 70 = I2C Slave SDA 71 = Cross connect interrupt 72 = LED Blinker 73-127 = Drive low (or high by also setting output INV bit)	0x00

2.28.1.31 GPIO Output Configuration 18

Short Name:GPIO_OUT_CFG_18

Address:0x1EF21E

Table 1750 **• GPIO Output Configuration 18**

Bit	Name	Access	Description	Default
6:0	GPIO_18_SEL	R/W	Selects the source for GPIO_18 output 0 = GPIO output 0 from channel 0 1 = GPIO output 1 from channel 0 2 = GPIO output 2 from channel 0 3 = GPIO output 3 from channel 0 4 = GPIO output 4 from channel 0 5 = GPIO output 5 from channel 0 6 = GPIO output 6 from channel 0 7 = GPIO output 7 from channel 0 8 = GPIO output 0 from channel 1 9 = GPIO output 1 from channel 1 10 = GPIO output 2 from channel 1 11 = GPIO output 3 from channel 1 12 = GPIO output 4 from channel 1 13 = GPIO output 5 from channel 1 14 = GPIO output 6 from channel 1 15 = GPIO output 7 from channel 1 16 = GPIO output 0 from channel 2 17 = GPIO output 1 from channel 2 18 = GPIO output 2 from channel 2 19 = GPIO output 3 from channel 2 20 = GPIO output 4 from channel 2 21 = GPIO output 5 from channel 2 22 = GPIO output 6 from channel 2 23 = GPIO output 7 from channel 2 24 = GPIO output 0 from channel 3 25 = GPIO output 1 from channel 3 26 = GPIO output 2 from channel 3 27 = GPIO output 3 from channel 3 28 = GPIO output 4 from channel 3 29 = GPIO output 5 from channel 3 30 = GPIO output 6 from channel 3 31 = GPIO output 7 from channel 3 32 = Tx Enable for channel 0 33 = Tx Enable for channel 1 34 = Tx Enable for channel 2 35 = Tx Enable for channel 3	0x00

Table 1750 • **GPIO Output Configuration 18** ***(continued)***

Bit	Name	Access	Description	Default
6:0	GPIO_18_SEL	R/W	*(continued)* Selects the source for GPIO_18 output 36 = PPS_0 from ip1588 37 = PPS_1 from ip1588 38 = PPS_2 from ip1588 39 = PPS_3 from ip1588 40 = PLL5G Lock status from Line PLL 41 = PLL5G Lock status from Host PLL 42 = RCOMP Busy 43 = N/A 44 = N/A 45 = N/A 46 = N/A 47 = N/A 48 = Channel interrupt 0 from channel 0 49 = Channel interrupt 1 from channel 0 50 = Channel interrupt 0 from channel 1 51 = Channel interrupt 1 from channel 1 52 = Channel interrupt 0 from channel 2 53 = Channel interrupt 1 from channel 2 54 = Channel interrupt 0 from channel 3 55 = Channel interrupt 1 from channel 3 56 = Interrupt from ip1588 channel 0 57 = Interrupt from ip1588 channel 1 58 = Interrupt from ip1588 channel 2 59 = Interrupt from ip1588 channel 3 60 = Timestamp FIFO !empty from ip1588 channel 0 61 = Timestamp FIFO !empty from ip1588 channel 1 62 = Timestamp FIFO !empty from ip1588 channel 2 63 = Timestamp FIFO !empty from ip1588 channel 3 64 = Aggregated interrupt 0 65 = Aggregated interrupt 1 66 = Aggregated interrupt 2 67 = Aggregated interrupt 3 68 = Interrupt from pll 0 69 = Interrupt from pll 1 70 = I2C Slave SDA 71 = Cross connect interrupt 72 = LED Blinker 73-127 = Drive low (or high by also setting output INV bit)	0x00

2.28.1.32 GPIO Output Configuration 19

Short Name:GPIO_OUT_CFG_19

Address:0x1EF21F

Table 1751 **• GPIO Output Configuration 19**

Bit	Name	Access	Description	Default
6:0	GPIO_19_SEL	R/W	Selects the source for GPIO_19 output 0 = GPIO output 0 from channel 0 1 = GPIO output 1 from channel 0 2 = GPIO output 2 from channel 0 3 = GPIO output 3 from channel 0 4 = GPIO output 4 from channel 0 5 = GPIO output 5 from channel 0 6 = GPIO output 6 from channel 0 7 = GPIO output 7 from channel 0 8 = GPIO output 0 from channel 1 9 = GPIO output 1 from channel 1 10 = GPIO output 2 from channel 1 11 = GPIO output 3 from channel 1 12 = GPIO output 4 from channel 1 13 = GPIO output 5 from channel 1 14 = GPIO output 6 from channel 1 15 = GPIO output 7 from channel 1 16 = GPIO output 0 from channel 2 17 = GPIO output 1 from channel 2 18 = GPIO output 2 from channel 2 19 = GPIO output 3 from channel 2 20 = GPIO output 4 from channel 2 21 = GPIO output 5 from channel 2 22 = GPIO output 6 from channel 2 23 = GPIO output 7 from channel 2 24 = GPIO output 0 from channel 3 25 = GPIO output 1 from channel 3 26 = GPIO output 2 from channel 3 27 = GPIO output 3 from channel 3 28 = GPIO output 4 from channel 3 29 = GPIO output 5 from channel 3 30 = GPIO output 6 from channel 3 31 = GPIO output 7 from channel 3 32 = Tx Enable for channel 0 33 = Tx Enable for channel 1 34 = Tx Enable for channel 2 35 = Tx Enable for channel 3	0x00

Table 1751 • **GPIO Output Configuration 19** ***(continued)***

Bit	Name	Access	Description	Default
6:0	GPIO_19_SEL	R/W	*(continued)* Selects the source for GPIO_19 output 36 = PPS_0 from ip1588 37 = PPS_1 from ip1588 38 = PPS_2 from ip1588 39 = PPS_3 from ip1588 40 = PLL5G Lock status from Line PLL 41 = PLL5G Lock status from Host PLL 42 = RCOMP Busy 43 = N/A 44 = N/A 45 = N/A 46 = N/A 47 = N/A 48 = Channel interrupt 0 from channel 0 49 = Channel interrupt 1 from channel 0 50 = Channel interrupt 0 from channel 1 51 = Channel interrupt 1 from channel 1 52 = Channel interrupt 0 from channel 2 53 = Channel interrupt 1 from channel 2 54 = Channel interrupt 0 from channel 3 55 = Channel interrupt 1 from channel 3 56 = Interrupt from ip1588 channel 0 57 = Interrupt from ip1588 channel 1 58 = Interrupt from ip1588 channel 2 59 = Interrupt from ip1588 channel 3 60 = Timestamp FIFO !empty from ip1588 channel 0 61 = Timestamp FIFO !empty from ip1588 channel 1 62 = Timestamp FIFO !empty from ip1588 channel 2 63 = Timestamp FIFO !empty from ip1588 channel 3 64 = Aggregated interrupt 0 65 = Aggregated interrupt 1 66 = Aggregated interrupt 2 67 = Aggregated interrupt 3 68 = Interrupt from pll 0 69 = Interrupt from pll 1 70 = I2C Slave SDA 71 = Cross connect interrupt 72 = LED Blinker 73-127 = Drive low (or high by also setting output INV bit)	0x00

2.28.1.33 GPIO Output Configuration 20

Short Name:GPIO_OUT_CFG_20

Address:0x1EF220

Table 1752 **• GPIO Output Configuration 20**

Bit	Name	Access	Description	Default
6:0	GPIO_20_SEL	R/W	Selects the source for GPIO_20 output 0 = GPIO output 0 from channel 0 1 = GPIO output 1 from channel 0 2 = GPIO output 2 from channel 0 3 = GPIO output 3 from channel 0 4 = GPIO output 4 from channel 0 5 = GPIO output 5 from channel 0 6 = GPIO output 6 from channel 0 7 = GPIO output 7 from channel 0 8 = GPIO output 0 from channel 1 9 = GPIO output 1 from channel 1 10 = GPIO output 2 from channel 1 11 = GPIO output 3 from channel 1 12 = GPIO output 4 from channel 1 13 = GPIO output 5 from channel 1 14 = GPIO output 6 from channel 1 15 = GPIO output 7 from channel 1 16 = GPIO output 0 from channel 2 17 = GPIO output 1 from channel 2 18 = GPIO output 2 from channel 2 19 = GPIO output 3 from channel 2 20 = GPIO output 4 from channel 2 21 = GPIO output 5 from channel 2 22 = GPIO output 6 from channel 2 23 = GPIO output 7 from channel 2 24 = GPIO output 0 from channel 3 25 = GPIO output 1 from channel 3 26 = GPIO output 2 from channel 3 27 = GPIO output 3 from channel 3 28 = GPIO output 4 from channel 3 29 = GPIO output 5 from channel 3 30 = GPIO output 6 from channel 3 31 = GPIO output 7 from channel 3 32 = Tx Enable for channel 0 33 = Tx Enable for channel 1 34 = Tx Enable for channel 2 35 = Tx Enable for channel 3	0x00

Table 1752 • **GPIO Output Configuration 20** ***(continued)***

Bit	Name	Access	Description	Default
6:0	GPIO_20_SEL	R/W	*(continued)* Selects the source for GPIO_20 output 36 = PPS_0 from ip1588 37 = PPS_1 from ip1588 38 = PPS_2 from ip1588 39 = PPS_3 from ip1588 40 = PLL5G Lock status from Line PLL 41 = PLL5G Lock status from Host PLL 42 = RCOMP Busy 43 = N/A 44 = N/A 45 = N/A 46 = N/A 47 = N/A 48 = Channel interrupt 0 from channel 0 49 = Channel interrupt 1 from channel 0 50 = Channel interrupt 0 from channel 1 51 = Channel interrupt 1 from channel 1 52 = Channel interrupt 0 from channel 2 53 = Channel interrupt 1 from channel 2 54 = Channel interrupt 0 from channel 3 55 = Channel interrupt 1 from channel 3 56 = Interrupt from ip1588 channel 0 57 = Interrupt from ip1588 channel 1 58 = Interrupt from ip1588 channel 2 59 = Interrupt from ip1588 channel 3 60 = Timestamp FIFO !empty from ip1588 channel 0 61 = Timestamp FIFO !empty from ip1588 channel 1 62 = Timestamp FIFO !empty from ip1588 channel 2 63 = Timestamp FIFO !empty from ip1588 channel 3 64 = Aggregated interrupt 0 65 = Aggregated interrupt 1 66 = Aggregated interrupt 2 67 = Aggregated interrupt 3 68 = Interrupt from pll 0 69 = Interrupt from pll 1 70 = I2C Slave SDA 71 = Cross connect interrupt 72 = LED Blinker 73-127 = Drive low (or high by also setting output INV bit)	0x00

2.28.1.34 GPIO Output Configuration 21

Short Name:GPIO_OUT_CFG_21

Address:0x1EF221

Table 1753 **• GPIO Output Configuration 21**

Bit	Name	Access	Description	Default
6:0	GPIO_21_SEL	R/W	Selects the source for GPIO_21 output 0 = GPIO output 0 from channel 0 1 = GPIO output 1 from channel 0 2 = GPIO output 2 from channel 0 3 = GPIO output 3 from channel 0 4 = GPIO output 4 from channel 0 5 = GPIO output 5 from channel 0 6 = GPIO output 6 from channel 0 7 = GPIO output 7 from channel 0 8 = GPIO output 0 from channel 1 9 = GPIO output 1 from channel 1 10 = GPIO output 2 from channel 1 11 = GPIO output 3 from channel 1 12 = GPIO output 4 from channel 1 13 = GPIO output 5 from channel 1 14 = GPIO output 6 from channel 1 15 = GPIO output 7 from channel 1 16 = GPIO output 0 from channel 2 17 = GPIO output 1 from channel 2 18 = GPIO output 2 from channel 2 19 = GPIO output 3 from channel 2 20 = GPIO output 4 from channel 2 21 = GPIO output 5 from channel 2 22 = GPIO output 6 from channel 2 23 = GPIO output 7 from channel 2 24 = GPIO output 0 from channel 3 25 = GPIO output 1 from channel 3 26 = GPIO output 2 from channel 3 27 = GPIO output 3 from channel 3 28 = GPIO output 4 from channel 3 29 = GPIO output 5 from channel 3 30 = GPIO output 6 from channel 3 31 = GPIO output 7 from channel 3 32 = Tx Enable for channel 0 33 = Tx Enable for channel 1 34 = Tx Enable for channel 2 35 = Tx Enable for channel 3	0x00

Table 1753 • **GPIO Output Configuration 21** ***(continued)***

Bit	Name	Access	Description	Default
6:0	GPIO_21_SEL	R/W	*(continued)* Selects the source for GPIO_21 output 36 = PPS_0 from ip1588 37 = PPS_1 from ip1588 38 = PPS_2 from ip1588 39 = PPS_3 from ip1588 40 = PLL5G Lock status from Line PLL 41 = PLL5G Lock status from Host PLL 42 = RCOMP Busy 43 = N/A 44 = N/A 45 = N/A 46 = N/A 47 = N/A 48 = Channel interrupt 0 from channel 0 49 = Channel interrupt 1 from channel 0 50 = Channel interrupt 0 from channel 1 51 = Channel interrupt 1 from channel 1 52 = Channel interrupt 0 from channel 2 53 = Channel interrupt 1 from channel 2 54 = Channel interrupt 0 from channel 3 55 = Channel interrupt 1 from channel 3 56 = Interrupt from ip1588 channel 0 57 = Interrupt from ip1588 channel 1 58 = Interrupt from ip1588 channel 2 59 = Interrupt from ip1588 channel 3 60 = Timestamp FIFO !empty from ip1588 channel 0 61 = Timestamp FIFO !empty from ip1588 channel 1 62 = Timestamp FIFO !empty from ip1588 channel 2 63 = Timestamp FIFO !empty from ip1588 channel 3 64 = Aggregated interrupt 0 65 = Aggregated interrupt 1 66 = Aggregated interrupt 2 67 = Aggregated interrupt 3 68 = Interrupt from pll 0 69 = Interrupt from pll 1 70 = I2C Slave SDA 71 = Cross connect interrupt 72 = LED Blinker 73-127 = Drive low (or high by also setting output INV bit)	0x00

2.28.1.35 GPIO Output Configuration 22

Short Name:GPIO_OUT_CFG_22

Address:0x1EF222

Table 1754 **• GPIO Output Configuration 22**

Bit	Name	Access	Description	Default
6:0	GPIO_22_SEL	R/W	Selects the source for GPIO_22 output 0 = GPIO output 0 from channel 0 1 = GPIO output 1 from channel 0 2 = GPIO output 2 from channel 0 3 = GPIO output 3 from channel 0 4 = GPIO output 4 from channel 0 5 = GPIO output 5 from channel 0 6 = GPIO output 6 from channel 0 7 = GPIO output 7 from channel 0 8 = GPIO output 0 from channel 1 9 = GPIO output 1 from channel 1 10 = GPIO output 2 from channel 1 11 = GPIO output 3 from channel 1 12 = GPIO output 4 from channel 1 13 = GPIO output 5 from channel 1 14 = GPIO output 6 from channel 1 15 = GPIO output 7 from channel 1 16 = GPIO output 0 from channel 2 17 = GPIO output 1 from channel 2 18 = GPIO output 2 from channel 2 19 = GPIO output 3 from channel 2 20 = GPIO output 4 from channel 2 21 = GPIO output 5 from channel 2 22 = GPIO output 6 from channel 2 23 = GPIO output 7 from channel 2 24 = GPIO output 0 from channel 3 25 = GPIO output 1 from channel 3 26 = GPIO output 2 from channel 3 27 = GPIO output 3 from channel 3 28 = GPIO output 4 from channel 3 29 = GPIO output 5 from channel 3 30 = GPIO output 6 from channel 3 31 = GPIO output 7 from channel 3 32 = Tx Enable for channel 0 33 = Tx Enable for channel 1 34 = Tx Enable for channel 2 35 = Tx Enable for channel 3	0x00

Table 1754 • **GPIO Output Configuration 22** ***(continued)***

Bit	Name	Access	Description	Default
6:0	GPIO_22_SEL	R/W	*(continued)* Selects the source for GPIO_22 output 36 = PPS_0 from ip1588 37 = PPS_1 from ip1588 38 = PPS_2 from ip1588 39 = PPS_3 from ip1588 40 = PLL5G Lock status from Line PLL 41 = PLL5G Lock status from Host PLL 42 = RCOMP Busy 43 = N/A 44 = N/A 45 = N/A 46 = N/A 47 = N/A 48 = Channel interrupt 0 from channel 0 49 = Channel interrupt 1 from channel 0 50 = Channel interrupt 0 from channel 1 51 = Channel interrupt 1 from channel 1 52 = Channel interrupt 0 from channel 2 53 = Channel interrupt 1 from channel 2 54 = Channel interrupt 0 from channel 3 55 = Channel interrupt 1 from channel 3 56 = Interrupt from ip1588 channel 0 57 = Interrupt from ip1588 channel 1 58 = Interrupt from ip1588 channel 2 59 = Interrupt from ip1588 channel 3 60 = Timestamp FIFO !empty from ip1588 channel 0 61 = Timestamp FIFO !empty from ip1588 channel 1 62 = Timestamp FIFO !empty from ip1588 channel 2 63 = Timestamp FIFO !empty from ip1588 channel 3 64 = Aggregated interrupt 0 65 = Aggregated interrupt 1 66 = Aggregated interrupt 2 67 = Aggregated interrupt 3 68 = Interrupt from pll 0 69 = Interrupt from pll 1 70 = I2C Slave SDA 71 = Cross connect interrupt 72 = LED Blinker 73-127 = Drive low (or high by also setting output INV bit)	0x00

2.28.1.36 GPIO Output Configuration 23

Short Name:GPIO_OUT_CFG_23

Address:0x1EF223

Table 1755 **• GPIO Output Configuration 23**

Bit	Name	Access	Description	Default
6:0	GPIO_23_SEL	R/W	Selects the source for GPIO_23 output 0 = GPIO output 0 from channel 0 1 = GPIO output 1 from channel 0 2 = GPIO output 2 from channel 0 3 = GPIO output 3 from channel 0 4 = GPIO output 4 from channel 0 5 = GPIO output 5 from channel 0 6 = GPIO output 6 from channel 0 7 = GPIO output 7 from channel 0 8 = GPIO output 0 from channel 1 9 = GPIO output 1 from channel 1 10 = GPIO output 2 from channel 1 11 = GPIO output 3 from channel 1 12 = GPIO output 4 from channel 1 13 = GPIO output 5 from channel 1 14 = GPIO output 6 from channel 1 15 = GPIO output 7 from channel 1 16 = GPIO output 0 from channel 2 17 = GPIO output 1 from channel 2 18 = GPIO output 2 from channel 2 19 = GPIO output 3 from channel 2 20 = GPIO output 4 from channel 2 21 = GPIO output 5 from channel 2 22 = GPIO output 6 from channel 2 23 = GPIO output 7 from channel 2 24 = GPIO output 0 from channel 3 25 = GPIO output 1 from channel 3 26 = GPIO output 2 from channel 3 27 = GPIO output 3 from channel 3 28 = GPIO output 4 from channel 3 29 = GPIO output 5 from channel 3 30 = GPIO output 6 from channel 3 31 = GPIO output 7 from channel 3 32 = Tx Enable for channel 0 33 = Tx Enable for channel 1 34 = Tx Enable for channel 2 35 = Tx Enable for channel 3	0x00

Table 1755 • **GPIO Output Configuration 23** ***(continued)***

Bit	Name	Access	Description	Default
6:0	GPIO_23_SEL	R/W	*(continued)* Selects the source for GPIO_23 output 36 = PPS_0 from ip1588 37 = PPS_1 from ip1588 38 = PPS_2 from ip1588 39 = PPS_3 from ip1588 40 = PLL5G Lock status from Line PLL 41 = PLL5G Lock status from Host PLL 42 = RCOMP Busy 43 = N/A 44 = N/A 45 = N/A 46 = N/A 47 = N/A 48 = Channel interrupt 0 from channel 0 49 = Channel interrupt 1 from channel 0 50 = Channel interrupt 0 from channel 1 51 = Channel interrupt 1 from channel 1 52 = Channel interrupt 0 from channel 2 53 = Channel interrupt 1 from channel 2 54 = Channel interrupt 0 from channel 3 55 = Channel interrupt 1 from channel 3 56 = Interrupt from ip1588 channel 0 57 = Interrupt from ip1588 channel 1 58 = Interrupt from ip1588 channel 2 59 = Interrupt from ip1588 channel 3 60 = Timestamp FIFO !empty from ip1588 channel 0 61 = Timestamp FIFO !empty from ip1588 channel 1 62 = Timestamp FIFO !empty from ip1588 channel 2 63 = Timestamp FIFO !empty from ip1588 channel 3 64 = Aggregated interrupt 0 65 = Aggregated interrupt 1 66 = Aggregated interrupt 2 67 = Aggregated interrupt 3 68 = Interrupt from pll 0 69 = Interrupt from pll 1 70 = I2C Slave SDA 71 = Cross connect interrupt 72 = LED Blinker 73-127 = Drive low (or high by also setting output INV bit)	0x00

2.28.1.37 GPIO Output Configuration 24

Short Name:GPIO_OUT_CFG_24

Address:0x1EF224

Table 1756 **• GPIO Output Configuration 24**

Bit	Name	Access	Description	Default
6:0	GPIO_24_SEL	R/W	Selects the source for GPIO_24 output 0 = GPIO output 0 from channel 0 1 = GPIO output 1 from channel 0 2 = GPIO output 2 from channel 0 3 = GPIO output 3 from channel 0 4 = GPIO output 4 from channel 0 5 = GPIO output 5 from channel 0 6 = GPIO output 6 from channel 0 7 = GPIO output 7 from channel 0 8 = GPIO output 0 from channel 1 9 = GPIO output 1 from channel 1 10 = GPIO output 2 from channel 1 11 = GPIO output 3 from channel 1 12 = GPIO output 4 from channel 1 13 = GPIO output 5 from channel 1 14 = GPIO output 6 from channel 1 15 = GPIO output 7 from channel 1 16 = GPIO output 0 from channel 2 17 = GPIO output 1 from channel 2 18 = GPIO output 2 from channel 2 19 = GPIO output 3 from channel 2 20 = GPIO output 4 from channel 2 21 = GPIO output 5 from channel 2 22 = GPIO output 6 from channel 2 23 = GPIO output 7 from channel 2 24 = GPIO output 0 from channel 3 25 = GPIO output 1 from channel 3 26 = GPIO output 2 from channel 3 27 = GPIO output 3 from channel 3 28 = GPIO output 4 from channel 3 29 = GPIO output 5 from channel 3 30 = GPIO output 6 from channel 3 31 = GPIO output 7 from channel 3 32 = Tx Enable for channel 0 33 = Tx Enable for channel 1 34 = Tx Enable for channel 2 35 = Tx Enable for channel 3	0x00

Table 1756 • **GPIO Output Configuration 24** ***(continued)***

Bit	Name	Access	Description	Default
6:0	GPIO_24_SEL	R/W	*(continued)* Selects the source for GPIO_24 output 36 = PPS_0 from ip1588 37 = PPS_1 from ip1588 38 = PPS_2 from ip1588 39 = PPS_3 from ip1588 40 = PLL5G Lock status from Line PLL 41 = PLL5G Lock status from Host PLL 42 = RCOMP Busy 43 = N/A 44 = N/A 45 = N/A 46 = N/A 47 = N/A 48 = Channel interrupt 0 from channel 0 49 = Channel interrupt 1 from channel 0 50 = Channel interrupt 0 from channel 1 51 = Channel interrupt 1 from channel 1 52 = Channel interrupt 0 from channel 2 53 = Channel interrupt 1 from channel 2 54 = Channel interrupt 0 from channel 3 55 = Channel interrupt 1 from channel 3 56 = Interrupt from ip1588 channel 0 57 = Interrupt from ip1588 channel 1 58 = Interrupt from ip1588 channel 2 59 = Interrupt from ip1588 channel 3 60 = Timestamp FIFO !empty from ip1588 channel 0 61 = Timestamp FIFO !empty from ip1588 channel 1 62 = Timestamp FIFO !empty from ip1588 channel 2 63 = Timestamp FIFO !empty from ip1588 channel 3 64 = Aggregated interrupt 0 65 = Aggregated interrupt 1 66 = Aggregated interrupt 2 67 = Aggregated interrupt 3 68 = Interrupt from pll 0 69 = Interrupt from pll 1 70 = I2C Slave SDA 71 = Cross connect interrupt 72 = LED Blinker 73-127 = Drive low (or high by also setting output INV bit)	0x00

2.28.1.38 GPIO Output Configuration 25

Short Name:GPIO_OUT_CFG_25

Address:0x1EF225

Table 1757 **• GPIO Output Configuration 25**

Bit	Name	Access	Description	Default
6:0	GPIO_25_SEL	R/W	Selects the source for GPIO_25 output 0 = GPIO output 0 from channel 0 1 = GPIO output 1 from channel 0 2 = GPIO output 2 from channel 0 3 = GPIO output 3 from channel 0 4 = GPIO output 4 from channel 0 5 = GPIO output 5 from channel 0 6 = GPIO output 6 from channel 0 7 = GPIO output 7 from channel 0 8 = GPIO output 0 from channel 1 9 = GPIO output 1 from channel 1 10 = GPIO output 2 from channel 1 11 = GPIO output 3 from channel 1 12 = GPIO output 4 from channel 1 13 = GPIO output 5 from channel 1 14 = GPIO output 6 from channel 1 15 = GPIO output 7 from channel 1 16 = GPIO output 0 from channel 2 17 = GPIO output 1 from channel 2 18 = GPIO output 2 from channel 2 19 = GPIO output 3 from channel 2 20 = GPIO output 4 from channel 2 21 = GPIO output 5 from channel 2 22 = GPIO output 6 from channel 2 23 = GPIO output 7 from channel 2 24 = GPIO output 0 from channel 3 25 = GPIO output 1 from channel 3 26 = GPIO output 2 from channel 3 27 = GPIO output 3 from channel 3 28 = GPIO output 4 from channel 3 29 = GPIO output 5 from channel 3 30 = GPIO output 6 from channel 3 31 = GPIO output 7 from channel 3 32 = Tx Enable for channel 0 33 = Tx Enable for channel 1 34 = Tx Enable for channel 2 35 = Tx Enable for channel 3	0x00

Table 1757 • **GPIO Output Configuration 25** ***(continued)***

Bit	Name	Access	Description	Default
6:0	GPIO_25_SEL	R/W	*(continued)* Selects the source for GPIO_25 output 36 = PPS_0 from ip1588 37 = PPS_1 from ip1588 38 = PPS_2 from ip1588 39 = PPS_3 from ip1588 40 = PLL5G Lock status from Line PLL 41 = PLL5G Lock status from Host PLL 42 = RCOMP Busy 43 = N/A 44 = N/A 45 = N/A 46 = N/A 47 = N/A 48 = Channel interrupt 0 from channel 0 49 = Channel interrupt 1 from channel 0 50 = Channel interrupt 0 from channel 1 51 = Channel interrupt 1 from channel 1 52 = Channel interrupt 0 from channel 2 53 = Channel interrupt 1 from channel 2 54 = Channel interrupt 0 from channel 3 55 = Channel interrupt 1 from channel 3 56 = Interrupt from ip1588 channel 0 57 = Interrupt from ip1588 channel 1 58 = Interrupt from ip1588 channel 2 59 = Interrupt from ip1588 channel 3 60 = Timestamp FIFO !empty from ip1588 channel 0 61 = Timestamp FIFO !empty from ip1588 channel 1 62 = Timestamp FIFO !empty from ip1588 channel 2 63 = Timestamp FIFO !empty from ip1588 channel 3 64 = Aggregated interrupt 0 65 = Aggregated interrupt 1 66 = Aggregated interrupt 2 67 = Aggregated interrupt 3 68 = Interrupt from pll 0 69 = Interrupt from pll 1 70 = I2C Slave SDA 71 = Cross connect interrupt 72 = LED Blinker 73-127 = Drive low (or high by also setting output INV bit)	0x00

2.28.1.39 GPIO Output Configuration 26

Short Name:GPIO_OUT_CFG_26

Address:0x1EF226

Table 1758 **• GPIO Output Configuration 26**

Bit	Name	Access	Description	Default
6:0	GPIO_26_SEL	R/W	Selects the source for GPIO_26 output 0 = GPIO output 0 from channel 0 1 = GPIO output 1 from channel 0 2 = GPIO output 2 from channel 0 3 = GPIO output 3 from channel 0 4 = GPIO output 4 from channel 0 5 = GPIO output 5 from channel 0 6 = GPIO output 6 from channel 0 7 = GPIO output 7 from channel 0 8 = GPIO output 0 from channel 1 9 = GPIO output 1 from channel 1 10 = GPIO output 2 from channel 1 11 = GPIO output 3 from channel 1 12 = GPIO output 4 from channel 1 13 = GPIO output 5 from channel 1 14 = GPIO output 6 from channel 1 15 = GPIO output 7 from channel 1 16 = GPIO output 0 from channel 2 17 = GPIO output 1 from channel 2 18 = GPIO output 2 from channel 2 19 = GPIO output 3 from channel 2 20 = GPIO output 4 from channel 2 21 = GPIO output 5 from channel 2 22 = GPIO output 6 from channel 2 23 = GPIO output 7 from channel 2 24 = GPIO output 0 from channel 3 25 = GPIO output 1 from channel 3 26 = GPIO output 2 from channel 3 27 = GPIO output 3 from channel 3 28 = GPIO output 4 from channel 3 29 = GPIO output 5 from channel 3 30 = GPIO output 6 from channel 3 31 = GPIO output 7 from channel 3 32 = Tx Enable for channel 0 33 = Tx Enable for channel 1 34 = Tx Enable for channel 2 35 = Tx Enable for channel 3	0x00

Table 1758 • **GPIO Output Configuration 26** ***(continued)***

Bit	Name	Access	Description	Default
6:0	GPIO_26_SEL	R/W	*(continued)* Selects the source for GPIO_26 output 36 = PPS_0 from ip1588 37 = PPS_1 from ip1588 38 = PPS_2 from ip1588 39 = PPS_3 from ip1588 40 = PLL5G Lock status from Line PLL 41 = PLL5G Lock status from Host PLL 42 = RCOMP Busy 43 = N/A 44 = N/A 45 = N/A 46 = N/A 47 = N/A 48 = Channel interrupt 0 from channel 0 49 = Channel interrupt 1 from channel 0 50 = Channel interrupt 0 from channel 1 51 = Channel interrupt 1 from channel 1 52 = Channel interrupt 0 from channel 2 53 = Channel interrupt 1 from channel 2 54 = Channel interrupt 0 from channel 3 55 = Channel interrupt 1 from channel 3 56 = Interrupt from ip1588 channel 0 57 = Interrupt from ip1588 channel 1 58 = Interrupt from ip1588 channel 2 59 = Interrupt from ip1588 channel 3 60 = Timestamp FIFO !empty from ip1588 channel 0 61 = Timestamp FIFO !empty from ip1588 channel 1 62 = Timestamp FIFO !empty from ip1588 channel 2 63 = Timestamp FIFO !empty from ip1588 channel 3 64 = Aggregated interrupt 0 65 = Aggregated interrupt 1 66 = Aggregated interrupt 2 67 = Aggregated interrupt 3 68 = Interrupt from pll 0 69 = Interrupt from pll 1 70 = I2C Slave SDA 71 = Cross connect interrupt 72 = LED Blinker 73-127 = Drive low (or high by also setting output INV bit)	0x00

2.28.1.40 GPIO Output Configuration 27

Short Name:GPIO_OUT_CFG_27

Address:0x1EF227

Table 1759 **• GPIO Output Configuration 27**

Bit	Name	Access	Description	Default
6:0	GPIO_27_SEL	R/W	Selects the source for GPIO_27 output 0 = GPIO output 0 from channel 0 1 = GPIO output 1 from channel 0 2 = GPIO output 2 from channel 0 3 = GPIO output 3 from channel 0 4 = GPIO output 4 from channel 0 5 = GPIO output 5 from channel 0 6 = GPIO output 6 from channel 0 7 = GPIO output 7 from channel 0 8 = GPIO output 0 from channel 1 9 = GPIO output 1 from channel 1 10 = GPIO output 2 from channel 1 11 = GPIO output 3 from channel 1 12 = GPIO output 4 from channel 1 13 = GPIO output 5 from channel 1 14 = GPIO output 6 from channel 1 15 = GPIO output 7 from channel 1 16 = GPIO output 0 from channel 2 17 = GPIO output 1 from channel 2 18 = GPIO output 2 from channel 2 19 = GPIO output 3 from channel 2 20 = GPIO output 4 from channel 2 21 = GPIO output 5 from channel 2 22 = GPIO output 6 from channel 2 23 = GPIO output 7 from channel 2 24 = GPIO output 0 from channel 3 25 = GPIO output 1 from channel 3 26 = GPIO output 2 from channel 3 27 = GPIO output 3 from channel 3 28 = GPIO output 4 from channel 3 29 = GPIO output 5 from channel 3 30 = GPIO output 6 from channel 3 31 = GPIO output 7 from channel 3 32 = Tx Enable for channel 0 33 = Tx Enable for channel 1 34 = Tx Enable for channel 2 35 = Tx Enable for channel 3	0x00

Table 1759 • **GPIO Output Configuration 27** ***(continued)***

Bit	Name	Access	Description	Default
6:0	GPIO_27_SEL	R/W	*(continued)* Selects the source for GPIO_27 output 36 = PPS_0 from ip1588 37 = PPS_1 from ip1588 38 = PPS_2 from ip1588 39 = PPS_3 from ip1588 40 = PLL5G Lock status from Line PLL 41 = PLL5G Lock status from Host PLL 42 = RCOMP Busy 43 = N/A 44 = N/A 45 = N/A 46 = N/A 47 = N/A 48 = Channel interrupt 0 from channel 0 49 = Channel interrupt 1 from channel 0 50 = Channel interrupt 0 from channel 1 51 = Channel interrupt 1 from channel 1 52 = Channel interrupt 0 from channel 2 53 = Channel interrupt 1 from channel 2 54 = Channel interrupt 0 from channel 3 55 = Channel interrupt 1 from channel 3 56 = Interrupt from ip1588 channel 0 57 = Interrupt from ip1588 channel 1 58 = Interrupt from ip1588 channel 2 59 = Interrupt from ip1588 channel 3 60 = Timestamp FIFO !empty from ip1588 channel 0 61 = Timestamp FIFO !empty from ip1588 channel 1 62 = Timestamp FIFO !empty from ip1588 channel 2 63 = Timestamp FIFO !empty from ip1588 channel 3 64 = Aggregated interrupt 0 65 = Aggregated interrupt 1 66 = Aggregated interrupt 2 67 = Aggregated interrupt 3 68 = Interrupt from pll 0 69 = Interrupt from pll 1 70 = I2C Slave SDA 71 = Cross connect interrupt 72 = LED Blinker 73-127 = Drive low (or high by also setting output INV bit)	0x00

2.28.1.41 GPIO Output Configuration 28

Short Name:GPIO_OUT_CFG_28

Address:0x1EF228

Table 1760 **• GPIO Output Configuration 28**

Bit	Name	Access	Description	Default
6:0	GPIO_28_SEL	R/W	Selects the source for GPIO_28 output 0 = GPIO output 0 from channel 0 1 = GPIO output 1 from channel 0 2 = GPIO output 2 from channel 0 3 = GPIO output 3 from channel 0 4 = GPIO output 4 from channel 0 5 = GPIO output 5 from channel 0 6 = GPIO output 6 from channel 0 7 = GPIO output 7 from channel 0 8 = GPIO output 0 from channel 1 9 = GPIO output 1 from channel 1 10 = GPIO output 2 from channel 1 11 = GPIO output 3 from channel 1 12 = GPIO output 4 from channel 1 13 = GPIO output 5 from channel 1 14 = GPIO output 6 from channel 1 15 = GPIO output 7 from channel 1 16 = GPIO output 0 from channel 2 17 = GPIO output 1 from channel 2 18 = GPIO output 2 from channel 2 19 = GPIO output 3 from channel 2 20 = GPIO output 4 from channel 2 21 = GPIO output 5 from channel 2 22 = GPIO output 6 from channel 2 23 = GPIO output 7 from channel 2 24 = GPIO output 0 from channel 3 25 = GPIO output 1 from channel 3 26 = GPIO output 2 from channel 3 27 = GPIO output 3 from channel 3 28 = GPIO output 4 from channel 3 29 = GPIO output 5 from channel 3 30 = GPIO output 6 from channel 3 31 = GPIO output 7 from channel 3 32 = Tx Enable for channel 0 33 = Tx Enable for channel 1 34 = Tx Enable for channel 2 35 = Tx Enable for channel 3	0x00

Table 1760 • **GPIO Output Configuration 28** ***(continued)***

Bit	Name	Access	Description	Default
6:0	GPIO_28_SEL	R/W	*(continued)* Selects the source for GPIO_28 output 36 = PPS_0 from ip1588 37 = PPS_1 from ip1588 38 = PPS_2 from ip1588 39 = PPS_3 from ip1588 40 = PLL5G Lock status from Line PLL 41 = PLL5G Lock status from Host PLL 42 = RCOMP Busy 43 = N/A 44 = N/A 45 = N/A 46 = N/A 47 = N/A 48 = Channel interrupt 0 from channel 0 49 = Channel interrupt 1 from channel 0 50 = Channel interrupt 0 from channel 1 51 = Channel interrupt 1 from channel 1 52 = Channel interrupt 0 from channel 2 53 = Channel interrupt 1 from channel 2 54 = Channel interrupt 0 from channel 3 55 = Channel interrupt 1 from channel 3 56 = Interrupt from ip1588 channel 0 57 = Interrupt from ip1588 channel 1 58 = Interrupt from ip1588 channel 2 59 = Interrupt from ip1588 channel 3 60 = Timestamp FIFO !empty from ip1588 channel 0 61 = Timestamp FIFO !empty from ip1588 channel 1 62 = Timestamp FIFO !empty from ip1588 channel 2 63 = Timestamp FIFO !empty from ip1588 channel 3 64 = Aggregated interrupt 0 65 = Aggregated interrupt 1 66 = Aggregated interrupt 2 67 = Aggregated interrupt 3 68 = Interrupt from pll 0 69 = Interrupt from pll 1 70 = I2C Slave SDA 71 = Cross connect interrupt 72 = LED Blinker 73-127 = Drive low (or high by also setting output INV bit)	0x00

2.28.1.42 GPIO Output Configuration 29

Short Name:GPIO_OUT_CFG_29

Address:0x1EF229

Table 1761 **• GPIO Output Configuration 29**

Bit	Name	Access	Description	Default
6:0	GPIO_29_SEL	R/W	Selects the source for GPIO_29 output 0 = GPIO output 0 from channel 0 1 = GPIO output 1 from channel 0 2 = GPIO output 2 from channel 0 3 = GPIO output 3 from channel 0 4 = GPIO output 4 from channel 0 5 = GPIO output 5 from channel 0 6 = GPIO output 6 from channel 0 7 = GPIO output 7 from channel 0 8 = GPIO output 0 from channel 1 9 = GPIO output 1 from channel 1 10 = GPIO output 2 from channel 1 11 = GPIO output 3 from channel 1 12 = GPIO output 4 from channel 1 13 = GPIO output 5 from channel 1 14 = GPIO output 6 from channel 1 15 = GPIO output 7 from channel 1 16 = GPIO output 0 from channel 2 17 = GPIO output 1 from channel 2 18 = GPIO output 2 from channel 2 19 = GPIO output 3 from channel 2 20 = GPIO output 4 from channel 2 21 = GPIO output 5 from channel 2 22 = GPIO output 6 from channel 2 23 = GPIO output 7 from channel 2 24 = GPIO output 0 from channel 3 25 = GPIO output 1 from channel 3 26 = GPIO output 2 from channel 3 27 = GPIO output 3 from channel 3 28 = GPIO output 4 from channel 3 29 = GPIO output 5 from channel 3 30 = GPIO output 6 from channel 3 31 = GPIO output 7 from channel 3 32 = Tx Enable for channel 0 33 = Tx Enable for channel 1 34 = Tx Enable for channel 2 35 = Tx Enable for channel 3	0x00

Table 1761 • **GPIO Output Configuration 29** ***(continued)***

Bit	Name	Access	Description	Default
6:0	GPIO_29_SEL	R/W	*(continued)* Selects the source for GPIO_29 output 36 = PPS_0 from ip1588 37 = PPS_1 from ip1588 38 = PPS_2 from ip1588 39 = PPS_3 from ip1588 40 = PLL5G Lock status from Line PLL 41 = PLL5G Lock status from Host PLL 42 = RCOMP Busy 43 = N/A 44 = N/A 45 = N/A 46 = N/A 47 = N/A 48 = Channel interrupt 0 from channel 0 49 = Channel interrupt 1 from channel 0 50 = Channel interrupt 0 from channel 1 51 = Channel interrupt 1 from channel 1 52 = Channel interrupt 0 from channel 2 53 = Channel interrupt 1 from channel 2 54 = Channel interrupt 0 from channel 3 55 = Channel interrupt 1 from channel 3 56 = Interrupt from ip1588 channel 0 57 = Interrupt from ip1588 channel 1 58 = Interrupt from ip1588 channel 2 59 = Interrupt from ip1588 channel 3 60 = Timestamp FIFO !empty from ip1588 channel 0 61 = Timestamp FIFO !empty from ip1588 channel 1 62 = Timestamp FIFO !empty from ip1588 channel 2 63 = Timestamp FIFO !empty from ip1588 channel 3 64 = Aggregated interrupt 0 65 = Aggregated interrupt 1 66 = Aggregated interrupt 2 67 = Aggregated interrupt 3 68 = Interrupt from pll 0 69 = Interrupt from pll 1 70 = I2C Slave SDA 71 = Cross connect interrupt 72 = LED Blinker 73-127 = Drive low (or high by also setting output INV bit)	0x00

2.28.1.43 GPIO Output Configuration 30

Short Name:GPIO_OUT_CFG_30

Address:0x1EF22A

Table 1762 **• GPIO Output Configuration 30**

Bit	Name	Access	Description	Default
6:0	GPIO_30_SEL	R/W	Selects the source for GPIO_30 output 0 = GPIO output 0 from channel 0 1 = GPIO output 1 from channel 0 2 = GPIO output 2 from channel 0 3 = GPIO output 3 from channel 0 4 = GPIO output 4 from channel 0 5 = GPIO output 5 from channel 0 6 = GPIO output 6 from channel 0 7 = GPIO output 7 from channel 0 8 = GPIO output 0 from channel 1 9 = GPIO output 1 from channel 1 10 = GPIO output 2 from channel 1 11 = GPIO output 3 from channel 1 12 = GPIO output 4 from channel 1 13 = GPIO output 5 from channel 1 14 = GPIO output 6 from channel 1 15 = GPIO output 7 from channel 1 16 = GPIO output 0 from channel 2 17 = GPIO output 1 from channel 2 18 = GPIO output 2 from channel 2 19 = GPIO output 3 from channel 2 20 = GPIO output 4 from channel 2 21 = GPIO output 5 from channel 2 22 = GPIO output 6 from channel 2 23 = GPIO output 7 from channel 2 24 = GPIO output 0 from channel 3 25 = GPIO output 1 from channel 3 26 = GPIO output 2 from channel 3 27 = GPIO output 3 from channel 3 28 = GPIO output 4 from channel 3 29 = GPIO output 5 from channel 3 30 = GPIO output 6 from channel 3 31 = GPIO output 7 from channel 3 32 = Tx Enable for channel 0 33 = Tx Enable for channel 1 34 = Tx Enable for channel 2 35 = Tx Enable for channel 3	0x00

Table 1762 • **GPIO Output Configuration 30** ***(continued)***

Bit	Name	Access	Description	Default
6:0	GPIO_30_SEL	R/W	*(continued)* Selects the source for GPIO_30 output 36 = PPS_0 from ip1588 37 = PPS_1 from ip1588 38 = PPS_2 from ip1588 39 = PPS_3 from ip1588 40 = PLL5G Lock status from Line PLL 41 = PLL5G Lock status from Host PLL 42 = RCOMP Busy 43 = N/A 44 = N/A 45 = N/A 46 = N/A 47 = N/A 48 = Channel interrupt 0 from channel 0 49 = Channel interrupt 1 from channel 0 50 = Channel interrupt 0 from channel 1 51 = Channel interrupt 1 from channel 1 52 = Channel interrupt 0 from channel 2 53 = Channel interrupt 1 from channel 2 54 = Channel interrupt 0 from channel 3 55 = Channel interrupt 1 from channel 3 56 = Interrupt from ip1588 channel 0 57 = Interrupt from ip1588 channel 1 58 = Interrupt from ip1588 channel 2 59 = Interrupt from ip1588 channel 3 60 = Timestamp FIFO !empty from ip1588 channel 0 61 = Timestamp FIFO !empty from ip1588 channel 1 62 = Timestamp FIFO !empty from ip1588 channel 2 63 = Timestamp FIFO !empty from ip1588 channel 3 64 = Aggregated interrupt 0 65 = Aggregated interrupt 1 66 = Aggregated interrupt 2 67 = Aggregated interrupt 3 68 = Interrupt from pll 0 69 = Interrupt from pll 1 70 = I2C Slave SDA 71 = Cross connect interrupt 72 = LED Blinker 73-127 = Drive low (or high by also setting output INV bit)	0x00

2.28.1.44 GPIO Output Configuration 31

Short Name:GPIO_OUT_CFG_31

Address:0x1EF22B

Table 1763 **• GPIO Output Configuration 31**

Bit	Name	Access	Description	Default
6:0	GPIO_31_SEL	R/W	Selects the source for GPIO_31 output 0 = GPIO output 0 from channel 0 1 = GPIO output 1 from channel 0 2 = GPIO output 2 from channel 0 3 = GPIO output 3 from channel 0 4 = GPIO output 4 from channel 0 5 = GPIO output 5 from channel 0 6 = GPIO output 6 from channel 0 7 = GPIO output 7 from channel 0 8 = GPIO output 0 from channel 1 9 = GPIO output 1 from channel 1 10 = GPIO output 2 from channel 1 11 = GPIO output 3 from channel 1 12 = GPIO output 4 from channel 1 13 = GPIO output 5 from channel 1 14 = GPIO output 6 from channel 1 15 = GPIO output 7 from channel 1 16 = GPIO output 0 from channel 2 17 = GPIO output 1 from channel 2 18 = GPIO output 2 from channel 2 19 = GPIO output 3 from channel 2 20 = GPIO output 4 from channel 2 21 = GPIO output 5 from channel 2 22 = GPIO output 6 from channel 2 23 = GPIO output 7 from channel 2 24 = GPIO output 0 from channel 3 25 = GPIO output 1 from channel 3 26 = GPIO output 2 from channel 3 27 = GPIO output 3 from channel 3 28 = GPIO output 4 from channel 3 29 = GPIO output 5 from channel 3 30 = GPIO output 6 from channel 3 31 = GPIO output 7 from channel 3 32 = Tx Enable for channel 0 33 = Tx Enable for channel 1 34 = Tx Enable for channel 2 35 = Tx Enable for channel 3	0x00

Table 1763 • **GPIO Output Configuration 31** ***(continued)***

Bit	Name	Access	Description	Default
6:0	GPIO_31_SEL	R/W	*(continued)* Selects the source for GPIO_31 output 36 = PPS_0 from ip1588 37 = PPS_1 from ip1588 38 = PPS_2 from ip1588 39 = PPS_3 from ip1588 40 = PLL5G Lock status from Line PLL 41 = PLL5G Lock status from Host PLL 42 = RCOMP Busy 43 = N/A 44 = N/A 45 = N/A 46 = N/A 47 = N/A 48 = Channel interrupt 0 from channel 0 49 = Channel interrupt 1 from channel 0 50 = Channel interrupt 0 from channel 1 51 = Channel interrupt 1 from channel 1 52 = Channel interrupt 0 from channel 2 53 = Channel interrupt 1 from channel 2 54 = Channel interrupt 0 from channel 3 55 = Channel interrupt 1 from channel 3 56 = Interrupt from ip1588 channel 0 57 = Interrupt from ip1588 channel 1 58 = Interrupt from ip1588 channel 2 59 = Interrupt from ip1588 channel 3 60 = Timestamp FIFO !empty from ip1588 channel 0 61 = Timestamp FIFO !empty from ip1588 channel 1 62 = Timestamp FIFO !empty from ip1588 channel 2 63 = Timestamp FIFO !empty from ip1588 channel 3 64 = Aggregated interrupt 0 65 = Aggregated interrupt 1 66 = Aggregated interrupt 2 67 = Aggregated interrupt 3 68 = Interrupt from pll 0 69 = Interrupt from pll 1 70 = I2C Slave SDA 71 = Cross connect interrupt 72 = LED Blinker 73-127 = Drive low (or high by also setting output INV bit)	0x00

2.28.1.45 GPIO Output Configuration 32

Short Name:GPIO_OUT_CFG_32

Address:0x1EF22C

Table 1764 **• GPIO Output Configuration 32**

Bit	Name	Access	Description	Default
6:0	GPIO_32_SEL	R/W	Selects the source for GPIO_32 output 0 = GPIO output 0 from channel 0 1 = GPIO output 1 from channel 0 2 = GPIO output 2 from channel 0 3 = GPIO output 3 from channel 0 4 = GPIO output 4 from channel 0 5 = GPIO output 5 from channel 0 6 = GPIO output 6 from channel 0 7 = GPIO output 7 from channel 0 8 = GPIO output 0 from channel 1 9 = GPIO output 1 from channel 1 10 = GPIO output 2 from channel 1 11 = GPIO output 3 from channel 1 12 = GPIO output 4 from channel 1 13 = GPIO output 5 from channel 1 14 = GPIO output 6 from channel 1 15 = GPIO output 7 from channel 1 16 = GPIO output 0 from channel 2 17 = GPIO output 1 from channel 2 18 = GPIO output 2 from channel 2 19 = GPIO output 3 from channel 2 20 = GPIO output 4 from channel 2 21 = GPIO output 5 from channel 2 22 = GPIO output 6 from channel 2 23 = GPIO output 7 from channel 2 24 = GPIO output 0 from channel 3 25 = GPIO output 1 from channel 3 26 = GPIO output 2 from channel 3 27 = GPIO output 3 from channel 3 28 = GPIO output 4 from channel 3 29 = GPIO output 5 from channel 3 30 = GPIO output 6 from channel 3 31 = GPIO output 7 from channel 3 32 = Tx Enable for channel 0 33 = Tx Enable for channel 1 34 = Tx Enable for channel 2 35 = Tx Enable for channel 3	0x00

Table 1764 • **GPIO Output Configuration 32** ***(continued)***

Bit	Name	Access	Description	Default
6:0	GPIO_32_SEL	R/W	*(continued)* Selects the source for GPIO_32 output 36 = PPS_0 from ip1588 37 = PPS_1 from ip1588 38 = PPS_2 from ip1588 39 = PPS_3 from ip1588 40 = PLL5G Lock status from Line PLL 41 = PLL5G Lock status from Host PLL 42 = RCOMP Busy 43 = N/A 44 = N/A 45 = N/A 46 = N/A 47 = N/A 48 = Channel interrupt 0 from channel 0 49 = Channel interrupt 1 from channel 0 50 = Channel interrupt 0 from channel 1 51 = Channel interrupt 1 from channel 1 52 = Channel interrupt 0 from channel 2 53 = Channel interrupt 1 from channel 2 54 = Channel interrupt 0 from channel 3 55 = Channel interrupt 1 from channel 3 56 = Interrupt from ip1588 channel 0 57 = Interrupt from ip1588 channel 1 58 = Interrupt from ip1588 channel 2 59 = Interrupt from ip1588 channel 3 60 = Timestamp FIFO !empty from ip1588 channel 0 61 = Timestamp FIFO !empty from ip1588 channel 1 62 = Timestamp FIFO !empty from ip1588 channel 2 63 = Timestamp FIFO !empty from ip1588 channel 3 64 = Aggregated interrupt 0 65 = Aggregated interrupt 1 66 = Aggregated interrupt 2 67 = Aggregated interrupt 3 68 = Interrupt from pll 0 69 = Interrupt from pll 1 70 = I2C Slave SDA 71 = Cross connect interrupt 72 = LED Blinker 73-127 = Drive low (or high by also setting output INV bit)	0x00

2.28.1.46 GPIO Output Configuration 33

Short Name:GPIO_OUT_CFG_33

Address:0x1EF22D

Table 1765 **• GPIO Output Configuration 33**

Bit	Name	Access	Description	Default
6:0	GPIO_33_SEL	R/W	Selects the source for GPIO_33 output 0 = GPIO output 0 from channel 0 1 = GPIO output 1 from channel 0 2 = GPIO output 2 from channel 0 3 = GPIO output 3 from channel 0 4 = GPIO output 4 from channel 0 5 = GPIO output 5 from channel 0 6 = GPIO output 6 from channel 0 7 = GPIO output 7 from channel 0 8 = GPIO output 0 from channel 1 9 = GPIO output 1 from channel 1 10 = GPIO output 2 from channel 1 11 = GPIO output 3 from channel 1 12 = GPIO output 4 from channel 1 13 = GPIO output 5 from channel 1 14 = GPIO output 6 from channel 1 15 = GPIO output 7 from channel 1 16 = GPIO output 0 from channel 2 17 = GPIO output 1 from channel 2 18 = GPIO output 2 from channel 2 19 = GPIO output 3 from channel 2 20 = GPIO output 4 from channel 2 21 = GPIO output 5 from channel 2 22 = GPIO output 6 from channel 2 23 = GPIO output 7 from channel 2 24 = GPIO output 0 from channel 3 25 = GPIO output 1 from channel 3 26 = GPIO output 2 from channel 3 27 = GPIO output 3 from channel 3 28 = GPIO output 4 from channel 3 29 = GPIO output 5 from channel 3 30 = GPIO output 6 from channel 3 31 = GPIO output 7 from channel 3 32 = Tx Enable for channel 0 33 = Tx Enable for channel 1 34 = Tx Enable for channel 2 35 = Tx Enable for channel 3	0x00

Table 1765 • **GPIO Output Configuration 33** ***(continued)***

Bit	Name	Access	Description	Default
6:0	GPIO_33_SEL	R/W	*(continued)* Selects the source for GPIO_33 output 36 = PPS_0 from ip1588 37 = PPS_1 from ip1588 38 = PPS_2 from ip1588 39 = PPS_3 from ip1588 40 = PLL5G Lock status from Line PLL 41 = PLL5G Lock status from Host PLL 42 = RCOMP Busy 43 = N/A 44 = N/A 45 = N/A 46 = N/A 47 = N/A 48 = Channel interrupt 0 from channel 0 49 = Channel interrupt 1 from channel 0 50 = Channel interrupt 0 from channel 1 51 = Channel interrupt 1 from channel 1 52 = Channel interrupt 0 from channel 2 53 = Channel interrupt 1 from channel 2 54 = Channel interrupt 0 from channel 3 55 = Channel interrupt 1 from channel 3 56 = Interrupt from ip1588 channel 0 57 = Interrupt from ip1588 channel 1 58 = Interrupt from ip1588 channel 2 59 = Interrupt from ip1588 channel 3 60 = Timestamp FIFO !empty from ip1588 channel 0 61 = Timestamp FIFO !empty from ip1588 channel 1 62 = Timestamp FIFO !empty from ip1588 channel 2 63 = Timestamp FIFO !empty from ip1588 channel 3 64 = Aggregated interrupt 0 65 = Aggregated interrupt 1 66 = Aggregated interrupt 2 67 = Aggregated interrupt 3 68 = Interrupt from pll 0 69 = Interrupt from pll 1 70 = I2C Slave SDA 71 = Cross connect interrupt 72 = LED Blinker 73-127 = Drive low (or high by also setting output INV bit)	0x00

2.28.1.47 GPIO Output Configuration 34

Short Name:GPIO_OUT_CFG_34

Address:0x1EF22E

Table 1766 **• GPIO Output Configuration 34**

Bit	Name	Access	Description	Default
6:0	GPIO_34_SEL	R/W	Selects the source for GPIO_34 output 0 = GPIO output 0 from channel 0 1 = GPIO output 1 from channel 0 2 = GPIO output 2 from channel 0 3 = GPIO output 3 from channel 0 4 = GPIO output 4 from channel 0 5 = GPIO output 5 from channel 0 6 = GPIO output 6 from channel 0 7 = GPIO output 7 from channel 0 8 = GPIO output 0 from channel 1 9 = GPIO output 1 from channel 1 10 = GPIO output 2 from channel 1 11 = GPIO output 3 from channel 1 12 = GPIO output 4 from channel 1 13 = GPIO output 5 from channel 1 14 = GPIO output 6 from channel 1 15 = GPIO output 7 from channel 1 16 = GPIO output 0 from channel 2 17 = GPIO output 1 from channel 2 18 = GPIO output 2 from channel 2 19 = GPIO output 3 from channel 2 20 = GPIO output 4 from channel 2 21 = GPIO output 5 from channel 2 22 = GPIO output 6 from channel 2 23 = GPIO output 7 from channel 2 24 = GPIO output 0 from channel 3 25 = GPIO output 1 from channel 3 26 = GPIO output 2 from channel 3 27 = GPIO output 3 from channel 3 28 = GPIO output 4 from channel 3 29 = GPIO output 5 from channel 3 30 = GPIO output 6 from channel 3 31 = GPIO output 7 from channel 3 32 = Tx Enable for channel 0 33 = Tx Enable for channel 1 34 = Tx Enable for channel 2 35 = Tx Enable for channel 3	0x00

Table 1766 • **GPIO Output Configuration 34** ***(continued)***

Bit	Name	Access	Description	Default
6:0	GPIO_34_SEL	R/W	*(continued)* Selects the source for GPIO_34 output 36 = PPS_0 from ip1588 37 = PPS_1 from ip1588 38 = PPS_2 from ip1588 39 = PPS_3 from ip1588 40 = PLL5G Lock status from Line PLL 41 = PLL5G Lock status from Host PLL 42 = RCOMP Busy 43 = N/A 44 = N/A 45 = N/A 46 = N/A 47 = N/A 48 = Channel interrupt 0 from channel 0 49 = Channel interrupt 1 from channel 0 50 = Channel interrupt 0 from channel 1 51 = Channel interrupt 1 from channel 1 52 = Channel interrupt 0 from channel 2 53 = Channel interrupt 1 from channel 2 54 = Channel interrupt 0 from channel 3 55 = Channel interrupt 1 from channel 3 56 = Interrupt from ip1588 channel 0 57 = Interrupt from ip1588 channel 1 58 = Interrupt from ip1588 channel 2 59 = Interrupt from ip1588 channel 3 60 = Timestamp FIFO !empty from ip1588 channel 0 61 = Timestamp FIFO !empty from ip1588 channel 1 62 = Timestamp FIFO !empty from ip1588 channel 2 63 = Timestamp FIFO !empty from ip1588 channel 3 64 = Aggregated interrupt 0 65 = Aggregated interrupt 1 66 = Aggregated interrupt 2 67 = Aggregated interrupt 3 68 = Interrupt from pll 0 69 = Interrupt from pll 1 70 = I2C Slave SDA 71 = Cross connect interrupt 72 = LED Blinker 73-127 = Drive low (or high by also setting output INV bit)	0x00

2.28.1.48 GPIO Output Configuration 35

Short Name:GPIO_OUT_CFG_35

Address:0x1EF22F

***Table 1767* • GPIO Output Configuration 35**

Bit	Name	Access	Description	Default
6:0	GPIO_35_SEL	R/W	Selects the source for GPIO_35 output 0 = GPIO output 0 from channel 0 1 = GPIO output 1 from channel 0 2 = GPIO output 2 from channel 0 3 = GPIO output 3 from channel 0 4 = GPIO output 4 from channel 0 5 = GPIO output 5 from channel 0 6 = GPIO output 6 from channel 0 7 = GPIO output 7 from channel 0 8 = GPIO output 0 from channel 1 9 = GPIO output 1 from channel 1 10 = GPIO output 2 from channel 1 11 = GPIO output 3 from channel 1 12 = GPIO output 4 from channel 1 13 = GPIO output 5 from channel 1 14 = GPIO output 6 from channel 1 15 = GPIO output 7 from channel 1 16 = GPIO output 0 from channel 2 17 = GPIO output 1 from channel 2 18 = GPIO output 2 from channel 2 19 = GPIO output 3 from channel 2 20 = GPIO output 4 from channel 2 21 = GPIO output 5 from channel 2 22 = GPIO output 6 from channel 2 23 = GPIO output 7 from channel 2 24 = GPIO output 0 from channel 3 25 = GPIO output 1 from channel 3 26 = GPIO output 2 from channel 3 27 = GPIO output 3 from channel 3 28 = GPIO output 4 from channel 3 29 = GPIO output 5 from channel 3 30 = GPIO output 6 from channel 3 31 = GPIO output 7 from channel 3 32 = Tx Enable for channel 0 33 = Tx Enable for channel 1 34 = Tx Enable for channel 2 35 = Tx Enable for channel 3	0x00

Table 1767 • **GPIO Output Configuration 35** ***(continued)***

Bit	Name	Access	Description	Default
6:0	GPIO_35_SEL	R/W	*(continued)* Selects the source for GPIO_35 output 36 = PPS_0 from ip1588 37 = PPS_1 from ip1588 38 = PPS_2 from ip1588 39 = PPS_3 from ip1588 40 = PLL5G Lock status from Line PLL 41 = PLL5G Lock status from Host PLL 42 = RCOMP Busy 43 = N/A 44 = N/A 45 = N/A 46 = N/A 47 = N/A 48 = Channel interrupt 0 from channel 0 49 = Channel interrupt 1 from channel 0 50 = Channel interrupt 0 from channel 1 51 = Channel interrupt 1 from channel 1 52 = Channel interrupt 0 from channel 2 53 = Channel interrupt 1 from channel 2 54 = Channel interrupt 0 from channel 3 55 = Channel interrupt 1 from channel 3 56 = Interrupt from ip1588 channel 0 57 = Interrupt from ip1588 channel 1 58 = Interrupt from ip1588 channel 2 59 = Interrupt from ip1588 channel 3 60 = Timestamp FIFO !empty from ip1588 channel 0 61 = Timestamp FIFO !empty from ip1588 channel 1 62 = Timestamp FIFO !empty from ip1588 channel 2 63 = Timestamp FIFO !empty from ip1588 channel 3 64 = Aggregated interrupt 0 65 = Aggregated interrupt 1 66 = Aggregated interrupt 2 67 = Aggregated interrupt 3 68 = Interrupt from pll 0 69 = Interrupt from pll 1 70 = I2C Slave SDA 71 = Cross connect interrupt 72 = LED Blinker 73-127 = Drive low (or high by also setting output INV bit)	0x00

2.28.1.49 GPIO Output Configuration 36

Short Name:GPIO_OUT_CFG_36

Address:0x1EF230

Table 1768 **• GPIO Output Configuration 36**

Bit	Name	Access	Description	Default
6:0	GPIO_36_SEL	R/W	Selects the source for GPIO_36 output 0 = GPIO output 0 from channel 0 1 = GPIO output 1 from channel 0 2 = GPIO output 2 from channel 0 3 = GPIO output 3 from channel 0 4 = GPIO output 4 from channel 0 5 = GPIO output 5 from channel 0 6 = GPIO output 6 from channel 0 7 = GPIO output 7 from channel 0 8 = GPIO output 0 from channel 1 9 = GPIO output 1 from channel 1 10 = GPIO output 2 from channel 1 11 = GPIO output 3 from channel 1 12 = GPIO output 4 from channel 1 13 = GPIO output 5 from channel 1 14 = GPIO output 6 from channel 1 15 = GPIO output 7 from channel 1 16 = GPIO output 0 from channel 2 17 = GPIO output 1 from channel 2 18 = GPIO output 2 from channel 2 19 = GPIO output 3 from channel 2 20 = GPIO output 4 from channel 2 21 = GPIO output 5 from channel 2 22 = GPIO output 6 from channel 2 23 = GPIO output 7 from channel 2 24 = GPIO output 0 from channel 3 25 = GPIO output 1 from channel 3 26 = GPIO output 2 from channel 3 27 = GPIO output 3 from channel 3 28 = GPIO output 4 from channel 3 29 = GPIO output 5 from channel 3 30 = GPIO output 6 from channel 3 31 = GPIO output 7 from channel 3 32 = Tx Enable for channel 0 33 = Tx Enable for channel 1 34 = Tx Enable for channel 2 35 = Tx Enable for channel 3	0x00

Table 1768 • **GPIO Output Configuration 36** ***(continued)***

Bit	Name	Access	Description	Default
6:0	GPIO_36_SEL	R/W	*(continued)* Selects the source for GPIO_36 output 36 = PPS_0 from ip1588 37 = PPS_1 from ip1588 38 = PPS_2 from ip1588 39 = PPS_3 from ip1588 40 = PLL5G Lock status from Line PLL 41 = PLL5G Lock status from Host PLL 42 = RCOMP Busy 43 = N/A 44 = N/A 45 = N/A 46 = N/A 47 = N/A 48 = Channel interrupt 0 from channel 0 49 = Channel interrupt 1 from channel 0 50 = Channel interrupt 0 from channel 1 51 = Channel interrupt 1 from channel 1 52 = Channel interrupt 0 from channel 2 53 = Channel interrupt 1 from channel 2 54 = Channel interrupt 0 from channel 3 55 = Channel interrupt 1 from channel 3 56 = Interrupt from ip1588 channel 0 57 = Interrupt from ip1588 channel 1 58 = Interrupt from ip1588 channel 2 59 = Interrupt from ip1588 channel 3 60 = Timestamp FIFO !empty from ip1588 channel 0 61 = Timestamp FIFO !empty from ip1588 channel 1 62 = Timestamp FIFO !empty from ip1588 channel 2 63 = Timestamp FIFO !empty from ip1588 channel 3 64 = Aggregated interrupt 0 65 = Aggregated interrupt 1 66 = Aggregated interrupt 2 67 = Aggregated interrupt 3 68 = Interrupt from pll 0 69 = Interrupt from pll 1 70 = I2C Slave SDA 71 = Cross connect interrupt 72 = LED Blinker 73-127 = Drive low (or high by also setting output INV bit)	0x00

2.28.1.50 GPIO Output Configuration 37

Short Name:GPIO_OUT_CFG_37

Address:0x1EF231

***Table 1769* • GPIO Output Configuration 37**

Bit	Name	Access	Description	Default
6:0	GPIO_37_SEL	R/W	Selects the source for GPIO_37 output 0 = GPIO output 0 from channel 0 1 = GPIO output 1 from channel 0 2 = GPIO output 2 from channel 0 3 = GPIO output 3 from channel 0 4 = GPIO output 4 from channel 0 5 = GPIO output 5 from channel 0 6 = GPIO output 6 from channel 0 7 = GPIO output 7 from channel 0 8 = GPIO output 0 from channel 1 9 = GPIO output 1 from channel 1 10 = GPIO output 2 from channel 1 11 = GPIO output 3 from channel 1 12 = GPIO output 4 from channel 1 13 = GPIO output 5 from channel 1 14 = GPIO output 6 from channel 1 15 = GPIO output 7 from channel 1 16 = GPIO output 0 from channel 2 17 = GPIO output 1 from channel 2 18 = GPIO output 2 from channel 2 19 = GPIO output 3 from channel 2 20 = GPIO output 4 from channel 2 21 = GPIO output 5 from channel 2 22 = GPIO output 6 from channel 2 23 = GPIO output 7 from channel 2 24 = GPIO output 0 from channel 3 25 = GPIO output 1 from channel 3 26 = GPIO output 2 from channel 3 27 = GPIO output 3 from channel 3 28 = GPIO output 4 from channel 3 29 = GPIO output 5 from channel 3 30 = GPIO output 6 from channel 3 31 = GPIO output 7 from channel 3 32 = Tx Enable for channel 0 33 = Tx Enable for channel 1 34 = Tx Enable for channel 2 35 = Tx Enable for channel 3	0x00

Table 1769 • **GPIO Output Configuration 37** ***(continued)***

Bit	Name	Access	Description	Default
6:0	GPIO_37_SEL	R/W	*(continued)* Selects the source for GPIO_37 output 36 = PPS_0 from ip1588 37 = PPS_1 from ip1588 38 = PPS_2 from ip1588 39 = PPS_3 from ip1588 40 = PLL5G Lock status from Line PLL 41 = PLL5G Lock status from Host PLL 42 = RCOMP Busy 43 = N/A 44 = N/A 45 = N/A 46 = N/A 47 = N/A 48 = Channel interrupt 0 from channel 0 49 = Channel interrupt 1 from channel 0 50 = Channel interrupt 0 from channel 1 51 = Channel interrupt 1 from channel 1 52 = Channel interrupt 0 from channel 2 53 = Channel interrupt 1 from channel 2 54 = Channel interrupt 0 from channel 3 55 = Channel interrupt 1 from channel 3 56 = Interrupt from ip1588 channel 0 57 = Interrupt from ip1588 channel 1 58 = Interrupt from ip1588 channel 2 59 = Interrupt from ip1588 channel 3 60 = Timestamp FIFO !empty from ip1588 channel 0 61 = Timestamp FIFO !empty from ip1588 channel 1 62 = Timestamp FIFO !empty from ip1588 channel 2 63 = Timestamp FIFO !empty from ip1588 channel 3 64 = Aggregated interrupt 0 65 = Aggregated interrupt 1 66 = Aggregated interrupt 2 67 = Aggregated interrupt 3 68 = Interrupt from pll 0 69 = Interrupt from pll 1 70 = I2C Slave SDA 71 = Cross connect interrupt 72 = LED Blinker 73-127 = Drive low (or high by also setting output INV bit)	0x00

2.28.1.51 GPIO Output Configuration 38

Short Name:GPIO_OUT_CFG_38

Address:0x1EF232

Table 1770 **• GPIO Output Configuration 38**

Bit	Name	Access	Description	Default
6:0	GPIO_38_SEL	R/W	Selects the source for GPIO_38 output 0 = GPIO output 0 from channel 0 1 = GPIO output 1 from channel 0 2 = GPIO output 2 from channel 0 3 = GPIO output 3 from channel 0 4 = GPIO output 4 from channel 0 5 = GPIO output 5 from channel 0 6 = GPIO output 6 from channel 0 7 = GPIO output 7 from channel 0 8 = GPIO output 0 from channel 1 9 = GPIO output 1 from channel 1 10 = GPIO output 2 from channel 1 11 = GPIO output 3 from channel 1 12 = GPIO output 4 from channel 1 13 = GPIO output 5 from channel 1 14 = GPIO output 6 from channel 1 15 = GPIO output 7 from channel 1 16 = GPIO output 0 from channel 2 17 = GPIO output 1 from channel 2 18 = GPIO output 2 from channel 2 19 = GPIO output 3 from channel 2 20 = GPIO output 4 from channel 2 21 = GPIO output 5 from channel 2 22 = GPIO output 6 from channel 2 23 = GPIO output 7 from channel 2 24 = GPIO output 0 from channel 3 25 = GPIO output 1 from channel 3 26 = GPIO output 2 from channel 3 27 = GPIO output 3 from channel 3 28 = GPIO output 4 from channel 3 29 = GPIO output 5 from channel 3 30 = GPIO output 6 from channel 3 31 = GPIO output 7 from channel 3 32 = Tx Enable for channel 0 33 = Tx Enable for channel 1 34 = Tx Enable for channel 2 35 = Tx Enable for channel 3	0x00

Table 1770 • **GPIO Output Configuration 38** ***(continued)***

Bit	Name	Access	Description	Default
6:0	GPIO_38_SEL	R/W	*(continued)* Selects the source for GPIO_38 output 36 = PPS_0 from ip1588 37 = PPS_1 from ip1588 38 = PPS_2 from ip1588 39 = PPS_3 from ip1588 40 = PLL5G Lock status from Line PLL 41 = PLL5G Lock status from Host PLL 42 = RCOMP Busy 43 = N/A 44 = N/A 45 = N/A 46 = N/A 47 = N/A 48 = Channel interrupt 0 from channel 0 49 = Channel interrupt 1 from channel 0 50 = Channel interrupt 0 from channel 1 51 = Channel interrupt 1 from channel 1 52 = Channel interrupt 0 from channel 2 53 = Channel interrupt 1 from channel 2 54 = Channel interrupt 0 from channel 3 55 = Channel interrupt 1 from channel 3 56 = Interrupt from ip1588 channel 0 57 = Interrupt from ip1588 channel 1 58 = Interrupt from ip1588 channel 2 59 = Interrupt from ip1588 channel 3 60 = Timestamp FIFO !empty from ip1588 channel 0 61 = Timestamp FIFO !empty from ip1588 channel 1 62 = Timestamp FIFO !empty from ip1588 channel 2 63 = Timestamp FIFO !empty from ip1588 channel 3 64 = Aggregated interrupt 0 65 = Aggregated interrupt 1 66 = Aggregated interrupt 2 67 = Aggregated interrupt 3 68 = Interrupt from pll 0 69 = Interrupt from pll 1 70 = I2C Slave SDA 71 = Cross connect interrupt 72 = LED Blinker 73-127 = Drive low (or high by also setting output INV bit)	0x00

2.28.1.52 GPIO Output Configuration 39

Short Name:GPIO_OUT_CFG_39

Address:0x1EF233

Table 1771 **• GPIO Output Configuration 39**

Bit	Name	Access	Description	Default
6:0	GPIO_39_SEL	R/W	Selects the source for GPIO_39 output 0 = GPIO output 0 from channel 0 1 = GPIO output 1 from channel 0 2 = GPIO output 2 from channel 0 3 = GPIO output 3 from channel 0 4 = GPIO output 4 from channel 0 5 = GPIO output 5 from channel 0 6 = GPIO output 6 from channel 0 7 = GPIO output 7 from channel 0 8 = GPIO output 0 from channel 1 9 = GPIO output 1 from channel 1 10 = GPIO output 2 from channel 1 11 = GPIO output 3 from channel 1 12 = GPIO output 4 from channel 1 13 = GPIO output 5 from channel 1 14 = GPIO output 6 from channel 1 15 = GPIO output 7 from channel 1 16 = GPIO output 0 from channel 2 17 = GPIO output 1 from channel 2 18 = GPIO output 2 from channel 2 19 = GPIO output 3 from channel 2 20 = GPIO output 4 from channel 2 21 = GPIO output 5 from channel 2 22 = GPIO output 6 from channel 2 23 = GPIO output 7 from channel 2 24 = GPIO output 0 from channel 3 25 = GPIO output 1 from channel 3 26 = GPIO output 2 from channel 3 27 = GPIO output 3 from channel 3 28 = GPIO output 4 from channel 3 29 = GPIO output 5 from channel 3 30 = GPIO output 6 from channel 3 31 = GPIO output 7 from channel 3 32 = Tx Enable for channel 0 33 = Tx Enable for channel 1 34 = Tx Enable for channel 2 35 = Tx Enable for channel 3	0x00

Table 1771 • **GPIO Output Configuration 39** ***(continued)***

Bit	Name	Access	Description	Default
6:0	GPIO_39_SEL	R/W	*(continued)* Selects the source for GPIO_39 output 36 = PPS_0 from ip1588 37 = PPS_1 from ip1588 38 = PPS_2 from ip1588 39 = PPS_3 from ip1588 40 = PLL5G Lock status from Line PLL 41 = PLL5G Lock status from Host PLL 42 = RCOMP Busy 43 = N/A 44 = N/A 45 = N/A 46 = N/A 47 = N/A 48 = Channel interrupt 0 from channel 0 49 = Channel interrupt 1 from channel 0 50 = Channel interrupt 0 from channel 1 51 = Channel interrupt 1 from channel 1 52 = Channel interrupt 0 from channel 2 53 = Channel interrupt 1 from channel 2 54 = Channel interrupt 0 from channel 3 55 = Channel interrupt 1 from channel 3 56 = Interrupt from ip1588 channel 0 57 = Interrupt from ip1588 channel 1 58 = Interrupt from ip1588 channel 2 59 = Interrupt from ip1588 channel 3 60 = Timestamp FIFO !empty from ip1588 channel 0 61 = Timestamp FIFO !empty from ip1588 channel 1 62 = Timestamp FIFO !empty from ip1588 channel 2 63 = Timestamp FIFO !empty from ip1588 channel 3 64 = Aggregated interrupt 0 65 = Aggregated interrupt 1 66 = Aggregated interrupt 2 67 = Aggregated interrupt 3 68 = Interrupt from pll 0 69 = Interrupt from pll 1 70 = I2C Slave SDA 71 = Cross connect interrupt 72 = LED Blinker 73-127 = Drive low (or high by also setting output INV bit)	0x00

2.28.1.53 Channel 0 Line LOPC Configuration

Short Name:CH0_LINE_LOPC_CFG

Address:0x1EF234

Table 1772 • **Channel 0 Line LOPC Configuration**

Bit	Name	Access	Description	Default
8	CH0_LINE_LOPC_INV	R/W	Set high to invert sense of LINE_LOPC 0 = Use GPIO state as is 1 = Invert GPIO input state	0x0

*Table 1772 • (continued)*Channel 0 Line LOPC Configuration

Bit	Name	Access	Description	Default
5:0	CH0_LINE_LOPC_SEL	R/W	Selects which GPIO is used for CH0 LINE_LOPC input 39:0 -> GPIO[39:0] 63:40 -> 0	0x22

2.28.1.54 Channel 1 Line LOPC Configuration

Short Name:CH1_LINE_LOPC_CFG

Address:0x1EF235

Table 1773 • Channel 1 Line LOPC Configuration

Bit	Name	Access	Description	Default
8	CH1_LINE_LOPC_INV	R/W	Set high to invert sense of LINE_LOPC 0 = Use GPIO state as is 1 = Invert GPIO input state	0x0
5:0	CH1_LINE_LOPC_SEL	R/W	Selects which GPIO is used for CH1 LINE_LOPC input 39:0 -> GPIO[39:0] 63:40 -> 0	0x23

2.28.1.55 Channel 2 Line LOPC Configuration

Short Name:CH2_LINE_LOPC_CFG

Address:0x1EF236

Table 1774 • Channel 2 Line LOPC Configuration

Bit	Name	Access	Description	Default
8	CH2_LINE_LOPC_INV	R/W	Set high to invert sense of LINE_LOPC 0 = Use GPIO state as is 1 = Invert GPIO input state	0x0
5:0	CH2_LINE_LOPC_SEL	R/W	Selects which GPIO is used for CH2 LINE_LOPC input 39:0 -> GPIO[39:0] 63:40 -> 0	0x24

2.28.1.56 Channel 3 Line LOPC Configuration

Short Name:CH3_LINE_LOPC_CFG

Address:0x1EF237

Table 1775 • Channel 3 Line LOPC Configuration

Bit	Name	Access	Description	Default
8	CH3_LINE_LOPC_INV	R/W	Set high to invert sense of LINE_LOPC 0 = Use GPIO state as is 1 = Invert GPIO input state	0x0
5:0	CH3_LINE_LOPC_SEL	R/W	Selects which GPIO is used for CH3 LINE_LOPC input 39:0 -> GPIO[39:0] 63:40 -> 0	0x25

2.28.1.57 Channel 0 Host LOPC Configuration

Short Name:CH0_HOST_LOPC_CFG

Address:0x1EF238

Table 1776 • **Channel 0 Host LOPC Configuration**

Bit	Name	Access	Description	Default
8	CH0_HOST_LOPC_INV	R/W	Set high to invert sense of HOST_LOPC 0 = Use GPIO state as is 1 = Invert GPIO input state	0x1
5:0	CH0_HOST_LOPC_SEL	R/W	Selects which GPIO is used for CH0 HOST_LOPC input 39:0 -> GPIO[39:0] 63:40 -> 0	0x3F

2.28.1.58 Channel 1 Host LOPC Configuration

Short Name:CH1_HOST_LOPC_CFG

Address:0x1EF239

Table 1777 • **Channel 1 Host LOPC Configuration**

Bit	Name	Access	Description	Default
8	CH1_HOST_LOPC_INV	R/W	Set high to invert sense of HOST_LOPC 0 = Use GPIO state as is 1 = Invert GPIO input state	0x1
5:0	CH1_HOST_LOPC_SEL	R/W	Selects which GPIO is used for CH1 HOST_LOPC input 39:0 -> GPIO[39:0] 63:40 -> 0	0x3F

2.28.1.59 Channel 2 Host LOPC Configuration

Short Name:CH2_HOST_LOPC_CFG

Address:0x1EF23A

Table 1778 • **Channel 2 Host LOPC Configuration**

Bit	Name	Access	Description	Default
8	CH2_HOST_LOPC_INV	R/W	Set high to invert sense of HOST_LOPC 0 = Use GPIO state as is 1 = Invert GPIO input state	0x1
5:0	CH2_HOST_LOPC_SEL	R/W	Selects which GPIO is used for CH2 HOST_LOPC input 39:0 -> GPIO[39:0] 63:40 -> 0	0x3F

2.28.1.60 Channel 3 Host LOPC Configuration

Short Name:CH3_HOST_LOPC_CFG

Address:0x1EF23B

Table 1779 • **Channel 3 Host LOPC Configuration**

Bit	Name	Access	Description	Default
8	CH3_HOST_LOPC_INV	R/W	Set high to invert sense of HOST_LOPC 0 = Use GPIO state as is 1 = Invert GPIO input state	0x1
5:0	CH3_HOST_LOPC_SEL	R/W	Selects which GPIO is used for CH3 HOST_LOPC input 39:0 -> GPIO[39:0] 63:40 -> 0	0x3F

2.28.1.61 Channel 0 TOSI Configuration

Short Name:CH0_TOSI_SDAT_CFG

Address:0x1EF23C

Table 1780 • **Channel 0 TOSI Configuration**

Bit	Name	Access	Description	Default
8	CH0_TOSI_SDAT_INV	R/W	Set high to invert state of selected GPIO 0 = Use GPIO as is 1 = Use inverted GPIO state	0x0
5:0	CH0_TOSI_SDAT_SEL	R/W	Selects which GPIO input routes to CH0 TOSI SDAT input 39:0 -> GPIO[39:0] 63:40 -> 0	0x00

2.28.1.62 Channel 1 TOSI Configuration

Short Name:CH1_TOSI_SDAT_CFG

Address:0x1EF23D

Table 1781 • **Channel 1 TOSI Configuration**

Bit	Name	Access	Description	Default
8	CH1_TOSI_SDAT_INV	R/W	Set high to invert state of selected GPIO 0 = Use GPIO as is 1 = Use inverted GPIO state	0x0
5:0	CH1_TOSI_SDAT_SEL	R/W	Selects which GPIO input routes to CH1 TOSI SDAT input 39:0 -> GPIO[39:0] 63:40 -> 0	0x00

2.28.1.63 Channel 2 TOSI Configuration

Short Name:CH2_TOSI_SDAT_CFG

Address:0x1EF23E

Table 1782 • **Channel 2 TOSI Configuration**

Bit	Name	Access	Description	Default
8	CH2_TOSI_SDAT_INV	R/W	Set high to invert state of selected GPIO 0 = Use GPIO as is 1 = Use inverted GPIO state	0x0
5:0	CH2_TOSI_SDAT_SEL	R/W	Selects which GPIO input routes to CH2 TOSI SDAT input 39:0 -> GPIO[39:0] 63:40 -> 0	0x00

2.28.1.64 Channel 3 TOSI Configuration

Short Name:CH3_TOSI_SDAT_CFG

Address:0x1EF23F

Table 1783 • **Channel 3 TOSI Configuration**

Bit	Name	Access	Description	Default
8	CH3_TOSI_SDAT_INV	R/W	Set high to invert state of selected GPIO 0 = Use GPIO as is 1 = Use inverted GPIO state	0x0
5:0	CH3_TOSI_SDAT_SEL	R/W	Selects which GPIO input routes to CH3 TOSI SDAT input 39:0 -> GPIO[39:0] 63:40 -> 0	0x00

2.28.1.65 Channel 0 I2C Master Data Configuration

Short Name:CH0_I2C_MST_DATA_IN_CFG

Address:0x1EF240

Table 1784 • **Channel 0 I2C Master Data Configuration**

Bit	Name	Access	Description	Default
8	CH0_I2C_MST_DATA_IN_INV	R/W	Set high to invert state of selected GPIO 0 = Use GPIO as is 1 = Use inverted GPIO state	0x0
5:0	CH0_I2C_MST_DATA_IN_SEL	R/W	Selects which GPIO input routes to CH0 I2C_MST_DATA_IN input 39:0 -> GPIO[39:0] 63:40 -> 0	0x00

2.28.1.66 Channel 1 I2C Master Data Configuration

Short Name:CH1_I2C_MST_DATA_IN_CFG

Address:0x1EF241

Table 1785 • **Channel 1 I2C Master Data Configuration**

Bit	Name	Access	Description	Default
8	CH1_I2C_MST_DATA_IN_INV	R/W	Set high to invert state of selected GPIO 0 = Use GPIO as is 1 = Use inverted GPIO state	0x0
5:0	CH1_I2C_MST_DATA_IN_SEL	R/W	Selects which GPIO input routes to CH1 I2C_MST_DATA_IN input 39:0 -> GPIO[39:0] 63:40 -> 0	0x00

2.28.1.67 Channel 2 I2C Master Data Configuration

Short Name:CH2_I2C_MST_DATA_IN_CFG

Address:0x1EF242

Table 1786 • **Channel 2 I2C Master Data Configuration**

Bit	Name	Access	Description	Default
8	CH2_I2C_MST_DATA_IN_INV	R/W	Set high to invert state of selected GPIO 0 = Use GPIO as is 1 = Use inverted GPIO state	0x0
5:0	CH2_I2C_MST_DATA_IN_SEL	R/W	Selects which GPIO input routes to CH2 I2C_MST_DATA_IN input 39:0 -> GPIO[39:0] 63:40 -> 0	0x00

2.28.1.68 Channel 3 I2C Master Data Configuration

Short Name:CH3_I2C_MST_DATA_IN_CFG

Address:0x1EF243

Table 1787 • **Channel 3 I2C Master Data Configuration**

Bit	Name	Access	Description	Default
8	CH3_I2C_MST_DATA_IN_INV	R/W	Set high to invert state of selected GPIO 0 = Use GPIO as is 1 = Use inverted GPIO state	0x0
5:0	CH3_I2C_MST_DATA_IN_SEL	R/W	Selects which GPIO input routes to CH3 I2C_MST_DATA_IN input 39:0 -> GPIO[39:0] 63:40 -> 0	0x00

2.28.1.69 Channel 0 I2C Master Clock Configuration

Short Name:CH0_I2C_MST_CLK_IN_CFG

Address:0x1EF244

Table 1788 • **Channel 0 I2C Master Clock Configuration**

Bit	Name	Access	Description	Default
8	CH0_I2C_MST_CLK_IN_INV	R/W	Set high to invert state of selected GPIO 0 = Use GPIO as is 1 = Use inverted GPIO state	0x0
5:0	CH0_I2C_MST_CLK_IN_SEL	R/W	Selects which GPIO input routes to CH0 I2C_MST_CLK_IN input 39:0 -> GPIO[39:0] 63:40 -> 0	0x00

2.28.1.70 Channel 1 I2C Master Clock Configuration

Short Name:CH1_I2C_MST_CLK_IN_CFG

Address:0x1EF245

Table 1789 • **Channel 1 I2C Master Clock Configuration**

Bit	Name	Access	Description	Default
8	CH1_I2C_MST_CLK_IN_INV	R/W	Set high to invert state of selected GPIO 0 = Use GPIO as is 1 = Use inverted GPIO state	0x0
5:0	CH1_I2C_MST_CLK_IN_SEL	R/W	Selects which GPIO input routes to CH1 I2C_MST_CLK_IN input 39:0 -> GPIO[39:0] 63:40 -> 0	0x00

2.28.1.71 Channel 2 I2C Master Clock Configuration

Short Name:CH2_I2C_MST_CLK_IN_CFG

Address:0x1EF246

Table 1790 • **Channel 2 I2C Master Clock Configuration**

Bit	Name	Access	Description	Default
8	CH2_I2C_MST_CLK_IN_INV	R/W	Set high to invert state of selected GPIO 0 = Use GPIO as is 1 = Use inverted GPIO state	0x0
5:0	CH2_I2C_MST_CLK_IN_SEL	R/W	Selects which GPIO input routes to CH2 I2C_MST_CLK_IN input 39:0 -> GPIO[39:0] 63:40 -> 0	0x00

2.28.1.72 Channel 3 I2C Master Clock Configuration

Short Name:CH3_I2C_MST_CLK_IN_CFG

Address:0x1EF247

Table 1791 • **Channel 3 I2C Master Clock Configuration**

Bit	Name	Access	Description	Default
8	CH3_I2C_MST_CLK_IN_INV	R/W	Set high to invert state of selected GPIO 0 = Use GPIO as is 1 = Use inverted GPIO state	0x0
5:0	CH3_I2C_MST_CLK_IN_SEL	R/W	Selects which GPIO input routes to CH3 I2C_MST_CLK_IN input 39:0 -> GPIO[39:0] 63:40 -> 0	0x00

2.28.1.73 EXP4 External Configuration

Short Name:EXP4_EXT_IN_CFG

Addresses:0x1EF248 - 0x1EF24F

Table 1792 • **EXP4 External Configuration**

Bit	Name	Access	Description	Default
8	EXP4_EXT_IN_INV	R/W	Set high to invert selected GPIO	0x0
5:0	EXP4_EXT_IN_SEL	R/W	Selects which GPIO input maps to the corresponding cross connect ext_in pin	0x00

2.28.1.74 AS External Configuration

Short Name:AS_EXT_IN_CFG

Addresses:0x1EF250 - 0x1EF257

Table 1793 • **AS External Configuration**

Bit	Name	Access	Description	Default
8	AS_EXT_IN_INV	R/W	Set high to invert selected GPIO	0x0
5:0	AS_EXT_IN_SEL	R/W	Selects which GPIO input maps to the corresponding clock auto-squelch ext_in pin	0x00

2.28.1.75 I2C Clock Configuration

Short Name:I2C_CLKIN_CFG

Address:0x1EF258

Table 1794 • **I2C Clock Configuration**

Bit	Name	Access	Description	Default
8	I2C_CLKIN_INV	R/W	Set high to invert selected GPIO	0x0
5:0	I2C_CLKIN_SEL	R/W	Selects which GPIO input maps to the I2C_CLKIN input	0x21

2.28.1.76 I2C Data Configuration

Short Name:I2C_DATAIN_CFG

Address:0x1EF259

Table 1795 • **I2C Data Configuration**

Bit	Name	Access	Description	Default
8	I2C_DATAIN_INV	R/W	Set high to invert selected GPIO	0x0
5:0	I2C_DATAIN_SEL	R/W	Selects which GPIO input maps to the I2C_DATAIN input	0x20

2.28.1.77 PMTick Configuration

Short Name:PMTICK_CFG

Address:0x1EF25A

Table 1796 • **PMTICK Configuration**

Bit	Name	Access	Description	Default
8	PMTICK_INV	R/W	Set high to invert selected GPIO	0x0
5:0	PMTICK_SEL	R/W	Selects which GPIO input maps to the PMTICK input	0x00

2.28.1.78 Blink Configuration

Short Name:BLINK_CFG

Address:0x1EF25B

Table 1797 • **Blink Configuration**

Bit	Name	Access	Description	Default
15:8	BLINKER_HIGH_TIME	R/W	Time LED stays high (in 2*ms)	0xFA
7:0	BLINKER_LOW_TIME	R/W	Time LED is low (in 2*ms). Disable blink circuit by setting to 0.	0xFA

2.28.1.79 Interrupt Source

Short Name:INTR_SRC_EN

Addresses:0x1EF25C - 0x1EF25F

Table 1798 • **Interrupt Source**

Bit	Name	Access	Description	Default
20	GPIO_INTR_EN	R/W		0x0
19	CLK_MUX_INTR_EN	R/W		0x0
18	EXP4_INTR_EN	R/W		0x0
17	LCPLL_1_INTR_EN	R/W		0x0
16	LCPLL_0_INTR_EN	R/W		0x0
15	IP1588_1_INTR3_EN	R/W		0x0
14	IP1588_1_INTR2_EN	R/W		0x0
13	IP1588_1_INTR1_EN	R/W		0x0
12	IP1588_1_INTR0_EN	R/W		0x0
11	IP1588_0_INTR3_EN	R/W		0x0

Table 1798 • **Interrupt Source *(continued)***

Bit	Name	Access	Description	Default
10	IP1588_0_INTR2_EN	R/W		0x0
9	IP1588_0_INTR1_EN	R/W		0x0
8	IP1588_0_INTR0_EN	R/W		0x0
7	CH3_INTR1_EN	R/W		0x0
6	CH3_INTR0_EN	R/W		0x0
5	CH2_INTR1_EN	R/W		0x0
4	CH2_INTR0_EN	R/W		0x0
3	CH1_INTR1_EN	R/W		0x0
2	CH1_INTR0_EN	R/W		0x0
1	CH0_INTR1_EN	R/W		0x0
0	CH0_INTR0_EN	R/W		0x0

2.28.1.80 Interrupt Status

Short Name:INTR_STAT

Addresses:0x1EF260 - 0x1EF263

Table 1799 • **Interrupt Status**

Bit	Name	Access	Description	Default
20	GPIO_INTR_STAT	R/O		0x0
19	CLK_MUX_INTR_STAT	R/O		0x0
18	EXP4_INTR_STAT	R/O		0x0
17	LCPLL_1_INTR_STAT	R/O		0x0
16	LCPLL_0_INTR_STAT	R/O		0x0
15	IP1588_1_INTR3_STAT	R/O		0x0
14	IP1588_1_INTR2_STAT	R/O		0x0
13	IP1588_1_INTR1_STAT	R/O		0x0
12	IP1588_1_INTR0_STAT	R/O		0x0
11	IP1588_0_INTR3_STAT	R/O		0x0
10	IP1588_0_INTR2_STAT	R/O		0x0
9	IP1588_0_INTR1_STAT	R/O		0x0
8	IP1588_0_INTR0_STAT	R/O		0x0
7	CH3_INTR1_STAT	R/O		0x0
6	CH3_INTR0_STAT	R/O		0x0
5	CH2_INTR1_STAT	R/O		0x0
4	CH2_INTR0_STAT	R/O		0x0
3	CH1_INTR1_STAT	R/O		0x0
2	CH1_INTR0_STAT	R/O		0x0
1	CH0_INTR1_STAT	R/O		0x0
0	CH0_INTR0_STAT	R/O		0x0