Table 19. NUCLEO-F746ZG, NUCLEO-F756ZG and NUCLEO-F767ZI pin assignments

Connector	Pin	Pin name	Signal name	STM32 pin	Function	Remark
		<u>l</u>	Left conne	ctors		
	1	NC	NC		-	ARDUINO® support
	3	IOREF	IOREF	-	3.3 V Ref	
	5	RESET	RESET	NRST	RESET	
	7	+3.3 V	+3.3 V		3.3 V input/output	
	9	+5 V	+5 V		5 V output	
	11	GND	GND	-	ground	
	13	GND	GND		ground	
	15	V _{IN}	V _{IN}		Power input	
CN8	2	D43	SDMMC_D0	PC8		
	4	D44	SDMMC_D1/ I2S_A_CKIN	PC9	SDMMC/I2S_A	
	6	D45	SDMMC_D2	PC10		
	8	D46	SDMMC_D3	PC11		-
	10	D47	SDMMC_CK	PC12		
	12	D48	SDMMC_CMD	PD2		
	14	D49	I/O	PG2		
	16	D50	I/O	PG3	1/0	
	1	A0	ADC	PA3	ADC123_IN3	ARDUINO [®] support
	3	A1	ADC	PC0	ADC123_IN10	
	5	A2	ADC	PC3	ADC123_IN13	
	7	А3	ADC	PF3	ADC3_IN9	
CN9	9	A4	ADC	PF5 or PB9 ⁽¹⁾	ADC3_IN15 (PF5) or I2C1_SDA (PB9)	
	11	A5	ADC	PF10 or PB8 ⁽¹⁾	ADC3_IN8 (PF10) or I2C1_SCL (PB8)	
	13	D72	NC	-	-	
	15	D71	I/O	PA7 ⁽²⁾	I/O	
	17	D70	I2C_B_SMBA	PF2		
	19	D69	I2C_B_SCL	PF1	I2C_2	-
	21	D68	I2C_B_SDA	PF0		
	23	GND	GND	-	ground	
	25	D67	CAN_RX	PD0	CAN_1	

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Table 19. NUCLEO-F746ZG, NUCLEO-F756ZG and NUCLEO-F767ZI pin assignments (continued)

Connector	Pin	Pin name	Signal name	STM32 pin	Function	Remark
	27	D66	CAN_TX	PD1	CAN_1	
	29	D65	I/O	PG0	I/O	
	2	D51	USART_B_SCLK	PD7		
	4	D52	USART_B_RX	PD6	USART_2	
	6	D53	USART_B_TX	PD5		
CN9	8	D54	USART_B_RTS	PD4		
	10	D55	USART_B_CTS	PD3		
	12	GND	GND	-	ground	
	14	D56	SAI_A_MCLK	PE2 ⁽³⁾		-
	16	D57	SAI_A_FS	PE4	SAI_1_A	
	18	D58	SAI_A_SCK	PE5		
	20	D59	SAI_A_SD	PE6		
	22	D60	SAI_B_SD	PE3		
	24	D61	SAI_B_SCK	PF8	CAL 4 D	
	26	D62	SAI_B_MCLK	PF7	SAI_1_B	
	28	D63	SAI_B_FS	PF9		
	30	D64	I/O	PG1	I/O	



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Table 19. NUCLEO-F746ZG, NUCLEO-F756ZG and NUCLEO-F767ZI pin assignments (continued)

pin accignments (commuca)						
Connector	Pin	Pin name	Signal name	STM32 pin	Function	Remark
Right Connectors						
	1	D16	I2S_A_MCK	PC6		
	3	D17	I2S_A_SD	PB15	126. 2	
	5	D18	I2S_A_CK	PB13 ⁽⁴⁾		
	7	D19	I2S_A_WS	PB12		
	9	D20	I2S_B_WS	PA15		
CN7	11	D21	I2S_B_MCK	PC7		-
	13	D22	I2S_B_SD/ SPI_B_MOSI	PB5	12S 3/SPI3	
	15	D23	I2S_B_CK/ SPI_B_SCK	PB3	123_37 3513	
	17	D24	SPI_B_NSS	PA4		
	19	D25	SPI_B_MISO	PB4		
	2	D15	I2C_A_SCL	PB8	I2C1_SCL	ARDUINO [®] support
	4	D14	I2C_A_SDA	PB9	I2C1_SDA	
	6	AREF	AREF		AVDD/VREF+	-
	8	GND	GND	_	ground	

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Table 19. NUCLEO-F746ZG, NUCLEO-F756ZG and NUCLEO-F767ZI pin assignments (continued)

Connector	Pin	Pin name	Signal name	STM32 pin	Function	Remark
	10	D13	SPI_A_SCK	PA5	SPI1_SCK	
	12	D12	SPI_A_MISO	PA6	SPI1_MISO	
	14	D11	SPI_A_MOSI/ TIM_E_PWM1	PA7 ⁽¹⁾⁽²⁾ or PB5 ⁽¹⁾	SPI1_MOSI/ TIM14_CH1	
CN7	16	D10	SPI_A_CS/ TIM_B_PWM3	PD14	SPI1_CS/ TIM4_CH3	
	18	D9	TIMER_B_PWM2	PD15	TIM4_CH4	
	20	D8	I/O	PF12	-	
	1	AVDD	AVDD	-	Analog VDD	
	3	AGND	AGND	-	Analog ground	
	5	GND	GND	-	ground	
	7	A6	ADC_A_IN	PB1	ADC12_IN9	
	9	A7	ADC_B_IN	PC2	ADC123_IN12	_
	11	A8	ADC_C_IN	PF4	ADC3_IN14	
	13	D26	QSPI_CS	PB6	QSPI_BK1	
	15	D27	QSPI_CLK	PB2	QSPI_CLK	
	17	GND	GND	-	ground	
	19	D28	QSPI_BK1_IO3	PD13		
	21	D29	QSPI_BK1_IO1	PD12	0001 014	
	23	D30	QSPI_BK1_IO0	PD11	QSPI_BK1	
	25	D31	QSPI_BK1_IO2	PE2 ⁽³⁾		
CN10	27	GND	GND	-	ground	
	29	D32	TIMER_C_PWM1	PA0	TIM2_CH1	
	31	D33	TIMER_D_PWM1	PB0	TIM3_CH3	
	33	D34	TIMER_B_ETR	PE0	TIM4_ETR	
	2	D7	I/O	PF13	-	
	4	D6	TIMER_A_PWM1	PE9	TIM1_CH1	
	6	D5	TIMER_A_PWM2	PE11	TIM1_CH2	
	8	D4	I/O	PF14	-	ARDUINO [®]
	10	D3	TIMER_A_PWM3	PE13	TIM1_CH3	support
	12	D2	I/O	PF15	-	
	14	D1	USART_A_TX	PG14	LICADTO	
	16	D0	USART_A_RX	PG9	USART6	
	18	D42	TIMER_A_PWM1N	PE8	TIM1_CH1N	
	20	D41	TIMER_A_ETR	PE7	TIM1_ETR	-

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Table 19. NUCLEO-F746ZG, NUCLEO-F756ZG and NUCLEO-F767ZI pin assignments (continued)

Connector	Pin	Pin name	Signal name	STM32 pin	Function	Remark
CN10	22	GND	GND	-	ground	
	24	D40	TIMER_A_PWM2N	PE10	TIM1_CH2N	
	26	D39	TIMER_A_PWM3N	PE12	TIM1_CH3N	
	28	D38	I/O	PE14	I/O	-
	30	D37	TIMER_A_BKIN1	PE15	TIM1_BKIN1	
	32	D36	TIMER_C_PWM2	PB10	TIM2_CH3	
	34	D35	TIMER_C_PWM3	PB11	TIM2_CH4	

- 1. For more details refer to Table 12: Solder bridges.
- PA7 is used as D11 and connected to CN7 pin 14 by default, if JP6 is ON, it is also connected to both Ethernet PHY as RMII_DV and CN9 pin 15. In this case only one function of the Ethernet or D11 must be used.
- 3. PE2 is connected to both CN9 pin 14 (SAI_A_MCLK) and CN10 pin 25 (QSPI_BK1_IO2). Only one function must be used at one time.
- 4. PB13 is used as I2S_A_CK and connected to CN7 pin 5 by default, if JP7 is ON, it is also connected to Ethernet PHY as RMII_TXD1. In this case only one function of the Ethernet or I2S_A must be used.

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