Joey Ah-kiow

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Education

University of Calgary Sept. 2018 – Present
B.Sc. in Electrical Engineering, GPA 3.75 Expected Graduation: May 2023

- Minor in Computer Engineering
- Relevant coursework: Digital Systems Design, Data Structures and Algorithms, Principles of Software Development

Experience

University of Calgary Calgary, AB
Research Assistant Feb. 2022 – Present

- Working in the domain of hardware security in Dr. Benjamin Tan's research group
- Collaborating with PhD students from NYU to explore possible security implications of High-Level Synthesis (HLS) for digital hardware design
- Developing HLS-synthesizable C/C++ code and reviewing resulting RTL design with manual inspection and simulation to identify security concerns and possible mitigations at both the C/C++ and HDL level
- Exploring hardware security literature on state-of-the-art topics like IFT, fuzzing and security property mining
- Learned foundational security concepts such as confidentiality, integrity, availability, access control, and cryptography

TC Energy Calgary, AB
Field Data Program Management Intern May 2021 – Present

- Communicating with internal and external stakeholders to ensure adherence to official specifications and provide support
- Reviewing and correcting NDE inspection data quality using SQL scripts and manual corrections
- Created a Power BI report to visualize and easily identify issues in cathodic protection data, saving $180000 per year
- Automated the pre-population of web-based forms for integrity excavations, saving $400000 per year
- Developed a Python script to automate the data extraction of ~150 Excel-based forms, reducing manual effort by 80 hours

Canadian Natural Resources Limited (CNRL) Calgary, AB
Data Provisioning Intern May 2020 – Aug. 2020

- Implemented SQL scripts to load, transform, and correct data for internal stakeholders
- Developed two applications using C# and .NET 4.8 to automate (1) the deployment of SSRS reports, and (2) the management of our Tableau server groups and users

Projects

Hack@DAC 2022
IEEE Conference Competition May 2022 – June 2022

- Found 10 possible security bugs/concerns, exploits and mitigations in the Verilog/SystemVerilog code of the AES cores, register locks, CSR registers, access control registers and the JTAG debug modules
- Completed security verification of a compromised RISC-V SoC using manual code reviews and simulation with C code
- Reviewed the RISC-V unprivileged, privileged and debug specifications to understand and define security requirements
- Explored specifications and RTL implementations of common digital system modules such as AES cores, JTAG, AXI

Proximity-controlled System | GitHub
Course Project Jan. 2021 – Apr. 2021

- Designed and simulated a proximity-controlled system using VHDL and implemented on the Terasic DE10-Lite FPGA board
- Used an ADC to interface a proximity sensor and output the readings to seven-segment displays in voltage or distance
- Controlled the frequency of a buzzer and the brightness of an LED array from the proximity sensor output using PWM
- Averaged the last 256 sensor readings using a pipelined adder tree to smooth system input with minimal performance hit
- Developed self-checking VHDL testbenches for all modules to verify functional correctness

Skills

Programming: C, C++, VHDL, Verilog/SystemVerilog, Java, Python, C#, SQL, MATLAB
Hardware: FPGA, PIC, Arduino, MIPS, RISC-V
Software: LTSpice, NI Multisim, Git, Intel Quartus, ModelSim, Verilator, GTKWave, Intel HLS Compiler, Siemens Catapult HLS