Design Project 2 – "Ideal" Voltage Controlled Switches

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ELECENG 2EI4 – Electronic Devices and Circuits I

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Properties of an Ideal Switch

An ideal switch is a concept used in electrical engineering device that switches perfectly regardless of the conditions. In the scope of 2EI4, an ideal switch has four key properties (that we care about) that differentiates it from real switches, which have minor non-idealities such as internal resistance and leakage currents.

The first property is that an ideal switch has zero resistance and voltage drop when ON. When the switch is closed, it operates as a perfect conducting path between the two terminals (like a wire). The input voltage equals the output voltage, and the voltage drop across the switch is zero. This property makes the switch 100% efficient and ensures that no power is dissipated when traveling through the switch. The second property of an ideal switch is that it has infinite resistance and allows zero current flow when OFF. When the switch is open, it acts as a perfect insulator, not allowing any current to flow through it and ensuring complete isolation between the input and output terminals (preventing any leakage current). The third property is that an ideal switch can handle an unlimited voltage range at the input and output terminals. It can sustain any voltage level at both terminals while performing as intended and not breaking down. There is no limit to the amount of voltage applied across the switch, meaning it can be used in any design regardless of voltage levels. The final property is bidirectional conductivity. Unlike some real switches that can only conduct in one direction (such as diodes), an ideal switch allows current to flow in both directions equally when in the ON state. This characteristic is fundamental in circuits requiring current to reverse direction, particularly in AC applications.

These properties emphasize the importance of the ideal switch as a concept in circuit analysis and design. Real switches have some non-ideal behaviours such as finite ON resistance, leakage currents and voltage limitations. These factors must be considered in practical applications, making circuits that contain real switches significantly more challenging to design and troubleshoot.

Switch Non-Idealities

In real life, switches do not act like an open circuit when they are OFF and a short circuit when they are ON. Rather, real-life switches have non-idealities that lower their efficiency compared to the ideal switch. We cover four primary non-idealities for the purposes of this course.

The first non-ideality is the small internal resistance that exists when the switch is ON. An ideal switch has zero resistance and voltage drop across the terminals when its ON, but real switches all contain different internal resistances. This will cause a small but still significant voltage drop across the switch and power that is dissipated, which increases as the current increases. This imperfection can be quantified using the AD3 by either measuring or calculating the internal resistance of the switch or the voltage drop across its terminals. Small as these values are, they can impose a significant effect on the system and must be taken into account. The next non-ideality is the slight leakage current when a real switch is turned off. In an ideal switch, no current flows through it in the off state. This isn't the case for switches in real life because its impossible to make a switch have infinite resistance when its OFF, meaning a small amount of current (called leakage current) can still flow through it. The amount of leakage current is typically very small, but it can still have a meaningful effect on circuits, especially ones that are at low power. This non-ideality can be measured by using the AD3's oscilloscope to measure current flow through the switch when its off. This measurement indicates how well the switch is isolating the circuit when it is supposed to be off. The next non-ideality is the limited voltage real switches can handle. As previously mentioned, ideal switches preform as intended under any supply voltage, whereas real switches are limited to a range of voltages for them to work properly. If you go outside this range, the switch will stop working or even break. This non-ideality can be measured by increasing the voltage in which a switch operates in until it breaks down. The maximum voltage a switch can handle can be found in its data sheet and should always be checked when designing any circuit. For this project, we are already limited to a voltage range which ensures neither terminal is exceeding its limit. The final non-ideality is real switches do not have symmetrical ON resistance. An ideal switch behaves the same regardless of the direction of the current, but real switches internal resistance can vary slightly depending on which terminal ius used as an input. This can be measured by measuring the switches resistance while ON using the AD3 when current is flowing from V1 to V2 and vice versa.

These non-idealities are what make real switches much more challenging than ideal switches. An important takeaway of this project is understanding these imperfections and how to measure and minimize them in any design.

Test Plan – Switch Type 1:

As previously mentioned, a real switch has several non-idealities that affect the performance of real-life circuits. To quantify these non-idealities, iv have developed a test detailed test plan to measure my circuits performance.

For switch type 1, I set $V_{supply} = +5V$, $V_1 = +5V$, and $V_{control}$ as a square wave with an amplitude of 5V (oscillates between 0V and 5V), that operates at a frequency of 500mHz.

The first non-ideality is the small internal resistance of a real switch when it is in the ON state. This imperfection can be quantified by measuring the voltage at both the input (V_{in}) and output (V_{out}) terminals when $V_{control}$ is at 0V (switch is in the ON state). Using these measurements the voltage drop across the switch ($V_{in} – V_{out}$) can be calculated. The internal resistance of the switch can then be calculated ($R_{ON} = \frac{V_{in}-V_{out}}{I}$).

The next non-ideality is the small amount of leakage current when the switch is in the OFF state. This imperfection can be observed quantitatively by measuring the voltage at the output terminal of the switch (V_{out}) when $V_{control}$ is at 5V (switch is in the OFF state). The leakage current can then be calculated ($I_{OFF} = \frac{V_{out}}{R}$).

The third non-ideality is that real switches can only operate in a specific voltage range. This can be measured quantitatively by using a ramp function of 0V to 5V and inputting it to the supply voltage (V_{supply}). The range at which the switch operates as intended can be observed by finding what supply voltage the switch starts to behave unexpectedly.

The fourth and final non-ideality is that real switches can not conduct symmetrically, as R_{ON} is not equal in both directions. This could be quantified by measuring voltage drop across the ON switch from both terminals and dividing this by the current to compare R_{ON} in both directions. However, this is not necessary as the calculations done when quantifying the first two non-idealities prove that real switches aren't symmetrical due to the varying internal resistance and leakage current of real switches.

Test Plan - Switch Type 2:

The test plan for switch type 2 is very similar to that of switch type 1. For switch type 2, I also set $V_{supply} = +5V$, $V_1 = +5V$, and $V_{control}$ as a square wave with an amplitude of 5V (oscillates between 0V and 5V), that operates at a frequency of 500mHz. This initial setup remains the same for both switch types.

The first non-ideality is the small internal resistance of a real switch when it is in the ON state. This imperfection can be quantified by measuring the voltage at both the input (V_{in}) and output (V_A and V_B) terminals when $V_{control}$ is at 0V (switch is in the ON state). Using these measurements the voltage drop across the switch and its internal resistance can be calculated using the same formula as for switch type 1.

The next non-ideality is the small amount of leakage current when the switch is in the OFF state. This imperfection can be observed quantitatively by measuring the voltage at the output terminals of the switch (V_A and V_B) when $V_{control}$ is at 5V (switch is in the OFF state). The leakage current can then be calculated using the same formula as for switch type 1.

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Switch Type 1

Figure 1 shows my circuit schematic for switch 1, which uses P-channel and N-channel MOSFET's. This design allows the switch to control connection between the supply voltage and the load resistor based on the state of the control voltage. This creates an efficient switching device which has minimal power being dissipated.

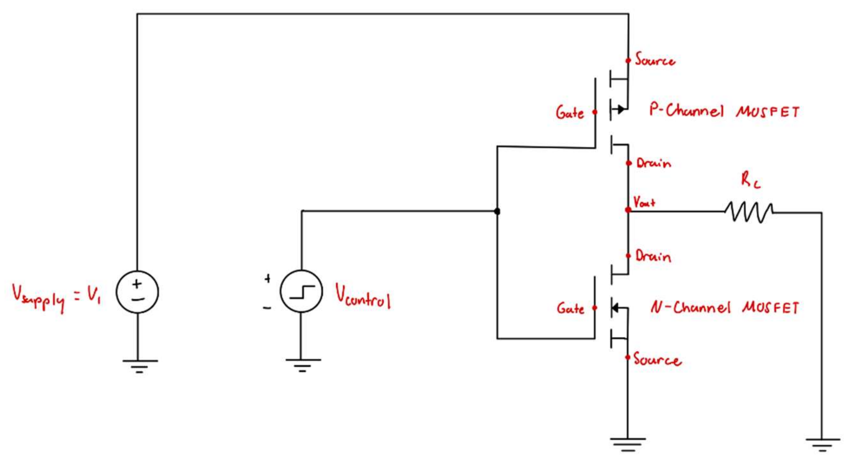

Figure 1: Switch Type 1 –Circuit Schematic

LTspice Simulation – Circuit and Results:

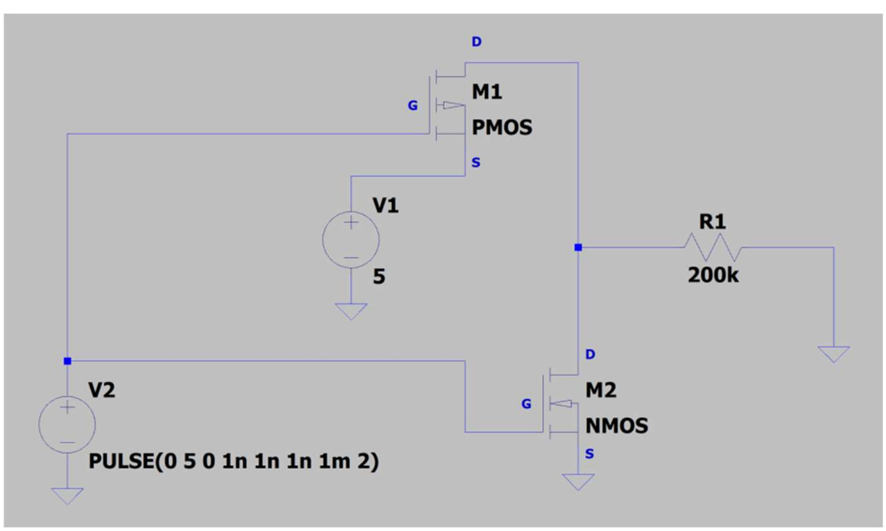

Figure 2: Switch Type 1: LTspice Circuit Schematic

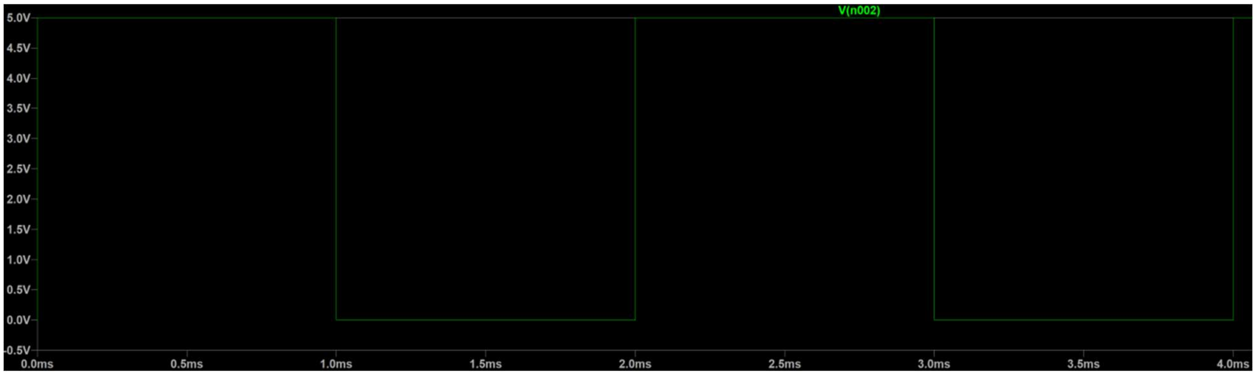

Figure 3: LTspice Simulation - Measured Control Voltage ($V_{control}$)

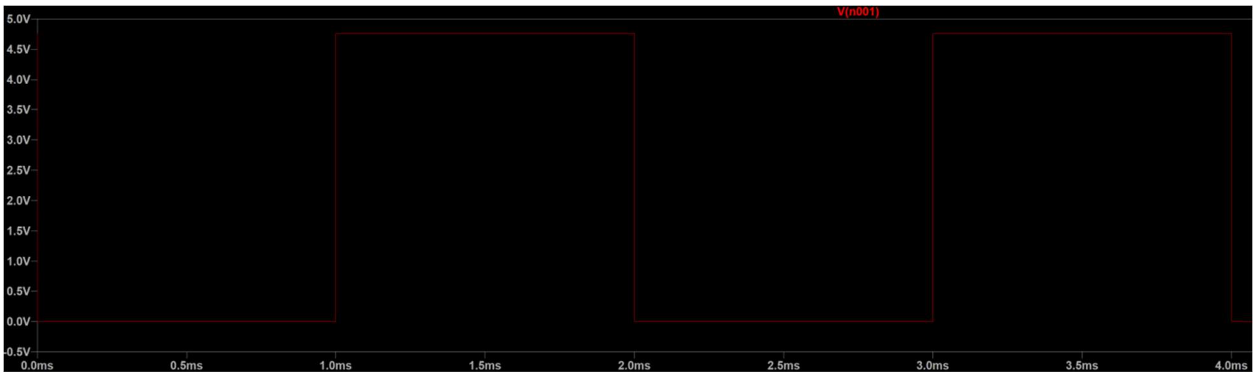

Figure 4: LTspice Simulation - Measured Output Voltage (V_{out})

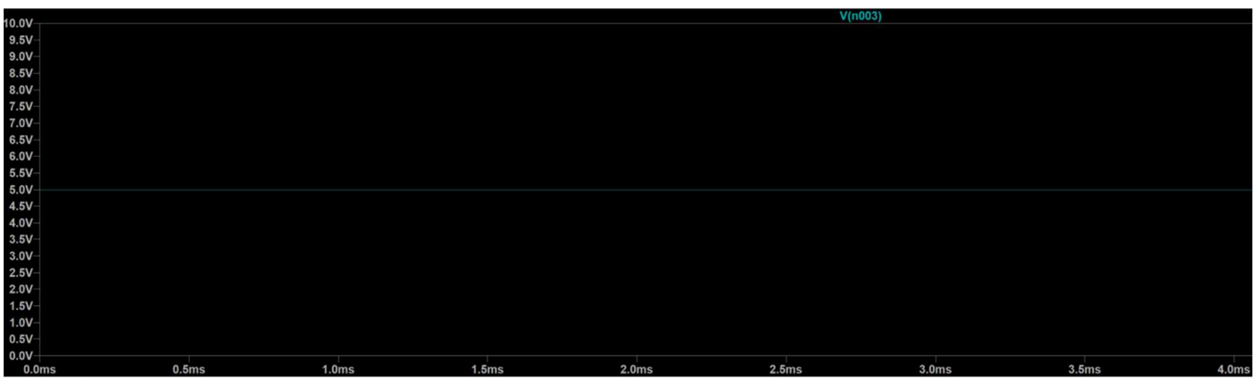

Figure 5: LTspice Simulation - Measured Supply Voltage (V_1)

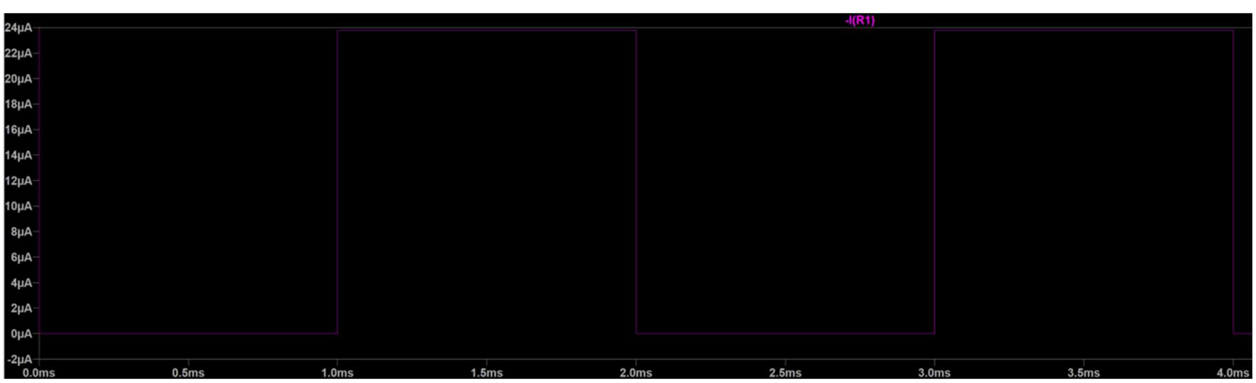

Figure 6: LTspice Simulation - Measured Current Through Switch (I_{OFF} when $V_{control}$ = 5V)

Theoretical Calculations:

Voltage Drop & Resistance in the ON State ($V_{control}$ = 0V, switch is closed):

For the N-channel MOSFET:

Threshold Voltage = $V_{T1} = 1.75V$, Transductance Parameter = $K = 7.7\mu A/V$ [1]

$V_{GS1} = 0V$, $V_{GS1} \leq V_{T1}$, ==> NMOS is in the cutoff region (drain current = $I_{DS} = 0mA$)

For the P-channel MOSFET:

Threshold Voltage = $V_{T2} = 1.7V$, Transductance Parameter = $K = 4.4\mu A/V$ [1]

$V_{SG2} = 5V$, $V_{SG2} > V_{T2}$, ==> PMOS is active (either in saturation or linear mode)

Assuming Saturation (as instructed in lecture):

$$I_{D2} = \frac{K}{2} * (V_{SG2} - V_T)^2$$

$$I_{D2} = \frac{4.4 * 10^{-6}}{2} * (5 - 1.7)^2$$

$$I_{D2} = 2.39 * 10^{-5} A$$

Now, with the current I_{D2} , V_{OUT} (which is equal to V_{SD2}) can be calculated using Ohm's law with $R_L = 200K\Omega$:

$$V_{OUT} = V_{SD2} = I_{D2} * R_L$$

$$V_{OUT} = (2.39 * 10^{-5}) * (200000)$$

$$V_{OUT} = 4.79V$$

Therefore, the theoretical voltage drop across the switch when ON is calculated as:

$$V_{IN} - V_{OUT} = 5V - 4.79V = 0.21V$$

This indicates an internal resistance of:

$$R_{ON} = \frac{(V_{IN} - V_{OUT})}{I_{D2}} = \frac{0.21V}{2.39 * 10^{-5}} = 8.787K\Omega$$

The power dissipated can also be found:

$$\mathrm{P} = I^2{}_{D2} * R_{ON} = (2.39 * 10^{-5})^2 * (8787) = 5.019\mu W$$

Figure 7: Theoretical Calculations for Voltage Drop Across the Switch

Leakage Current in the OFF State ($V_{control}$ = 5V, switch is open):

For the P-channel MOSFET:

$$V_{SG} = V_{source} - V_{gate} = 5V - 5V = 0V$$

The PMOS stays in the cutoff region when:

$$V_{SG} \leq V_{T2} \text{ },0V \leq 1.7V$$

Since this condition holds true, the drain current is:

$$I_{DS} = 0A$$

Figure 8: Theoretical Calculations for Leakage Current

Voltage Supply Limits:

In the ON State (Switch is Closed, $V_{control}$ = 0V):

The P-channel MOSFET must operate in saturation. For Saturation to hold:

$$V_{SD2} \geq V_{SG2} - V_{T2}$$

$$V_{SD2} \geq 5V - 1.7V$$

$$V_{SD2} \geq 3.3V$$

Therefore, the voltage across the PMOS from source to drain must be at least 3.3V to maintain saturation.

In the OFF State (Switch is Open, $V_{control}$ = 5V):

For the P-channel MOSFET to remain completely OFF, it must be in the cutoff region The condition for cutoff to hold is:

$$V_{SG2} \leq V_{T2}$$

$$V_{S2} - V_{G2} \leq 1.7V$$

$$V_{S2} \leq 1.7V + 5V$$

$$V_{S2} \leq 6.7V$$

Therefore, for the PMOS to remain in cutoff, the supply voltage must be less than or equal to 6.7V. However, this project limits the supply voltage to 5V, so this value will be used for the upper limit.

Figure 9: Theoretical Calculations for the Voltage Supply Range

The theoretical calculations preformed above confirm the results found by the LTspice simulation. The voltage drop of 0.21V across the switch, calculated in Figure 7, can be observed in Figure 4, which shows the output voltage when the switch is ON to be slightly less than the input of 5V. The 0A of leakage current, calculated in Figure 8, can be observed in Figure 6, which shows the current through the load resistor to be 0A when the switch is OFF. Finally, the voltage range calculated in Figure 9 is respected in Figure 5, which shows the supply voltage is constantly set to 5V.

Physical Circuit:

After the completion of the LTspice simulation and theoretical calculations confirming the switch's behaviours, I constructed the physical switch circuit. This section covers the real-world performance of the switch and compares the observed behaviour to the simulation results to assess the switch's behaviour under real conditions. Figure 10 shows the physical implementation of switch type 1.

The AD3 was used to provide the power supply, control signal and to measure the key voltages needed for observation or calculations. Figure 11 shows the Wavegen Settings used to power the circuit and Figure 12 shows the measured control voltage and output voltage, which verify the switch's functionality.

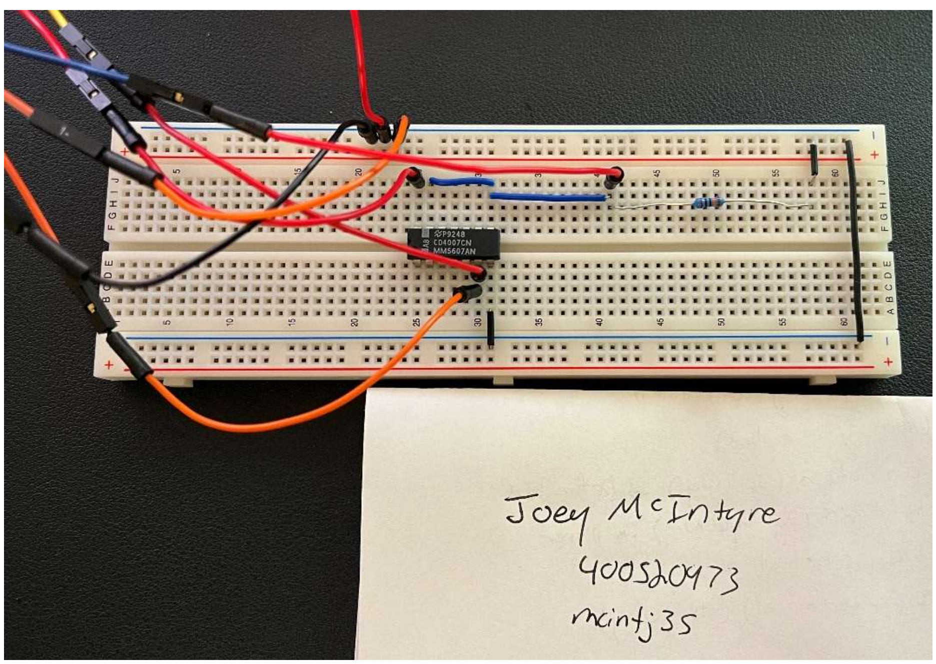

Figure 10: Physical Circuit - Switch Type 1

Figure 11: AD3 Wavegen Settings

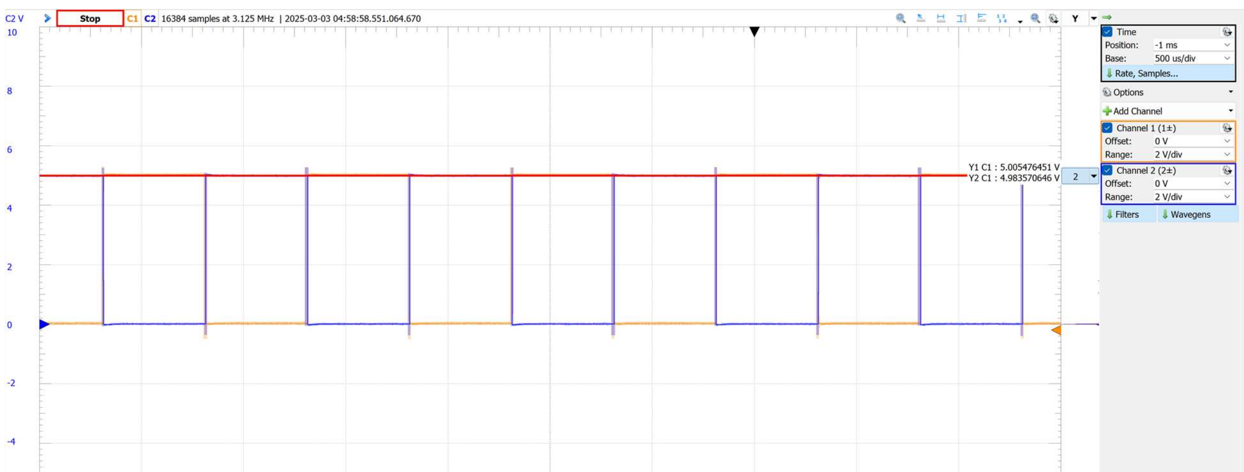

Figure 12: AD3 Measurements - Vcontrol (Orange) and Vout (Blue)

Experimental Measurements and Calculations:

After using the AD3 to gather measurements from the physical circuit, experimental calculations were preformed to quantitatively assess the performance of the switch. These calculations determine key parameters including the voltage drop across the switch, the resistance when ON, and the leakage current.

These values are then compared to the expected theoretical values to quantify the key non-idealities of a real switch and assess how accurately my physical switch can approximate the behaviour of an ideal switch.

Voltage Drop in the ON State ($V_{control}$ = 0V, switch is closed):

$$V_{IN} = 5.005V, V_{OUT} = 4.984V \text{ [Figure 12]}$$

The experimental voltage drop across the switch when ON is:

$$V_{SD} = V_S - V_D = V_{IN} - V_{OUT}$$

$$V_{SD} = 5.005V - 4.984V = 0.021\text{V}$$

Figure 13: Experimental Calculations for Voltage Drop Across the Switch

Leakage Current in the OFF State ($V_{control}$ = 5V, switch is open):

$$V_{OUT} = -11.3mV, R_L = 200k\Omega \text{ [Figure 12]}$$

The experimental leakage current when the switch is OFF can be calculated by:

$$I_{RL} = \frac{V_D}{R_L} = \frac{V_{OUT}}{R_L}$$

$$I_{RL} = \frac{0.0113V}{200000\Omega} = 5.65 * 10^{-8}A$$

Figure 14: Experimental Calculations for Voltage Drop Across the Switch

To evaluate the switch's operating range, a ramp voltage was used as the supply as shown in Figure 15. Figure 16 shows the outputted voltage when the switch is ON, and Figure 17 shows the outputted voltage when the switch is OFF, which allows the switch's operating range to be determined. According to Figure 16, the switch operates properly in the ON state when the supply voltage is within the range: $1.72 \leq V_{supply} \leq 5V$. According to Figure 17, the switch operates properly in the OFF state when the supply voltage is within the range $3.37 \leq V_{supply} \leq 5V$.

Figure 15: AD3 Wavegen Settings to Measure V_{supply} Range

Figure 16: V_{supply} Operating Range when ON ($V_{control}$ = 0V)

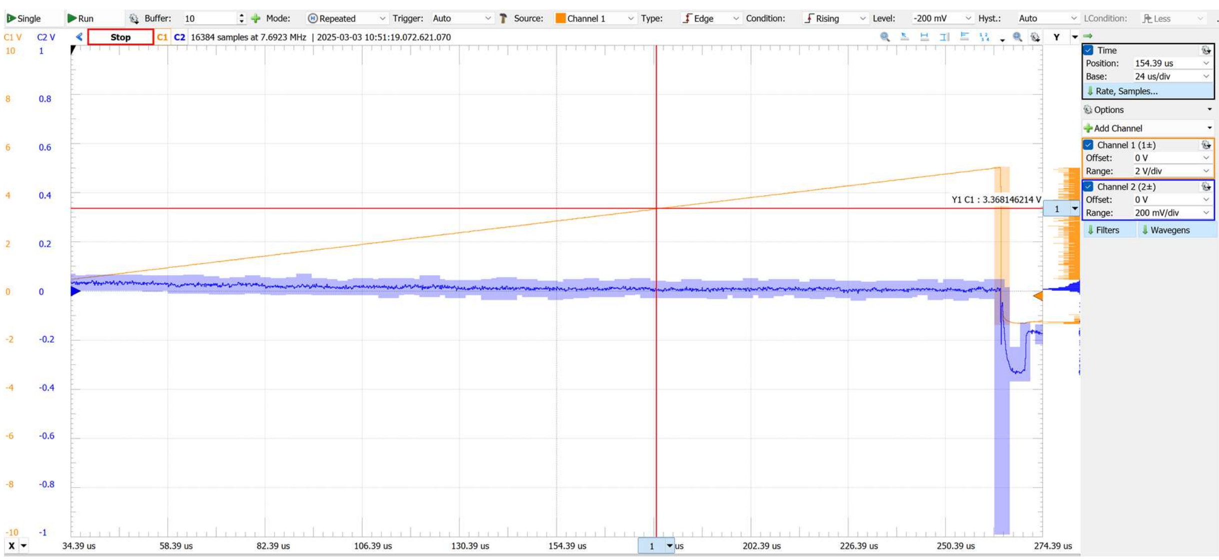

Figure 17: V_{supply} Operating Range when OFF ($V_{control}$ = 5V)

Experimental Results vs. Theoretical Results:

Comparing the experimental results collected with the AD3 to the theoretical calculations and the simulation confirms the accurate performance of my switch design while also quantifying the non-idealities that exist in a real switch.

When comparing the voltage drop when the switch is on, the experimental value of 0.021V is significantly lower than the theoretical value of 0.21V. This difference can be attributed to lower current than in testing and non-ideal conditions. This reduced voltage drop also implies that the real switch I made has a lower internal effective resistance under the test conditions than the theoretical simulated switch. Current leakage was calculated to be 0A in the theoretical ideal switch, the experimental leakage current was found to be 5.65µA. This is a relatively normal amount of leakage current from the MOSFETs used in the real circuit and is unavoidable under non-ideal conditions. The supply voltage range when the switch is ON was theoretically calculated to be $V_{supply} \geq 3.3V$, but the real switch operated over a wider range than predicted ($1.72V \leq V_{supply} \leq 5V$). This is likely due to the MOSFET entering saturation at a lower voltage than assumed. The supply voltage range when the switch is OFF was theoretically calculated to be $V_{supply} \leq 5V$, however the experimental results showed a range of $3.37V \leq V_{supply} \leq 5V$. This is likely due to a higher amount of voltage needed to make the real PMOS enter the cutoff region.

In summary, the experimental results align closely with the theoretical and simulated results. There are small deviations between the two due to the non-idealities of real-world scenarios, which is unavoidable given our limited resources. Overall, switch type 1 preforms within the acceptable parameters and meets all the projects design constraints.

Design Tradeoffs:

When designing switch type 1, several design tradeoffs had to be made to balance performance, complexity and cost. Tradeoffs are a important consideration in any real-world electrical engineering project. In an ideal scenario, performance, complexity and cost could all be maximized; however, this is simply unrealistic in real life. Tradeoffs must be made to find a good balance of all the important categories.

From a performance perspective, using P-channel and N-channel MOSFETs can provide reliable switching between the ON and OFF states, however this comes at a cost. The internal resistance of the MOSFETs cause a measurable voltage drop when the switch is in the ON state, and a small amount of leakage current when the switch is OFF. These non-idealities were minimized given the resources available in this course but cannot be fully eliminated. When it comes to complexity, my design only uses 2 MOSFETs and one load resistor, making it relatively straightforward. Adding additional components could reduce the non-idealities of the switch, but this would make the design and testing process much more difficult. From a cost standpoint, I designed my switch so that it could be built using components from the mandatory kits I have purchased for courses up to this point in my education. All these kits are relatively affordable, apart from the AD3.

Although this may not be the most efficient switch design in an ideal scenario, it is as cost efficient as possible, reliable, and optimized to the best of my abilities given the constraints.

Switch Type 2

The schematic shown in Figure 18 shows my design for switch type two. This design uses two P-channel MOSFETs and two N-channel MOSFETs to create an efficient switching device that accepts a control voltage, supply voltage, and returns two outputs. This design meets all of the design constraints listed in the Project 2 Instructions.

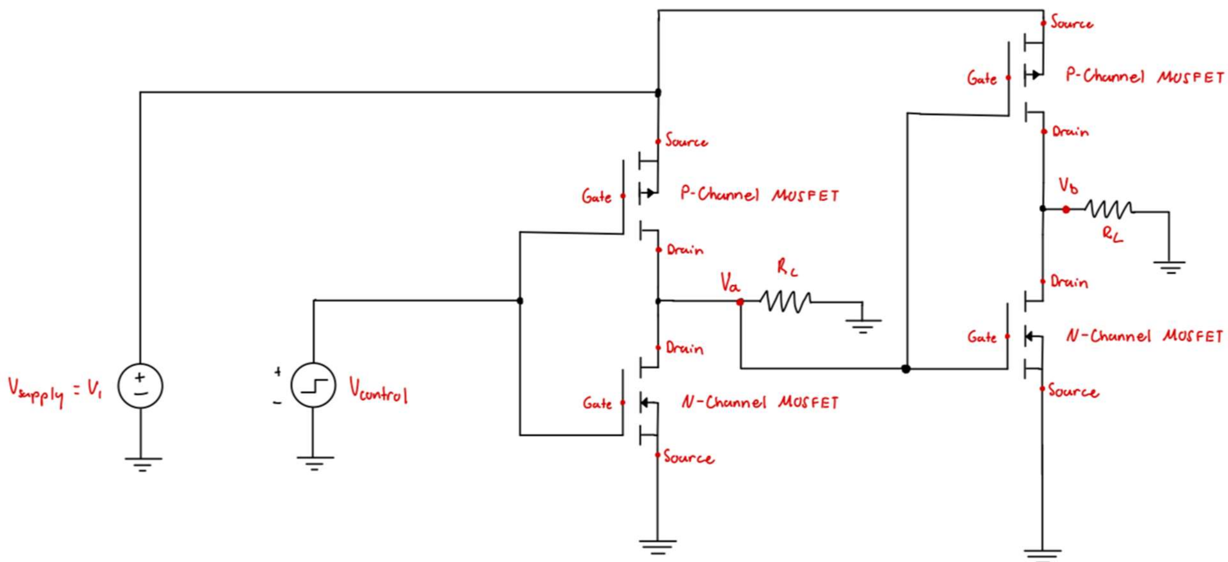

Figure 18: Switch Type 2 – Circuit Schematic

LTspice Simulation – Circuit and Results:

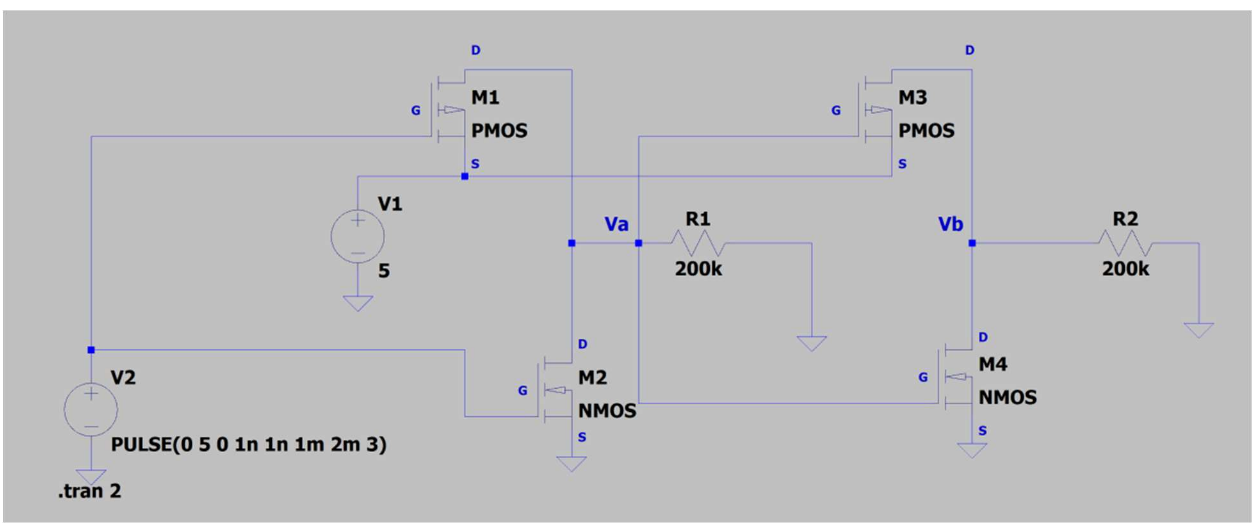

Figure 19: Switch Type 2: LTspice Circuit Schematic

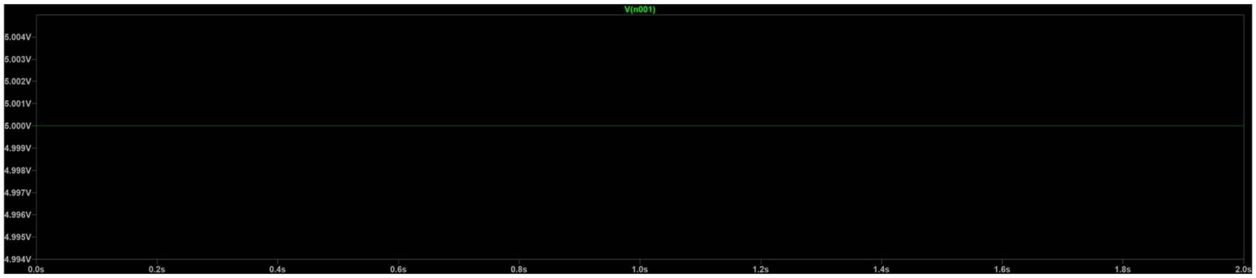

Figure 20: LTspice Simulation - Measured Supply Voltage (V1)

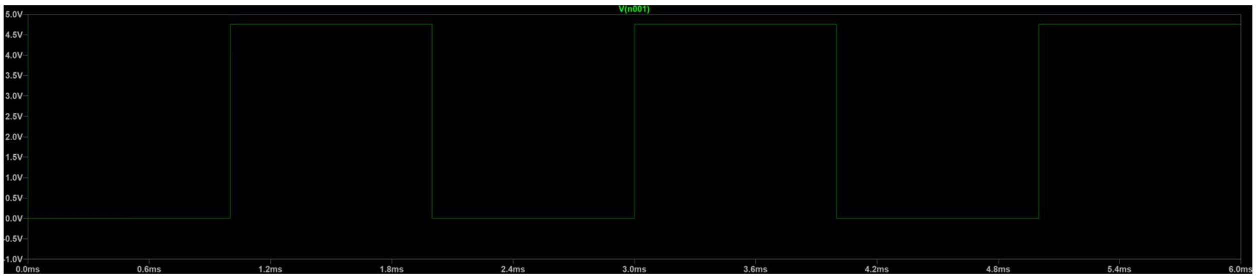

Figure 21: LTspice Simulation - Measured Output Voltage (V_A)

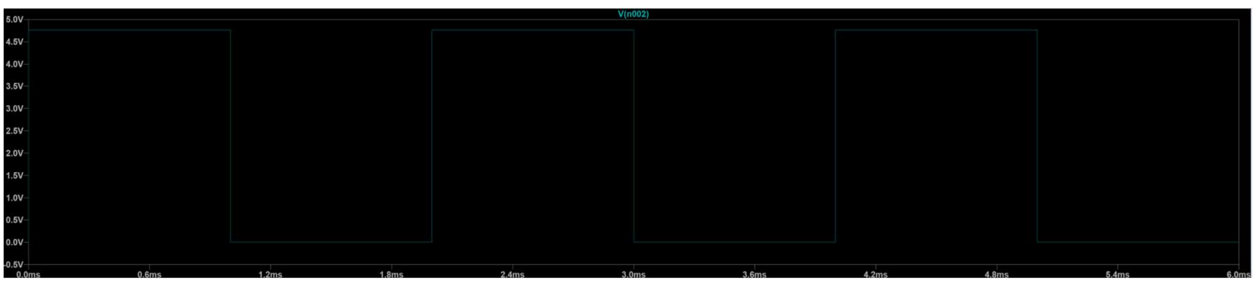

Figure 22: LTspice Simulation - Measured Output Voltage (V_B)

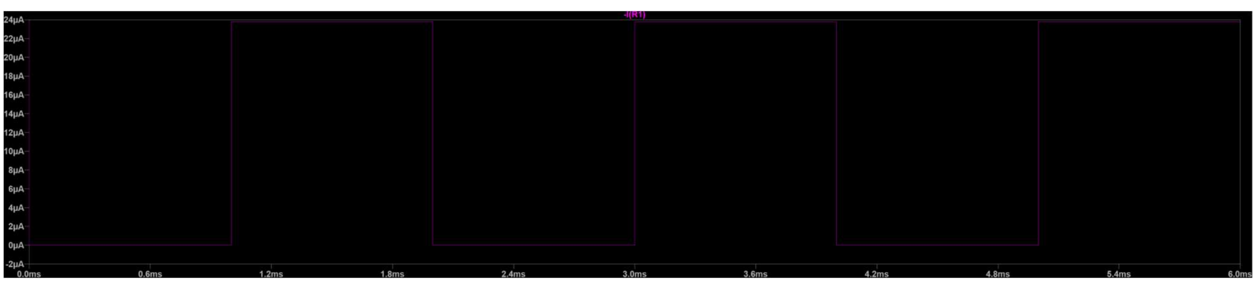

Figure 23: LTspice Simulation - Measured Current Load Resistor 1 (I_{OFF} when $V_{control}$ = 5V)

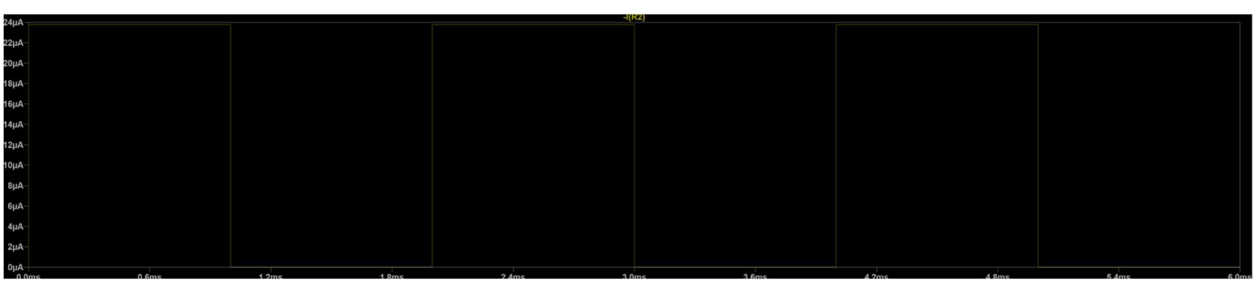

Figure 24: LTspice Simulation - Measured Current Load Resistor 2 (I_{OFF} when $V_{control}$ = 5V)

For theoretical calculations, refer to Figure 7, Figure 8, and Figure 9 as they either remain the same from switch type 1 or can be easily deduced.

Physical Circuit:

After completing the LTspice simulation of switch type 2, I built the phisical circuit using components from the course kit as well as the AD3. The design goal was to construct a device that behaves as a real-world switching device that has output V_A or V_B be as close to 5V as possible depending on the control signal. Figure 25 shows the physical circuit for switch type 2.

The AD3 was used to supply the supply voltage (5V), the control signal, and to measure key voltages using its built in oscilloscope. The Wavegen settings to achieve this are shown in Figure 26. The measured values of V_A and V_B from the AD3's oscilloscope are shown in Figure 27. These measurements help us verify that the switch is preforming as designed under real conditions. They provide an insight into how switch type 2 operates, and allow us to compare experimental results with theoretical results to identify non-idealities that exist in real components.

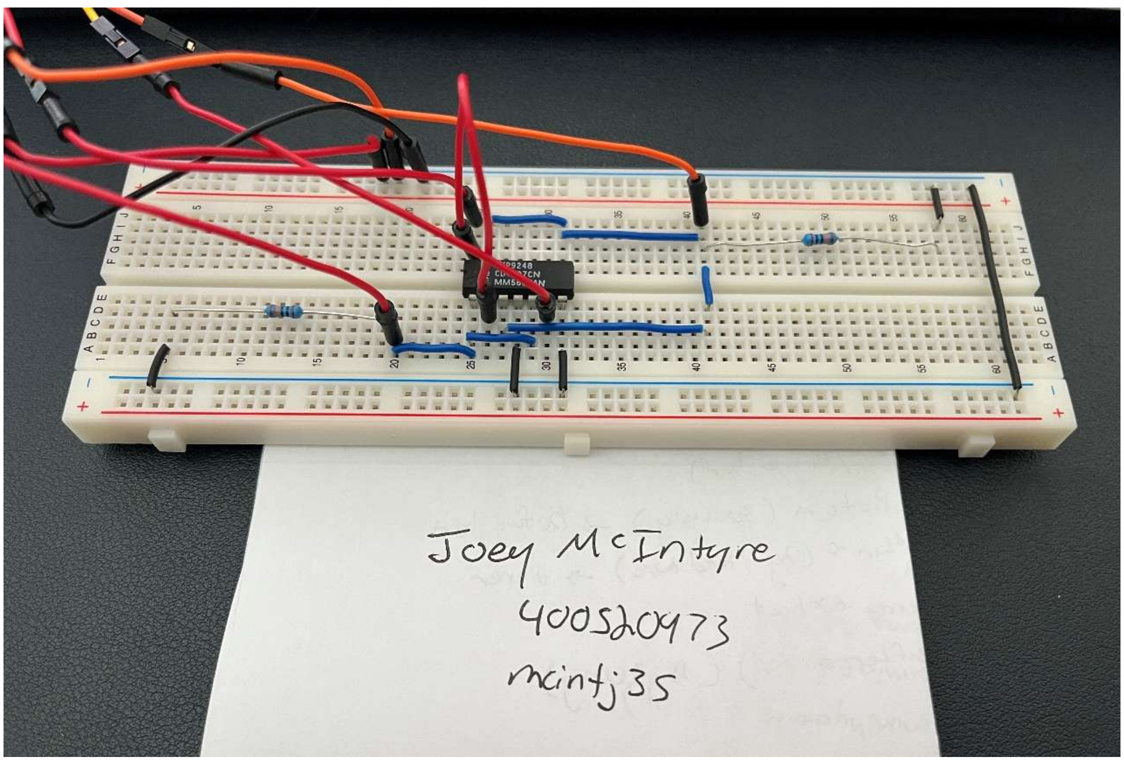

Figure 25: Physical Circuit – Switch Type 2

Figure 26: AD3 Wavegen Settings

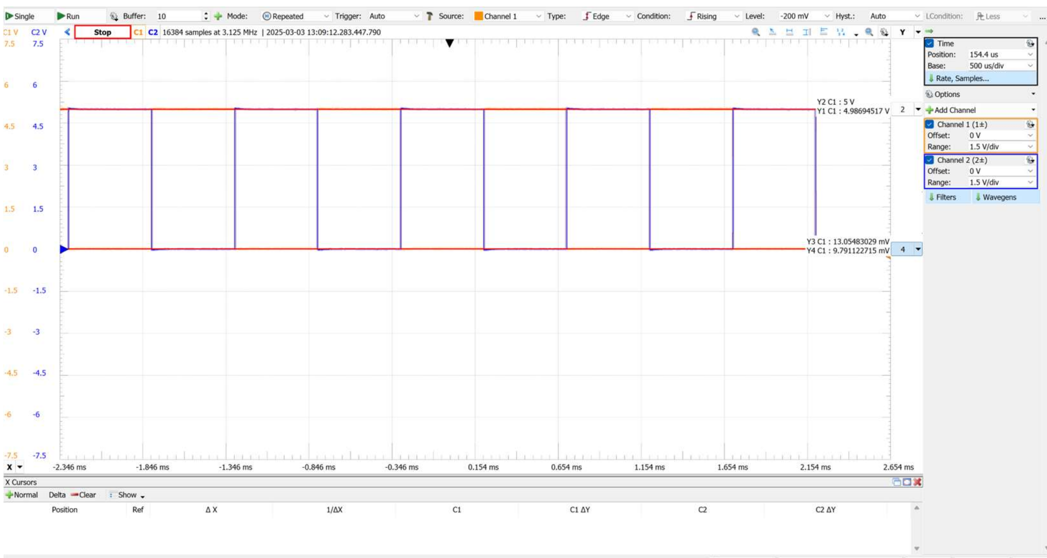

Figure 27: AD3 Measurements – V_A (Orange) and V_B (Blue)

Experimental Measurements and Calculations:

Following the collection of physical circuit measurements with the AD3, experimental calculations were carried out to evaluate the switch's performance quantitatively. The resistance when the switch is on, the voltage drop across the switch, and the leakage current are all determined by these calculations.

To measure the main non-idealities of a real switch and determine how well my physical switch can mimic the behavior of an ideal switch, these values are then compared to the predicted theoretical values.

Voltage Drop When V_A Conducts ($V_{control}$ = 0V):

$$V_{IN} = 5.005V, V_{OUT} = V_A = 5.000V \text{ [Figure 27]}$$

The experimental voltage drop across the switch is:

$$V_{SD} = V_S - V_D = V_{IN} - V_{OUT}$$

$$V_{SD} = 5.005V - 5.000V = 0.005\text{V}$$

Figure 28: Experimental Calculations for Voltage Drop Across the Switch When V_A Conducts

Voltage Drop When V_B Conducts ($V_{control}$ = 5V):

$$V_{IN} = 5.005V, V_{OUT} = V_B = 4.987 \text{ [Figure 27]}$$

The experimental voltage drop across the switch is:

$$V_{SD} = V_S - V_D = V_{IN} - V_{OUT}$$

$$V_{SD} = 5.005V - 4.987 = 0.018\text{V}$$

Figure 29: Experimental Calculations for Voltage Drop Across the Switch When V_B Conducts

Leakage Current when V_A Conducts ($V_{control}$ = 5V), (across second load resistor):

$$V_{OUT} = V_B = 13.055mV, R_L = 200k\Omega \text{ [Figure 27]}$$

The experimental leakage current can be calculated by:

$$I_{RL} = \frac{V_D}{R_L} = \frac{V_{OUT}}{R_L}$$

$$I_{RL2} = \frac{0.013055V}{200000\Omega} = 6.53 * 10^{-8}A$$

Figure 30: Experimental Calculations for Voltage Drop Across the Switch When V_A Conducts

Leakage Current when V_B Conducts ($V_{control}$ = 5V), (across first load resistor):

$$V_{OUT} = V_A = 9.791mV, R_L = 200k\Omega \text{ [Figure 27]}$$

The experimental leakage current can be calculated by:

$$I_{RL} = \frac{V_D}{R_L} = \frac{V_{OUT}}{R_L}$$

$$I_{RL1} = \frac{0.009791V}{200000\Omega} = 4.8955 * 10^{-8}A$$

Figure 30: Experimental Calculations for Voltage Drop Across the Switch When V_A Conducts

To evaluate the switch's operating range when V_A and V_B conduct, a ramp voltage was used as the supply. Figure 31 shows the outputted voltage when V_A conducts, and Figure 32 shows the outputted voltage when V_B conducts, which allows the switch's operating range to be determined. According to Figure 31, the switch operates properly in this state when the supply voltage is within the range: $1.75 \leq V_{supply} \leq 5V$. As observed in Figure 32, the switch operates properly in this state when the supply voltage is within the range $2.64 \leq V_{supply} \leq 5V$.

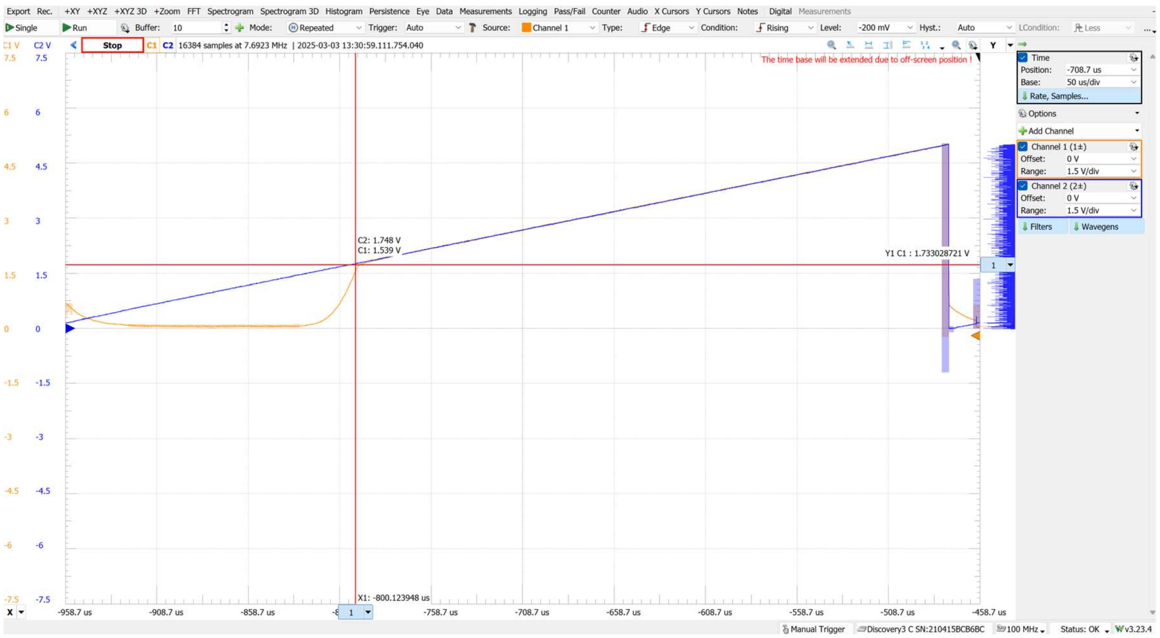

Figure 31: V_{supply} Operating Range when V_A Conducts

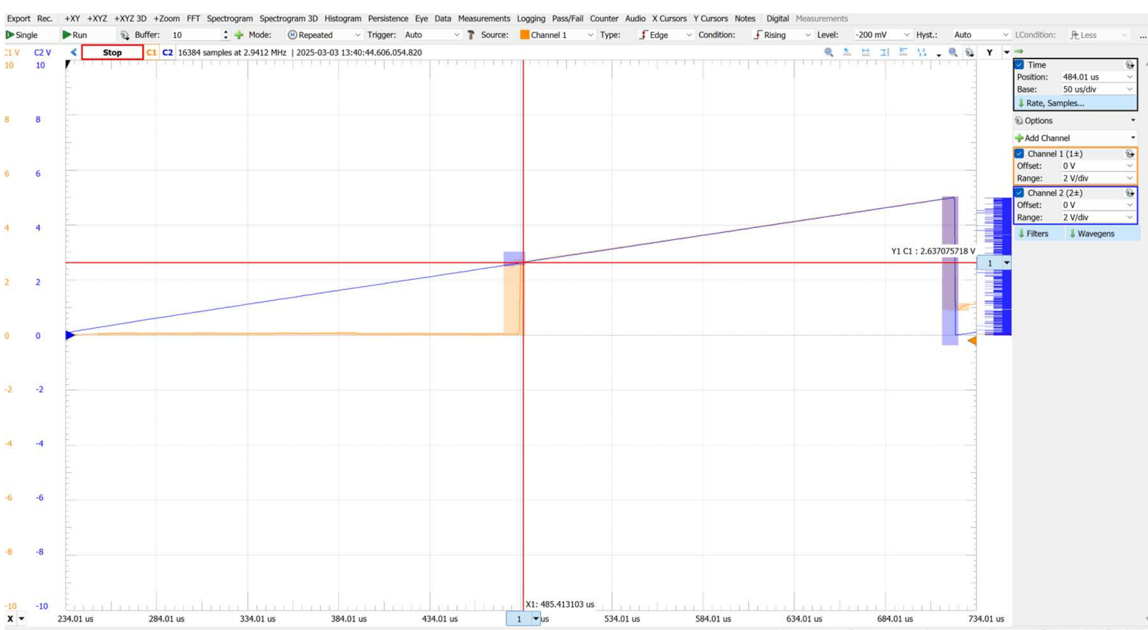

Figure 32: V_{supply} Operating Range when V_B Conducts

Experimental Results vs. Theoretical Results:

Comparing the theoretical measurements from switch type 2 to the theoretical expectations of its behaviour help us evaluate how well the switch is preforming and give a real-life example of the non-idealities we have researched.

Comparing the theoretically expected Voltage drop of 0.21V to the experimental voltage drop across V_A (0.005V) and V_B (0.018V), both are significantly smaller. This small voltage drop indicates a low internal resistance in the MOSFETs and is likely due to the small amount of current within this circuit. When observing the experimental leakage currents of 6.53µA and 4.90µA when V_A or V_B are conducting respectively, both values are slightly higher than the theoretically expected value of zero. The reality is, there will always be some leakage current that gets through real components because its impossible for them to have infinite resistance. These current values are both within an acceptable limit considering the components used in the circuit. The supply voltage range when V_A is conducting was expected to be when V_{supply} is greater than or equal to 3.3V. However, it was experimentally found that the switch preforms in this state when the supply voltage is within the range: $1.75 \leq V_{supply} \leq 5V$, which is slightly wider than expected. The supply voltage range when V_B is conducting was expected to be when $V_{supply} \leq 5V$, but it was found experimentally that the switch operates properly in this state when the supply voltage is within the range $2.64 \leq V_{supply} \leq 5V$. These observations are very similar to switch type 1. The supply voltage ranges are slightly off from what was expected, likely for the same reasons.

In summary, the data collected experimentally with the AD3 is very similar to the theoretical expectations. The minor derivations can be attributed to the non-idealities of switches we have covered in the scope of this course.

Design Tradeoffs:

Several design tradeoffs were made during the design process for switch type 2. The goal was to come up with a design that balances performance, complexity and cost. These are important metrics to consider in any project as they all influence each other, so a good design need to find a good balance between these categories. In terms of the design's performance, using the two sets of MOSFET pairs to make a switching device that switches from V_A and V_B as outputs depending on a control signal is fully functional. The switching between outputs is reliable and the voltage drops and leakage currents are quite low. In terms of complexity, compared to switch type 1, this design is slightly more complicated. It has double the number of components, however if you understand how switch type 1 works, switch type 2 should make sense as well as it uses the same concepts. This shows that my design is not only functional and relatively simple, but it can also be scaled. When considering costs, once again the entire design was built with the required kits for this course. All these components are very affordable, making my design very cost effective. In conclusion, this design for switch type 2 was proven to function very well, while being simple to understand and very cost effective, which means all my goals for this design project were met.

References

[1] “Lab,” *cmosedu.com*.
https://cmosedu.com/jbaker/courses/ee420L/s19/students/skellj1/lab8.htm