Design Project 4 – MOSFET Based XOR Gate

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ELECENG 2EI4 – Electronic Devices and Circuits I

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Circuit Schematic

The circuit schematic I designed for the MOSFET based XOR gate uses 12 MOSFET's in total. The pull-down network uses 4 NMOS transistors, the pull-up network uses 4 PMOS transistors, and the two inverters each use one NMOS and one PMOS transistor. I came to this decision using DeMorgan's Theorem and Boolean Algebra as we covered in lecture multiple times. The resulting Boolean Expression was calculated as shown in Figure 1.

$$Y = A \oplus B = A'B + B'A = (A'B + B'A)'' = ((A'B)' + B'A)')' = ((A + B') \cdot (B + A'))' = (AB + (AB)')$$

Figure 1: Derivation of the Boolean Expression for XOR

From the equation derived in Figure 1, I can deduce that the pull-down network needs to have A be in series with B which is parallel with A' and B' connected in series. The pull-up network is then implemented by mirroring this with PMOS transistors and switching the parallel and series networks.

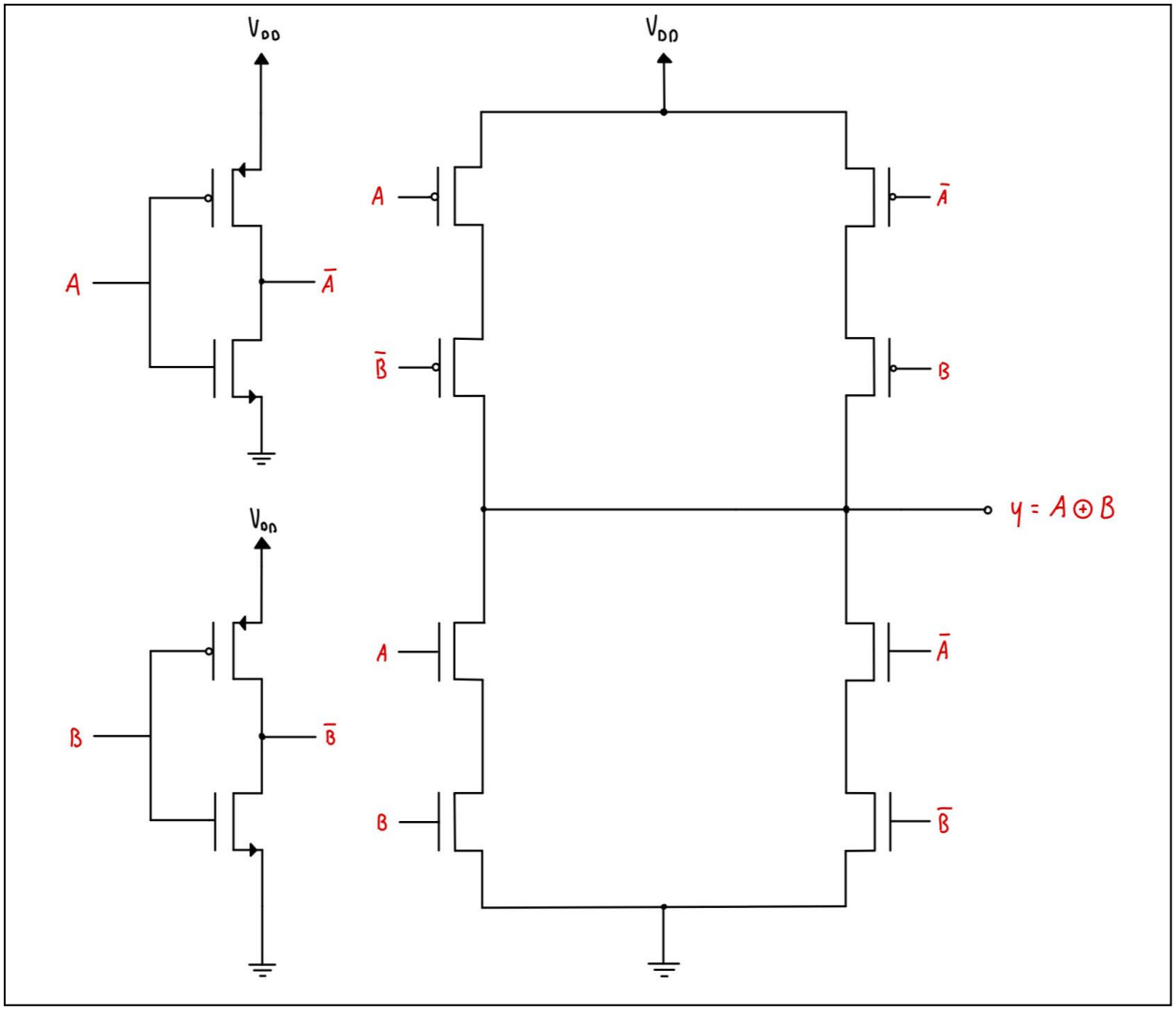

Figure 2: Circuit Schematic of CMOS XOR Gate and Inverter

Ideal Sizing

To ensure optimal performance for my MOSFET based XOR circuit, it is important to appropriately size the PMOS and NMOS transistors. PMOS devices conduct with holes, which are a lot slower than the electrons that are used in NMOS devices, which is why PMOS have to be wider to match the speed of the NMOS. As discussed in lecture, we know that the average sizing for a PMOS is $\left(\frac{W}{L}\right)_P = \frac{5}{1}$ and for NMOS is $\left(\frac{W}{L}\right)_N = \frac{2}{1}$. This demonstrated the mobility ratio between electrons and holes which is around 2.5, meaning NMOS transistors are about 2.5X faster than PMOS.

Looking at my circuit schematic, both the pull-up and pull-down networks have paths where two transistors are in series. This means that for the longest path, the effective resistance of the pull-down network will be $\frac{n}{2}$, and the pull-up network will be $\frac{p}{2}$. Using this information, we can calculate the sizing ratio between the PMOS and NMOS transistors as shown in Figure 3.

$$\text{PMOS: } \left(\frac{W}{L}\right)_P = \frac{5}{1} \text{NMOS: } \left(\frac{W}{L}\right)_N = \frac{2}{1}$$

$$\frac{2 * PMOS}{2 * NMOS} = \frac{5}{2} = 2.5$$

Figure 3: Ideal Sizing Ratio Between PMOS and NMOS MOSFET Types

Feasibility of Ideal Sizing

In my circuit, it can be observed that the longest part from VDD to ground is going through 2 PMOS transistors and 2 NMOS transistors. From this information, I can calculate the ideal sizing for my design to be $\frac{2*PMOS}{2*NMOS} = \frac{5}{2} = 2.5$. Since this is identical to the theoretical ideal sizing ration I calculated in the previous section, it is possible to implement ideal sizing in my hardware design.

Functional Testing

Utilizing the AD3s Digital IO pins, I was able to confirm my physical circuit's function. I had DIO 0 measure the input A, DIO 1 measure the input B, and DIO 2 measure the output voltage. The AD3s logic measurements in Figure 4 match the behaviour of an XOR gate as shown by the truth table in Figure 5, confirming that my circuit is functioning properly.

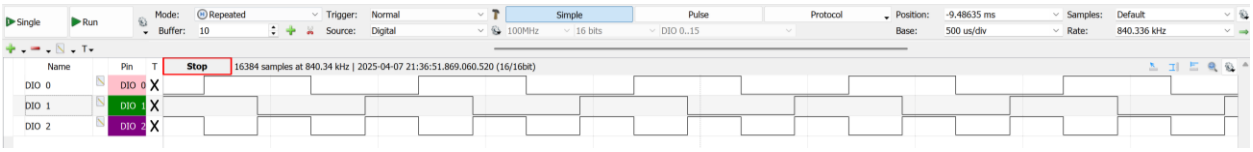

Figure 4: Functional Testing - Confirming XOR Logic Using AD3s Digital IO Pins

A	B	y
0	0	0
0	1	1
1	0	1
1	0	0

Figure 5: XOR Gate Truth Table

Figure 6 shows my physical circuit implementation of the MOSFET based XOR gate. The logic measurements using the AD3s Digital IO pins came from this circuit. The AD3 Waveform settings used to generate the inputs A and B are shown in Figure 7. The supply voltage V_{DD} was 5V.

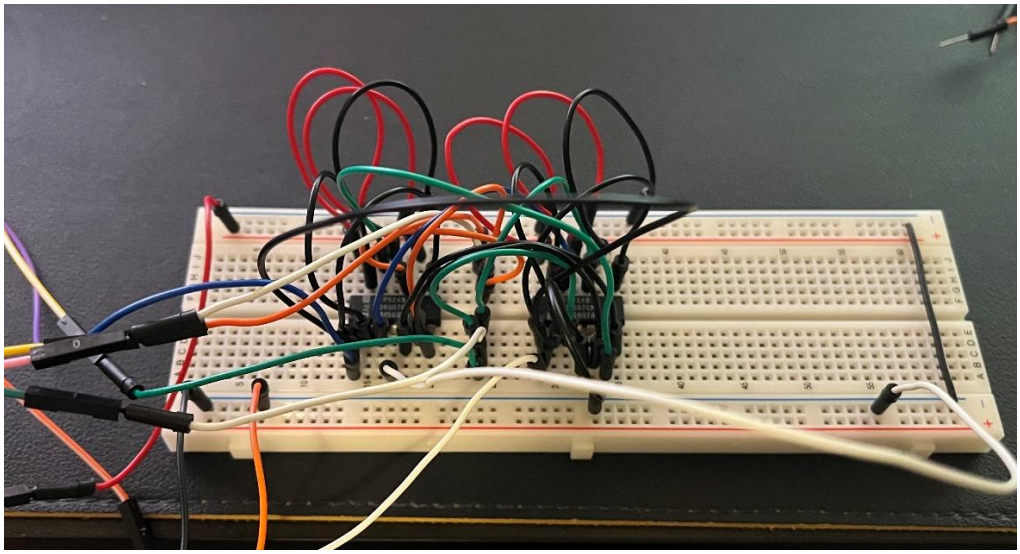

Figure 6: Physical Circuit of MOSFET based XOR Gate

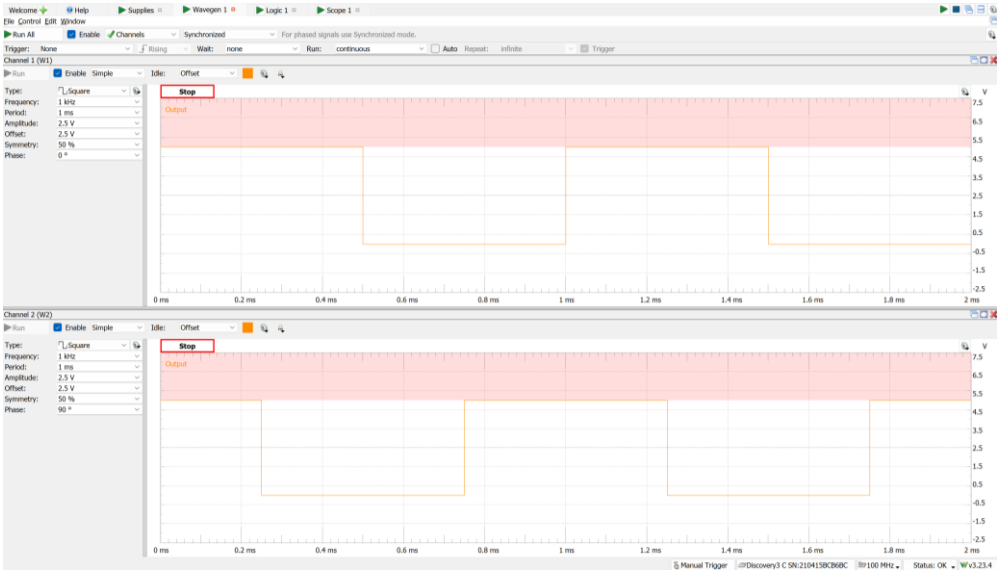

Figure 7: AD3 Wavegen Settings for Input Voltages A & B

Static Level Testing

For the first static level test, I set input A to logic-1 (+5V), and input B as a square wave between 0V and 5V. The measured output with the AD3s oscilloscope can be observed in Figure 8. Then I switched the inputs and measured the output again to determine whether this changes the outcome, which can be observed in Figure 9.

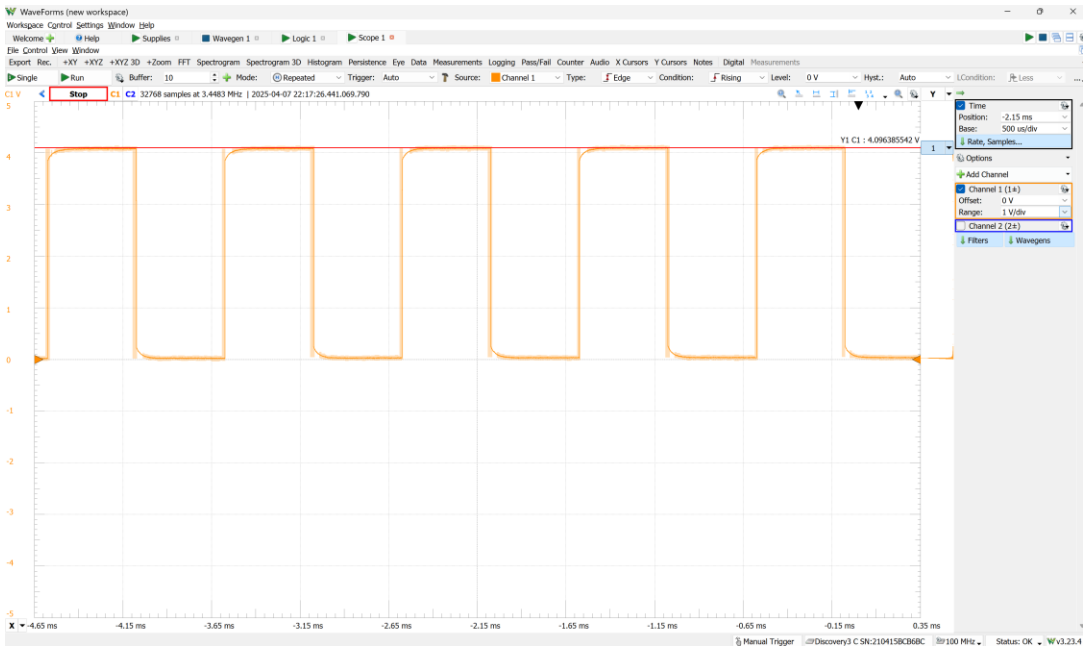

Figure 8: Static Level Testing: Input A Set to +5V, Input B Set to a 0-5V Square Wave

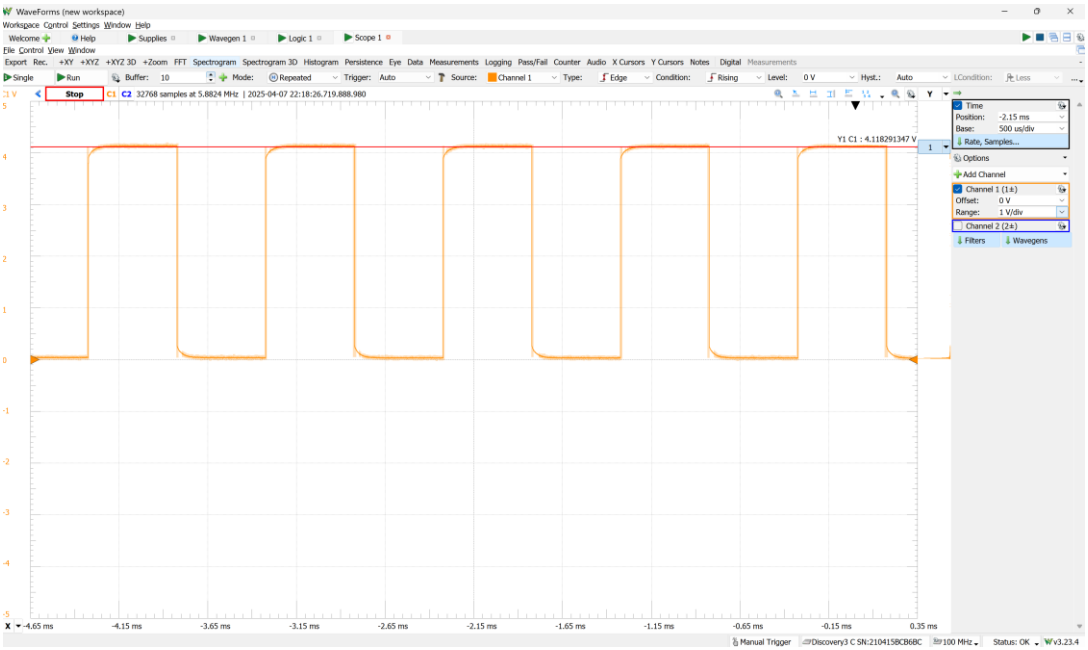

Figure 9: Static Level Testing: Input B Set to +5V, Input A Set to a 0-5V Square Wave

As observed in Figures 8 and 9, switching which input is set to logic high and which one is the square wave doesn't change the values of V_H or V_L in a significant manner. The slight variations can be attributed to small internal resistances of the components and wires in the physical circuit, and imperfect oscilloscope measurements from the AD3. The V_H was experimentally found to be approximately 4.10V, and the V_L was experimentally found to be 2.12mV.

Timing

For the timing aspect of this design project, I set input A to logic-1 (+5V), and input B as a square wave between 0-5V. Then, I connected a 100nF capacitor at the output to simulate a load as per the project specifications. Using the AD3s oscilloscope and cursors, I was able to determine the rise and fall times of the output waveform, as shown in Figure 10.

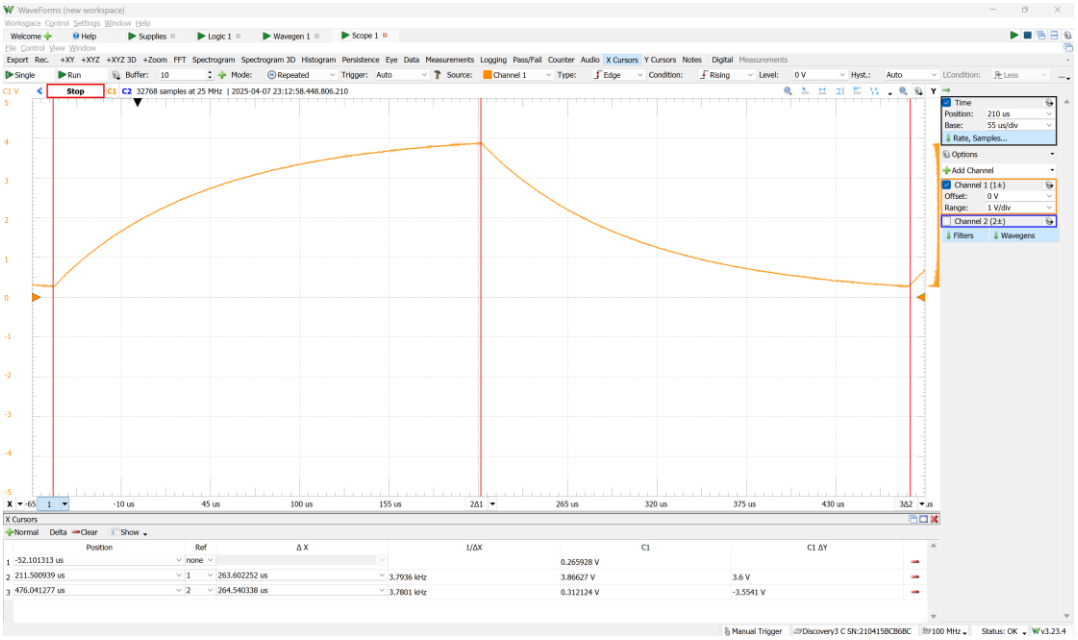

Figure 10: Rise and Fall Times

The rise time is found by measuring the time for the signal to go from 10% to 90% of its HIGH value. This was measured to be 242.1us. The fall time is found by measuring the time it takes for the signal to go from 90% to 10% of its final LOW value. The fall time was measured to be 243.5us.

Using the graph, I can also determine τ_{PLH}, τ_{PHL}, and τ_P. τ_{PLH} can be found by multiplying the rise time by 0.5: $\tau_{PLH} = 0.5(242.1\,us) = 121.05\,us$. τ_{PHL} can be found by multiplying the fall time by 0.5: $\tau_{PHL} = 0.5(243.5\,us) = 121.75\,us$. Finally, τ_P can be calculated by finding the average between the two previously calculated values: $\tau_P = 0.5(\tau_{PLH} + \tau_{PHL}) = 0.5(242.1 + 243.5) = 242.8\,us$.