Lab 4 – Feedback Circuits

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ELECENG 3EJ4 – Electronic Devices and Circuits II

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Part 1: Negative Feedback Amplifier

A. SPICE Simulation – Op-Amp Characterization

1.1

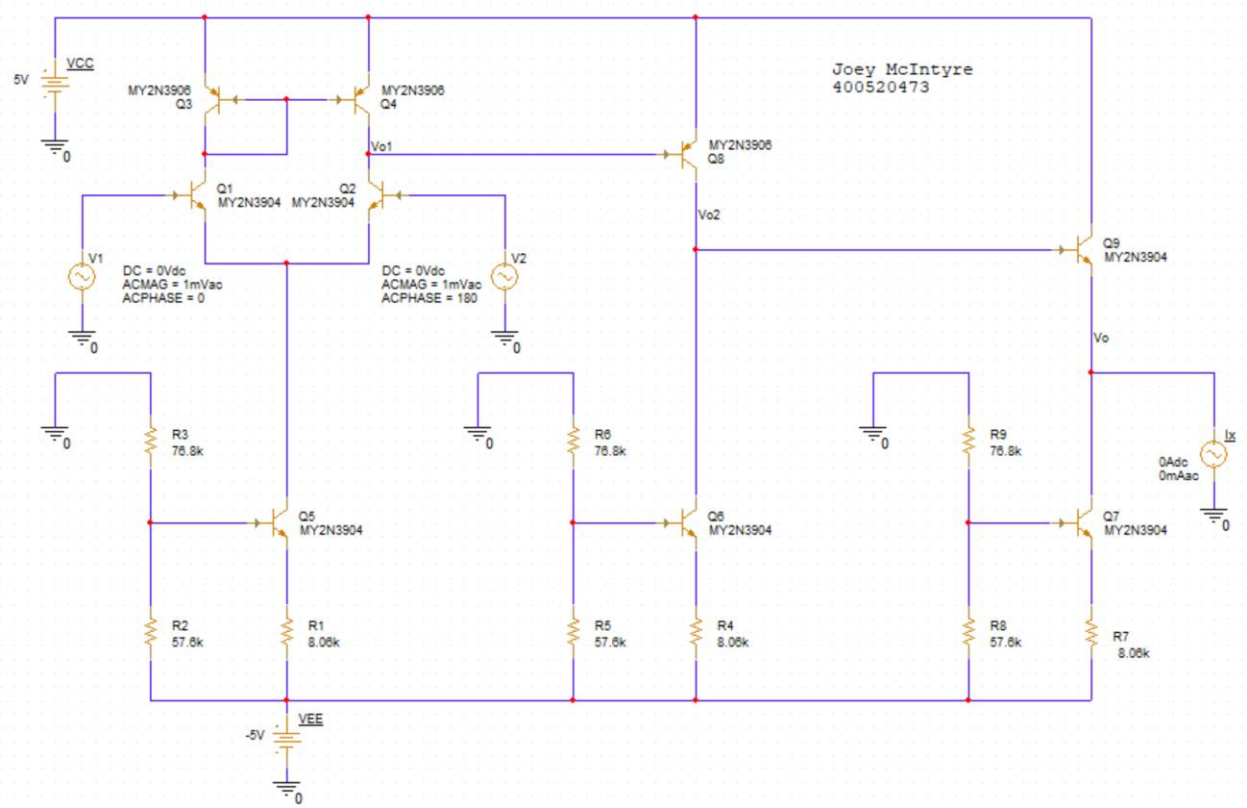


Figure 1: PSpice circuit used for simulation - Op-Amp Characterization

1.2

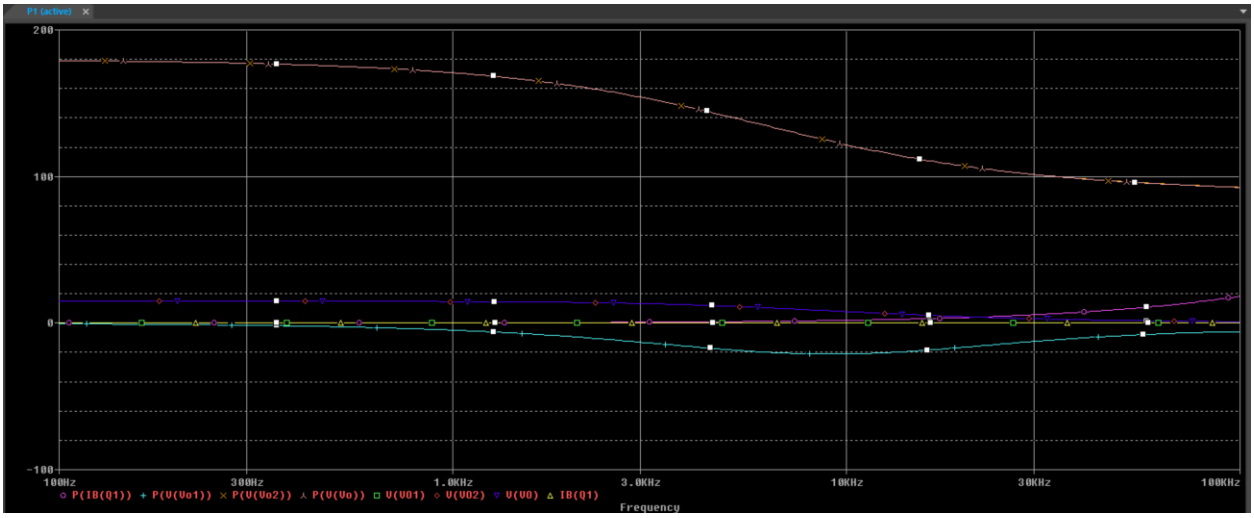


Figure 2: PSpice simulation results – Voltage gain

1.3

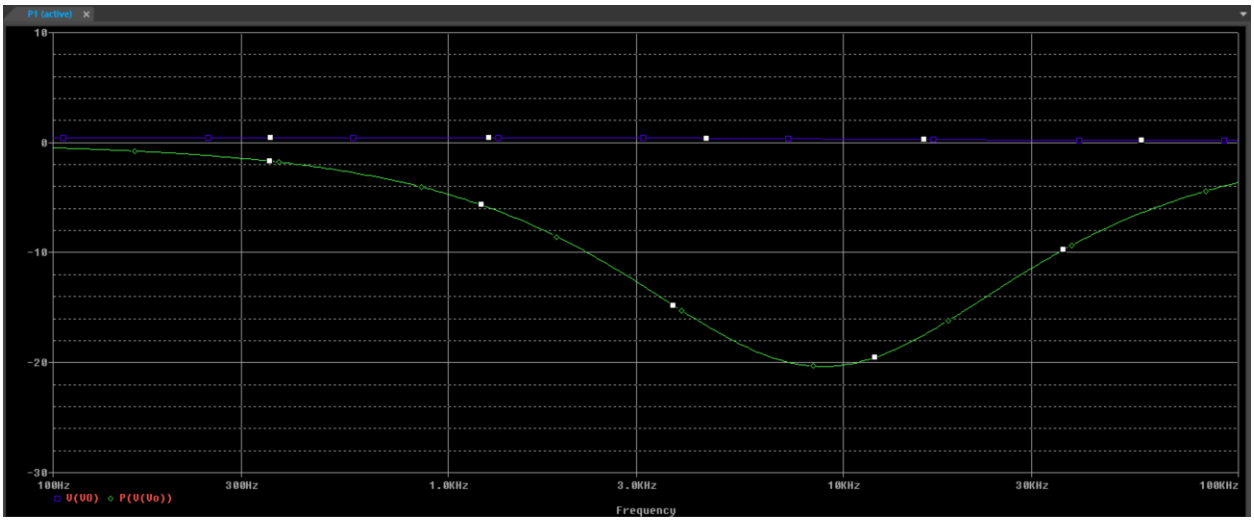


Figure 3: PSpice simulation results - Frequency Response

B. SPICE Simulation – Negative Feedback Amplifier

1.4

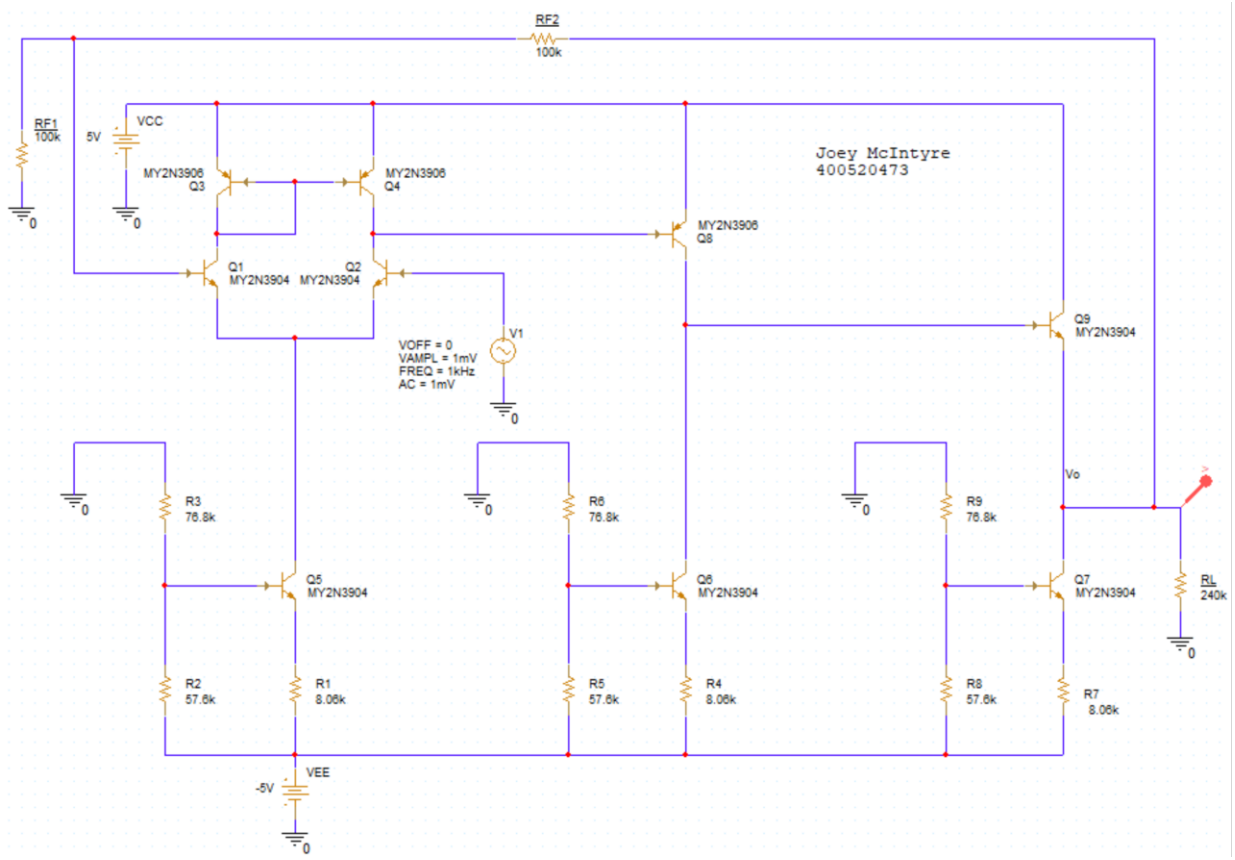


Figure 4: PSpice circuit used for simulation - Negative Feedback Amplifier

1.6

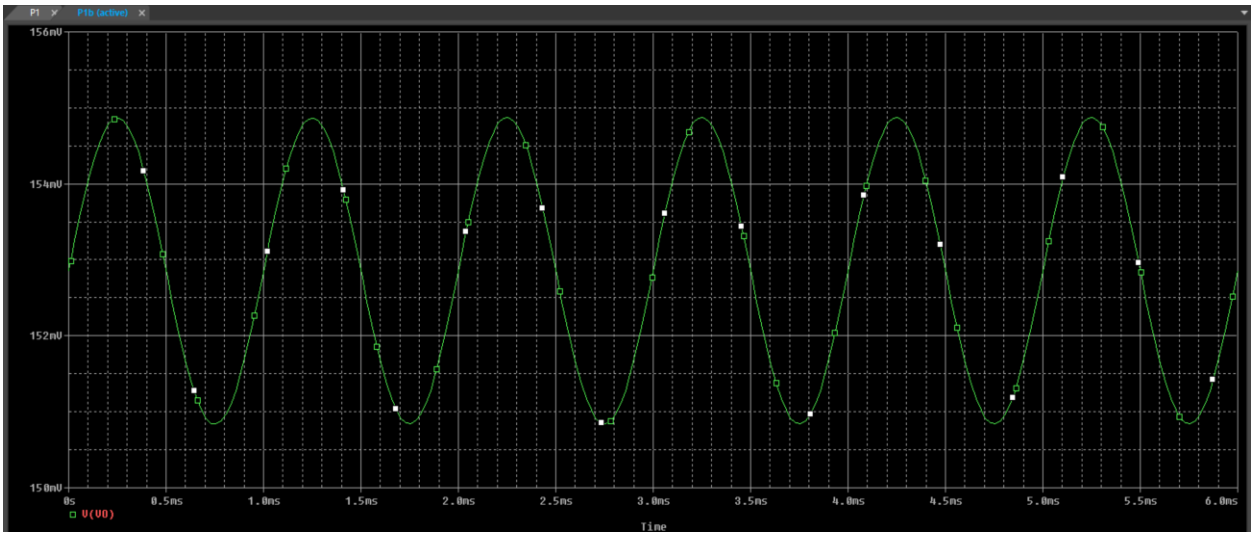


Figure 5: PSpice simulation results - Voltage Gain

1.7

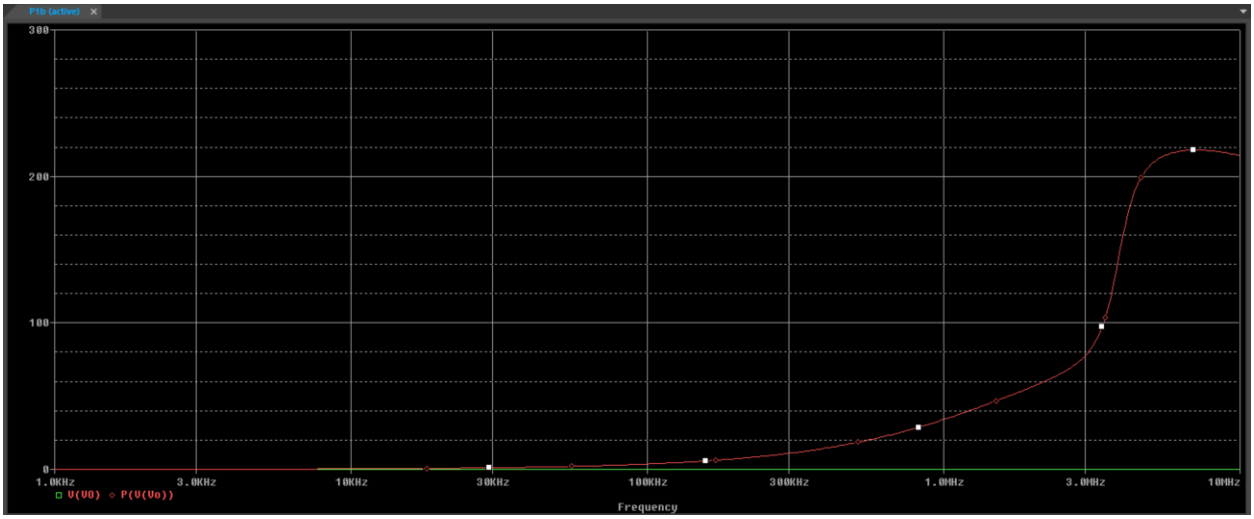


Figure 6: PSpice simulation results - Frequency Response

C. AD3 Measurement

1.11

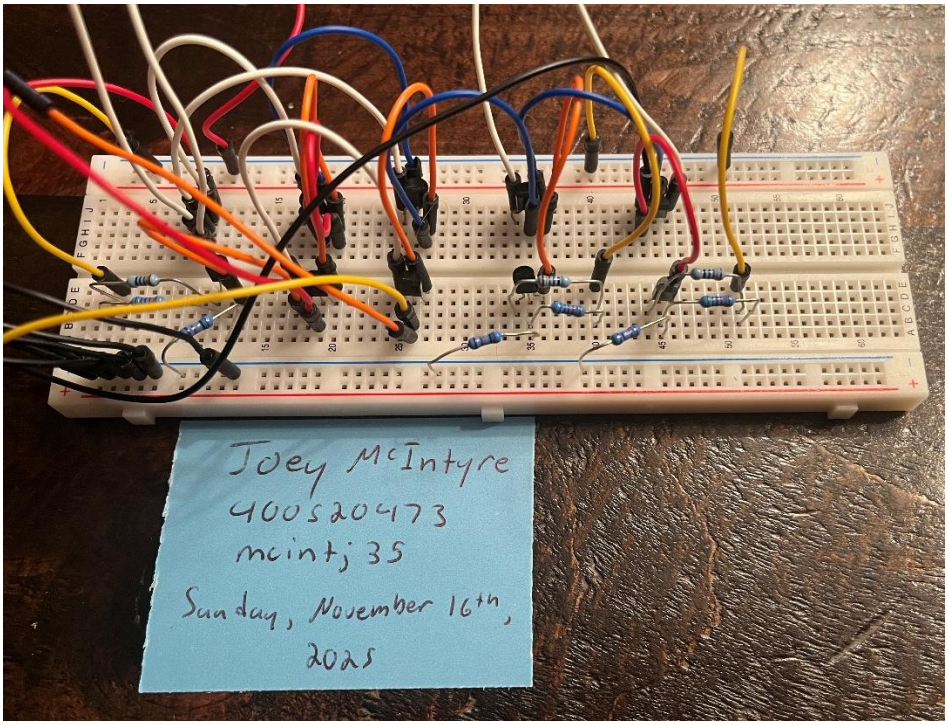


Figure 7: Physical circuit used for AD3 measurement – DC multi-stage operational amplifier

1.13

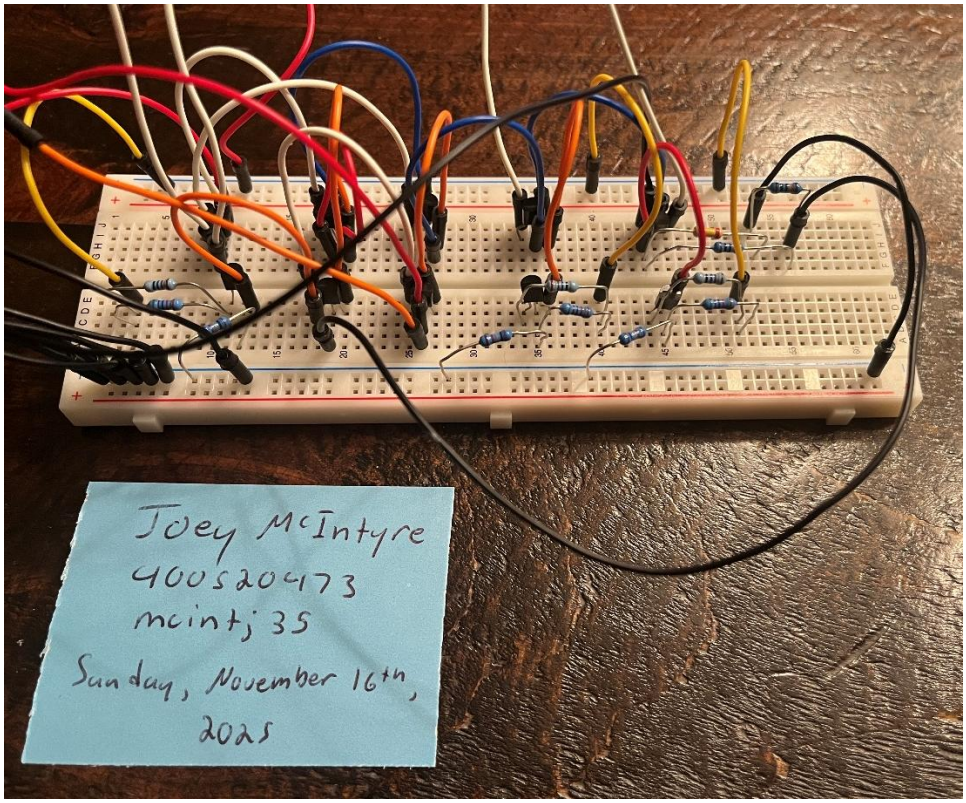


Figure 8: Physical circuit used for AD3 measurement - Negative feedback amplifier

D. Questions for Part 1

Q1. (10 Points) (1) Based on the simulation data obtained in Step 1.2, what is the low-frequency (i.e., f = 100 Hz) voltage gain in dB for the first-stage differential amplifier Ad1 , the second-stage CE amplifier Ad2 , and the third-stage CC amplifier Ad3 , respectively, for the differential-mode signal? **(2)** What is the overall voltage gain for the differential-mode signal? **(3)** Which input (V1 or V2) is the non-inverting input of the operational amplifier? **(4)** What is the upper 3-dB frequency f H of the amplifier?

(1)

Based on the simulation data obtained in Step 1.2, the low frequency voltage gain for each differential amplifier was as follows:

- First-stage differential amplifier: A_{d1} = 7.38 dB
- Second-stage CE amplifier: A_{d2} = 70.05 dB
- Third-stage CC amplifier: A_{d3} = 0 dB

(2)

The overall voltage gain for the differential-mode signal was found to be A_d = 77.43 dB = 7434.5 V/V.

(3)

The non-inverting input of the operational amplifier is the input is observed to be V_2. This is because V_2 is in phase with the output voltage V_o (both 179.07 degrees at low frequency).

(4)

The upper 3-dB frequency can be found by observing the frequency at which the original phase (179.07 degrees) decreases by 45 degrees. The phase of the output voltage is 134.07 degrees at a frequency of approximately 6338.41 Hz. This means the upper 3-dB frequency of the amplifier is f_H = 6338.41 Hz.

Frequency	M(I(Q1:B))	P(I(Q1:B))	M(V(Vo1))	P(V(Vo1))	M(V(Vo2))	P(V(Vo2))	M(V(Vo))	P(V(Vo))	Ad1	Ad2	Ad3	Ad	Ad	Rin = R11
Hz	Amps	Degrees	Volts	Degrees	Volts	Degrees	Volts	Degrees	dB	dB	dB	dB	V/V	Ohm
100	2.45E-08	0.019001953	0.004677087	-0.489610766	14.86962947	179.0738603	14.86897389	1.79E+02	7.38	70.05	0.00	77.43	7434.5	81757.3
6338.408102	2.45E-08	1.202714084	0.003631442	-19.96200659	10.39231697	134.2729755	10.39185652	1.34E+02	5.18	69.13	0.00	74.31	5195.9	81737.0

Q2. (5 Points) Compare the simulated differential-mode gain Ad1 found in Q1 and the simulated gain Ad in Q5 of Lab 3. What causes these two gains to be so different from each other for the same differential amplifier?

In question 5 of lab 3, the simulated voltage gain A_d for the differential mode signal was found to be 70.07 dB. This is significantly larger than the simulated differential mode gain A_{d1} of 7.38 dB found in question 1 of this lab.

This large difference in gain for the same differential amplifier can be attributed to the use of a feedback stage within the first stage of the circuit in this lab. Feedback circuits are known to have a significantly lower gain because their purpose is to prioritize stability at the cost of sacrificing the gain.

Q3. (5 Points) Based on the simulated results obtained in Steps 1.2 and 1.3, what are the input resistance Rin and the output resistance Ro of the Op-Amp?

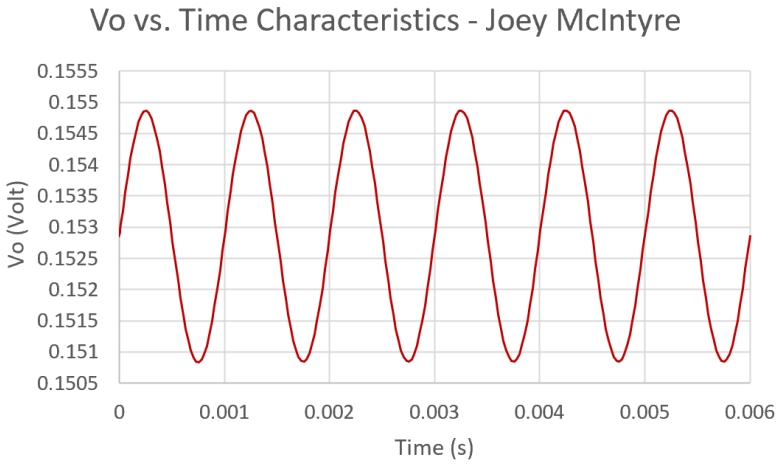
Based on the simulation results obtained in steps 1.2 and 1.3, the input resistance of the op-amp R_{in} = 81757.3Ω, and the output resistance R_o = 460.9Ω.

Rin = R11	Rout
Ohm	Ohm
81757.3	460.9

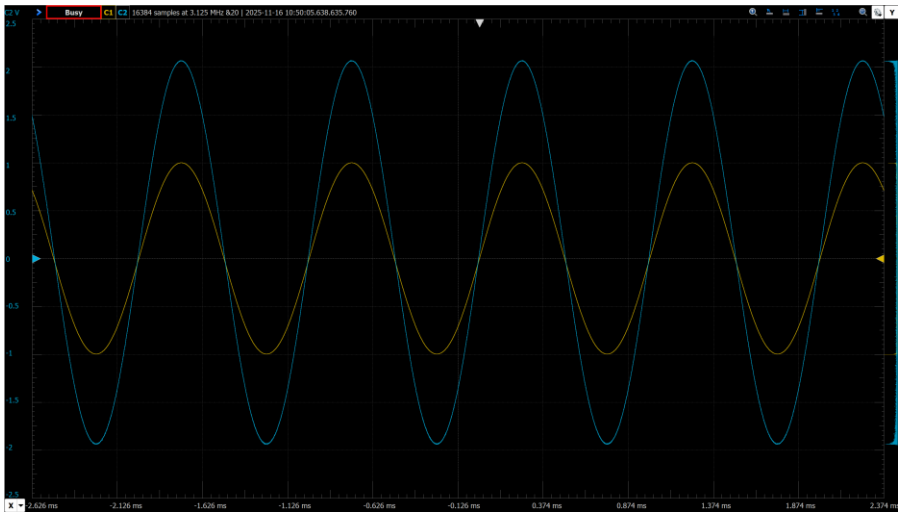
Q4. (10 Points) (1) Based on the simulated and measured results from Steps 1.6 and 1.13, plot the simulated and measured output voltages Vo vs. time characteristics at 1 kHz. **(2)** Calculate the simulated and measured peak-to-peak voltage Vpp, the AC amplitude Vp, and the dc voltage Vdc of Vo, and compare the simulation and measurement results.

(1)

Based on the simulated results from step 1.6, the output voltage V_o vs. time characteristics at 1kHz plot can be obtained:



Based on the measured results from step 1.13, the V_o vs. time characteristics at 1kHz plot can also be obtained:



(2)

For the simulated results from step 1.6:

- Peak-to-peak voltage: $V_{pp} = 0.154866 - 0.150837 = 0.004029$ V
- AC amplitude: $V_p = \frac{V_{pp}}{2} = \frac{0.004029}{2} = 0.0020145\ V$
- DC voltage of V_o: $V_{DC} = 0.154866 - 0.0020145 = 0.1528515\ V$

For the measured results from step 1.13:

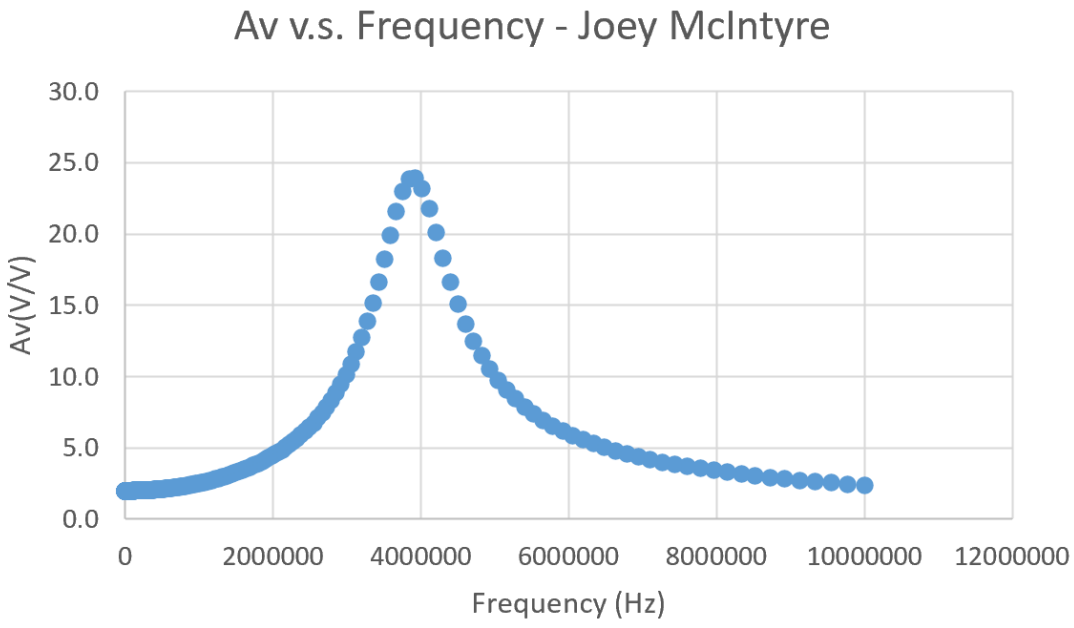
- Peak-to-peak voltage: $V_{pp} = 2.05 - (-1.95) = 4\ V$
- AC amplitude: $V_p = \frac{V_{pp}}{2} = \frac{4}{2} = 2\ V$
- DC voltage of V_o: $V_{DC} \approx 2.05 - 2 = 0.05$ V

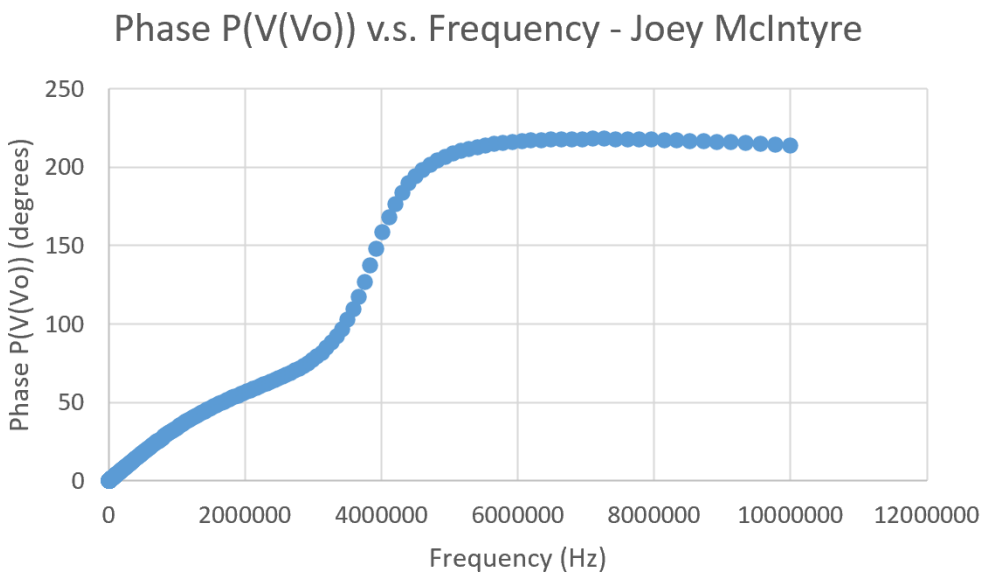
It is apparent that the simulation results and the measured results are significantly different. This difference can be explained by the different AC input voltages in each step. In step 1.6, the amplitude of the simulated AC input was 1mV, where in step 1.13, the amplitude of the AC input was 1V.

Q5. (10 Points) (1) Based on the simulated and measured results from Steps 1.7 and 1.14, plot the simulated and measured voltage gain magnitude and phase vs. frequency characteristics. What is the low-frequency gain of this amplifier? **(2)** To operate this amplifier, what is its highest operating frequency to provide a constant gain as designed?

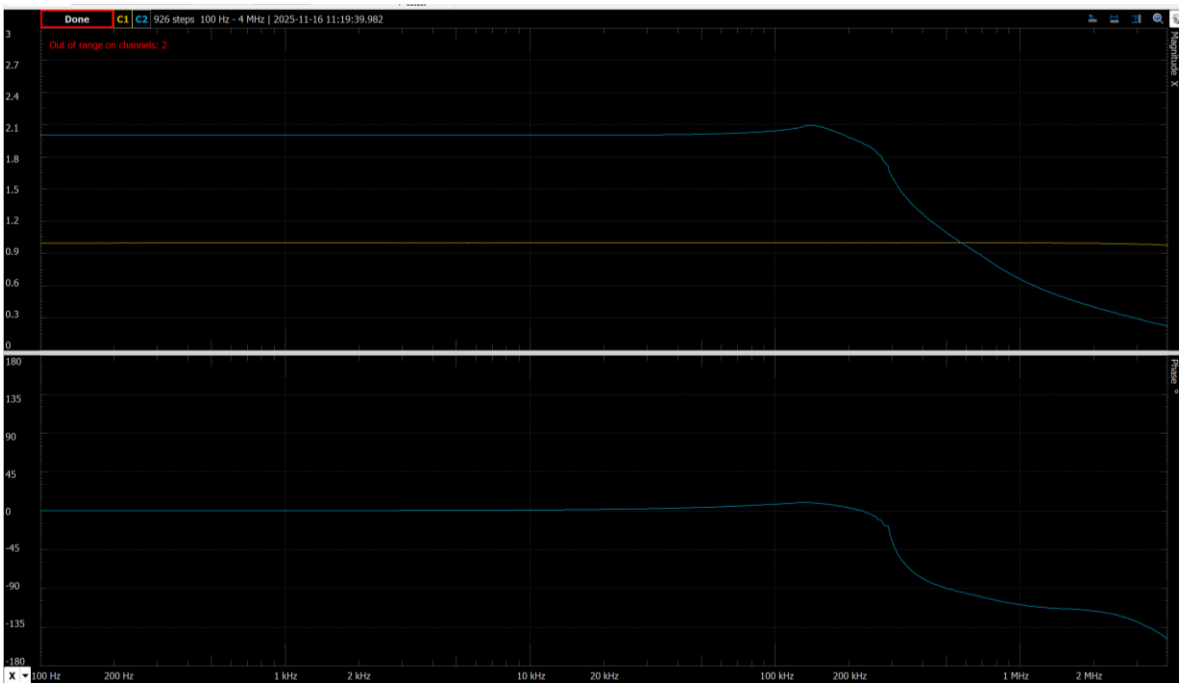
(1)

Based on the simulated results from step 1.7, the voltage gain magnitude and phase vs frequency characteristics plot can be obtained:





Based on the measured results from step 1.13, the measured voltage gain magnitude and phase vs. frequency characteristics plot can be obtained:



From steps 1.7 and 1.13, the low-frequency gain of this amplifier can be observed at 1000 Hz to be 2.0 V/V.

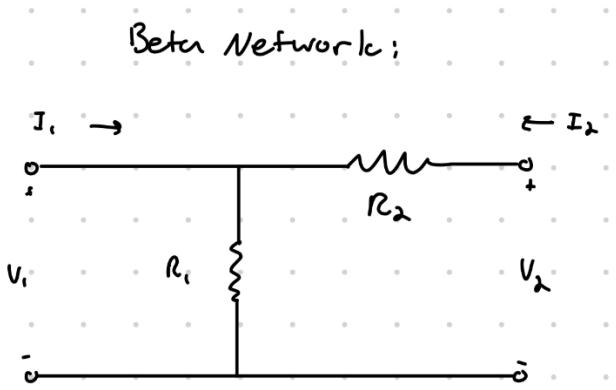
(2)

To operate this amplifier, the highest operating frequency to provide a constant gain as designed is observed to be approximately 100 KHz. After this point, the gain begins to fluctuate and is therefore no longer constant.

Q6. (5 Points) What kind of feedback configurations (e.g., shunt-shunt) is it for the amplifier in Fig. 2?

The amplifier in Fig. 2 uses series-shunt feedback. The output voltage is sampled through a shunt connection, and the feedback voltage is applied in series with the input at the base of Q2, forming a non-inverting voltage-amplifier configuration.

Q7. (10 Points) Find the beta network and the feedback components β, R11 , and R22 , respectively.

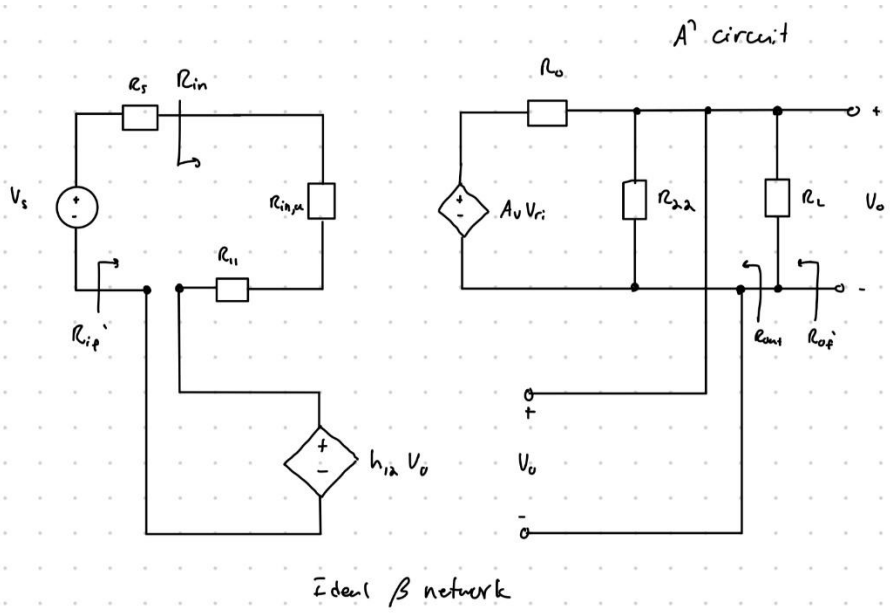


$R_{11} = R_1 // R_2 = 100k // 100k = 50k\Omega$

$R_{22} = R_1 + R_2 = 100k + 100k = 200k\Omega$

$$\beta = \frac{R_1}{R_1 + R_2} = \frac{100k}{100k + 100k} = 0.5$$

Q8. (15 Points) Use the feedback theory and simulation results to find the amplifier's voltage gain, input resistance, and output resistance, respectively.



$$A'_{vf} = \frac{A_v{}'}{1 + A_v{}'\beta} \approx \frac{1}{\beta} = \frac{1}{0.5} = 2V/V$$

$$R_{in} = R'_{if} - R_s = (R'_i)(1 + A'_v\beta) - R_s = \left(R_{in,a} + R_{11} + R_s\right)(1 + 0.5\beta) - R_s = 330\ M\Omega$$

$$R_{out} = \frac{1}{\frac{1}{R_{of}{}'} - \frac{1}{R_L}} = \frac{1}{\frac{1}{\frac{R_{22}||R_L||R_o}{1 + A_v{}'\beta}} - \frac{1}{R_L}} = 0.2\Omega$$

Part 2: Positive Feedback Circuit – Oscillator

A. Spice Simulation

2.2

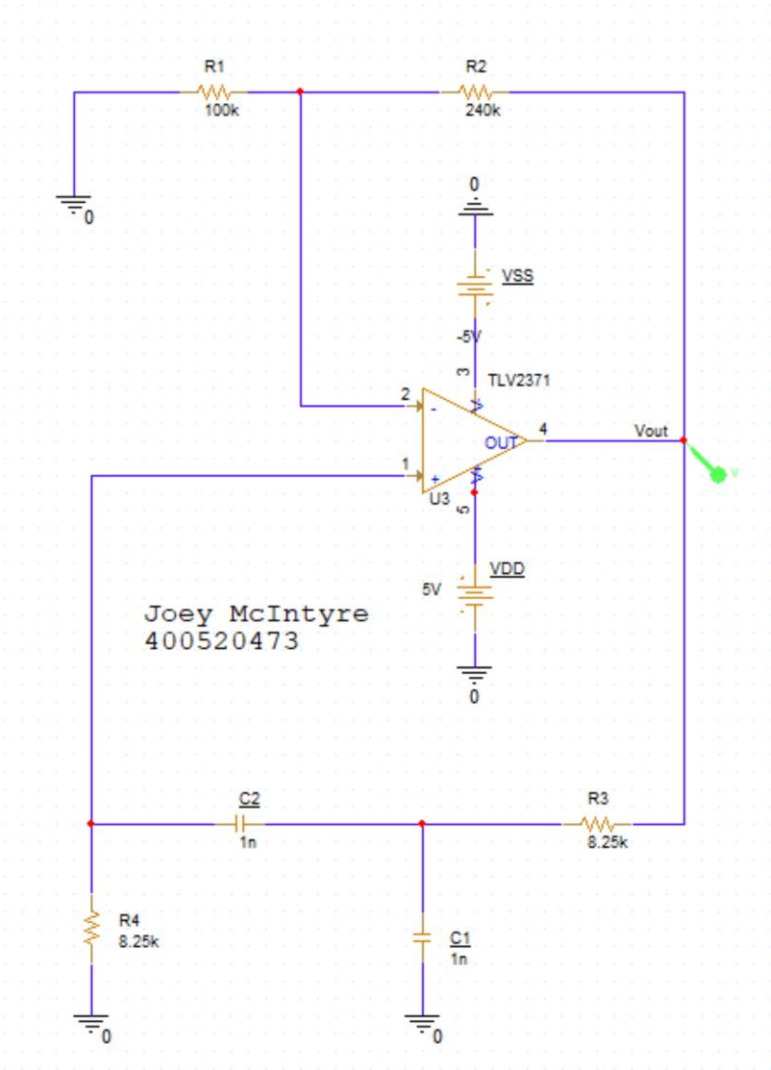


Figure 9: PSpice circuit used for simulation - Positive Feedback Circuit - Oscillator

2.3

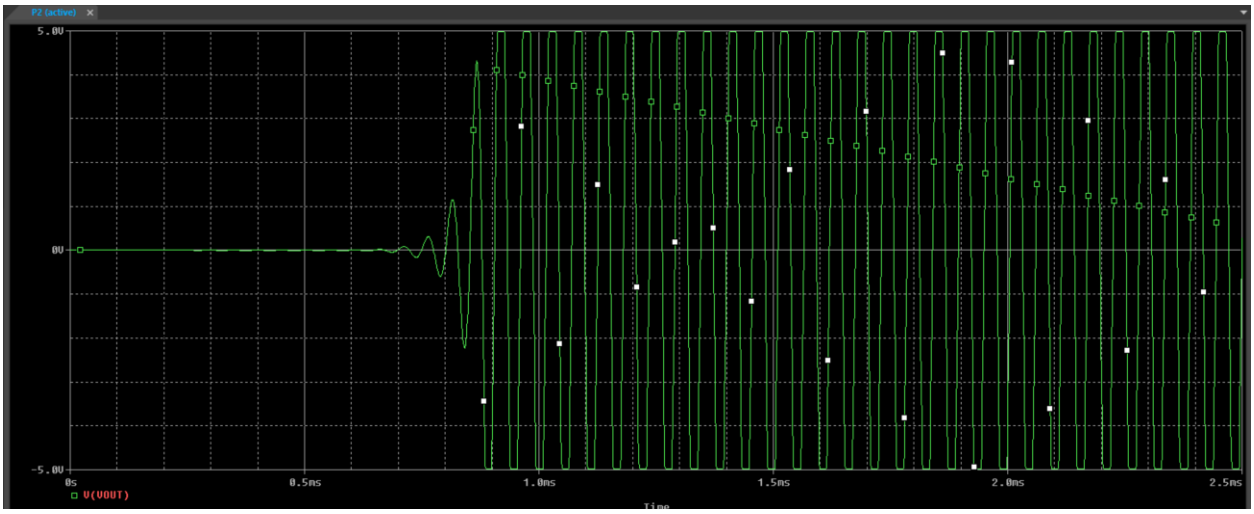


Figure 10: PSpice simulation results - Time Domain (Transient) Response

R_2 = 240kΩ: Settling time = 0.000923434 s

1017	0.000923434	4.986655922

2.4

220k:

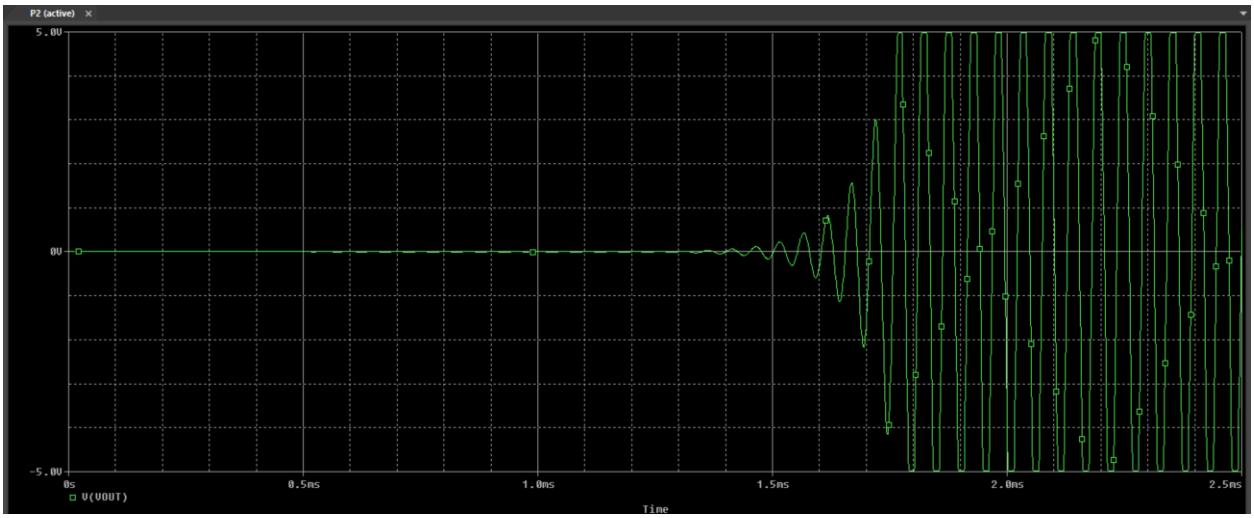


Figure 11: PSpice simulation results - Time Domain (Transient) Response

R_2 = 220kΩ: Settling time = 0.001773 s

0.001773	4.985254

280k:

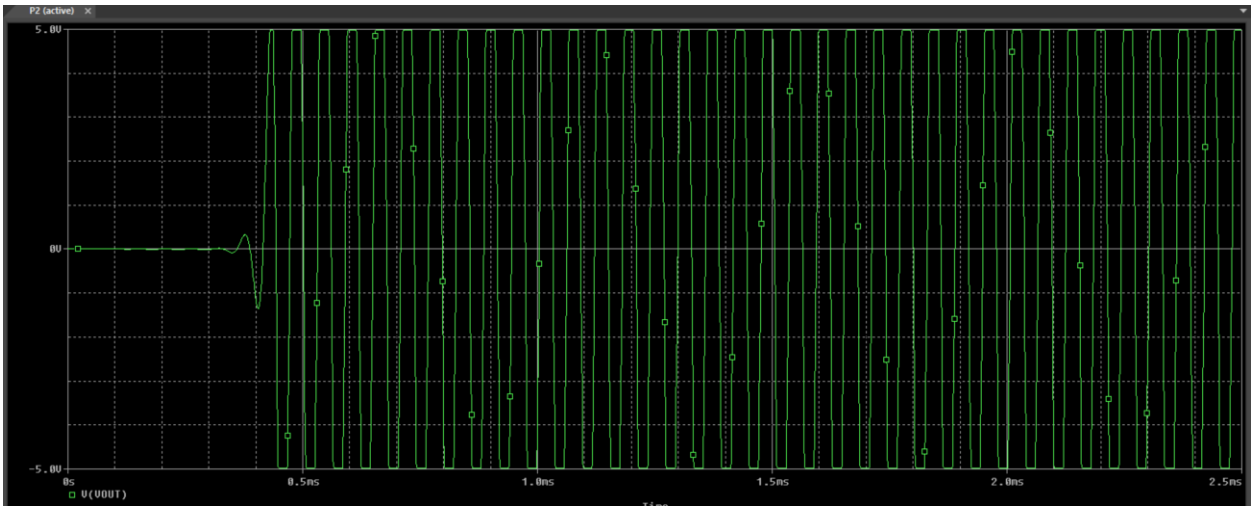


Figure 12: PSpice simulation results - Time Domain (Transient) Response

R_2 = 280kΩ: Settling time = 0.000494 s

0.000494	4.988147

2.5

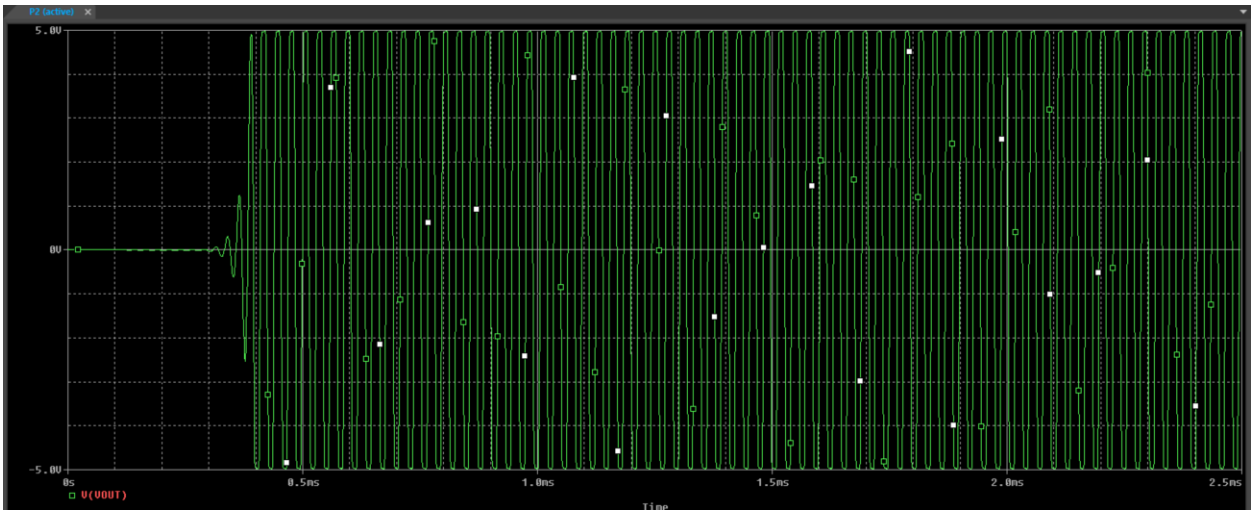


Figure 13: PSpice simulation results - Time Domain (Transient) Response

B. AD3 Measurement

2.6

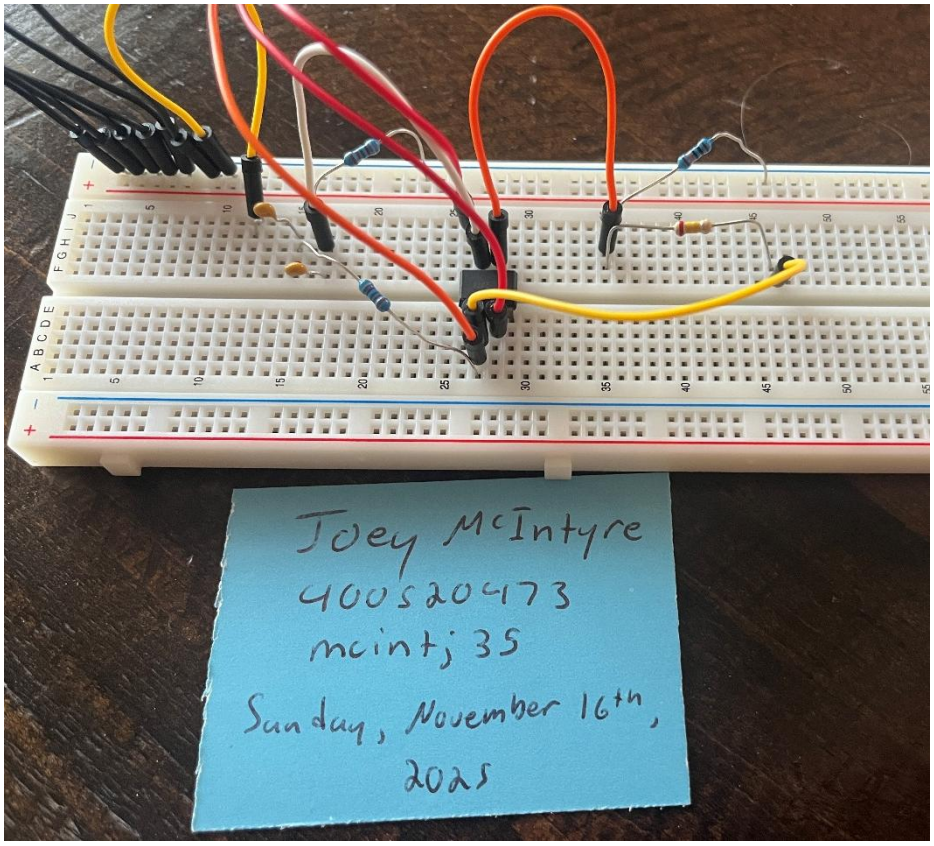
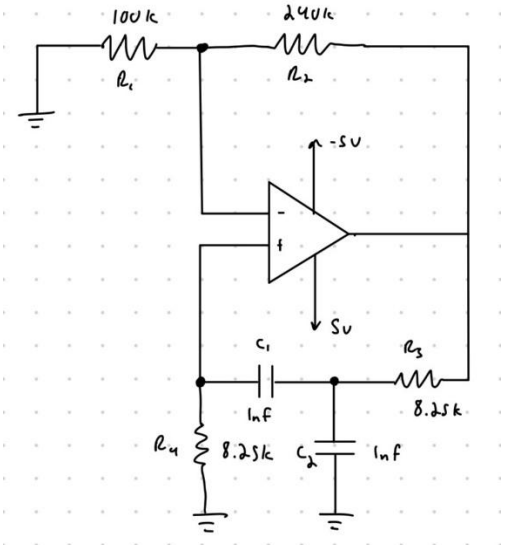


Figure 14: Physical circuit for AD3 measurement - Transient Response and Oscillation Frequency

C. Questions for Part 2

Q9. (15 Points) For the oscillator circuit in Fig. 5, find its loop gain L(s), the frequency for the zero loop phase, and R2 /R1 for oscillation.



$$C = C_1 = C_2 = 1nF$$

$$R = R_3 = R_4 = 1nF$$

$$V_o = V_+\left(1 + \frac{1}{sCR}\right) + RV_+\left(\frac{1}{R} + sC\left(1 + \frac{1}{sCR}\right)\right)$$

$$V_o = V_+\left(1 + \frac{1}{sCR}\right) + V_+(2 + sCR)$$

$$\frac{V_+}{V_o} = \frac{\frac{s}{CR}}{s^2 + s\left(\frac{3}{CR}\right) + \left(\frac{1}{CR}\right)^2}$$

$$\boldsymbol{Loop\ gain}: \boldsymbol{L(s)} = \left(\mathbf{1} + \frac{\boldsymbol{R_2}}{\boldsymbol{R_1}}\right)\frac{\frac{\boldsymbol{s}}{\boldsymbol{CR}}}{\boldsymbol{s^2} + \boldsymbol{s}\left(\frac{\mathbf{3}}{\boldsymbol{CR}}\right) + \left(\frac{\mathbf{1}}{\boldsymbol{CR}}\right)^2}$$

$$\boldsymbol{Zero\ loop\ phase\ frequency}: \boldsymbol{\omega} = \frac{\mathbf{1}}{\boldsymbol{CR}}$$

$$At\ the\ zero\ loop\ phase\ frequency: |L(j\omega)| = \frac{1}{3}\left(1 + \frac{R_2}{R_1}\right)$$

$$Therefore\ for\ oscillation: \frac{1}{3}\left(1 + \frac{R_2}{R_1}\right) \geq 1 \rightarrow \boldsymbol{\frac{R_2}{R_1} \geq 2}$$

Q10. (5 Points) Based on the simulated results in Step 2.4, what are the settling times for R2 = 220 kΩ, 240 kΩ, and 280 kΩ, respectively? What do you observe? Explain the observed trend.

Based on the simulation results in step 2.4, the settling times are:

- For R_2 = 220kΩ: Settling time = 0.001773 s = 1.773 ms
- For R_2 = 240kΩ: Settling time = 0.000923434 s = 0.923434 ms
- For R_2 = 280kΩ: Settling time = 0.000494 s = 0.494 ms

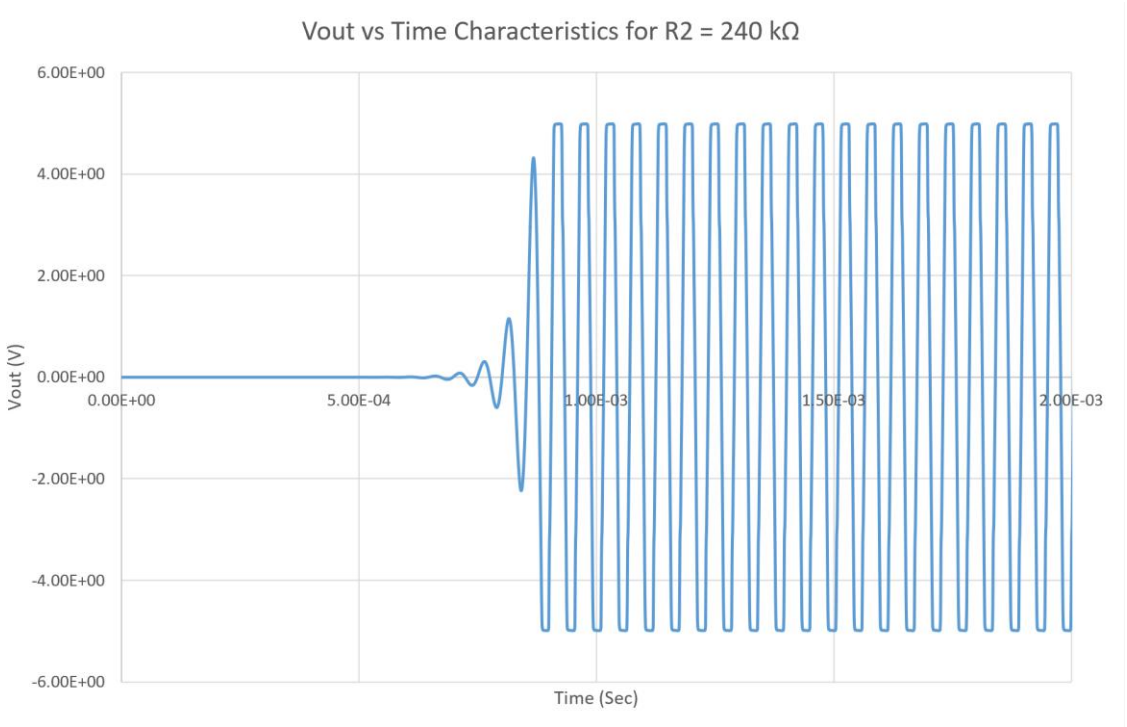
R2 = 220 kΩ	R2 = 240 kΩ	R2 = 280 kΩ
Settling Time (ms)	Settling Time (ms)	Settling Time (ms)
0.001773	0.000923434	0.000494

From these results, we can observe an inverse relationship between the resistance and the settling time. As the resistance of R_2 increases, the settling time decreases. This trend can be explained using the equation for the loop gain derived from question 9. In that equation, it is clear that an increase in R_2 also increases the loop gain (L(s)). When the loop gain is increased, the dominant pole of the circuit is shifted to a higher frequency, which subsequentially leads to a quicker settling time.

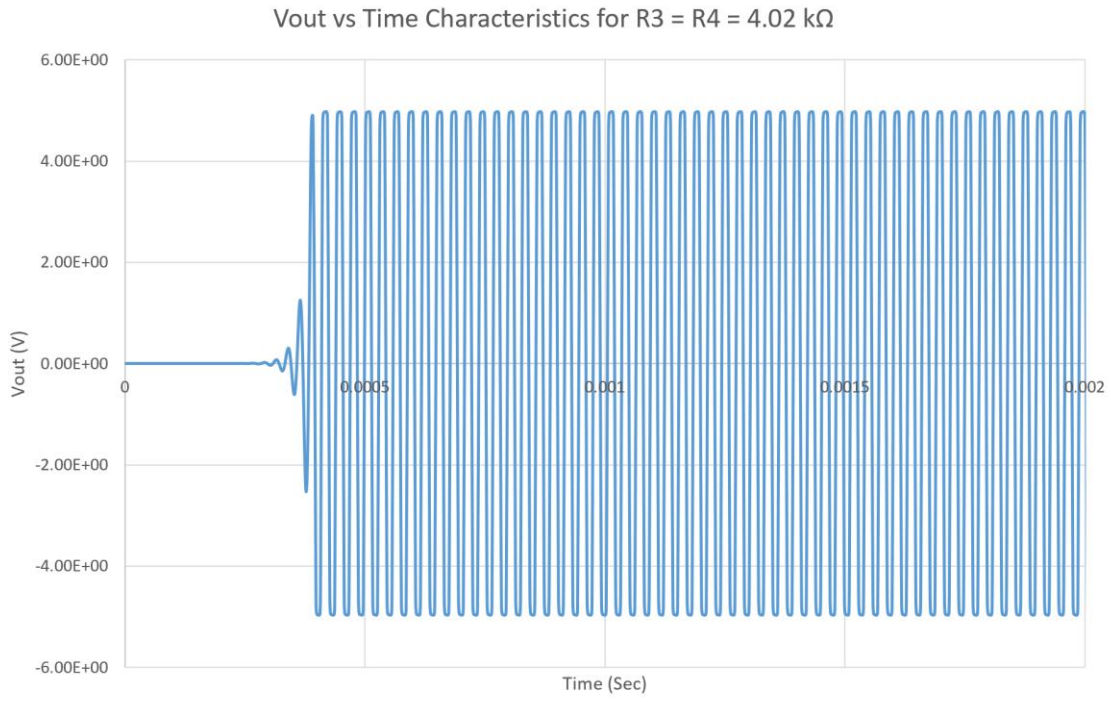
Q11. (10 Points) (1) Based on the setup in Steps 2.3, 2.5, 2.8, and 2.9, plot the simulated and measured Vout. **(2)** Calculate the simulated and measured oscillation frequencies in each case. Compare and discuss them with the results from the theory.

(1)

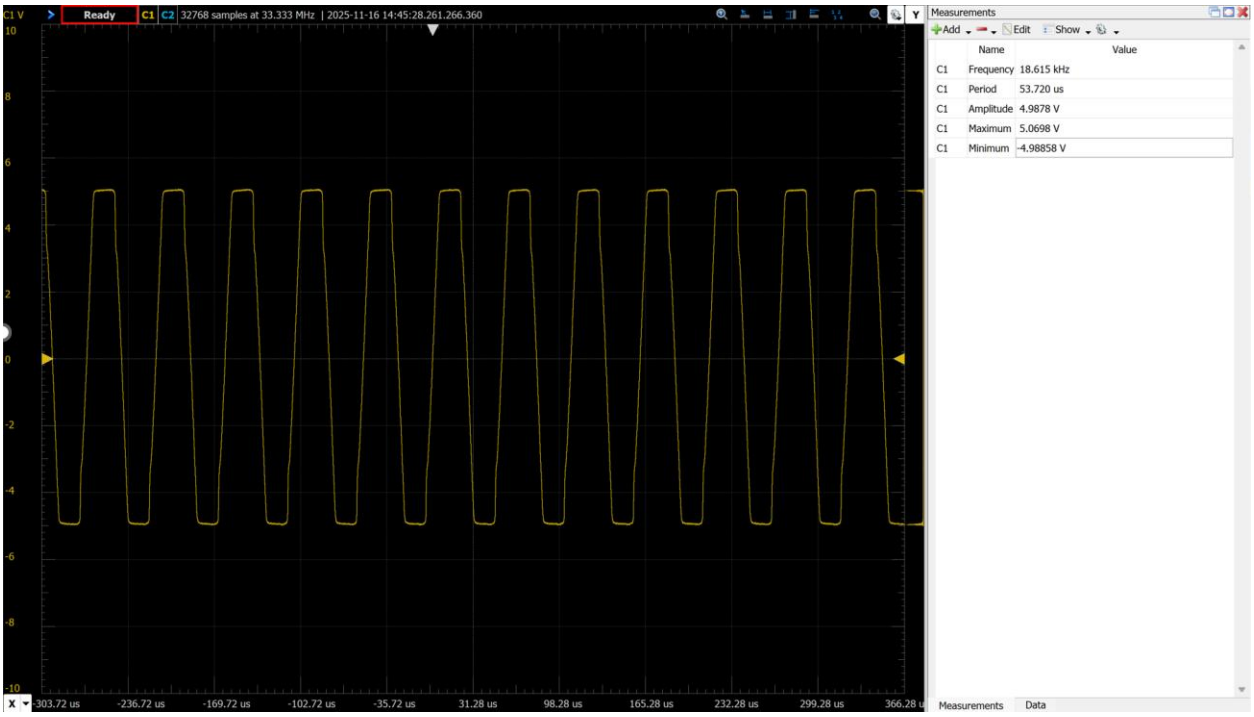
Based on the setup in step 2.3, the simulated V_{out} is:



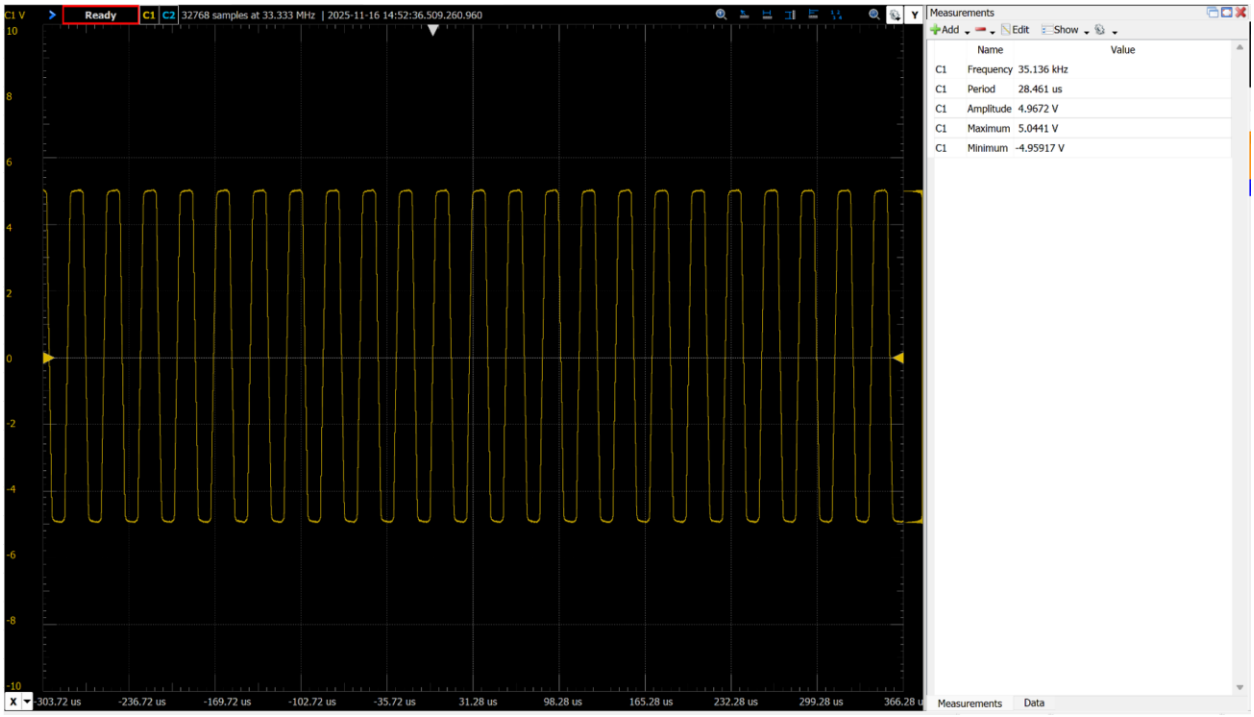
Based on the setup in step 2.5, the simulated V_{out} is:



Based on the setup in step 2.8, the measured V_{out} is:



Based on the setup in step 2.9, the measured V_{out} is:



(2)

From step 2.3, the simulated oscillation frequency was found to be 18 kHz. For the same setup (step 2.8), the measured oscillation frequency was found to be approximately 18.615 kHz.

From step 2.5, the simulated oscillation frequency was found to be 34 kHz. For the same setup (step 2.9), the measured oscillation frequency was found to be approximately 35.136 kHz.

Both the simulated and measured results line up with each other nicely, helping to confirm one another's validity. These experimental results also align with the theoretical results. From the frequency formula used in question 9 ($\omega = \frac{1}{CR}$), we know that the frequency is inversely proportional to the resistance. In step 2.5 and 2.9, we decreased R_3 and R_4 from 8.25kΩ each to 4.02kΩ, which resulted in the frequency increasing by a similar factor. Therefore, since the simulated and measured data match each other closely, and they both behave as theoretically expected, we can conclude that the experiment was done correctly.