Lab 2 – Single-Stage Amplifiers

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ELECENG 3EJ4 – Electronic Devices and Circuits II

Dr. Chih-Hung Chen

Sunday, October 5th, 2025

Part 1: Common-emitter (CE) Amplifier

A) SPICE Simulation – Constant Current Sink

1.1

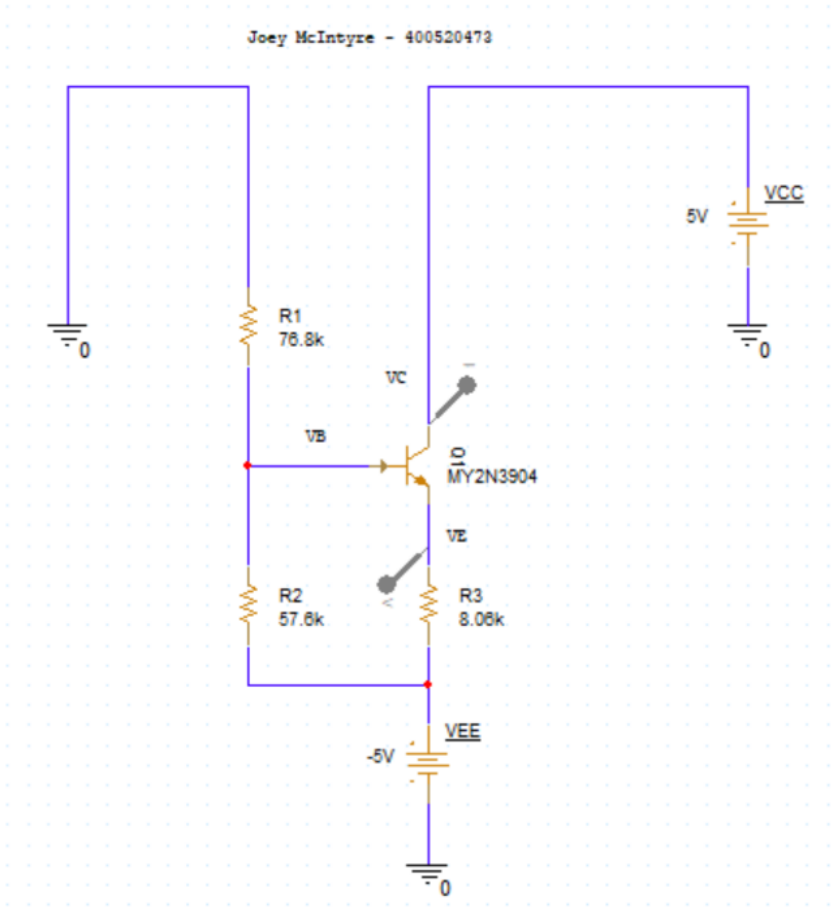

Figure 1: Circuit used for PSpice simulation of Current Sink

1.2

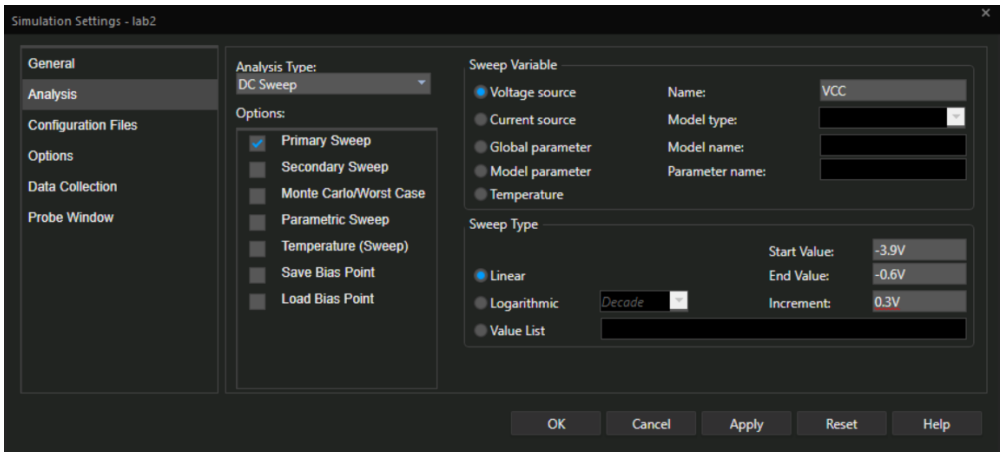

Figure 2: PSpice simulation settings for DC Sweep

B) SPICE Simulation – CE Amplifier

1.4

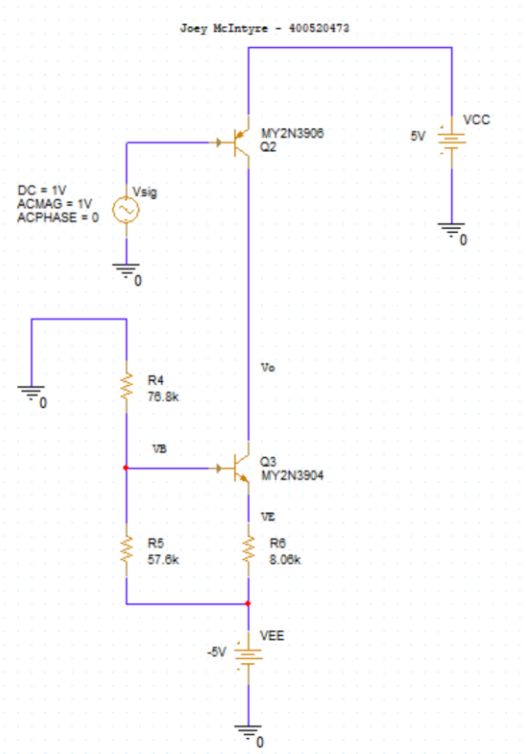

Figure 3: Circuit used for PSpice simulation of CE Amplifier

1.5

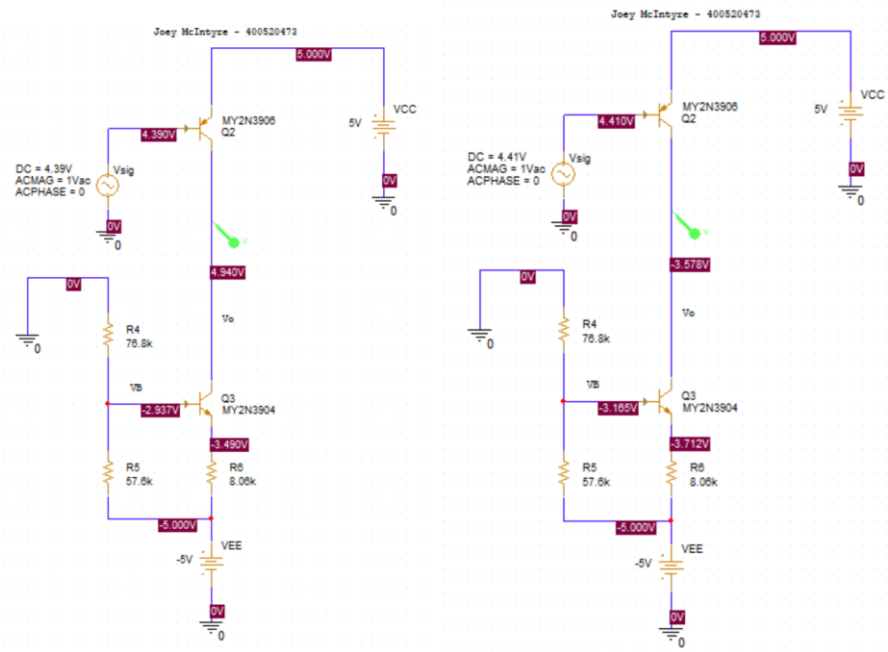

Figure 4: PSpice circuits used to find Quiescent Point

1.6

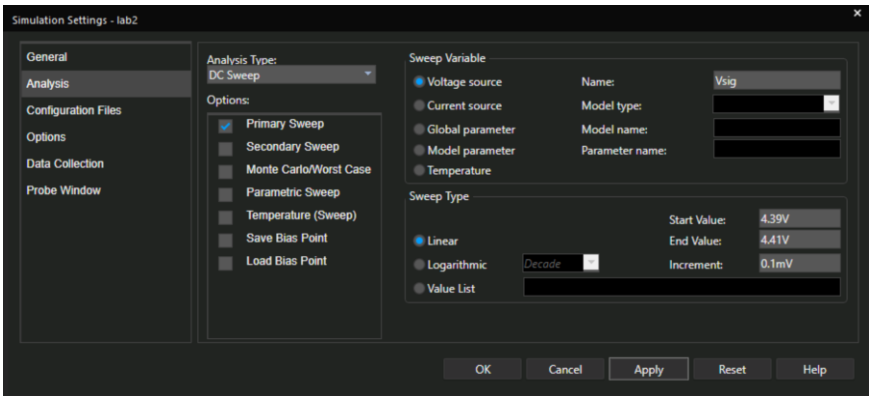

Figure 5: PSpice simulation settings for DC Sweep

$V_{sig} = V_{BQ2}$ that results in Vo ≈ 0V was found to be 4.4018V.

1.7

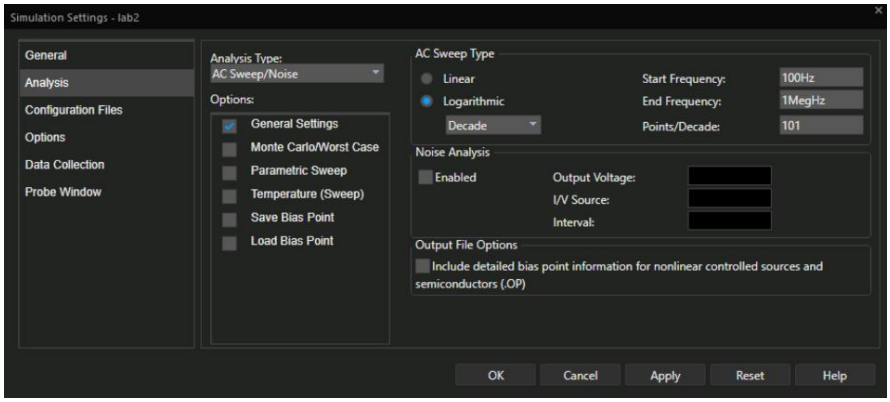

Figure 6: PSpice simulation settings for AC sweep

C) AD3 Measurement – Constant Current Sink

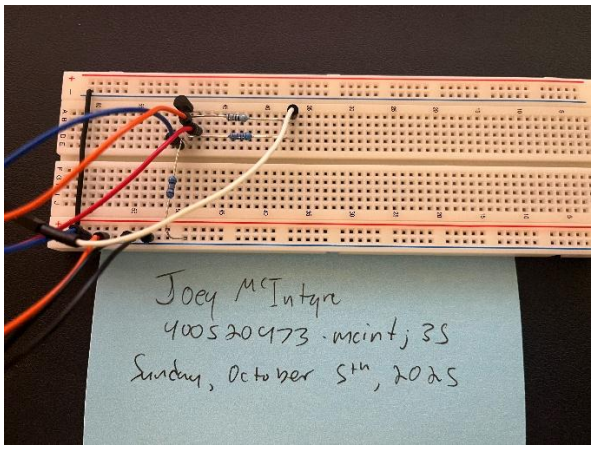

Figure 7: Physical circuit used for AD3 measurement of the Constant Current Sink

D) AD3 Measurement – CE Amplifier

1.14

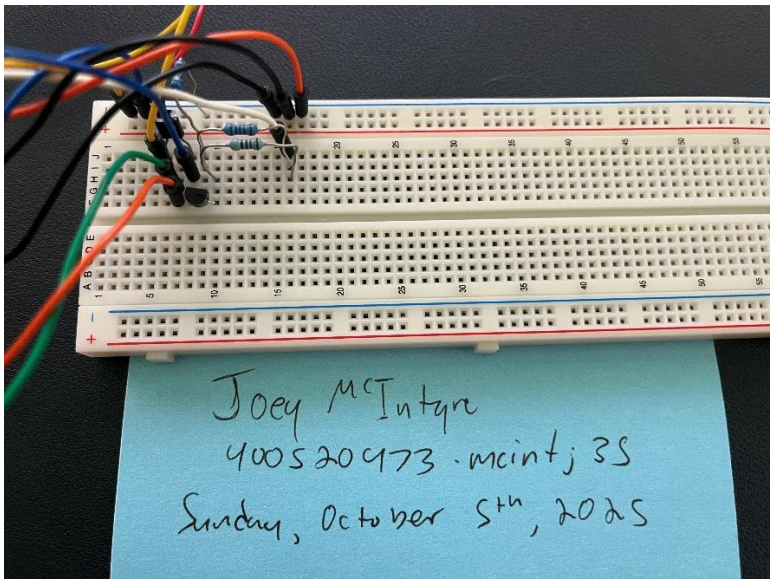

Figure 8: Physical circuit used for AD3 measurement of the CE Amplifier

1.17

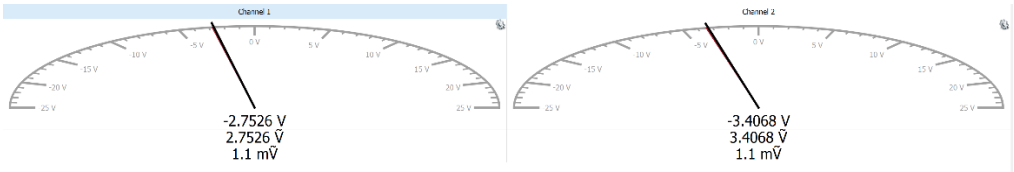

Figure 9: AD3 voltmeter readings to find Quiescent Point

1.19

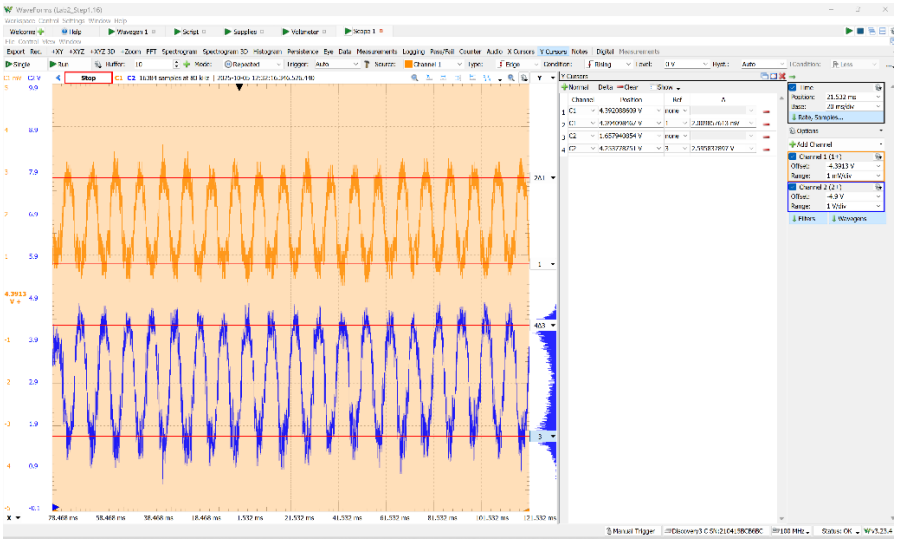

Figure 10: AD3 scope function displaying results

E) Questions for Part 1

For the common emitter (CE) amplifier designed, answer the following questions with simulated and measured data and discuss any discrepancy between the simulation and measurement results.

Q1. (10 Points) (1) Based on the simulation data obtained in Step 1.2, what are the $V_{o,min}$, and I_o of the current sink? Use the measurement data obtained in Step 1.10 to verify the $V_{o,min}$ and I_o. **(2)** Based on the simulation data obtained in Step 1.2 and the measurement data obtained in Step 1.10, what are the ranges of the simulated and measured output resistance R_o of the current sink for V_{CC} larger than $V_{o,min}$?

(1)

Based on the simulation data obtained in step 1.2, $V_{o,min}$ = -3V, and I_o = 0.185mA. This is found by observing where the IC values flatten, and where the IC stops changing much.

Based on the measurement data obtained in step 1.10, $V_{o,min}$ = -3V, and I_o = 0.196mA. This experimental data verifies the simulated data because both $V_{o,min}$ and I_o match well in both cases. $V_{o,min}$ is -3V in both cases, and the I_o differs by a factor of less than 10%, which is acceptable given real-world imperfections in the experiment.

(2)

V_{CC} larger than $V_{o,min}$ is the active region to the right of -3V. Based on the simulated data in Step 1.2, R_o ranges from 2.26 Mega Ohms to 4.07 Mega Ohms. Based on the experimental data in step 1.10, R_o ranges from 3.42 Mega Ohms to 219 Mega Ohms. The much larger measured value and the negative outlier in step 1.10 are consistent with numerical slope noise and the AD3's measurement tolerances.

Q2. (10 Points) What are the values of V_{o1} and V_{o2} obtained in Step 1.5? Check the Q-points of Q_2 under these two conditions and explain/justify the results obtained qualitatively.

V_{o1} = 4.940 V (Q2 in saturation), and V_{o2} = -3.578 V (Q2 near cutoff). This follows from the PNP CE stage. At 4.39V the base-emitter is forward-biased (V_{EB} ~ 0.61V), forcing $V_o \sim +V_{CC}$. At 4.41V, V_{EB} falls to around 0.59V and Q2 supplies little current, so the current sink takes V_o towards V_{EE}.

Q3. (15 Points) Based on the simulation data obtained in Step 1.6, **(1)** plot the simulated DC V_o vs. V_{sig} characteristics. Discuss/justify the simulated characteristics. **(2)** For the circuit to work as an amplifier, find the DC input range for V_{sig} and the output voltage range for V_o. **(3)** Find the V_{sig} value and its corresponding collector current I_{C2} that results in $V_o \approx 0$ V. **(4)** Based on the measurement data obtained in Step 1.16, plot the measured DC V_o vs. V_{sig} characteristics.

(1)

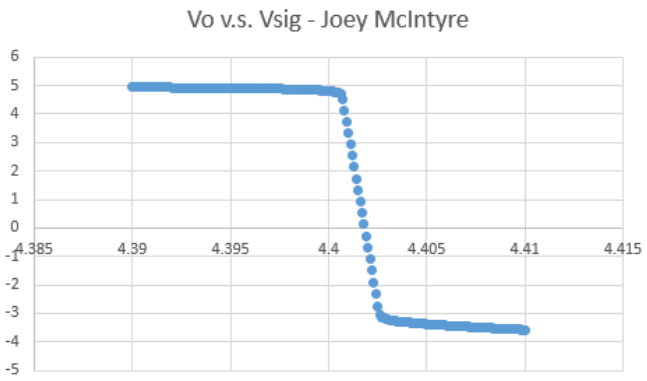

Figure 11: Simulated DC Vo vs. Vsig characteristics

The shape of this graph is exactly as expected. The top rail is when Q2 is saturated, the steep transition region leads into the bottom rail which is when Q2 nears cutoff. Lowering the PNP base increases V_{EB}, meaning more source current, resulting in V_o being near $+V_{CC}$. Raising the base reduces V_{EB}, turning Q2 off, resulting in the sink pulling V_o towards V_{EE}.

(2)

For the circuit to work as an amplifier, the DC input range for V_{sig} and the output range for V_o is as follows:

V_{sig} required DC input range = [4.4007 V, 4.4027 V]

V_o output range = [4.503336 V, -3.13947 V]

This can be visually confirmed by observing the graph.

(3)

V_o is closest to 0V when:

V_{sig} = 4.4018 V, V_o = 0.124312 V, and I_{C2} = 0.000184885 A.

(4)

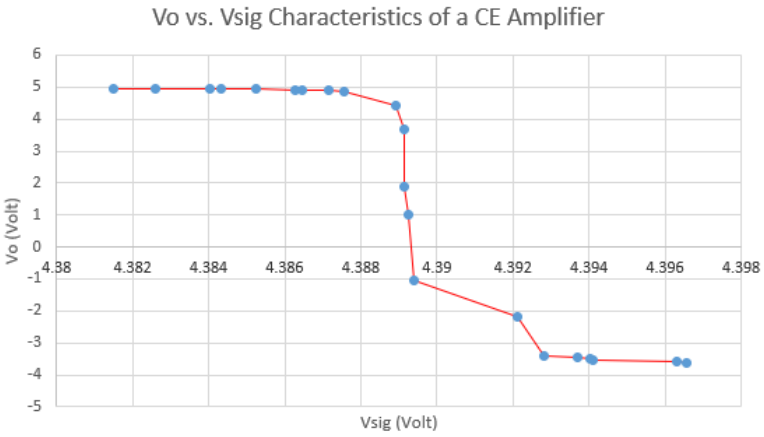

Figure 12: Measured DC Vo vs Vsig characteristics

The measured value for V_{BQ2} was found to be 4.3913V.

Q4. (10 Points) (1) Based on the simulation data obtained in Step 1.7, what are the magnitude (in dB) and phase of intrinsic voltage gain A_{vo} at low frequency (i.e., 100 Hz) and the upper 3-dB frequency f_{3dB} (i.e., the frequency at which the amplitude becomes $\frac{1}{\sqrt{2}} = 0.707$ of its low-frequency value, or the phase changes 45°) of this CE amplifier? **(2)** Verify the voltage gain A_{vo} using the measurement data obtained in Steps 1.18 and 1.19. **(3)** Increase the frequency of W1 to the upper 3-dB frequency f_{3dB} obtained from the simulation, check the value of A_{vo}, and see if it is about 0.707 of its low-frequency value obtained at 100 Hz. Provide WaveForms screenshots of your measurement results.

(1)

Based on the simulation data obtained in step 1.7, the magnitude and phase of intrinsic voltage gain at the following frequencies are as follows:

At low frequency (100Hz):

- $A_{Vo} = 20\log\left(\frac{V_o}{V_i}\right) = 20\log\left(\frac{4.047106376}{0.002}\right) = 66.12dB$
- Phase = 179.59 degrees

At the upper 3-dB frequency:

This is the frequency at which the amplitude becomes $\frac{1}{\sqrt{2}} = 0.707$ of its low-frequency value, or the phase changes 45 degrees. The closest point to this is when V_o =~2.87V:

- $f_{3dB} = 14077.15\ Hz$
- $A_{Vo} = 20\log\left(\frac{V_o}{V_i}\right) = 20\log\left(\frac{2.872320086}{0.002}\right) = 63.14dB$
- Phase = 135.51 degrees

(2)

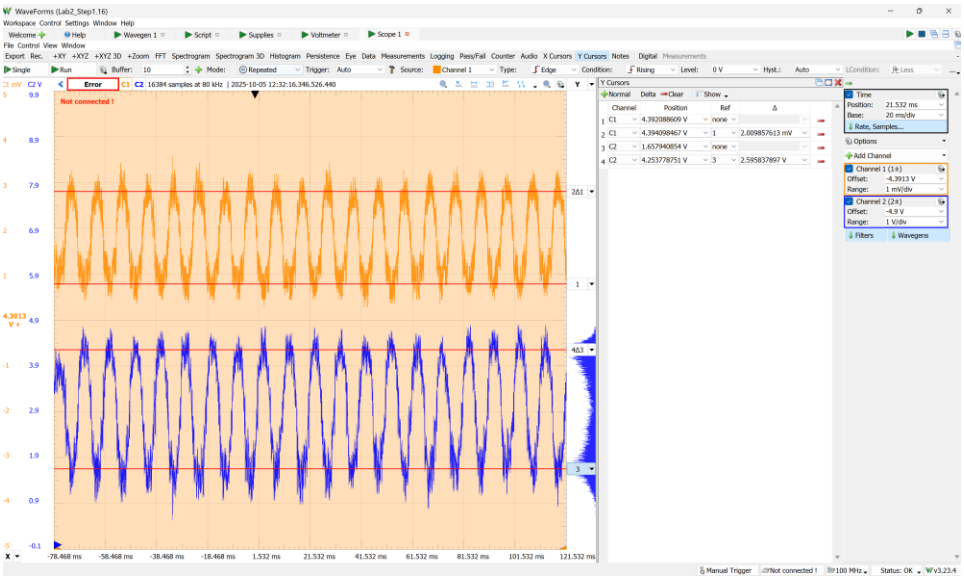

Figure 13: Measurement data obtained from steps 1.18 and 1.19

ΔC1 (V)	ΔC2 (V)	Gain Av (dB)
2.01E-03	2.5958	62.2

The experimental data obtained in steps 1.18 and 1.19 show that this amplifier has a low-frequency gain of around 62.2dB, which is a reasonable result considering the small imperfections that result from real-world measurements. Therefore, the experimental results differ from the simulated results by 5.9%, meaning they verify each other.

(3)

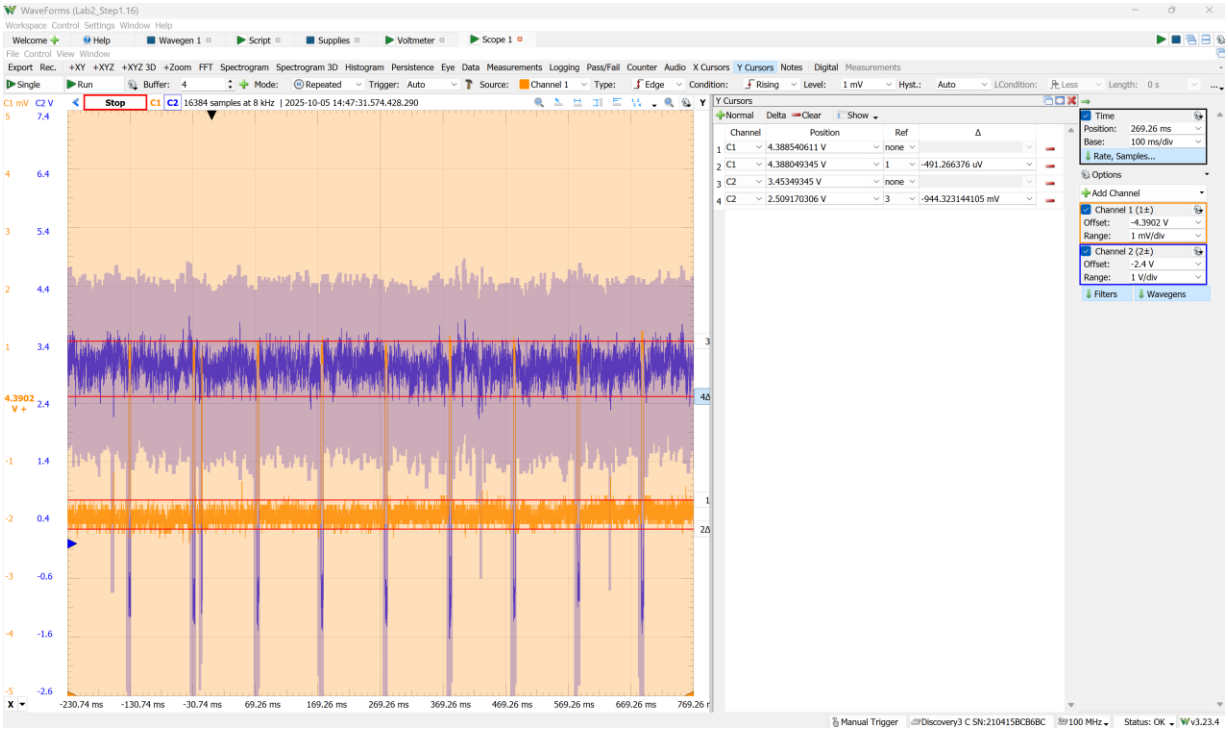

Figure 14: Measurement results for increase in W1 frequency

This is the result of changing the frequency of W1 to match the previously calculated f_{3dB} = 14007 Hz.

$$A_{Vo} = 20\log\left(\frac{V_o}{V_i}\right)$$

$$A_{Vo} = 20\log\left(\frac{0.764192}{0.000491266}\right)$$

$$A_{Vo} = 63.8dB$$

We would theoretically expect $A_v(f_{3dB}) = A_V(100Hz)*0.707 = 44dB$. This means there is likely some error in the experimental data as it doesn't quite align with the simulated data, however there are some similar trends between the two.

Part 2: Differential Amplifier - Common-mode (CM) Signal
A) SPICE Simulation - CM Signal

2.1

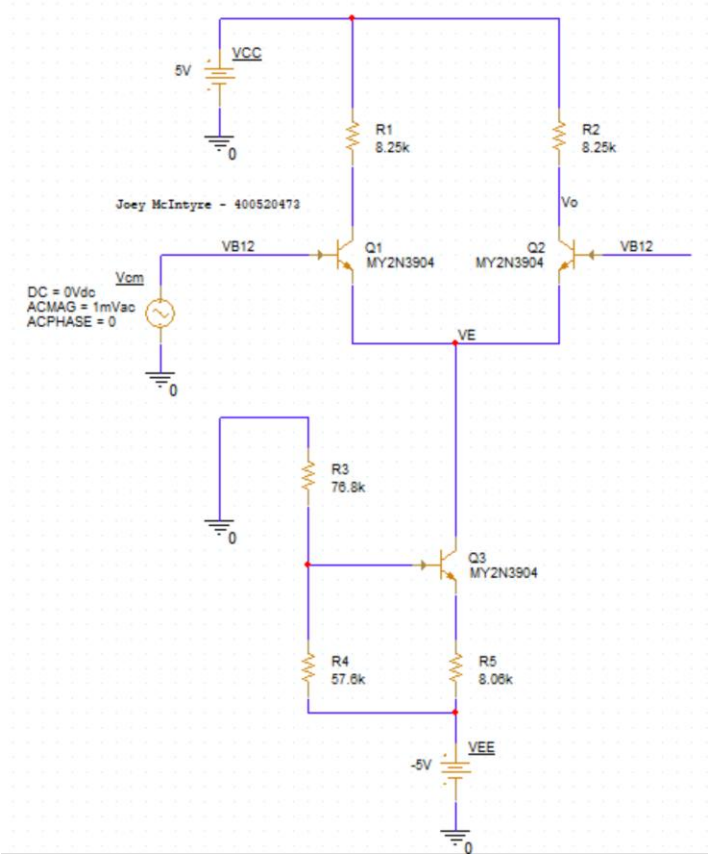

Figure 15: Circuit used for PSpice simulation - CM Signal

2.2

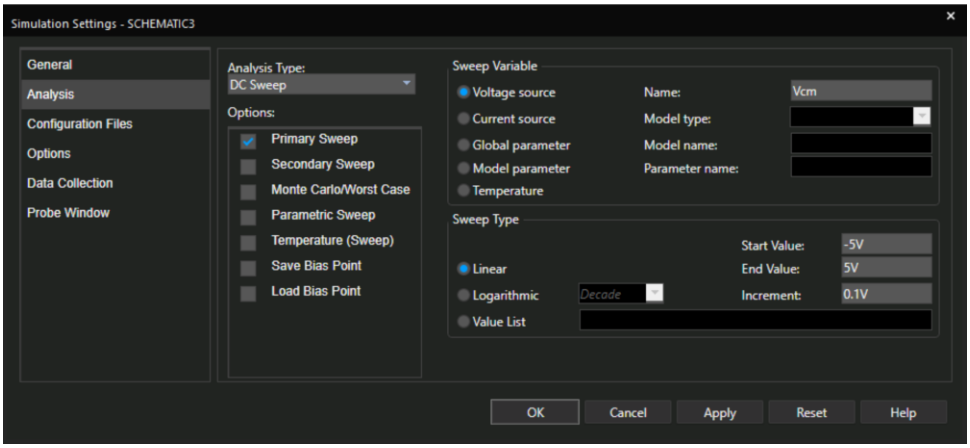

Figure 16: PSpice simulation settings for DC Sweep

2.3

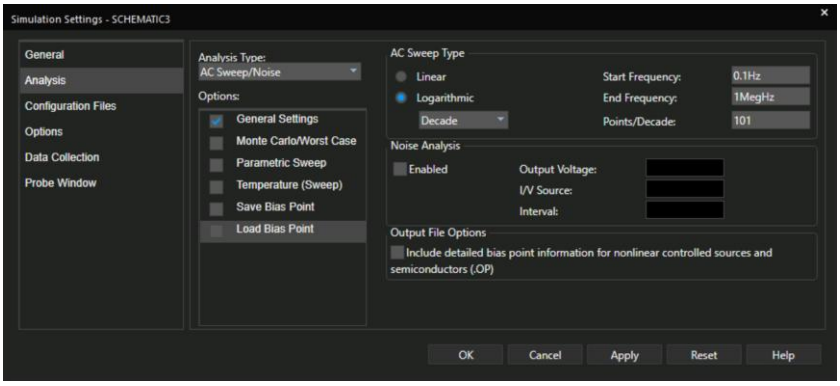

Figure 17: PSpice simulation settings for AC Sweep

B) AD3 Measurement – CM Signal

2.6

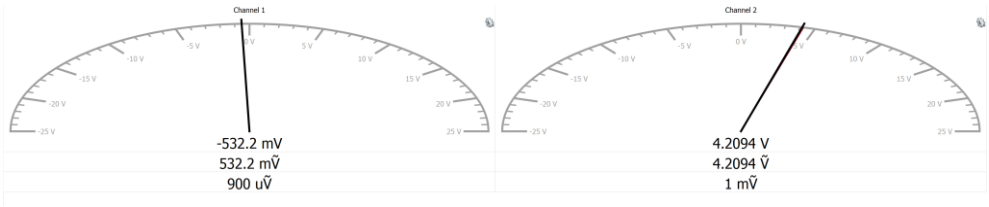

Figure 18: AD3 voltmeter readings to find Quiescent Point

2.7 / 2.8

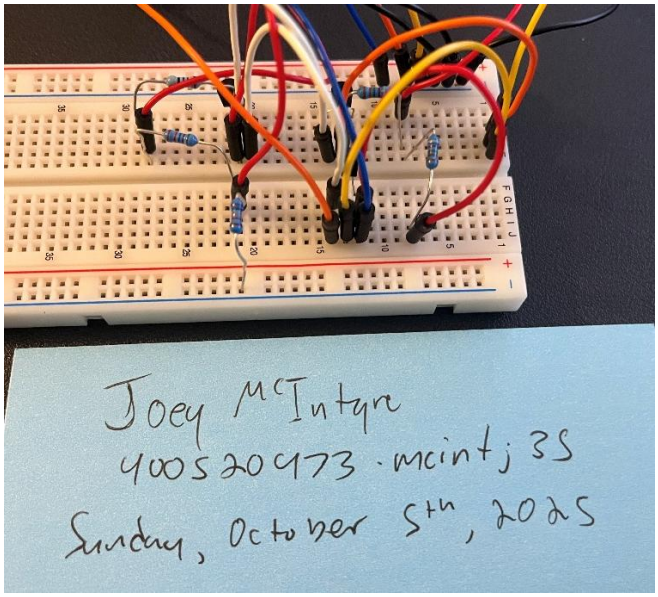

Figure 19: Physical circuit used for AD3 measurement - CM Signal

C) Questions for Part 2

For the differential amplifier designed, answer the following questions with simulated and measured data and discuss any discrepancy between the simulation and measurement results.

Q5. (15 Points) Based on the simulation data obtained in Step 2.2, **(1)** what are the voltages of V_o and V_E, and I_{C2} of Q_2 when $V_{CM} = 0V$, **(2)** what is the input common-mode range (i.e., the voltage range of V_{CM} to maintain the same out voltage), and **(3)** what determines the upper and lower bounds of the input common-mode range? **(4)** Based on the measurement data obtained in Steps 2.7 and 2.8, verify the common-mode range by experimental data.

(1)

When $V_{CM} = 0V$:

$V_o = 4.249991$ V

$V_E = -0.525365$ V

$I_{C2} = 9.10 \times 10^{-5}$ A

(2)

By observing the simulated results from step 2.2, we can see that for V_o (output voltage) to remain constant (at around 4.25 V), V_{CM} must fall between -2.6V and 4.5V.

(3)

The upper and lower bounds of the input common mode range is determined by the individual needs of the transistors. The upper CM limit is determined by the voltage when the current sink transistor cant hold a constant current anymore. The lower CM limit is determined by the voltage at which the input transistors begin to saturate, so the output can't remain constant.

(4)

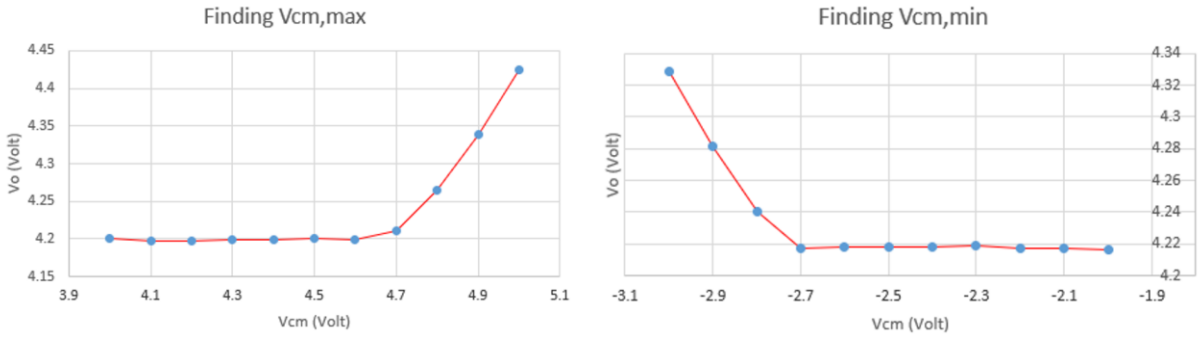

Figure 10: AD3 measurement data from step 2.7 and 2.8

The graphs made from the experimental data collected in steps 2.7 and 2.8 can be used to verify the common-mode range. The graph from step 2.7 shows that the maximum V_{CM} is between 4.5V and 4.7V. The graph from step 2.8 shows that the minimum V_{CM} is between -2.7V and -2.6V. This confirms the simulated range of [-2.6, 4.5].

Q6. (10 Points) Based on the simulated data obtained in Step 2.3, what is the low-frequency voltage gain A_{cm} in dB for the common-mode signal?

In previous questions, the low-frequency voltage gain was found at a frequency of 100Hz, however this question doesn't specify what frequency to use. To keep things consistent, if we consider 100Hz to be low frequency, that it can be observed from the simulated data obtained in step 2.3 that when f = 100Hz, the low-frequency voltage gain is A_{CM} = -86.24 dB.

However, its worth noting that we measured at a frequency as low as f = 0.1Hz, where the common-mode gain was found to be A_{CM} = -86.90.

Part 3: Differential Amplifier – Differential-mode (DM) Signal
A) SPICE Simulation - DM Signal

3.1

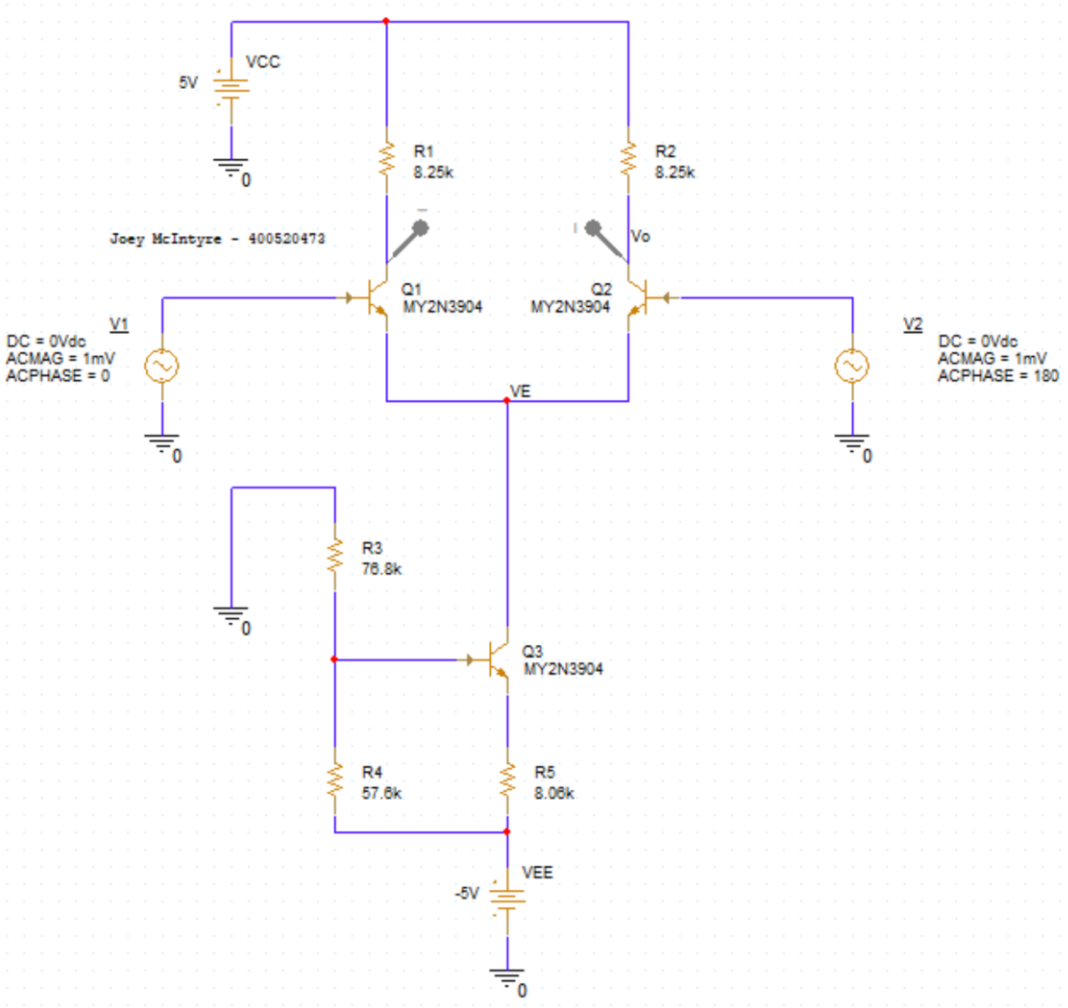

Figure 21: Circuit used for PSpice simulation - DM Signal

3.2

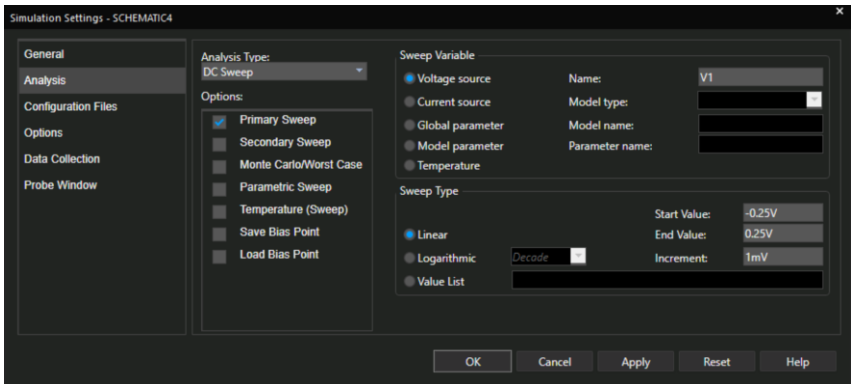

Figure 22: PSpice simulation settings for DC Sweep

3.3

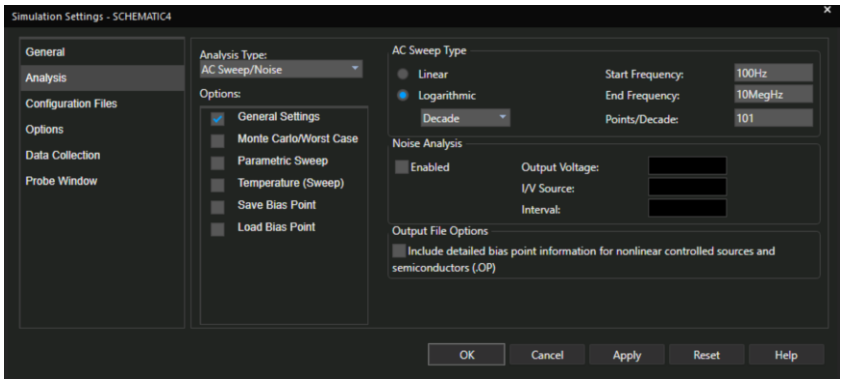

Figure 23: PSpice simulation settings for AC Sweep

B) AD3 Measurement – DM Signal

3.5/3.6

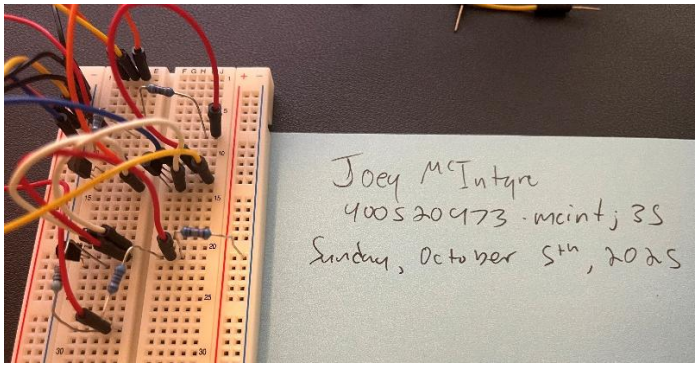

Figure 24: Physical circuit used for AD3 measurement - DM Signal

3.7

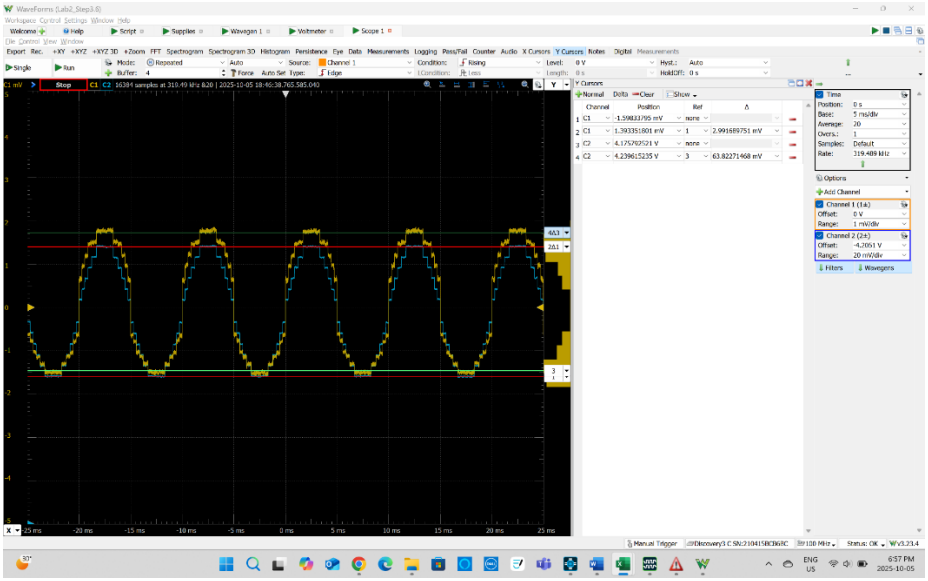

Figure 25: AD3 oscilloscope results

C) Questions for Part 3

For the differential amplifier designed in Part 3, answer the following questions with simulated and measured data and discuss any discrepancy between the simulation and measurement results.

Q7. (10 Points) Based on the simulation data obtained in Step 3.2 and the description in Section 9.2.3 Large-Signal Operation of the textbook, **(1)** what are the DC and AC input differential-mode ranges? **(2)** How do we determine the upper and lower bounds of these input differential-mode ranges?

(1)

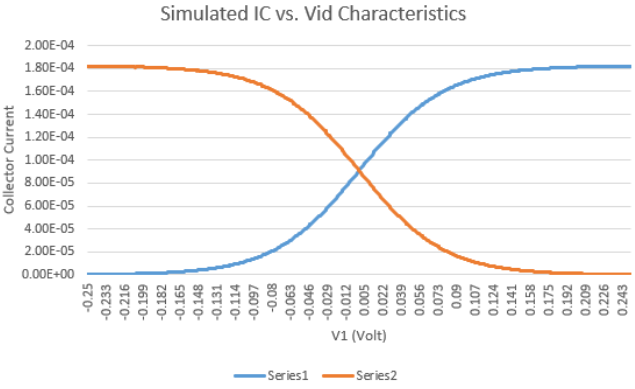

Figure 26: Simulated IC vs Vid Characteristics

The definitions for the DC and AC input differential-mode ranges are defined in our textbook and lecture notes. To begin, we know that V_T of a BJT is the thermal voltage, 25mV or 0.025V. The limitations for the differential input in the AC case is +- V_T / 2 about the POI of the two series, and in the DC case is +- $4V_T$ (formulas from lecture 2 and the textbook). The intersection of the

two series in step 3.2 was found to be at $V_1 = 2.15 * 10^{-16}$ which we can treat as zero. Therefore, the ranges for the differential mode can be calculated:

$$V_{dm\,(AC)} = \left[\left(0 - \frac{0.025}{2}\right)V, \left(0 + \frac{0.025}{2}\right)\right] = [-0.0125\,V, 0.0125\,V]$$

$$V_{DM\,(DC)} = [(0 - 4 * 0.025)V, (0 + 4 * 0.025)] = [-0.1\,V, 0.1\,V]$$

(2)

The DC differential-mode bounds are set where one transistor is essentially off and the other carries almost all the current, which occurs at +- $4V_T$. The AC (small signal) bounds are set by the linearity around where the two signals cross paths. The input needs to be small so that the tanh law is nearly linear. That's why it occurs at +-$V_T/2$.

Q8. (10 Points) (1) Based on the simulation data obtained in Step 3.3, what is the voltage gain A_d in dB for the differential-mode signal? **(2)** Estimate its upper 3-dB frequency f_{3dB} (i.e., the frequency at which the amplitude becomes 0.707 of its low-frequency value or the phase changes 45°) and calculate the gain-bandwidth product (GBW) in hertz (Hz). **(3)** Compare the upper 3-dB frequency f_{3dB} of this differential amplifier with that of the CE amplifier obtained in Q4. **(4)** Based on the measurement data obtained in Step 3.6, calculate the measured low-frequency differential voltage gain A_d in dB.

(1)

Based on the simulation data obtained in step 3.3, the voltage gain A_d for the differential mode signal at 100Hz was 19.63 dB.

(2)

The upper 3dB frequency is when the amplitude becomes 0.707 of its low-frequency or the phase changes 45 degrees. This point of the data from step 3.3 can be observed below:

8332821.508	0.014132946	-45.41565072	16.98	1.42E+08

Therefore, the f_{3dB} = 8332821.508 Hz, and the GBW is 1.42E+08.

(3)

From Question 4: $f_{3dB} = 14077.15\,Hz$

From Question 8: $f_{3dB} = 8332821.508$ Hz

It is clear that the 3-dB frequency is significantly higher in question 8 than in question 4.

(4)

According to the measured data in step 3.6, the differential voltage gain of this amplifier is A_d = 20.6dB. This is calculated in the excel.

Q9. (10 Points) Based on the simulation data, what is the common-mode rejection ratio (CMRR) of the amplifier in dB?

The common-mode rejection ratio can be calculated using a formula discussed in lecture and in the textbook:

$$CMPR = \frac{|A_d|}{|A_{CM}|} = \left|\frac{19.63}{-86.90}\right| = 0.2258918297\ dB$$

NOTE: A_{CM} comes from question 6 in section 2. I decided to use the A_{CM} for the lowest frequency we tested which was f=0.1Hz, as the question didn't specify what frequency to use for the low-frequency voltage gain. If the low-frequency voltage gain was supposed to be calculated at f=100Hz (like it was in numerous other sections), the CMPR would be approximately 0.2276 dB.