

**McMaster University**  
**Electrical and Computer Engineering Department**  
**EE3EJ4 Electronic Devices and Circuits II - Fall 2025**

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**Lab. 3 Multistage Amplifiers**

**Lab Report Due on Nov. 2, 2025**

**Objective:** To characterize BJT-based common-collector (CC) amplifier and current mirror and use them to design a multistage differential amplifier for high-gain applications.

**Attributes Evaluated:** These are the attributes you need to demonstrate in your solutions.

- Competence in specialized engineering knowledge to simulate circuit performance using a SPICE-based circuit simulator and conduct analog circuit debugging;
- Ability to obtain substantiated conclusions as a result of a problem solution, including recognizing the limitations of the approaches and solutions and
- Ability to assess the accuracy and precision of results.

**Test Equipment:**

- Analog Discovery 2 (or 3) (AD2/3)
- [WaveForms from Digilent Link](#)
- [Analog Discovery 2 Quick Start Series Videos](#)
- [WaveForms Reference Manual](#)

**Components:**

- |                |                      |                      |
|----------------|----------------------|----------------------|
| • Transistors: | 5 × NPN-BJT 2N3904   | 2 × PNP-BJT 2N3906   |
| • Resistors:   | 2 × 76.8 kΩ resistor | 2 × 57.6 kΩ resistor |
|                |                      | 2 × 8.06 kΩ resistor |

**Information of Components:**

For a detailed description of these transistors, please check the following websites:

<https://www.onsemi.com/pub/Collateral/2N3903-D.PDF>

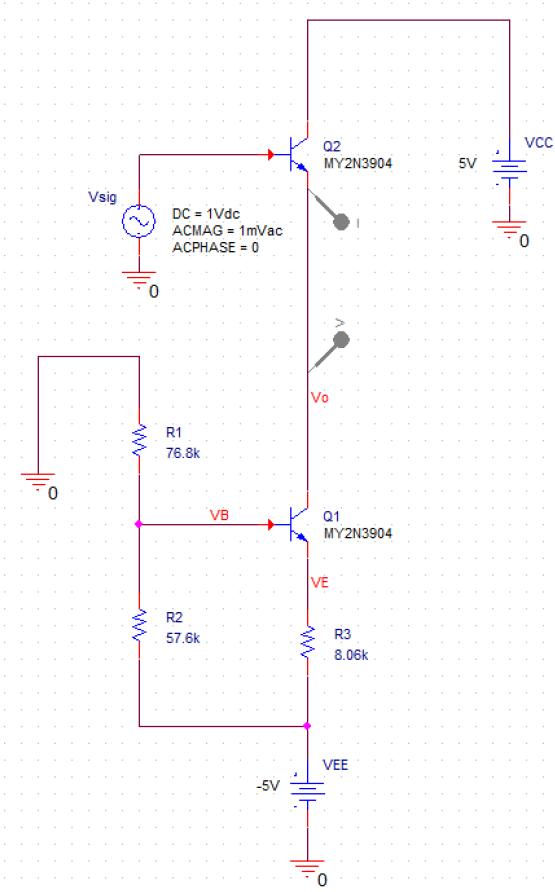
<https://www.onsemi.com/pub/Collateral/2N3906-D.PDF>

**Reminder:** Switch off the DC power suppliers first whenever you need to change the circuit configurations. Switch on the DC power suppliers only when you no longer have to change the circuit connection.

## **Part 1: Common-Collector (CC) Amplifier/Emitter Follower**

### **A. SPICE Simulation**

- 1.1 In [PSpice](#), construct the CC amplifier, as shown in Fig. 1, using an NPN-BJT 2N3904 and the current sink characterized in Fig. 1, Lab 2. Here,  $V_{sig}$  provides the required DC bias for  $Q_2$  and the AC signal for the CC amplifier.
- 1.2 **DC Characteristics:** Sweep the DC voltage of  $V_{sig}$  from -5 V to 5V with a 0.5 V step and measure the output voltage  $V_o$  at the emitter of  $Q_2$  and the emitter current  $I_{E2}$  of  $Q_2$ . In the PSpice simulator window, (1) Edit -> Select All, and (2) Edit -> Copy. Open Excel and paste the data into an Excel sheet. Record the simulated  $V_o$  and  $I_{E2}$  in the sheet “Step 1.2” of the Excel file “Lab 3 – Multistage Amplifier.xlsx”. Mark the DC value of  $V_{sig} = V_{BQ2}$ , which results in  $V_o \approx 0V$ .
- 1.3 **Frequency Response:** Set the DC value of  $V_{sig} = V_{BQ2}$  and the AC amplitude of  $V_{sig} = 1$  mV. Conduct AC sweep for  $V_o$  in Logarithmic with Start Frequency = 100 Hz, End Frequency = 1 MegHz, and Points/Decade = 101. In the simulator window, click the Add Trace icon , choose Plot Window Templates under Functions or Macros, select Bode Plot – dual Y axes(1), select V(Vo) in Simulation Output Variables, and press OK. Record the simulated magnitude and phase of  $V_o$  in the sheet “Step 1.3” of the Excel file “Lab 3 – Multistage Amplifier.xlsx”.



**Fig. 1** Schematic diagram of the common-collector (CC) amplifier

## B. AD2/3 Measurement

- 1.4 Based on Fig. 1, construct the measurement setup for the common-collector (CC) amplifier. Use  $V_+ = 5V$  for  $V_{CC}$ ,  $V_- = -5V$  for  $V_{EE}$ , and Wavegen 1 (W1) for  $V_{sig}$ . Connect GNDV+, GNDV-, and GNDW1 to a common ground line.
- 1.5 Connect Scope Ch. 1 Positive (1+) to  $V_{sig}$  at the base of  $Q_2$  and Scope Ch. 2 Positive (2+) to  $V_o$  at the emitter of  $Q_2$ . Connect Scope Ch. 1 Negative (1-) and Scope Ch. 2 Negative (2-) to the common ground.
- 1.6 **DC Characteristics:** In WaveForms, click Workspace, open the provided workspace script “Lab3\_Step1.6.dwf3work”, and press Run. This script will sweep the DC voltage of Wavegen 1 (W1) from -5 V to 5 V with a 0.5 V step and measure the input voltage  $V_{sig}$  at the base of  $Q_2$  and the output voltage  $V_o$  at the emitter of  $Q_2$ , respectively. Record the measured  $V_{sig}$  and  $V_o$  in the sheet “Step 1.6” of the Excel file “Lab 3 – Multistage Amplifier.xlsx”.
- 1.7 **AC Voltage Gain:** In WaveForms, click Workspace, open the provided workspace script “Lab3\_Step1.7.dwf3work”, and press Run. This script will enable Channel 1 (W1), set the Type = Sine, Frequency = 100 Hz, Amplitude = 1 mV (Note: in theory, the amplitude cannot exceed  $0.2V_T = 5$  mV), Symmetry = 50%, and Channel 1 (W1) Phase = 0°. It returns the voltage gain  $A_v$ . It also finds the  $V_{sig} = V_{BQ2}$  to result in  $V_o \approx 0$  V and sets the offset voltage of W1 accordingly.
- 1.8 **Using Scopes:** Display the measurement results using the Scope function in WaveForms. Use Y Cursors to set their upper and lower peak values and the Ref function to calculate the difference. Record the measured amplitudes of Scope Ch. 1 Positive (1+) and Scope Ch. 2 Positive (2+) in the sheet “Step 1.8” of the Excel file “Lab 3 – Multistage Amplifier.xlsx” to calculate the voltage gain  $A_v$  in dB. Copy and paste the screenshot of the measurement results to replace the one in the sheet “Step 1.8” of the Excel file “Lab 3 – Multistage Amplifier.xlsx” to support your calculation. Capture the date and time of your PC in the screenshot to avoid mark deduction.
- 1.9 Disconnect the circuit from the power supply  $V_{CC}$ , but keep the rest of the CC amplifier circuit connected. We will use it again in Step 3.9 in Part 3 and Lab 4 to design a directly coupled operational amplifier.

## C. Questions for Part 1

For the common collector (CC) amplifier characterized, answer the following questions with simulated and measured data and discuss any discrepancy between the simulation and measurement results.

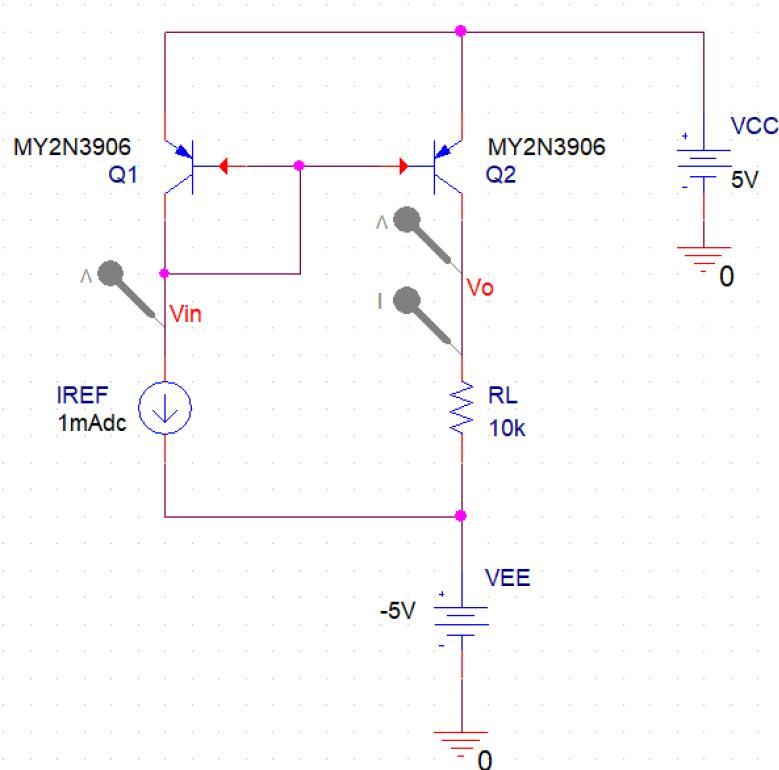
**Q1. (15 Points)** Based on the simulation and measurement data obtained in Steps 1.2 and 1.6, (1) plot the simulated and measured  $V_o$  vs.  $V_{sig}$  characteristics and discuss/justify the characteristics. (2) To ensure the circuit works as a common-collector (CC) amplifier, find the DC input range for  $V_{sig}$  and the output voltage range for  $V_o$ . (3) Find the  $V_{sig}$  value that results in  $V_o \approx 0$  V.

**Q2. (10 Points)** Based on the simulation and measurement data obtained in Steps 1.3 and 1.8, what are the simulated and measured intrinsic voltage gain  $A_{vo}$  at low frequency (i.e., 100 Hz) for this CC amplifier? Report its magnitude in dB and phase in degree.

## **Part 2: Differential Amplifier with Current Mirror (CM) Load**

### **A. SPICE Simulation – DC Analysis of a Current Mirror**

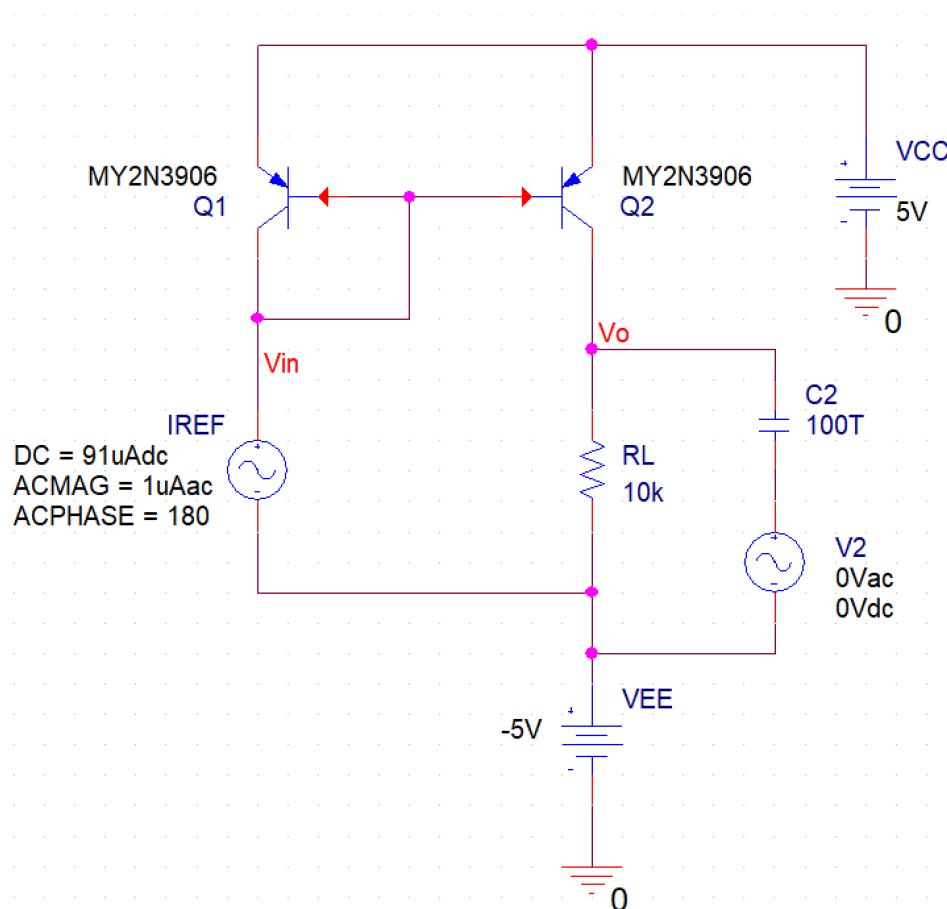
- 2.1 The current mirror transfers the AC signal to the output port from one side of a differential pair. To characterize a current mirror, construct the circuit in [PSpice](#) with the resistance value and supply voltages, as shown in Fig. 2. Here, the current source  $I_{REF}$  represents the reference current to be transferred, and the  $R_L$  represents the load at the output of the current mirror.
- 2.2 **DC Characteristics:** Sweep  $I_{REF}$  from 0.1 mA to 1 mA with a 0.01 mA current step, measure the output current  $I_o$ , which is the current flowing into the resistor  $R_L$ , and the voltages  $V_{in}$  and  $V_o$  at the collectors of Q1 and Q2, respectively. Record the simulated  $I_{REF}$ ,  $I_o$ ,  $V_{in}$ , and  $V_o$  in the sheet “Step 2.2” of the Excel file “Lab 3 – Multistage Amplifier.xlsx”.
- 2.3 **Quiescent (Q-) Point Characterization:** Sweep  $I_{REF}$  from 85  $\mu$ A to 95  $\mu$ A with 0.1  $\mu$ A current step, measure the output current  $I_o$ , which is the current flowing into the resistor  $R_L$ , and the voltages  $V_{in}$  and  $V_o$  at the collectors of  $Q_1$  and  $Q_2$ , respectively. This sweeping range corresponds to the designed bias current of the transistor in the differential-pair amplifier. Record the simulated  $I_{REF}$ ,  $I_o$ ,  $V_{in}$ , and  $V_o$  in the sheet “Step 2.3” of the Excel file “Lab 3 – Multistage Amplifier.xlsx”.



**Fig. 2** Schematic diagram of the current mirror for the DC analysis

## B. SPICE Simulation – Two-Port Network of a Current Mirror

- 2.4 As shown in Fig. 3, construct the circuit using [PSpice](#). Here,  $C_2$  is a dummy bypass capacitor with 100 TF, and  $V_2$  is a dummy AC voltage source as the port 2 stimulus used in the AC analysis.
- 2.5 **Current Gain & Input Impedance:** Set the DC value of  $I_{REF} = 91.0 \mu\text{A}$  (the DC current of each differential pair amplifier in Part 2, Lab 2) and its AC magnitude to  $1 \mu\text{A}$ . Since SPICE uses a passive sign convention, i.e., positive current flows from the (+) node of the current/voltage source to its (-) node, we set its AC phase to  $180^\circ$  for the current flowing into  $V_{in}$ , as required by the linear two-port network theory. Set the DC and AC voltages of  $V_2$  equal to zero. Conduct AC sweep in Linear with Start Frequency = 100 Hz, End Frequency = 200 Hz, and Total Points = 11. Record the simulated magnitude and phase of  $V_{in}$  and  $I_2$  in the sheet “Step 2.5” of the Excel file “Lab 3 – Multistage Amplifier.xlsx”.
- 2.6 **Output Impedance:** Set the DC value of  $I_{REF} = 91.0 \mu\text{A}$  and its AC value to 0  $\mu\text{A}$ . Set the DC value of  $V_2$  to 0 V and the AC voltage of  $V_2$  to 1  $\mu\text{V}$  in magnitude and 0 degree in phase. Conduct AC sweep in Linear with Start Frequency = 100 Hz, End Frequency = 200 Hz, and Total Points = 11. Record the simulated magnitude and phase of  $V_{in}$  and  $I_2$ , i.e., the current flowing through  $V_2$ , in the sheet “Step 2.6” of the Excel file “Lab 3 – Multistage Amplifier.xlsx”.



**Fig. 3** Schematic diagram of the current mirror for the AC analysis

### C. Questions for Part 2

For the current mirror designed in Part 2, answer the following questions with simulated data and justify the simulation results.

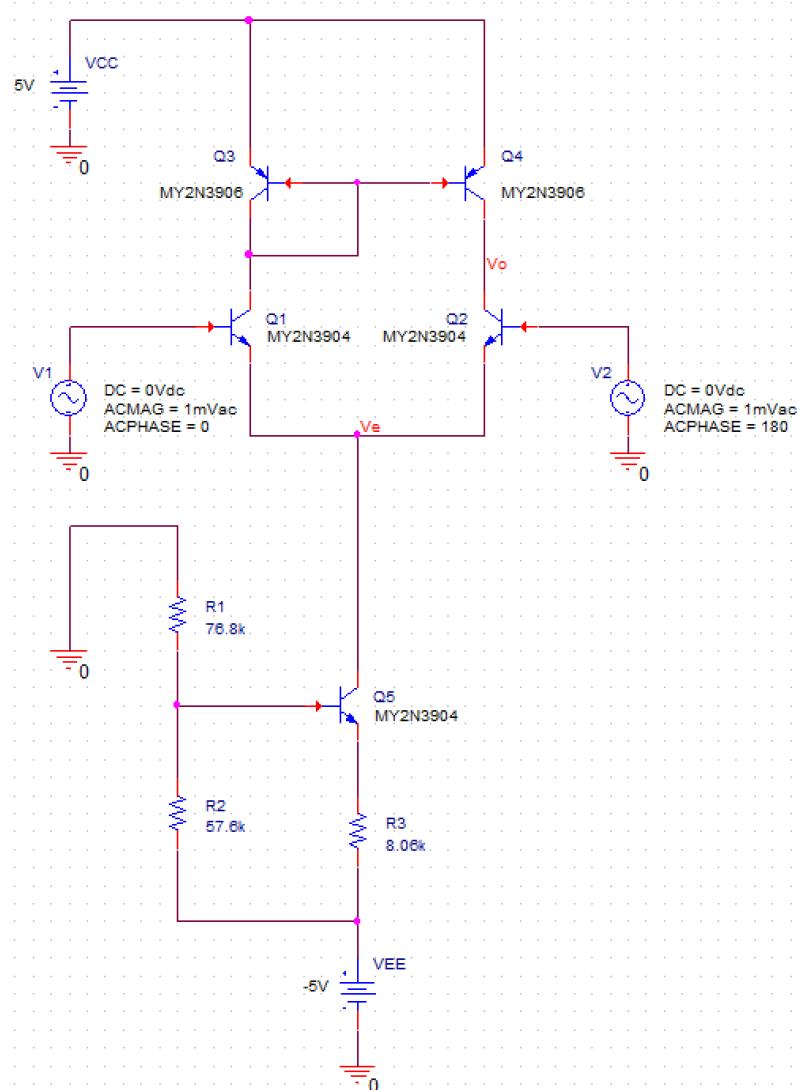
**Q3. (15 Points)** (1) Based on Section 8.2.3 in the textbook, derive the relationship to express  $I_o$  as a function of  $I_{REF}$ . (2) Based on the simulation data obtained in Step 2.2, when  $I_{REF}$  is 0.1 mA, how is  $I_o$  compared with  $I_{ERF}$ ? When  $I_{REF}$  is 1 mA, how is  $I_o$  compared with  $I_{ERF}$ ? (3) Justify the observation between the theoretical prediction and the simulated result at  $I_{REF}$  is 0.1 mA and 1 mA, respectively.

**Q4. (15 Points)** (1) Based on the simulation data obtained in Step 2.5, what is the input impedance  $R_{in}$  looking from  $V_{in}$  toward the collector of Q1? What is the current gain  $A_i$  of the current mirror? (2) Based on the simulation data obtained in 2.6, what is the output impedance  $R_o$  of the current mirror looking into the collector of Q2? (3) Based on the information obtained in (1) and (2), draw the linear two-port network for the current mirror using its  $h$ -parameters.

### **Part 3: Differential Amplifier with a Current Mirror (CM) Load**

#### **A. SPICE Simulation**

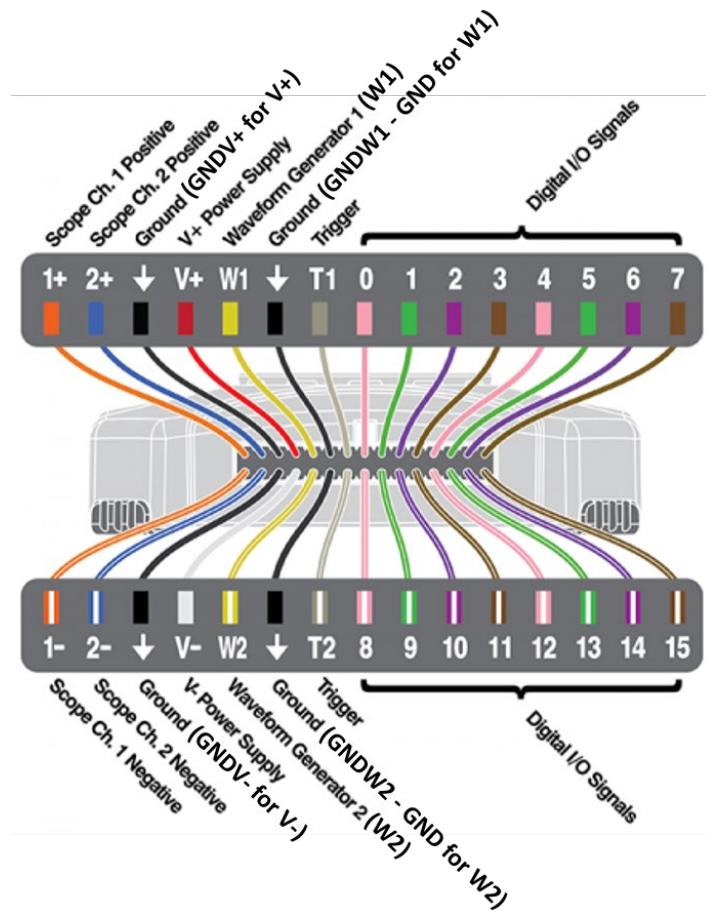
- 3.1 As shown in Fig. 4, construct a differential amplifier in [PSpice](#) using the current mirror (CM) load characterized in Part 1.
- 3.2 **Frequency Response:** Set the DC values of  $V_1$  and  $V_2 = 0$  V and their AC amplitude 1 mV. For the differential-mode signal, set the phases of the AC signal  $V_1$  and  $V_2$  to be  $0^\circ$  and  $180^\circ$ , respectively, as shown in Fig. 4. In this setting, the differential-mode signal  $v_{id} = V_1 - V_2 = 1$  mV – ( $-1$  mV) = 2 mV. Conduct AC sweep for  $V_o$  in Logarithmic with Start Frequency = 100 Hz, End Frequency = 100 kHz, and Points/Decade = 101. In the simulator window, click the Add Trace icon , choose Plot Window Templates under Functions or Macros, select Bode Plot – dual Y axes(1), select V(Vo) in Simulation Output Variables, and press OK. Record the simulated magnitude and phase of  $V_o$  in the sheet “Step 3.2” of the Excel file “Lab 3 – Multistage Amplifier.xlsx”.



**Fig. 4** Schematic diagram of the differential amplifier with a CM load for differential-mode analysis  
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## B. AD2/3 Measurement

- 3.3 Use the port definition diagram of the AD2/3 shown in Fig. 5 when setting up your circuits.
- 3.4 Based on Fig. 4, construct the measurement setup for the differential amplifier with a current mirror load. **Tip:** Replace the two  $8.25\text{ k}\Omega$  resistors in Lab 2 with the current mirror.



**Fig. 5** Diagram for the port definition of an Analog Discovery 2 (or 3) (AD2/3)

- 3.5 Use  $V_+ = 5\text{V}$  for  $V_{CC}$ ,  $V_- = -5\text{V}$  for  $V_{EE}$ , Wavegen 1 (W1) for  $V_1$  and Wavegen 2 (W2) for  $V_2$ . Connect GNDV+, GNDV-, GNDW1, and GNDW2 to a common ground line.
- 3.6 **DC Offset Voltage:** Due to the finite  $\beta$  and Early effect of  $Q_3$  and  $Q_4$ , as described in **Error! Reference source not found.** and **Error! Reference source not found.**, they result in a mismatch between the collector currents of  $Q_1$  and  $Q_2$ . We need to balance their DC currents by applying offset voltage to  $Q_2$  (or  $Q_1$ ). To find the required DC offset voltage, connect Scope Ch. 1 Positive (1+) to the collector of  $Q_1$  and Scope Ch. 2 Positive (2+) to  $V_o$  (i.e., the collector of  $Q_2$ ). In WaveForms, click Workspace, open the provided workspace script “Lab3\_Step3.6.dwf3work”, and press Run. This script will set the offset voltage of Wavegen 1 (W1) to 0 V and gradually change the offset voltage of Wavegen 2 (W2) until the DC voltages  $V_{C1}$  at the collector of  $Q_1$  and  $V_o$  at the collector of  $Q_2$  are the same (or very close). Record the measured  $V_{C1}$  and  $V_o$  in the sheet “Step 3.6” of the Excel file “Lab 3 – Multistage

Amplifier.xlsx". **Tip:** Calculate  $V_{BC3}$  of  $Q_3$  by  $V_{BC3} = V_{C1} - V_o$  to ensure  $V_{BC3}$  is larger than -0.4 V to have  $Q_3$  work in the active region. If  $Q_3$  does not work in the active region (e.g.,  $V_{C1} = 4.39$  V and  $V_o = 4.93$  V),  $Q_3$  and  $Q_4$  no longer function as a current mirror.

- 3.7 **Differential-mode Voltage Gain:** Connect Scope Ch. 1 Positive (1+) to Wavegen 1 (W1), Scope Ch. 2 Positive (2+) to  $V_o$  (the collector of  $Q_2$ ). In WaveForms, click Workspace, open the provided workspace script "Lab3\_Step3.7.dwf3work", change the W2Offset value in the script to the value obtained in Step 3.6 and press Run. This script will enable both Channel 1 (W1) and Channel 2 (W2) and set their Type = Sine, Frequency = 100 Hz, Amplitude = 1 mV, Channel 1 (W1) Offset = 0 V, Channel 2 (W1) Offset = W2Offset, Symmetry = 50%, the Channel 1 (W1) Phase = 0°, and Channel 2 (W2) Phase = 180°. It will return the differential-mode gain  $A_{vd}$  in dB.
- 3.8 **Using Scopes:** Display the measurement results using the Scope function in WaveForms. Use Y Cursors to set their upper and lower peak values and the Ref function to calculate the difference. Record the measured peak-to-peak amplitudes of Scope Ch. 1 Positive (1+) and Scope Ch. 2 Positive (2+) in the sheet "Step 3.8" of the Excel file "Lab 3 – Multistage Amplifier.xlsx" to calculate the differential-mode voltage gain  $A_{vd}$  in dB. Copy and paste the screenshot of the measurement results to replace the one in the sheet "Step 3.8" of the Excel file "Lab 3 – Multistage Amplifier.xlsx" to support your calculation. Make sure to capture the date and time of your PC in the screenshot to avoid mark deduction.
- 3.9 **Multistage Amplifier Gain:** Connect the output (the collector of  $Q_2$  in Fig. 4) of the differential amplifier to the input (the base of  $Q_2$  in Fig. 1) of the common-collector (CC) amplifier to form a multistage (or 2-stage) amplifier. Connect Scope Ch. 2 Positive (2+) to  $V_o$  (the emitter of  $Q_2$  in Fig. 1). Run workspace script "Lab3\_Step3.7.dwf3work" again with the same W2Offset value set in Step 3.7. Display the measurement results using the Scope function in WaveForms. Use Y Cursors to set their upper and lower peak values and the Ref function to calculate the difference. Record the measured peak-to-peak amplitudes of Scope Ch. 1 Positive (1+) and Scope Ch. 2 Positive (2+) in the sheet "Step 3.9" of the Excel file "Lab 3 – Multistage Amplifier.xlsx" to calculate the differential-mode voltage gain  $A_{vd}$  in dB. Copy and paste the screenshot of the measurement results to replace the one in the sheet "Step3.9" of the Excel file "Lab 3 – Multistage Amplifier.xlsx" to support your calculation. Make sure to capture the date and time of your PC in the screenshot to avoid mark deduction.
- 3.10 Disconnect the circuit from the power supply  $V_{CC}$ , but keep the rest of the differential amplifier connected. We will use it again in Lab 4 to design a directly coupled operational amplifier.

## C. Questions for Part 3

For the differential amplifier designed in Part 3, answer the following questions with simulated and measured data and discuss any discrepancy between the simulation and measurement results.

**Q5. (15 Points)** (1) Based on the simulation data obtained in Step 3.2, what is the voltage gain  $A_d$  in dB for the differential-mode signal? (2) Did you observe any mismatch in Step 3.6? If yes, how much offset voltage did you apply at  $V_2$ ? (3) Compare your simulated result with the measured result obtained in Step 3.8.

**Q6. (10 Points)** Estimate its upper 3-dB frequency  $f_H$  (i.e., the frequency at which the amplitude becomes  $1/\sqrt{2} = 0.707$  of its low-frequency value or the phase changes  $45^\circ$ ).

**Q7. (10 Points)** Compare the upper 3-dB frequency  $f_{3\text{dB}}$  of this differential amplifier with a current mirror load with that of the differential amplifier using resistive loads obtained in Q8 of Lab 2. Why does the differential amplifier with the current mirror load have a smaller  $f_{3\text{dB}}$ ?

**Q8. (10 Points)** What are the gain-bandwidth products (GBW) in Hz of the two differential amplifiers with the current mirror load and the resistive load, respectively?