Lab 3 – Multistage Amplifiers

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ELECENG 3EJ4 – Electronic Devices and Circuits II

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Part 1: Common-Collector (CC) Amplifier/Emitter Follower

A) SPICE Simulation

1.1

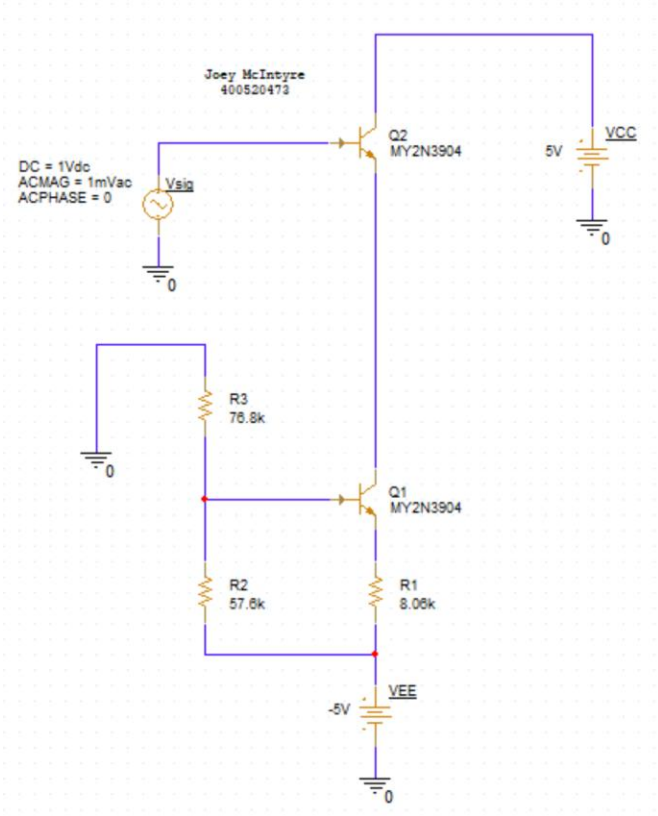


Figure 1: Circuit used for PSpice simulation - Common-collector amplifier

1.2

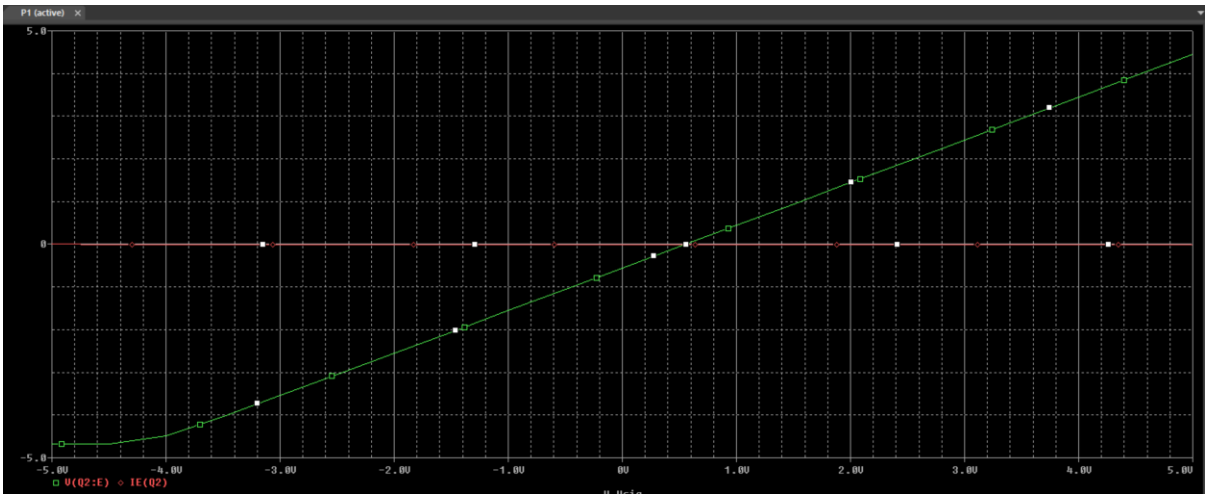


Figure 2: PSpice simulation results – DC Sweep

$V_{BQ2} = V_{sig}$ when V_o is closest to 0 = 0.5V

1.3

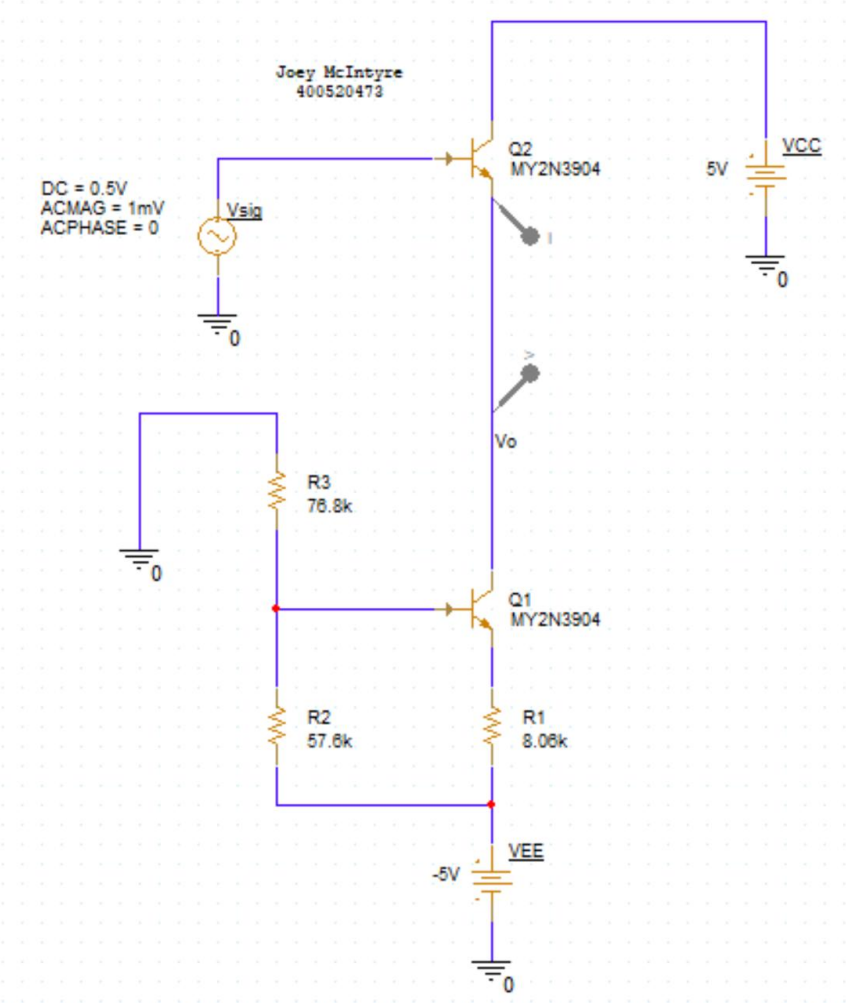


Figure 3: Circuit used for PSpice simulation - Common-collector amplifier

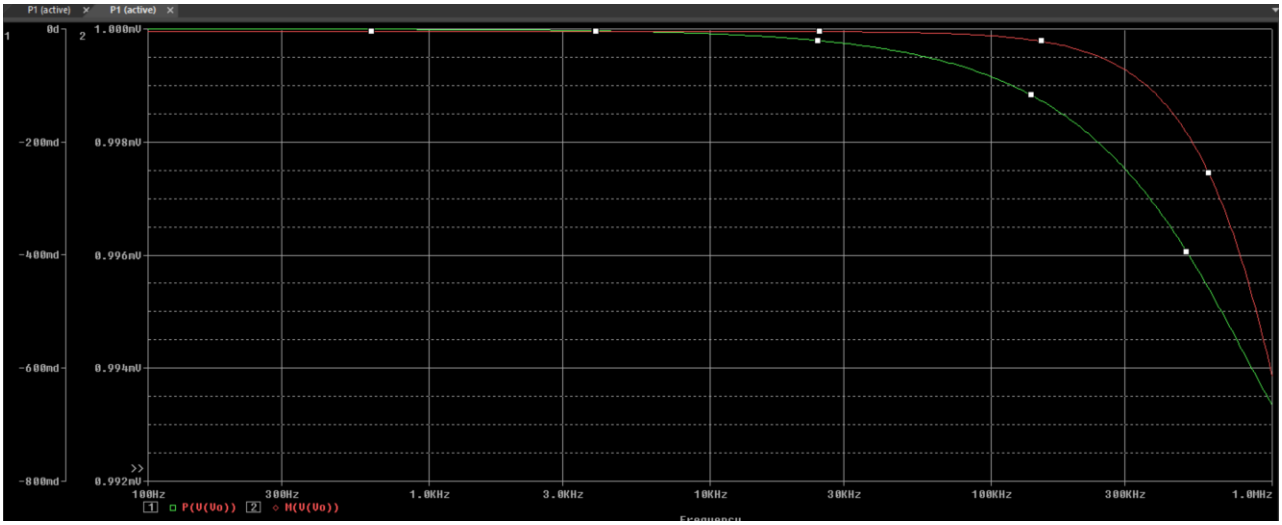


Figure 4: PSpice simulation results - AC sweep

B) AD3 Measurement

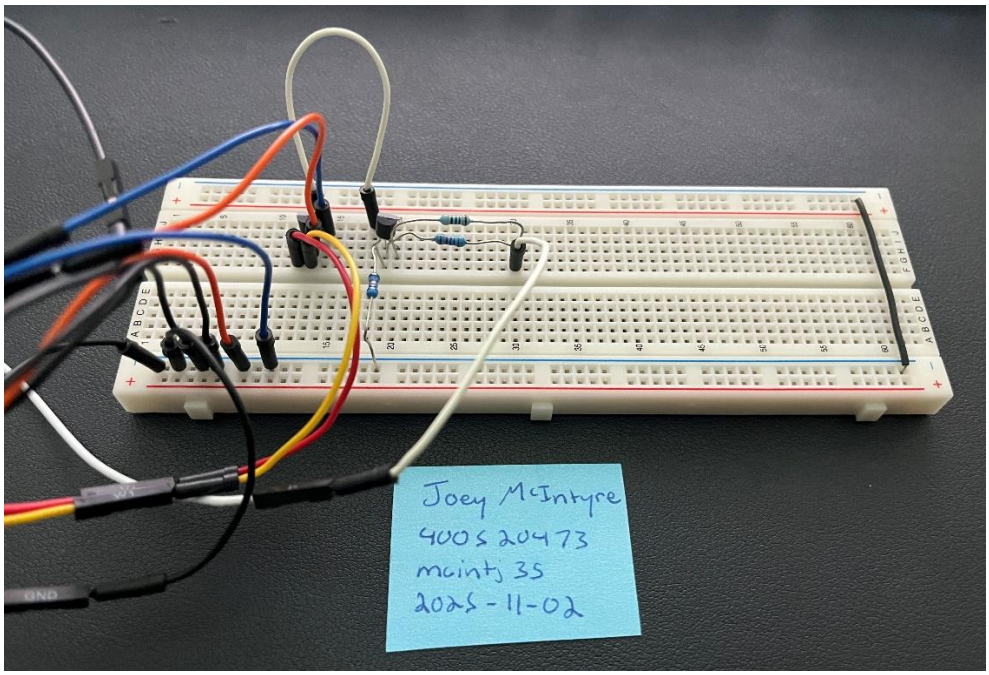


Figure 5: Physical circuit used for AD3 measurement - Common-collector amplifier

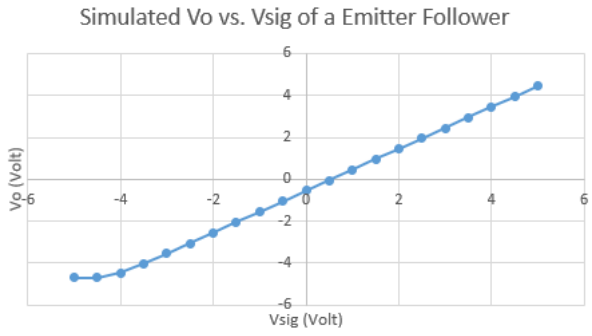
C) Questions for Part 1

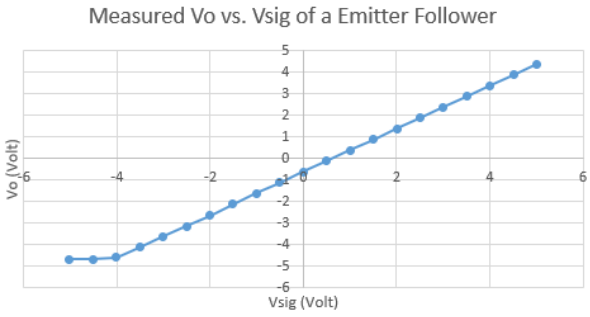
Q1. (15 Points) Based on the simulation and measurement data obtained in Steps 1.2 and 1.6, **(1)** plot the simulated and measured V_0 vs. V_{sig} characteristics and discuss/justify the characteristics. **(2)** To ensure the circuit works as a common-collector (CC) amplifier, find the DC input range for V_{sig} and the output voltage range for V_o. **(3)** Find the V_{sig} value that results in V_o = 0V.

(1)

Below are the graphs from the simulation and measurement data obtained in steps 1.2 and 1.6 respectively.

It can be observed that the graphs of the simulated and measured data are almost identical. They follow the same shape, range of values, all the way down to each data point. Both graphs show a linear relationship between V_o and V_{sig}. This confirms the validity of each experiment.





(2)

Based on the obtained data, the DC input range for V_{sig} and the output voltage range for V_o that allows the circuit to operate as a common collector amplifier can be determined.

The range for V_{sig} can be observed to be -4.5V <= V_{sig} <= 5V. The output range for V_o can be observed to be -4.5V <= V_o <= 4.5V.

(3)

According to the simulated data obtained in step 1.2, the V_{sig} value that results in V_o closest to 0 (V_o = -0.0526V) is V_{sig} = 0.5V. According to the measured data, the V_{sig} value that results in V_o closest to 0 (V_o = -0.113V) is also V_{sig} = 0.5V (measured to actually be Vsig = 0.489V using CH1).

Below are images of the simulated data and the measured data, with the V_{sig} value that results in V_o closest to 0 in bold text.

Vsig	Vo	IE2
Volts	Volts	Amps
-5	-4.683472277	2.24E-09
-4.5	-4.683223253	-3.15E-08
-4	-4.478345155	-2.82E-05
-3.5	-4.024650411	-9.13E-05
-3	-3.545404773	-0.000154408
-2.5	-3.052495105	-0.000184748
-2	-2.552539257	-0.000184869
-1.5	-2.052561188	-0.00018499
-1	-1.552583106	-0.000184863
-0.5	-1.052605055	-0.000184736
0	-0.552626992	-0.000184876
0.5	**-0.052648962**	**-0.000185017**
1	0.44732908	-0.000184889
1.5	0.947307092	-0.000184762
2	1.447285115	-0.000184902
2.5	1.947263106	-0.000185043
3	2.447241107	-0.000184915
3.5	2.94721908	-0.000184788
4	3.447197061	-0.000184928
4.5	3.947175015	-0.000185069
5	4.447152937	-0.000184941

Vsig (W1)	Vsig (CH1)	Vo (CH2)
Volts	Volts	Volts
-5	-5.01886	-4.67858
-4.5	-4.51664	-4.67758
-4	-4.01444	-4.57112
-3.5	-3.51796	-4.10638
-3	-3.00764	-3.62418
-2.5	-2.50932	-3.12634
-2	-2.00346	-2.62964
-1.5	-1.5091	-2.12458
-1	-1.00444	-1.62558
-0.5	-0.50438	-1.124
0	-0.00604	-0.62072
0.5	**0.48946**	**-0.11336**
1	1.00562	0.37712
1.5	1.5062	0.87718
2	2.00494	1.37928
2.5	2.50318	1.87934
3	3.00098	2.38304
3.5	3.50578	2.88082
4	4.0023	3.38636
4.5	4.50968	3.88098
5	5.00744	4.38446

Q2: (10 Points) Based on the simulation and measurement data obtained in Steps 1.3 and 1.8, what are the simulated and measured intrinsic voltage gain A_{vo} at low frequency (i.e. 100 Hz) for this CC amplifier? Report its magnitude in dB and phase in degrees.

Based on the simulation data obtained in step 1.3, the intrinsic voltage gain A_{vo} at low frequency (100Hz) for this CC amplifier has a magnitude of 0.00dB. Based on the measurement data obtained in step 1.8, the intrinsic voltage gain A_{vo} at low frequency for this CC amplifier has a magnitude of 2.0dB. These both occur at a phase of approximately $-8.47 * 10^{-5}$ degrees.

Part 2: Differential Amplifier with Current Mirror (CM) Load

A) SPICE Simulation – DC Analysis of a Current Mirror

2.1

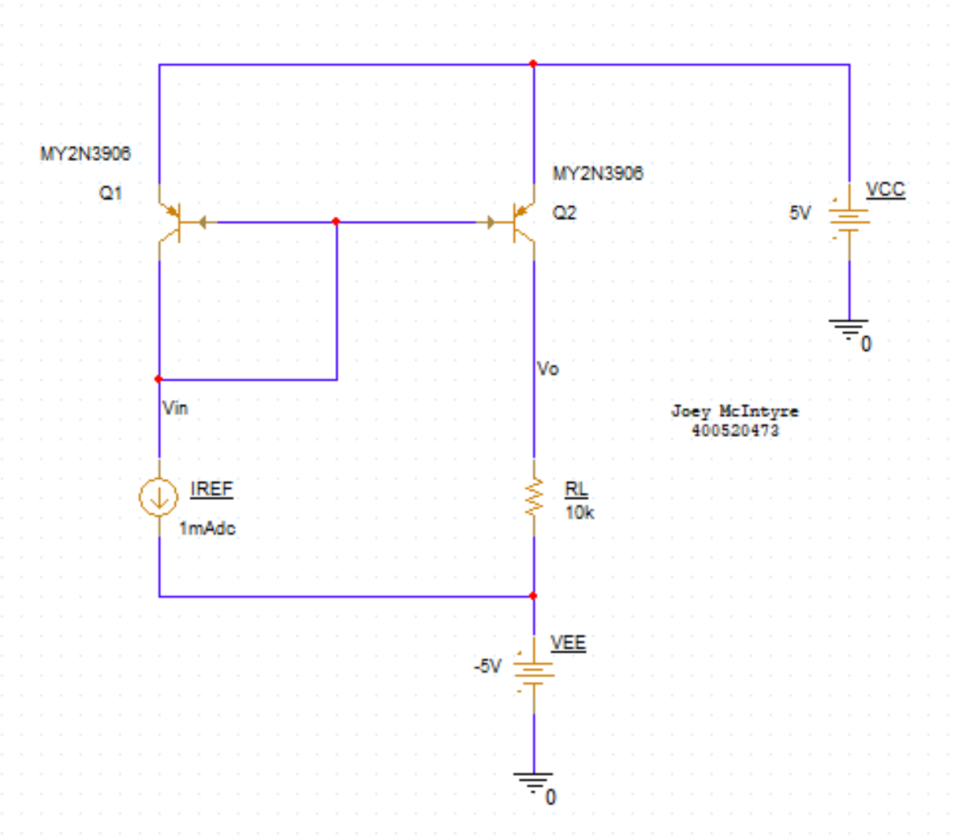


Figure 6: Circuit used for PSpice simulation - Current mirror

2.2

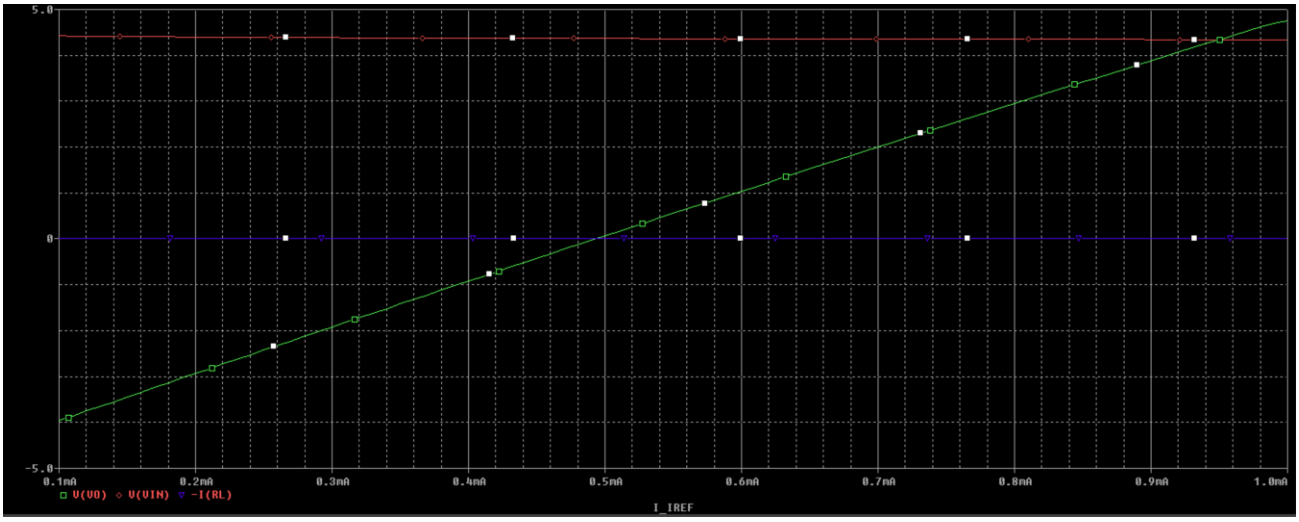


Figure 7: PSpice simulation results – DC sweep

2.3

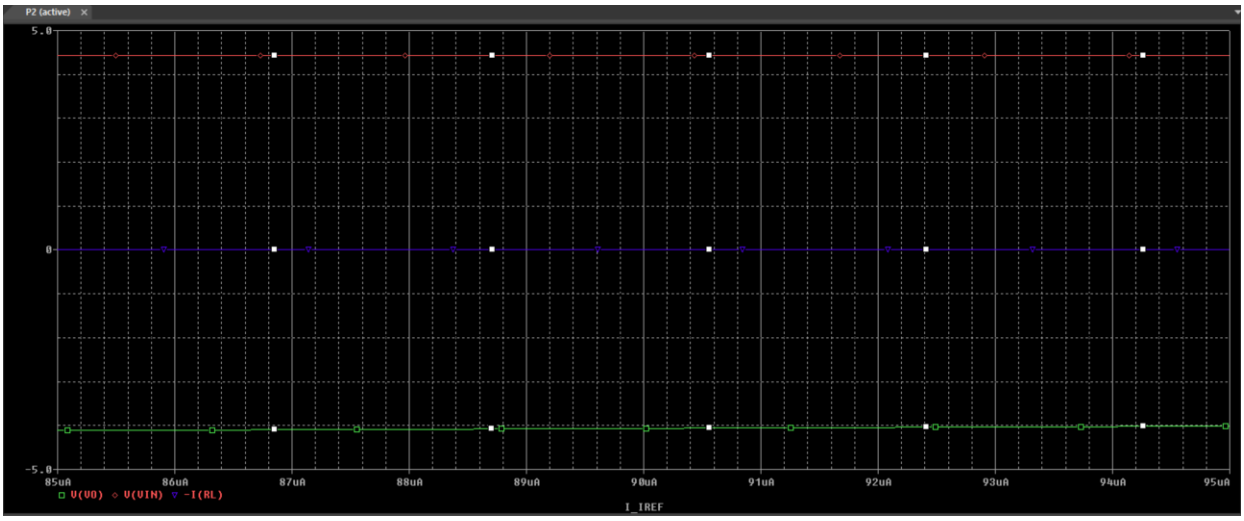


Figure 8: PSpice simulation results - DC sweep

B) SPICE Simulation – Two-Port Network of a Current Mirror

2.4

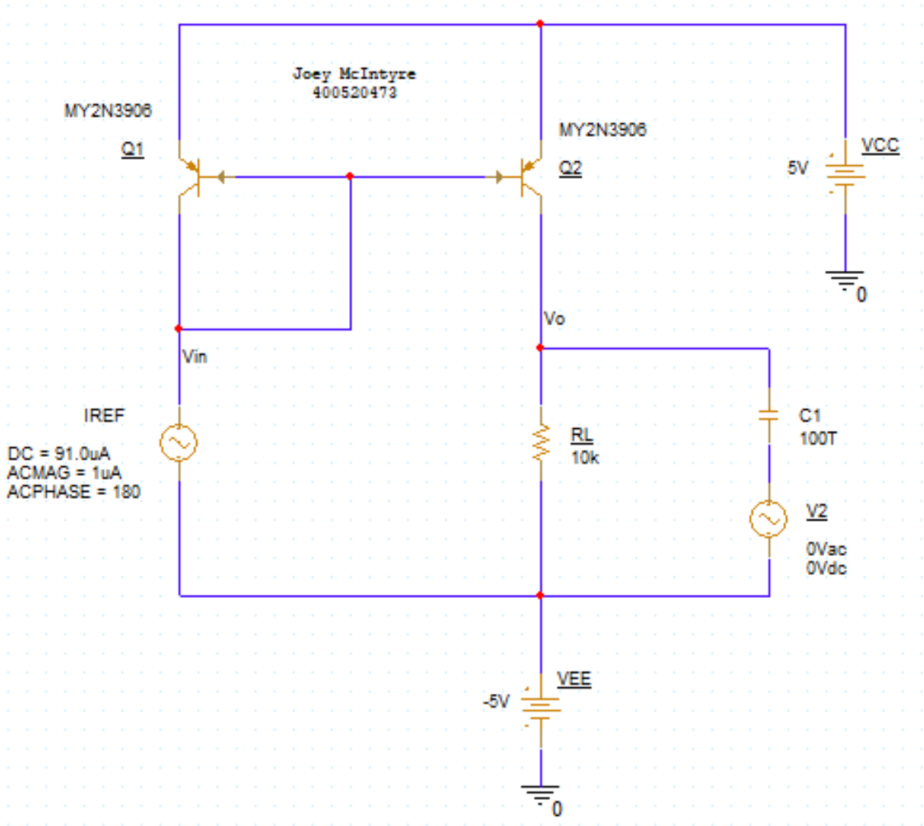


Figure 9: Circuit used for PSpice simulation - Two-port network of a current mirror

2.5

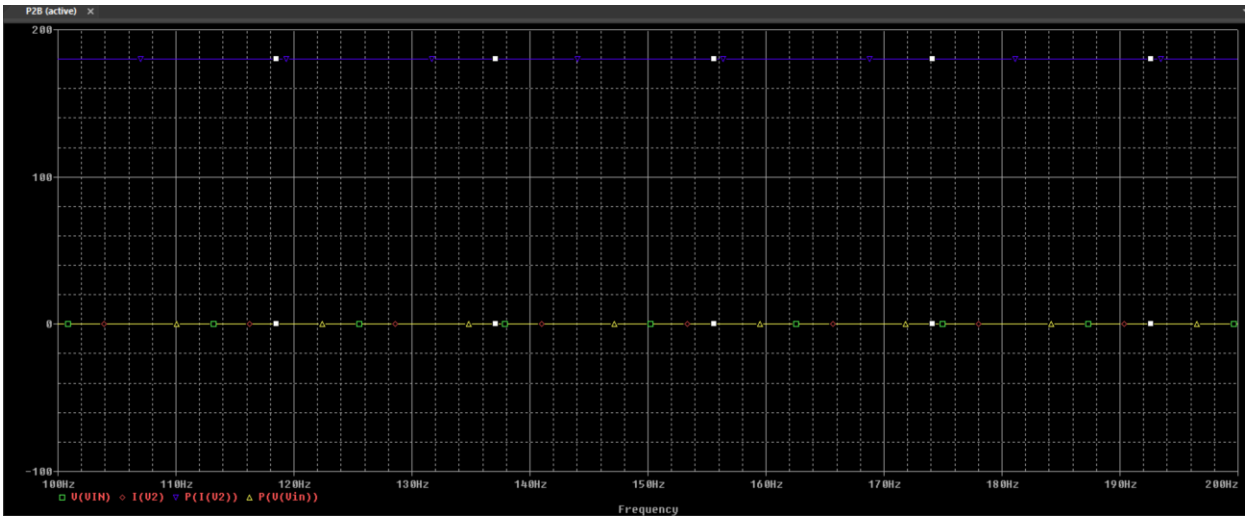


Figure 10: PSpice simulation results - Linear AC sweep

2.6

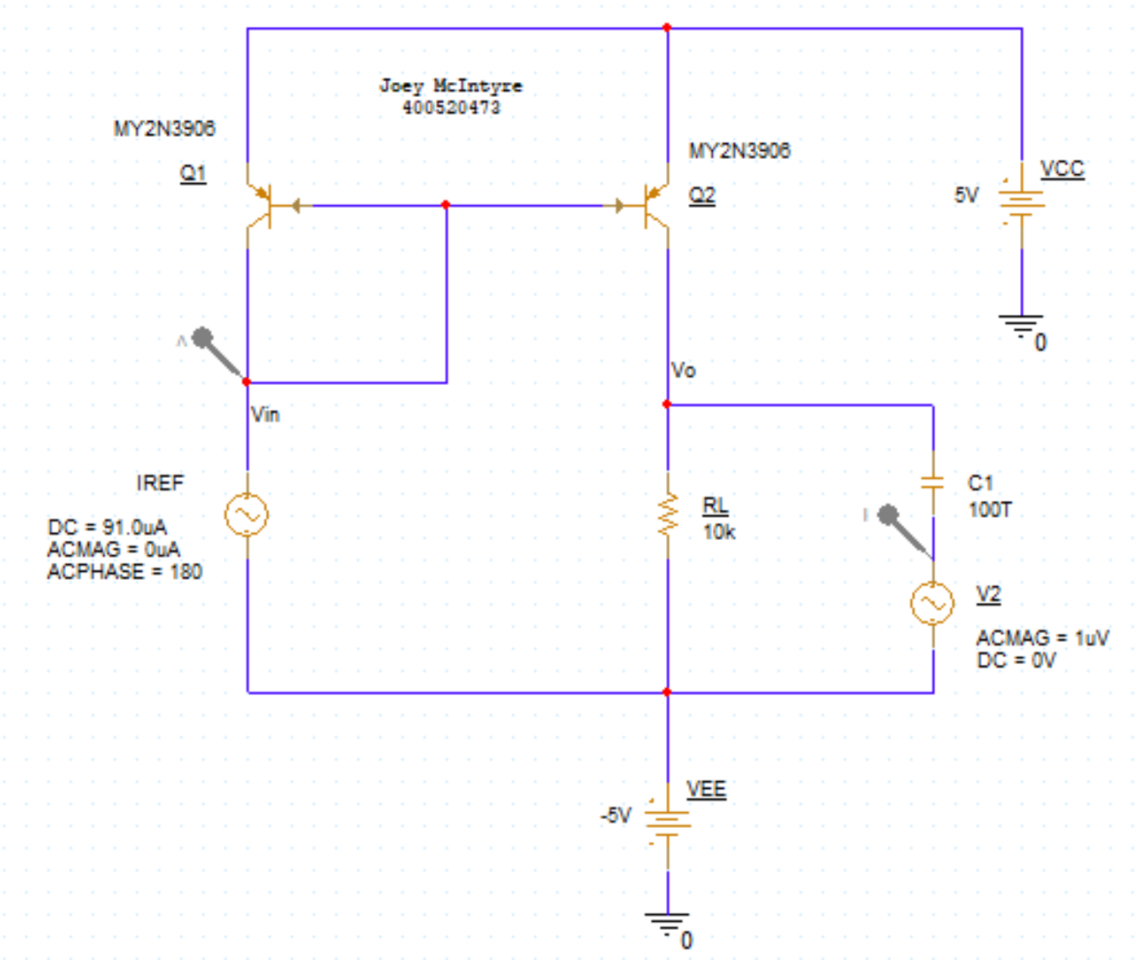


Figure 11: Circuit used for PSpice simulation - Two-port network of a current mirror

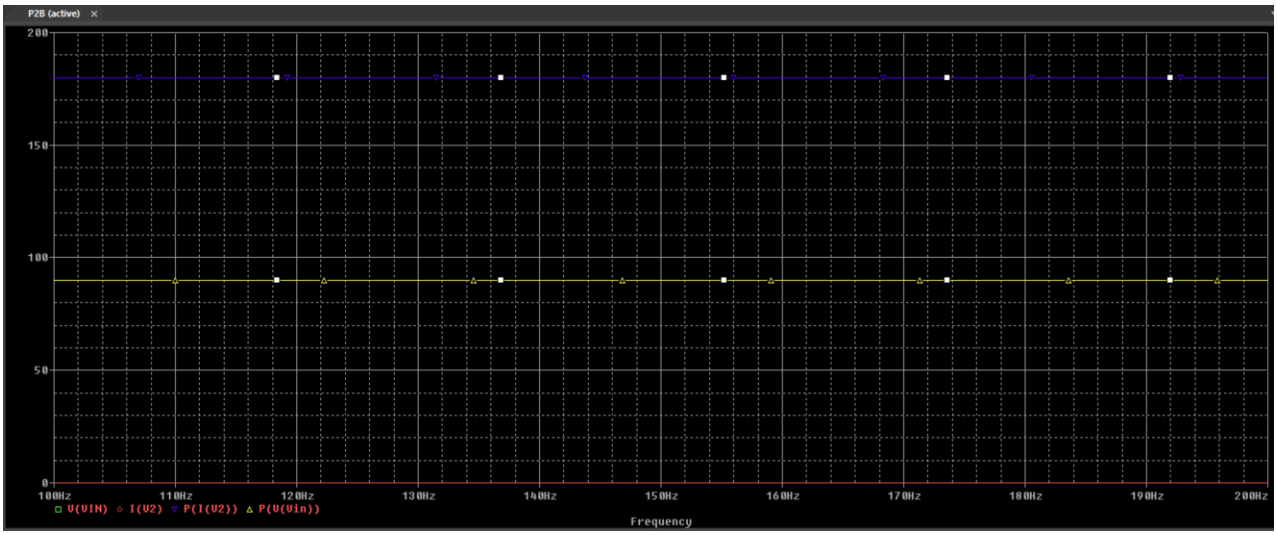


Figure 12: PSpice simulation results - Linear AC sweep

C) Questions for Part 2

Q3. (15 Points) (1) Based on section 8.2.3 in the textbook, derivate the relationship to express I_o as a function of I_{REF}. **(2)** Based on the simulation data obtained in Step 2.2, when I_{REF} is 0.1 mA, how is I_o compared with I_{REF}? When I_{REF} is 1mA, how is I_o compared with I_{REF}? **(3)** Justify the observation between the theoretical prediction and the simulated result at I_{REF} = 0.1 mA and 1mA, respectively.

(1)

Based on section 8.2.3 in the textbook, we know that the relationship between I_o and I_{REF} is that $\frac{I_o}{I_{REF}}$ is related to the area of the EBJ junction of the transistors used. Since the transistors in this experiment are the same, the area od the junction will also be the same. This means we can say that $I_o = I_{REF}$.

(2)

Based on the simulation data obtained in step 2.2, when I_{REF} = 0.1mA, the corresponding I_o is equal to 0.104mA. At this moment, I_o = 1.04 * I_{REF}. When I_{REF} = 1mA, the corresponding I_o is equal to 0.975mA. At this point, I_o = 0.975 * I_{REF}.

IREF	Io	Vin	Vo	VEC(Q1) = VEB(Q1)	VEC(Q2)
Amps	Amps	Volts	Volts	Volts	Volts
0.0001	0.000104	4.423166	-3.961	0.58	8.96
0.001	0.000975	4.341335	4.746068	0.66	0.25

(3)

Based on the conclusions made in Q3 part 1, we would predict that when I_{REF} = 0.1mA, I_o should also be 0.1mA, and when I_{REF} = 1mA, I_o should also be 1mA. Comparing these to the simulated values we obtained in step 2.2; we can see the predictions and simulated results align very closely.

When I_{REF} = 0.1mA, we would theoretically expect I_o = 0.1mA. Through simulation, I_o was found to be 0.104mA, which rounds to 0.1mA. When I_{REF} = 1mA, we would theoretically expect I_o = 1mA. Through

simulation, I_o was found to be 0.975mA, which rounds to 1mA. Therefore, the closeness of these results show that the theoretical predictions and simulated result align with each other.

Q4. (15 Points) (1) Based on the simulation data obtained in Step 2.5, what is the input impedance R_{in} looking from V_{in} toward the collector of Q1? What is the current gain A_i of the current mirror? **(2)** Based on the simulation data obtained in 2.6, what is the output impedance R_o of the current mirror looking into the collector of Q2? **(3)** Based on the information obtained in (1) and (2), draw the linear two-port network for the current mirror using its h-parameters.

(1)

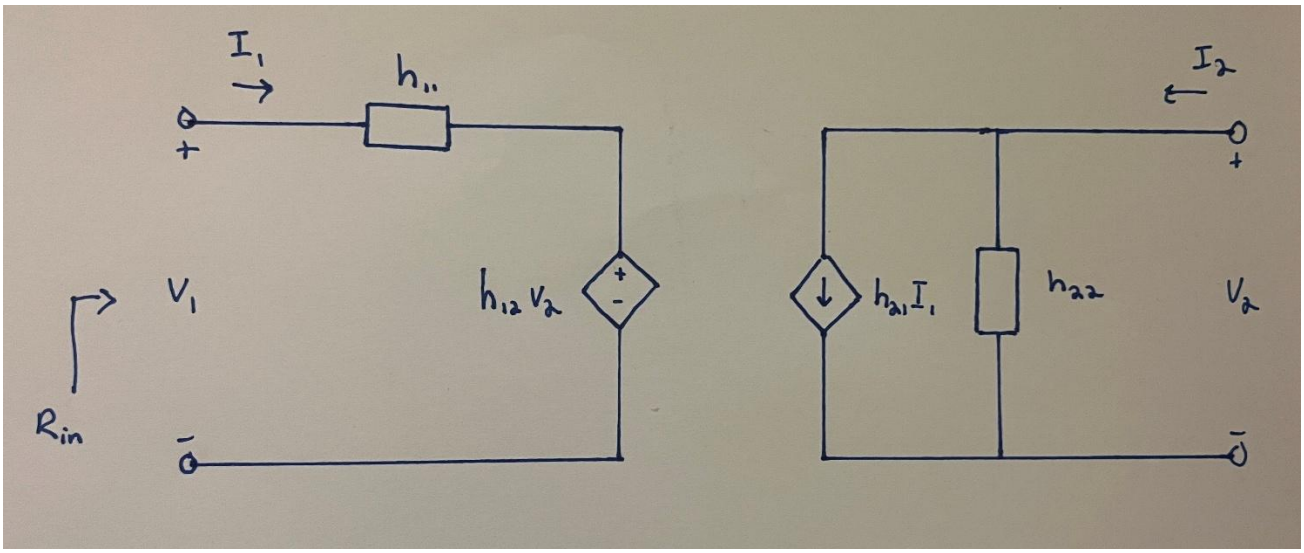
Based on the simulation data obtained in step 2.5, we know that the input impedance looking from V_{in} toward the collector of Q1 is $R_{in} = h_{11} = 389.12\Omega$. From this same data, we also know that the current gain of the current mirror is $A_i = h_{21} = 1.04$ A/A.

(2)

Based on the simulation data obtained in step 2.6, the output impedance of the current mirror looking into the collector of Q2 is $R_o = \frac{1}{(h_{22} - \frac{1}{R_L})} = 1.58 * 10^6\Omega$.

(3)

Using the information obtained in part (1) and (2), the linear two port network for the current mirror using its h-parameters is shown below.



The h-parameters are as follows:

$$h_{11} = 389.12\Omega$$

$$h_{21} = 1.04$$

$$h_{22} = 1.01 * 10^{-4}\ S$$

$$h_{12} = from\ 7.07 * 10^{-7}\ @\ 100Hz\ to\ 1.41 * 10^{-6}\ @\ 200Hz$$

h12 = v1/v2@i1=0	h22 = i2/v2@i1=0	R11 = h11 = v1/i1@v2=0 (Ohm)	Ai = h21 = i2/i1@v2=0 (A/A)
V/V	S	Ohm	A/A
7.05E-07	1.01E-04	389.12	1.04
7.75E-07	1.01E-04	389.12	1.04
8.46E-07	1.01E-04	389.12	1.04
9.16E-07	1.01E-04	389.12	1.04
9.87E-07	1.01E-04	389.12	1.04
1.06E-06	1.01E-04	389.12	1.04
1.13E-06	1.01E-04	389.12	1.04
1.20E-06	1.01E-04	389.12	1.04
1.27E-06	1.01E-04	389.12	1.04
1.34E-06	1.01E-04	389.12	1.04
1.41E-06	1.01E-04	389.12	1.04

<u>Part 3:</u> Differential Amplifier with a Current Mirror (CM) Load

A) SPICE Simulation

3.1

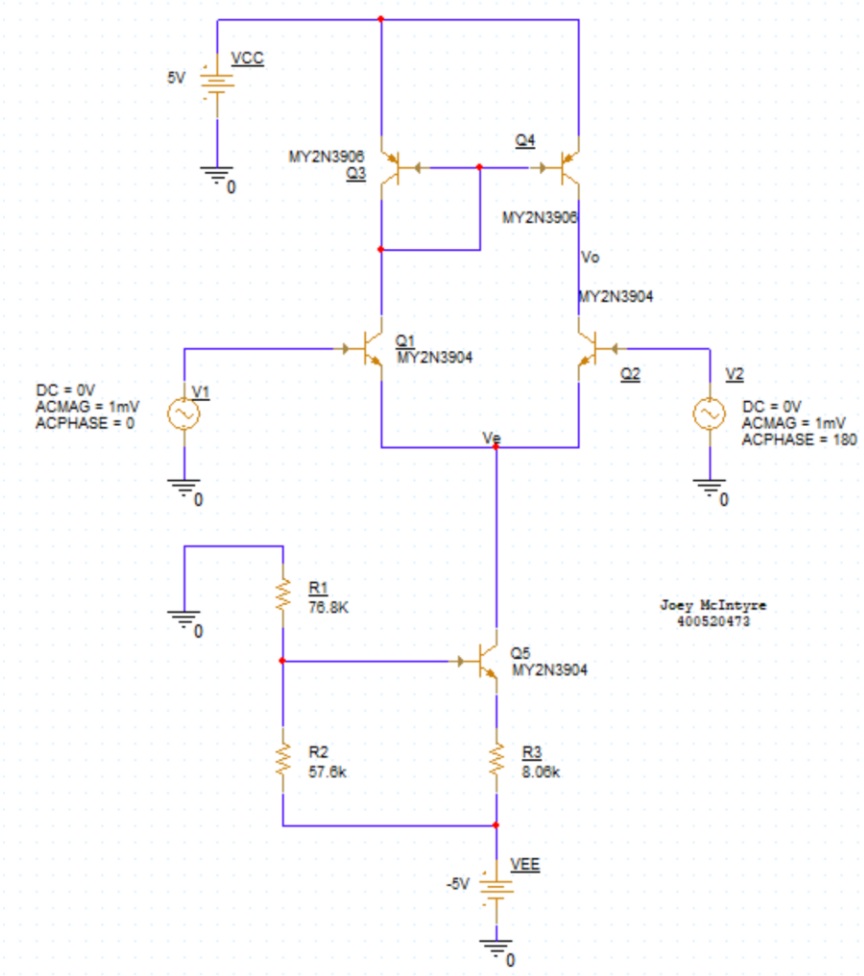


Figure 13: Circuit used for PSpice simulation - Differential amplifier with a current mirror load

3.2

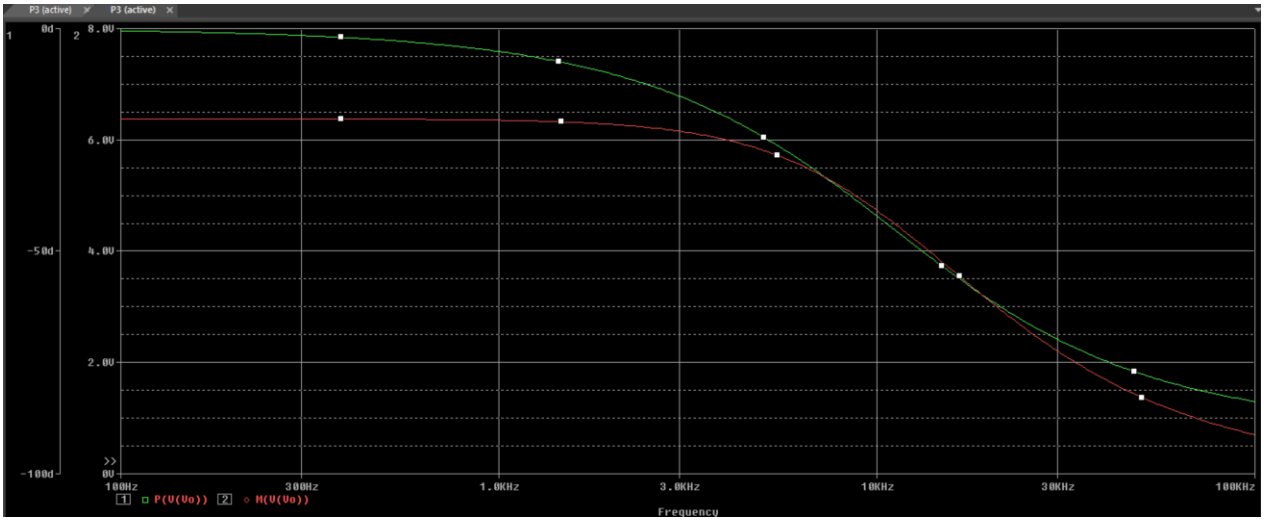


Figure 14: PSpice simulation results - Logarithmic AC sweep

B) AD3 Measurement

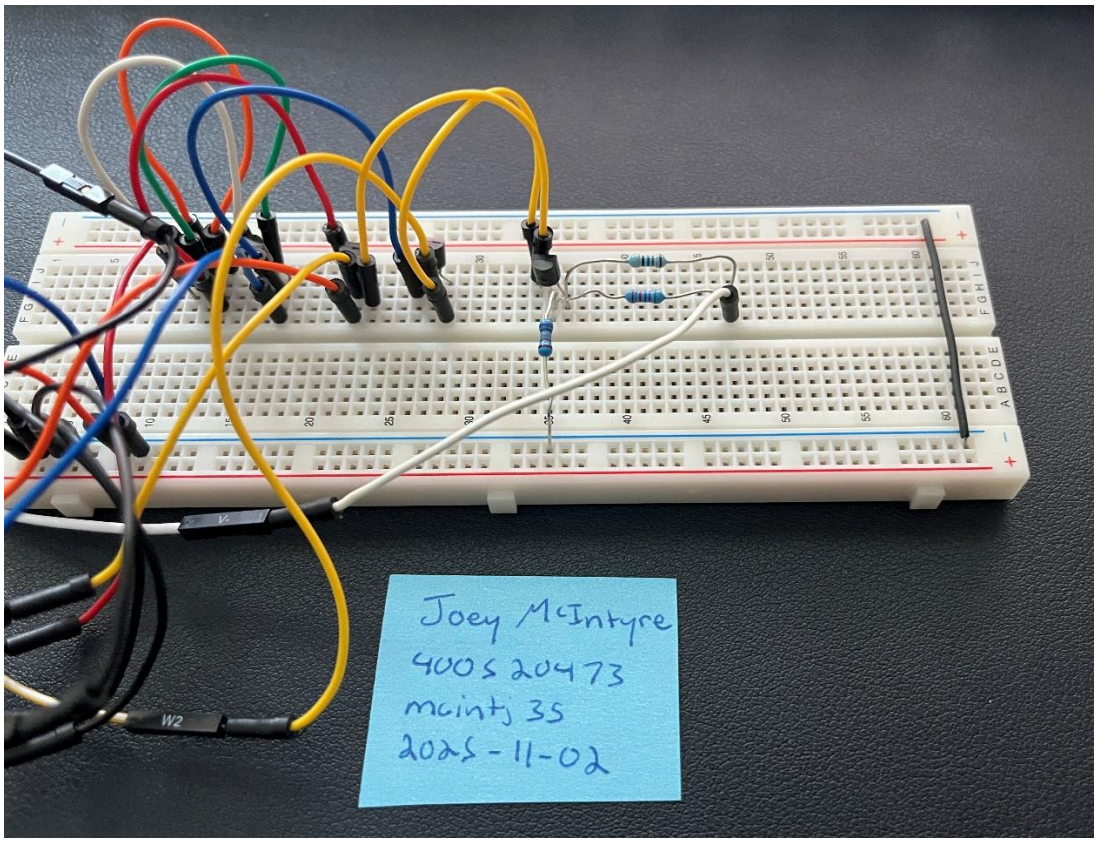


Figure 15: Physical circuit used for AD3 measurements - Differential amplifier with a current mirror load

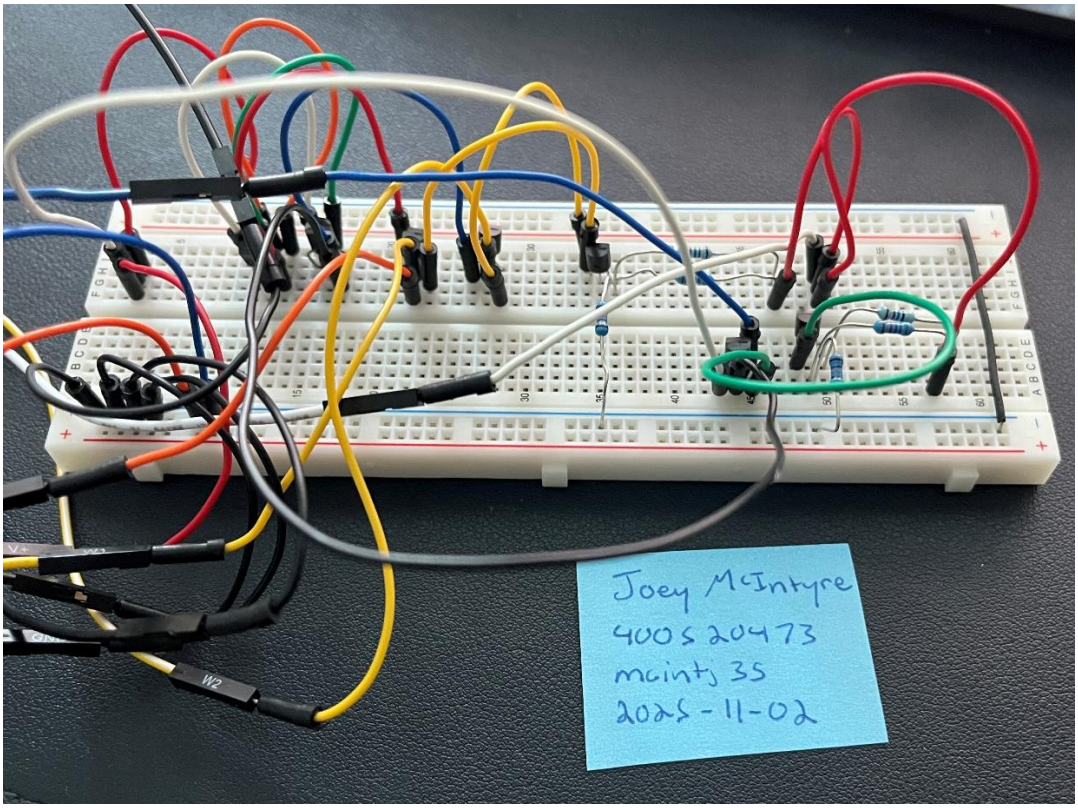


Figure 16: Physical circuit used for AD3 measurements - Multistage amplifier

C) Questions for Part 3

Q5. (15 Points) (1) Based on the simulation data obtained in Step 3.2, what is the voltage gain A_d in dB for the differential-mode signal? **(2)** Did you observe any mismatch in Step 3.6? If yes, how much offset voltage did you apply at V_2? **(3)** Compare your simulated result with the measured result obtained in Step 3.8.

(1)

Based on the simulation data obtained in step 3.2, the voltage gain A_d was 70.07dB.

Frequency	M(V(Vo))	P(V(Vo))	Ad = 20*log(|Vo|/2mV)	GBW	GBW in Step 3.6, Lab 2
Hz	Volts	Degrees	dB	Hz	Hz
100	6.378607263	-0.518045114	70.07	3.57E+07	7.95E+07

(2)

From the experimental data obtained in step 3.6, the mismatch voltage was found to be -0.00165V (-1.65mV). This was the amount at which V_2 was offset by in all future steps.

VCC =VE3 = VE4	VC1 (= VC3 = VB3 = VB4)	Vo (= VC2 = VC4)	VEB3	VBC4	W2Offset
Volt	Volt	Volt	Volt	Volt	Volt
5.0	4.4233	4.4513	0.5767	-0.028	-1.65E-03
			Q3 is ON if VEB3 > 0.6	Q4 is in Active Region if VBC4 > -0.4 V	

(3)

The measured voltage gain from step 3.8 was found to be 57.3dB. This is significantly lower than the simulated value obtained in step 3.2.

Q6. (10 Points) Estimate its upper 3-dB frequency f_H (i.e., the frequency at which the amplitude becomes $\frac{1}{\sqrt{2}} = 0.707$ of its low-frequency value or the phase changes 45 degrees).

The value at which the upper 3-dB frequency occurs can be determined by finding the point at which the amplitude becomes 0.707 of the low frequency (100Hz) value.

At low frequency, the output voltage has a magnitude of 6.3786V. This means that the upper 3-dB frequency occurs when the output voltage is 0.707 * 6.3786V, which is 4.5V. From the data obtained in step 3.2, we can determine that the upper 3-dB frequency is approximately 11207Hz.

Frequency	M(V(Vo))	P(V(Vo))	Ad = 20*log(|Vo|/2mV)
Hz	Volts	Degrees	dB
100	6.378607263	-0.518045114	70.07
11207.40201	4.480927677	-45.38531235	67.01

Q7. (10 Points) Compare the upper 3-dB frequency f_{3dB} of this differential amplifier with a current mirror load with that of the differential amplifier using resistive loads obtained in Q8 of Lab 2. Why does the differential amplifier with the current mirror load have a smaller f_{3dB}?

From Question 8 in Lab 2, we found that the upper 3-dB frequency of the differential amplifier using resistive loads was 8332821Hz. This value is far greater than the upper 3-dB frequency found in this lab.

The differential amplifier with the current mirror load has a smaller upper 3-dB frequency due to Miller Theorem, which states that a larger voltage gain results in a larger Miller Capacitance, therefore resulting in a lower upper 3-dB frequency.

Q8. (10 Points) What are the gain-bandwidth products (GBW) in Hz of the two differential amplifiers with the current mirror load and the resistive load, respectively?

In this lab, we found that the differential amplifier with the current mirror had a GBW of 3.57 * 10^7 Hz. In lab 2, it was found that the differential amplifier with a resistive load had a GBW of 7.95 * 10^7 Hz.

GBW	GBW in Step 3.6, Lab 2
Hz	Hz
3.57E+07	7.95E+07