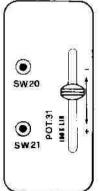
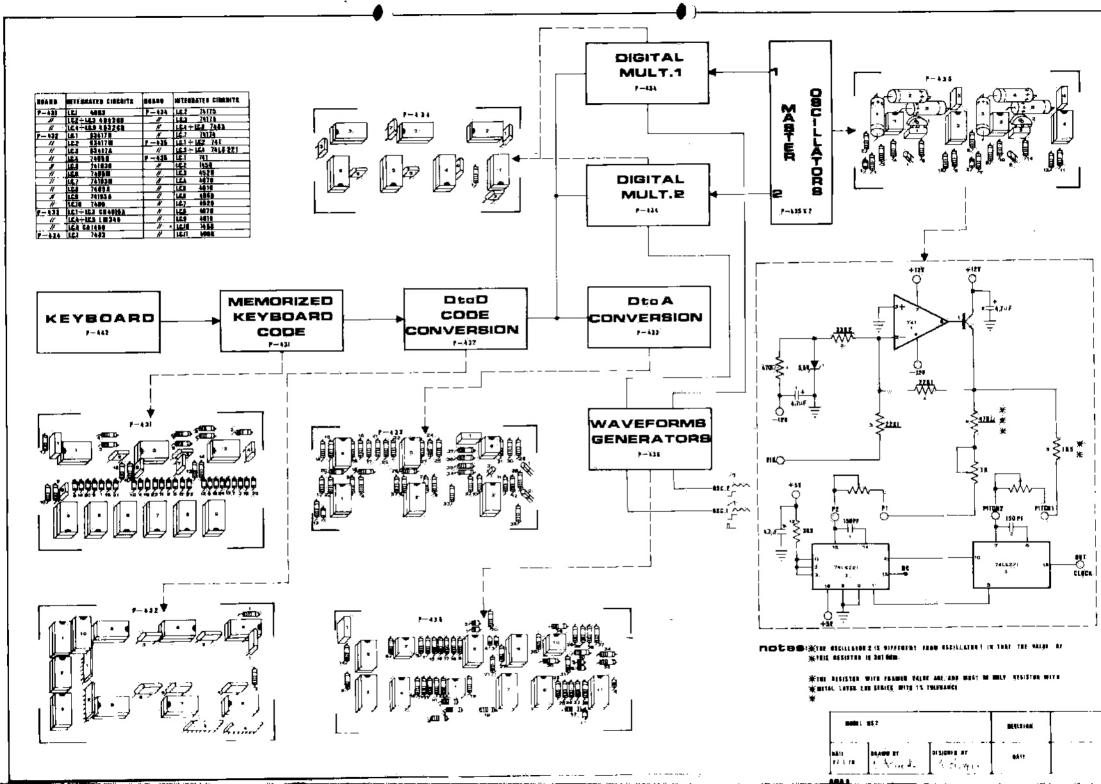
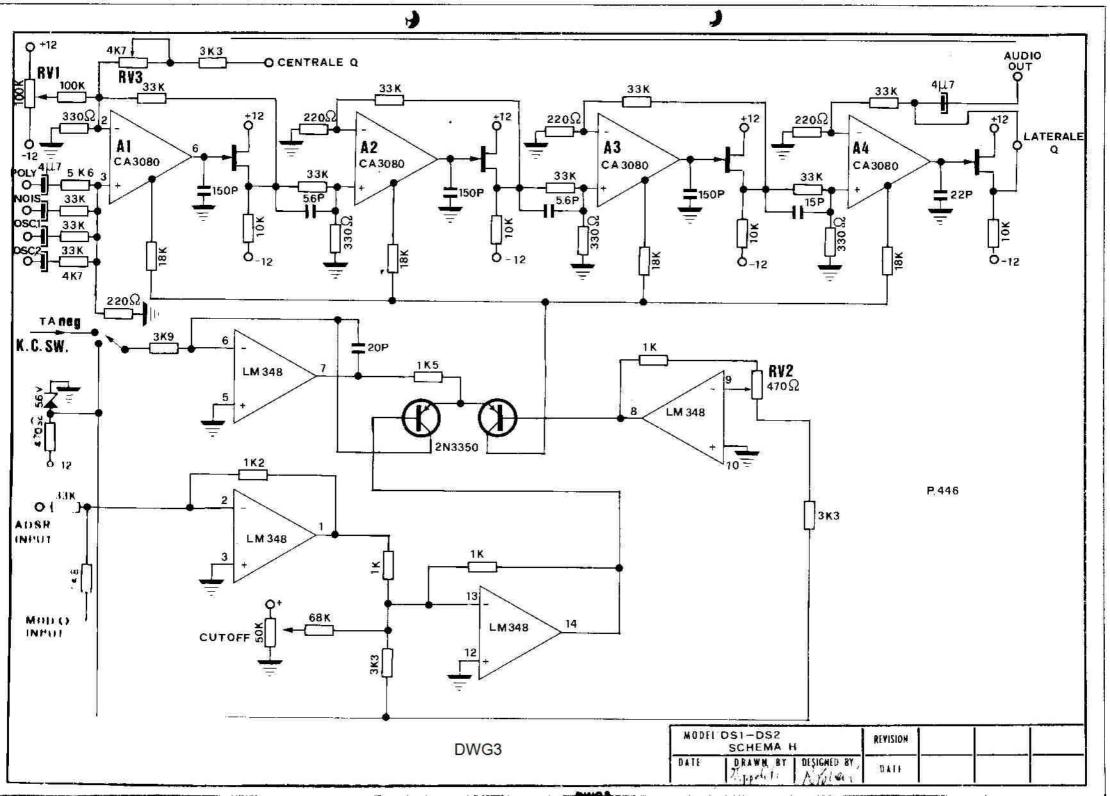


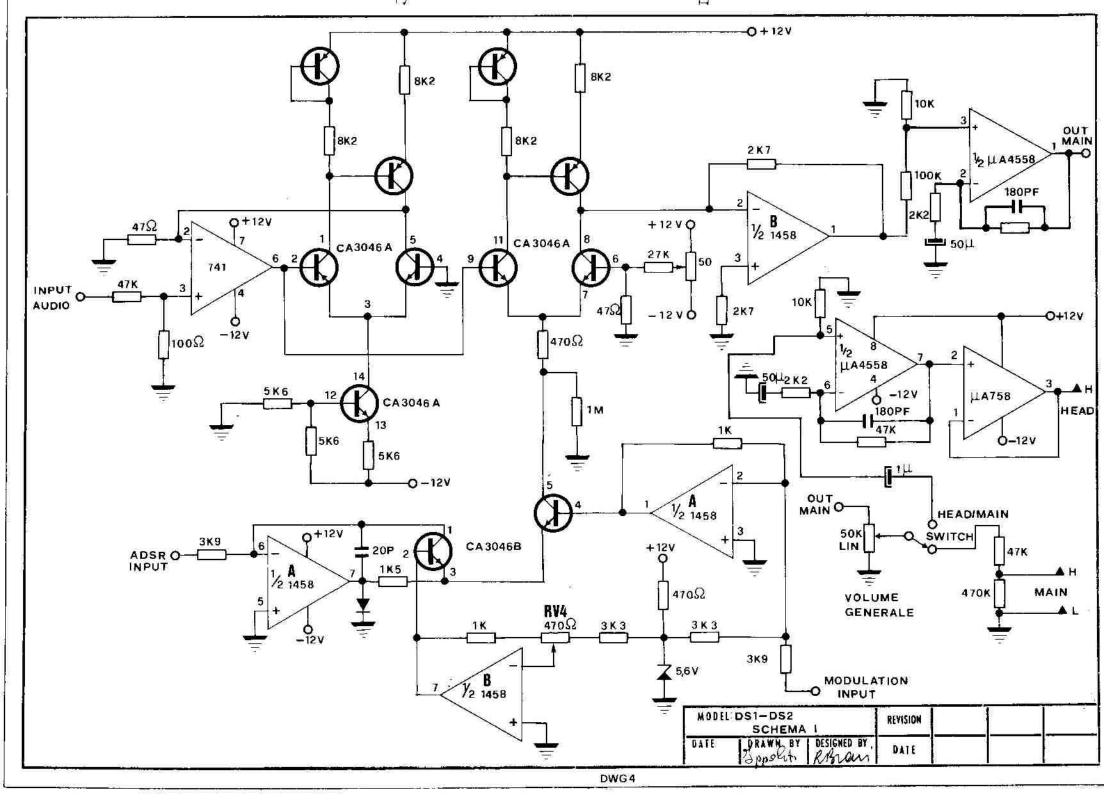
DIGITAL SYNTHESIZER DS 2

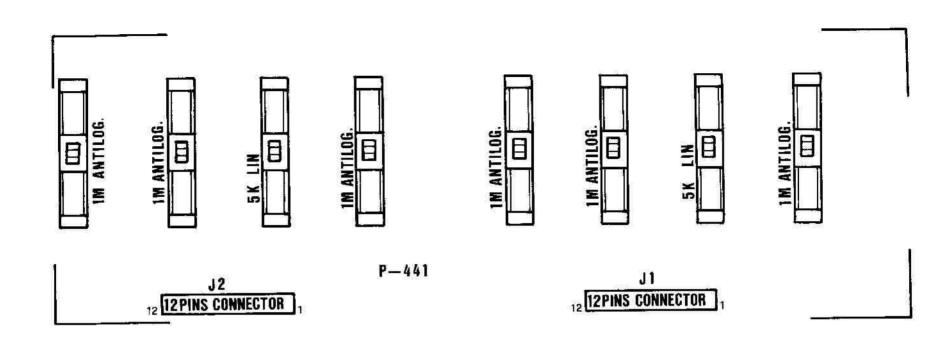


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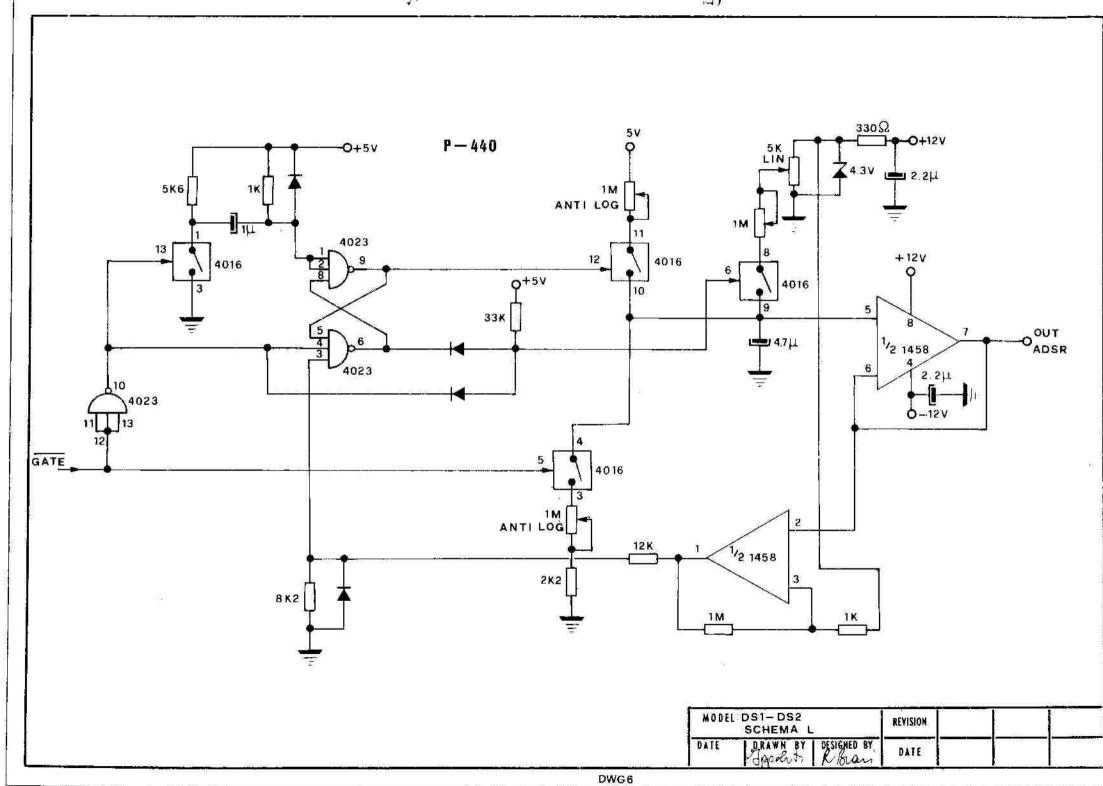




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PIN	REFERENCE J2	PIN	REFERENCE J1
1	OUT ADSR VCF	1	+127
2	n a ii	2	-12V
3	11 11 11	3	R POT.
4	+57	4	S POT.
5	R POT.	5	GND
6	S POT.	6	11
7	GND	7	1 11
8	T III	8	11
9	11	9	D POT.
10	111	10	A POT.
11	D POT.	11	GATE
12	A POT.	12	OUT ADSR VCA

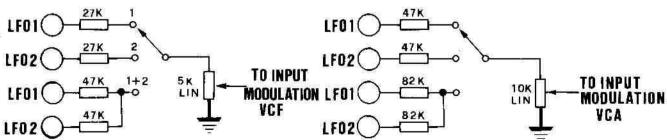
MODEL	DS2	HEMA L	REVISION	
DATE			DATI	



2 PINS CONNEC J2	TOR	÷		12 PI	NS CONNECTOR J1
1458	4016	4023	1458	4016	4023
	- Contract				

PIN	REFERENCE J1	PIN	REFERENCE J2
1	+12 V	1	
2	-12 V	2	OUT ADSR VCF
3	R POT	3	· · · · · · · · · · · · · · · · · · ·
4	S POT	4	+57
5	GND	5	R POT
6	GND	6	S POT
7	GND	7	GND
8	GND	8	GND
9	D POT	9	GND
10	A POT	10	GND
11	GATE	11	D POT
12	OUT ADSR VCA	12	A POT

MODEL DS DS SCHEMA L	REVISION	623 623	
DATE DRAWN BY DESIGNED BY	DATE		



**OFF** 

39K

100K 1+2

39K

100K

1 1458 A

8K2

1<sub>2</sub> 1458A

8K2

100K 1+2

LF01

LF02

LF01

LFO 2

LFO1 (

LFO2(

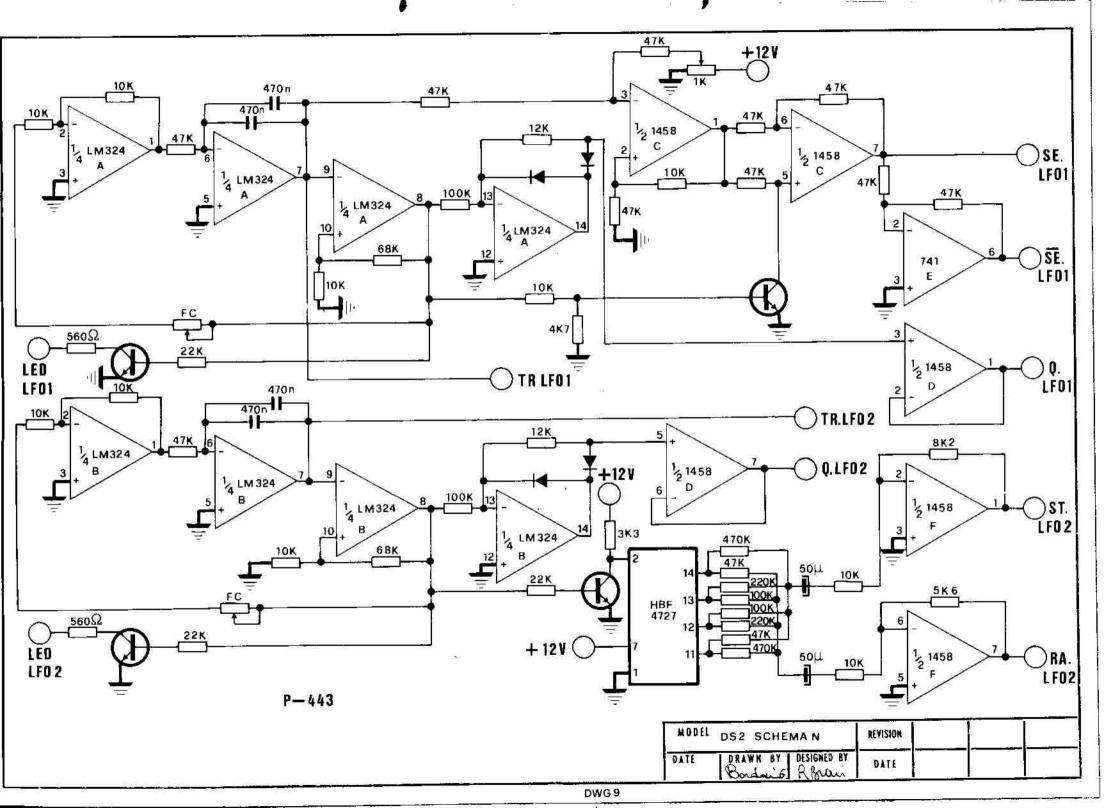
LF01

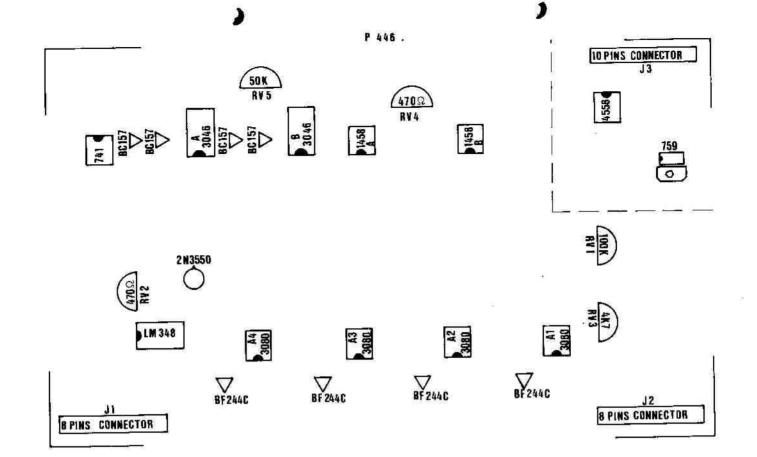
LF02

DS2 SCHEMA M REVISION

DATE DRAWN BY DISIGNED BY DATE

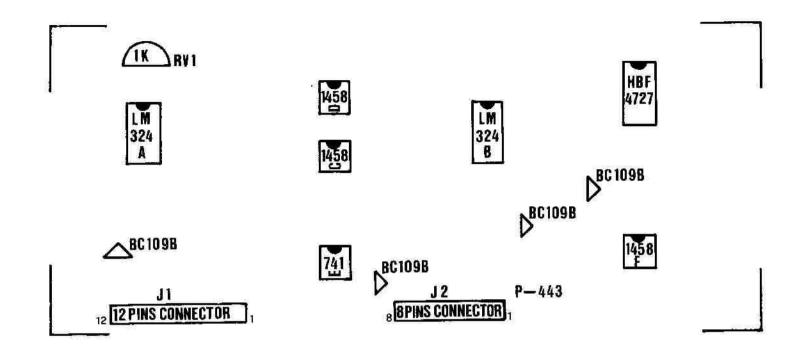
DETAIL OF REPLECT DATE





PIN	REFERENCE J1	PIN	REFERENCE J2	PIN	REFERENCE J3
1	-5.6 V	1 2	GND	1	ADSR VCA
2	CUTOFF POT	3	RESON CENTR-	2	MODULAT INPUT
3	END	4	POLY	3	-12V
4	MODULAT INPUT	5	NOISE	4.	+124
5	ADSR VCF	6	0SC 1	5	GNO
6	KT SW TA	7	OSC 2	6	GND
Ť	RESONANCE LATER.	В		7	OUT VOL GEN
8	GNO	14-2	1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 -	8	INPUT HEAD PH
Ŭ	4114	8000 E		9	GND
-				10	OUT HEAD PH

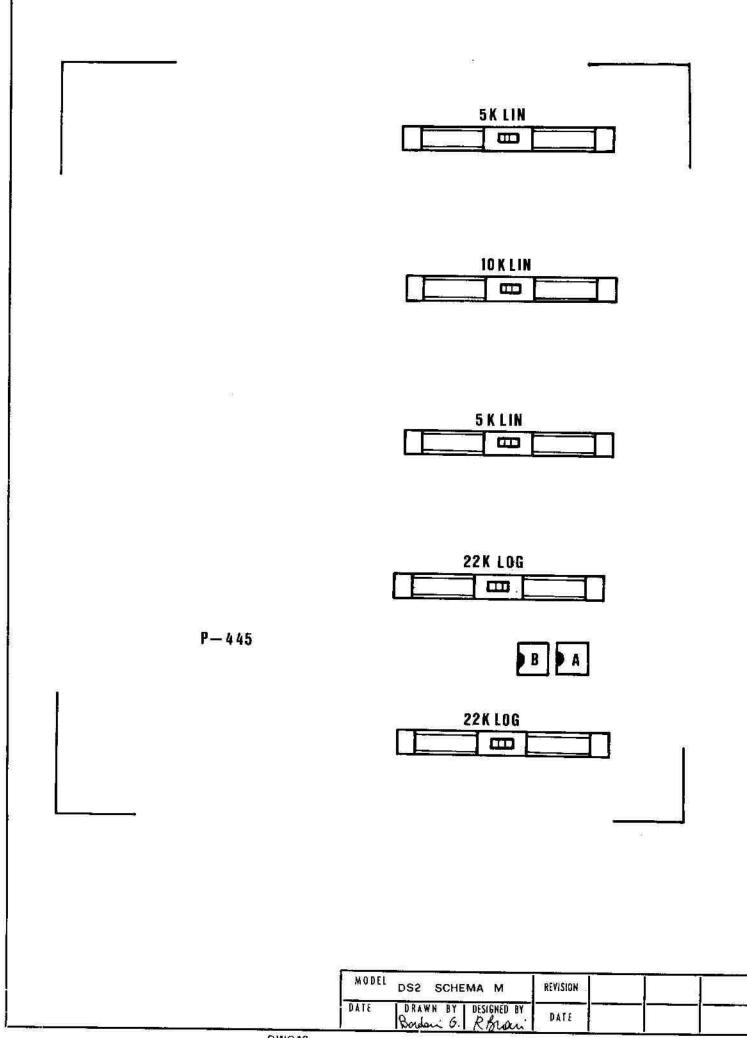
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M0011	051 052	NI VISION	10
	SCHEMA H.		
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	ingress of	Oak .	



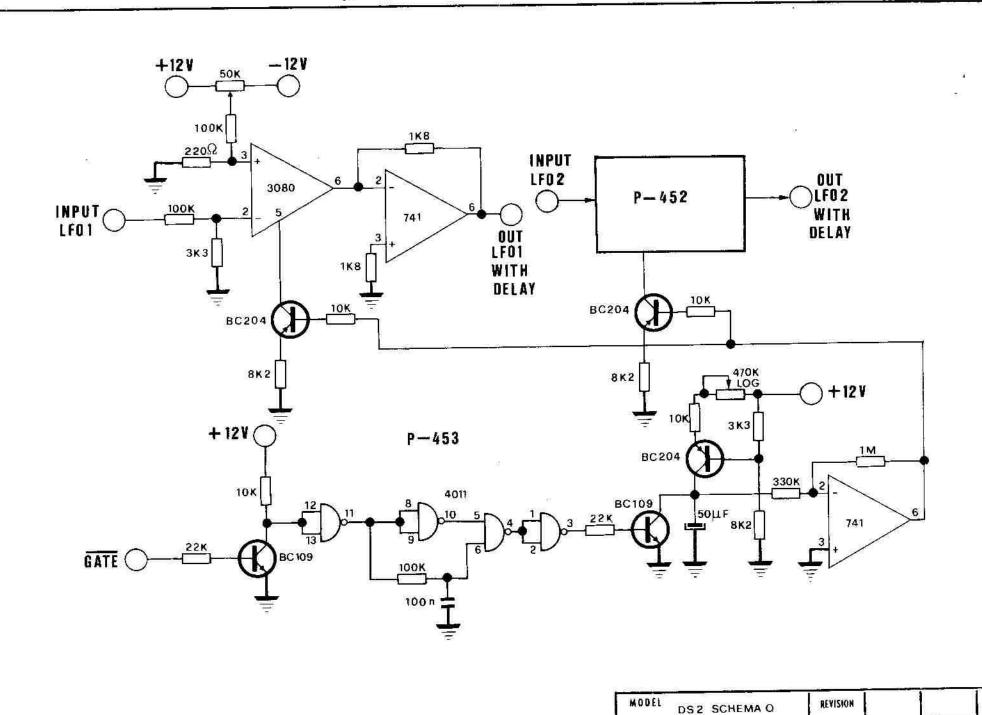
IN	REFERENCE J1	PIN	REFERENCE J2
1	SE. LF01	1.1	STAIRCASE
2	SE. LFO1	2	II .
3	QUADRA LF01	3	Sell
4	FC LF01	4	LED LF02
5	-12V	5	FC LFO 2
6	TRI. LFO1	6	QUADRA LFO 2
7	GND	7	TRI. LFO 2
8	11	8	FC LF02
9			
10	LED LF01		
11	FC LF01	5 <u></u> 8	
12	+12V		

MODEL	DS2 SCHEMA N	REVISION	
DATE	BOORDING RESIGNED BY	I DAIL L	

DWG11



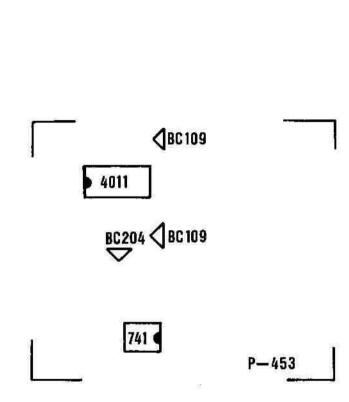
DWG12

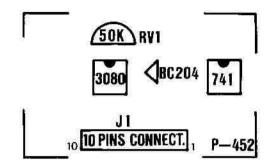


DATE

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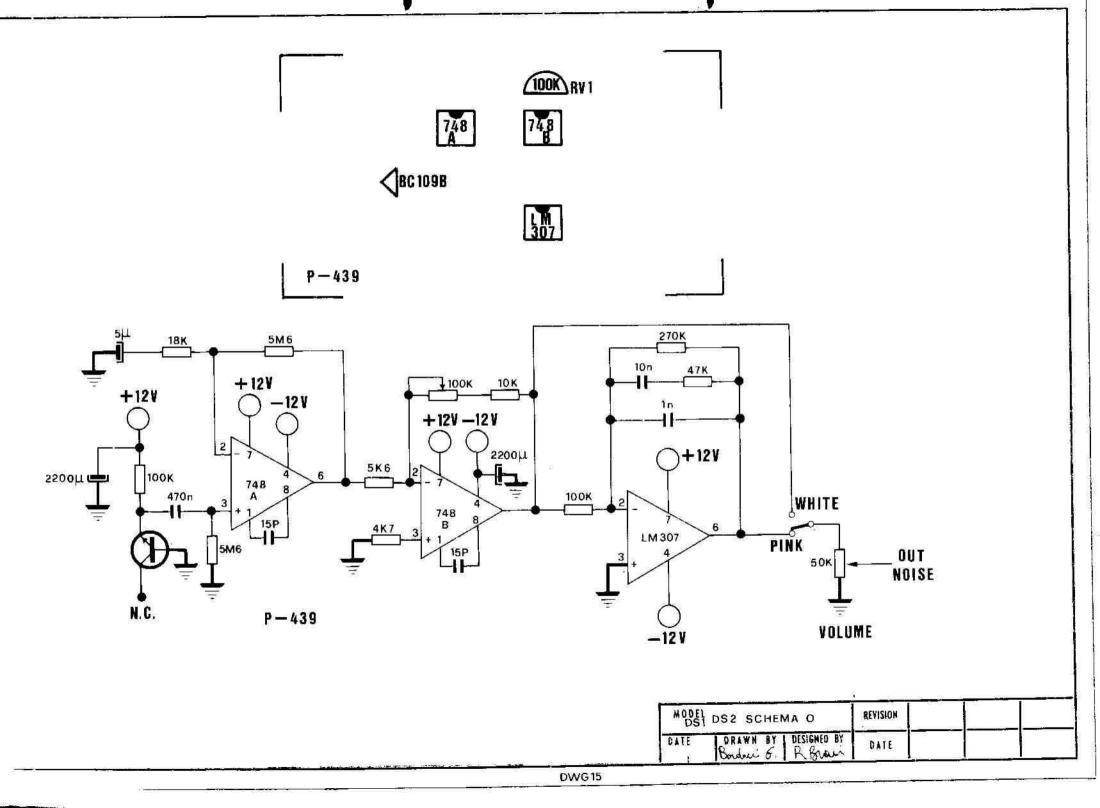
DATE

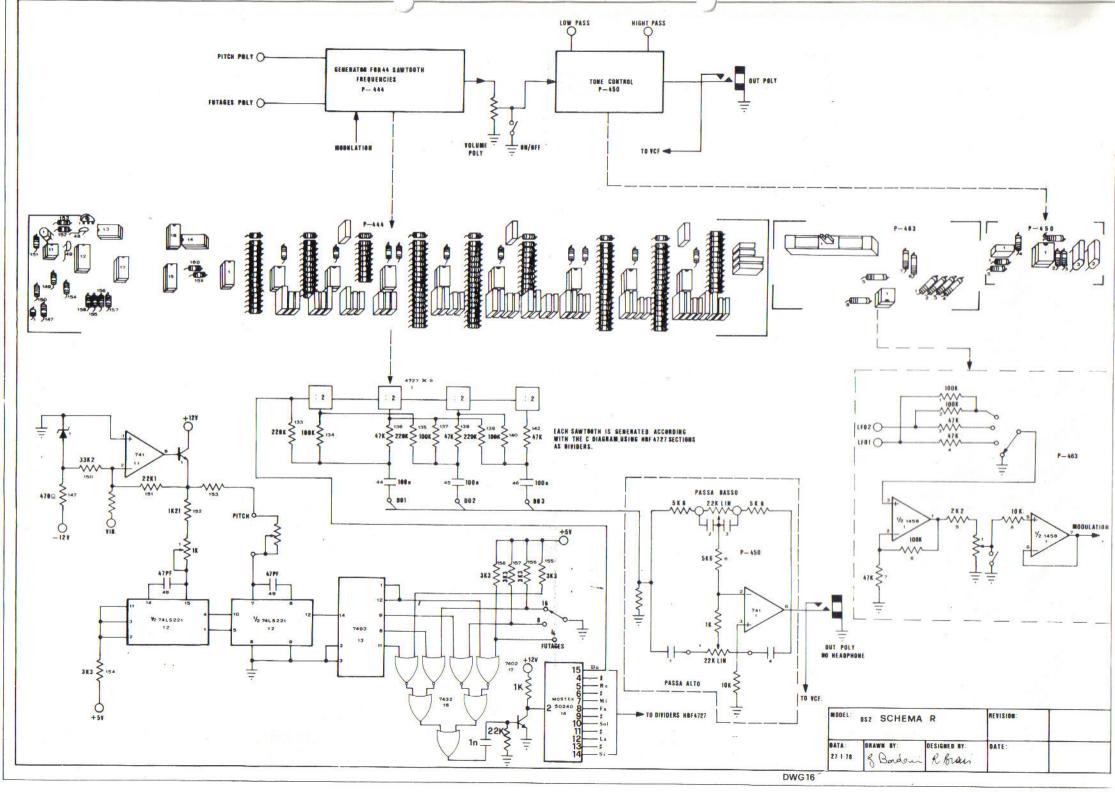


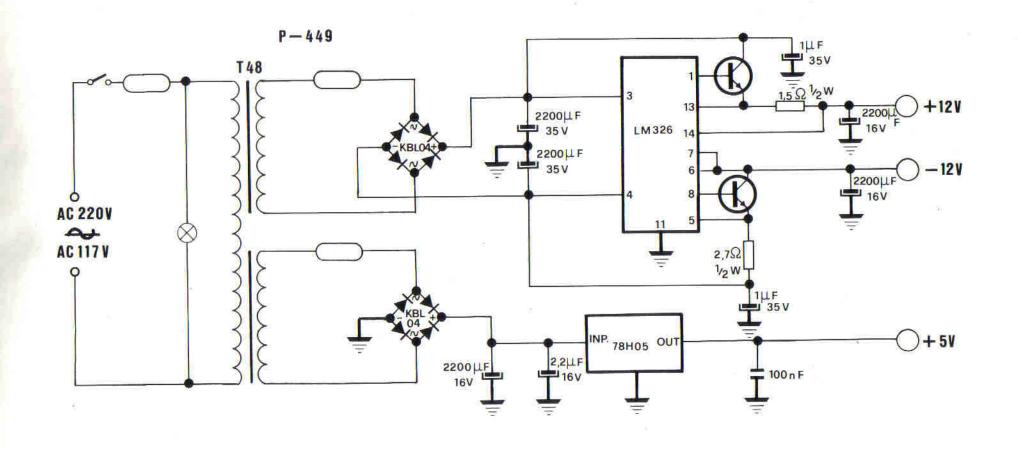


PIN	REFERENCE J1
1	+12V
2	OUT LF01 or LF02 WITH DELA
3	PIN 6 741
4	-12V
5	GND
6	11
7	
8	INP. LF01or LF02
9	n n n
10	11 11 11 11

MODEL	DS2 SCHEMA Q	REVISION	
DATE	Bodaig Rham	DATE	-







MODEL	DS 2 SCHEMA P	REVISION	
DATE	Brawn BY DESIGNED BY	DATE	

