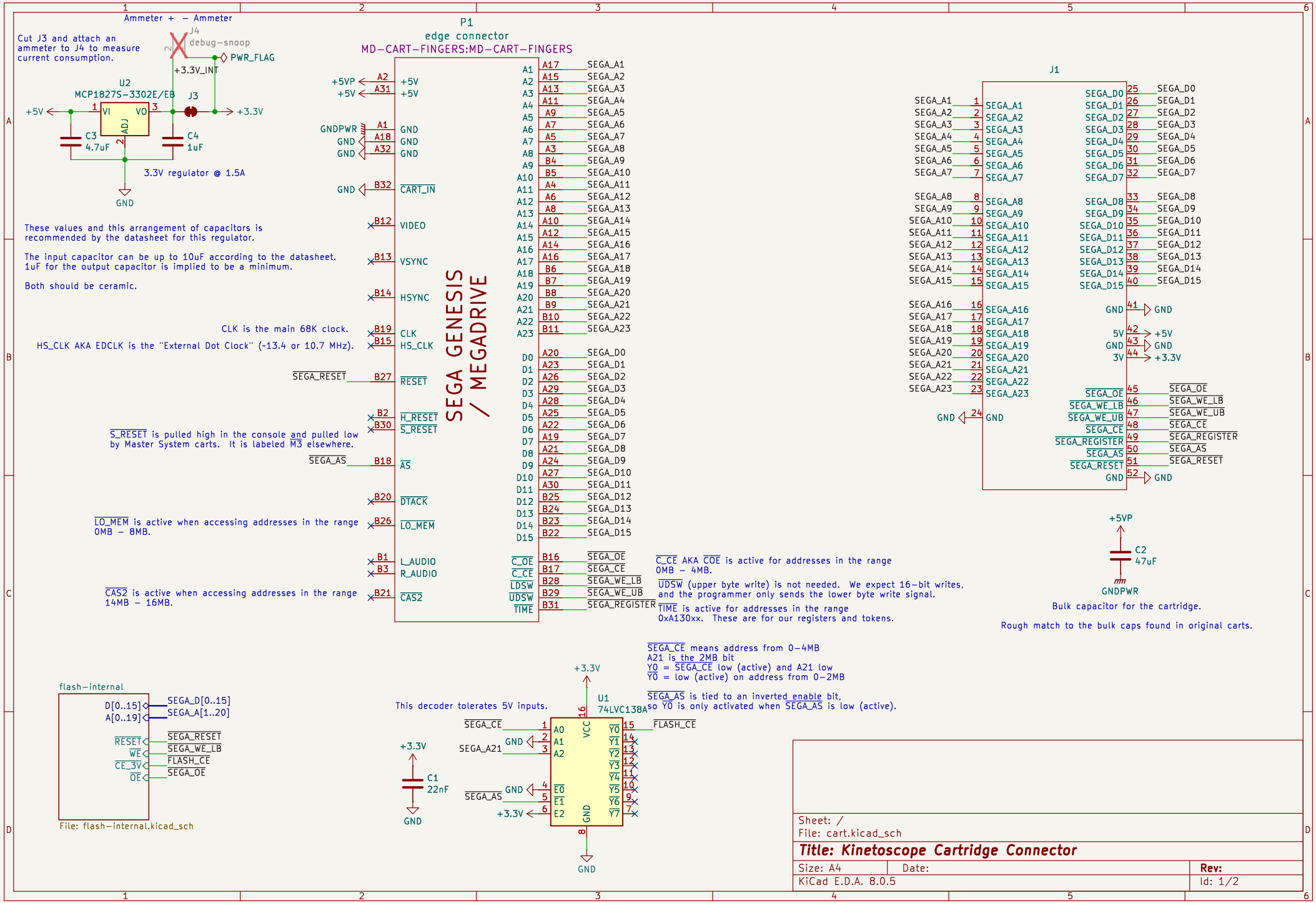

Ammeter + − Ammeter
Cut J3 and attach an ammeter to J4 to measure current consumption.
J4
debug−snoop
PWR_FLAG
+3.3V_INT
U2
MCP1827S−3302E/EB
J3
+5V
VI
VO
ADJ
+3.3V
C3
4.7uF
C4
1uF
3.3V regulator @ 1.5A
GND
These values and this arrangement of capacitors is recommended by the datasheet for this regulator.
The input capacitor can be up to 10uF according to the datasheet. 1uF for the output capacitor is implied to be a minimum.
Both should be ceramic.
P1
edge connector
MD−CART−FINGERS:MD−CART−FINGERS
SEGA GENESIS / MEGADRIVE
+5VP
GNDPWR
CART_IN
VIDEO
VSYNC
HSYNC
CLK is the main 68K clock.
HS_CLK AKA EDCLK is the "External Dot Clock" (~13.4 or 10.7 MHz).
CLK
HS_CLK
SEGA_RESET
RESET
H_RESET
S_RESET
S_RESET is pulled high in the console and pulled low by Master System carts. It is labeled M3 elsewhere.
SEGA_AS
AS
DTACK
LO_MEM is active when accessing addresses in the range 0MB − 8MB.
LO_MEM
L_AUDIO
R_AUDIO
CAS2 is active when accessing addresses in the range 14MB − 16MB.
CAS2
C_OE
C_CE
LDSW
UDSW
TIME
C_CE AKA COE is active for addresses in the range 0MB − 4MB.
UDSW (upper byte write) is not needed. We expect 16−bit writes, and the programmer only sends the lower byte write signal.
TIME is active for addresses in the range 0xA130xx. These are for our registers and tokens.
J1
SEGA_OE
SEGA_WE_LB
SEGA_WE_UB
SEGA_CE
SEGA_REGISTER
SEGA_AS
SEGA_RESET
+5V
GND
+3.3V
C2
47uF
GNDPWR
Bulk capacitor for the cartridge.
Rough match to the bulk caps found in original carts.
flash−internal
D[0..15]
A[0..19]
SEGA_D[0..15]
SEGA_A[1..20]
RESET
WE
CE_3V
OE
SEGA_WE_LB
FLASH_CE
File: flash−internal.kicad_sch
This decoder tolerates 5V inputs.
U1
74LVC138A
SEGA_A21
VCC
SEGA_CE means address from 0−4MB
A21 is the 2MB bit
Y0 = SEGA_CE low (active) and A21 low
Y0 = low (active) on address from 0−2MB
SEGA_AS is tied to an inverted enable bit, so Y0 is only activated when SEGA_AS is low (active).
C1
22nF
Sheet: /
File: cart.kicad_sch
Title: Kinetoscope Cartridge Connector
Size: A4
Date:
Rev:
KiCad E.D.A. 8.0.5
Id: 1/2

This is where the cartridge "ROM" image is stored. Not an actual ROM, or EPROM, but Flash RAM, which is way cheaper.

Maximum ROM size is 2MB.

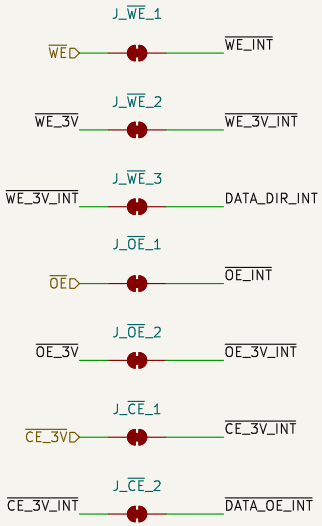
The flash chip is compatible with the Krikzz Flashkit MD Programmer. This chip gets its own voltage regulator so that this base cartridge board can be programmed directly without any other boards attached.

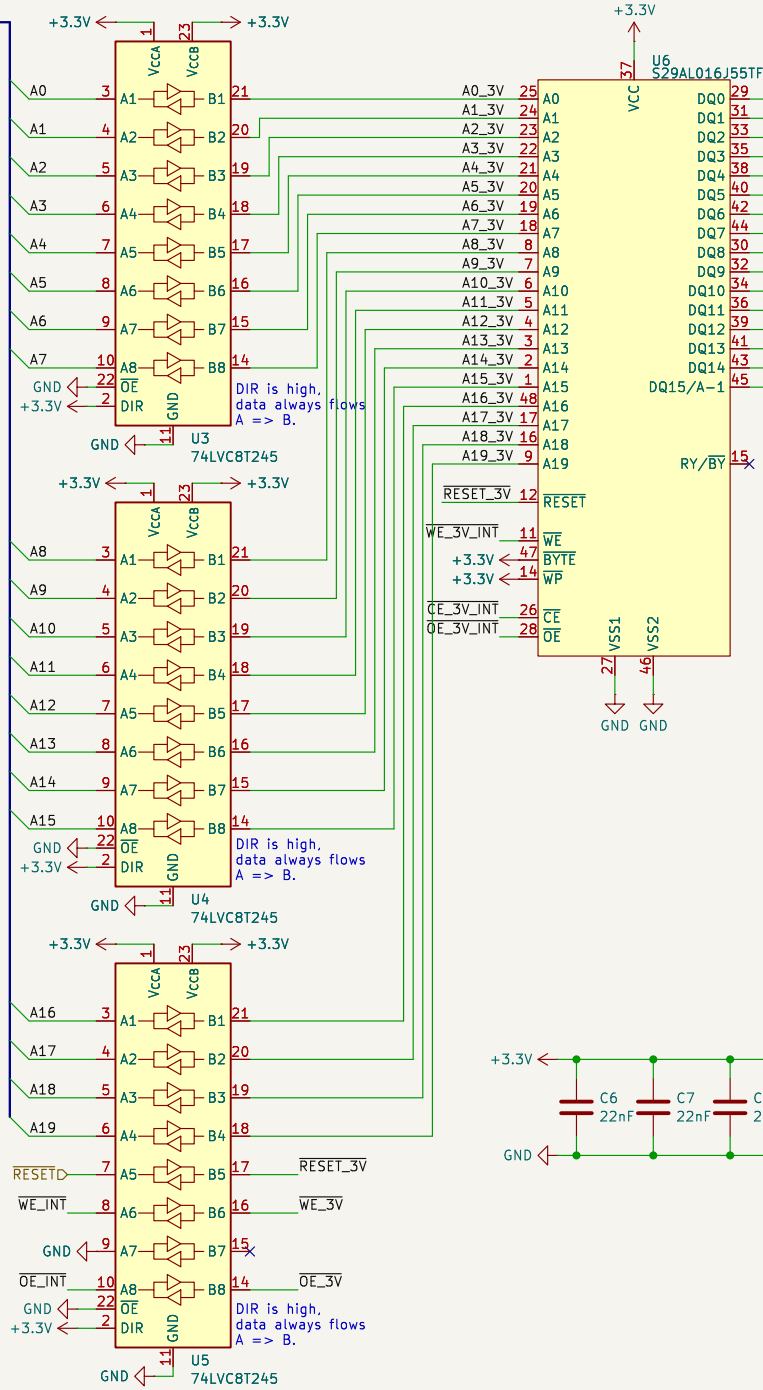
This 3.3V chip talks through a series of level translators. Because the FlashKit programmer uses 3.3V logic, all inputs to this sheet must work as either 5V or 3.3V. The translators will tolerate 5V input at all supply voltages, so we supply both sides with 3.3V.

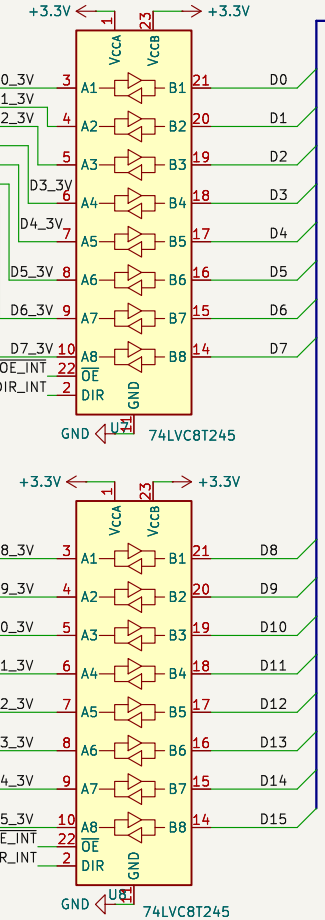
If we used 5V for VccA, then the minimum high level for input would 3.5V (VCC * 0.7), and the levels from our 3.3V programmer would not work.

This arrangement allows for compatibility with both 3.3V signals from the FlashKit Programmer and 5V signals from the Sega.

These bridges can be used to snoop on these signals, or cut with a knife to hijack them.





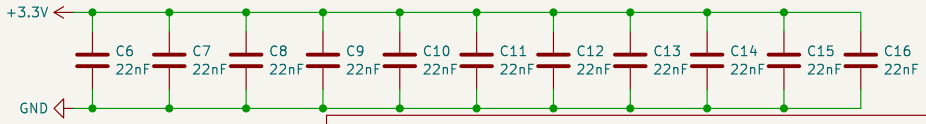


This outputs at 3.3V logic levels, which are compatible with the Sega's 5V TTL system. We rely on this fact so that the cart can remain compatible with both the Sega and the FlashKit programmer. If we made the right side 5V, then the minimum high level for data input would be 3.5V (VccB * 0.7), which would cause 3.3V inputs not to work right.

By using 3.3V on both sides, we can take advantage of the chip's 5V-tolerant input so that anything over 3.3V * 0.7 (= 2.31V) is considered high, and the input when writing can be 3.3V.

DIR is high to pass data from A to B.
DIR is connected to WE via DATA_DIR_INT.
WE is high when we're reading.
Therefore the reading side (flash chip side) should be A.

OE is connected to CE_3V via DATA_OE_INT and CE_3V_INT. Throughput (in either direction) will be enabled any time the address space indicates reading or writing flash (0-2MB).



Sheet: /flash-internal/
File: flash-internal.kicad_sch

Title: Kinetoscope Flash chip and related support circuits

Size: A4	Date:	Rev:
KiCad E.D.A. 8.0.5		Id: 2/2