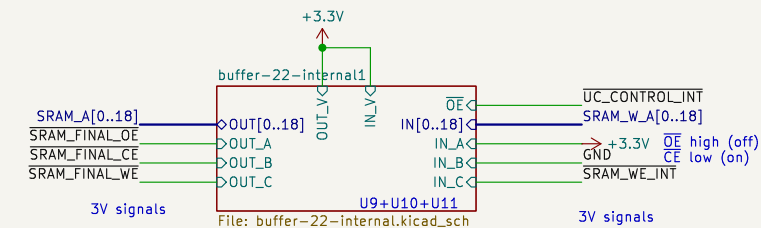
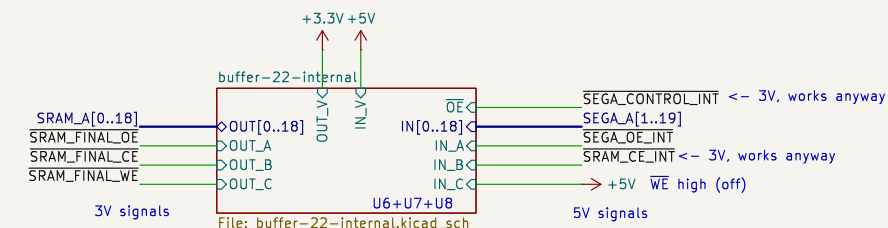
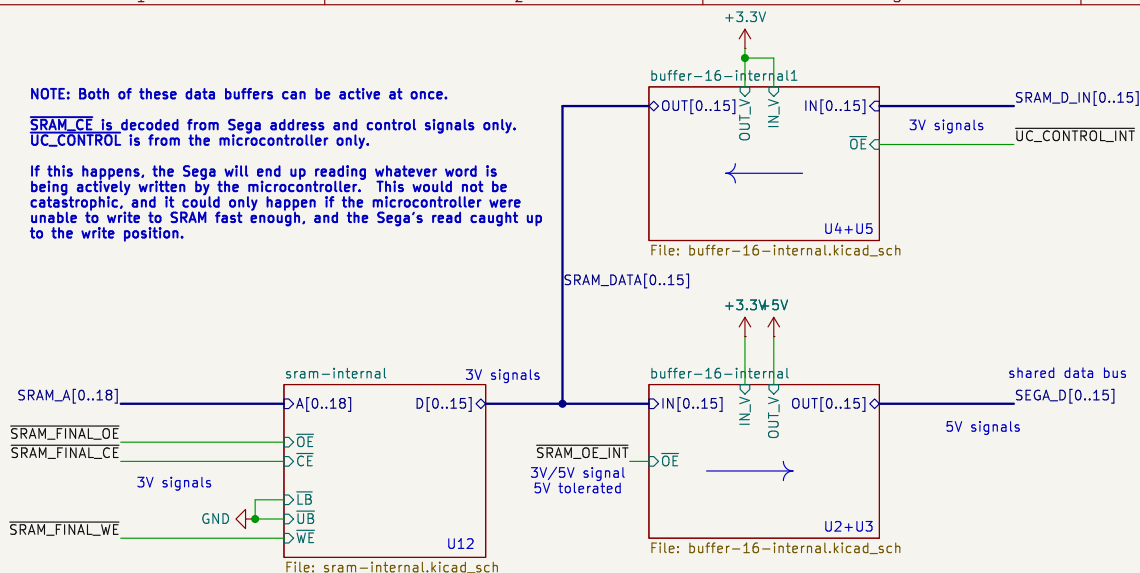


NOTE: Both of these data buffers can be active at once.

SRAM\_CE is decoded from Sega address and control signals only.  
UC\_CONTROL is from the microcontroller only.

If this happens, the Sega will end up reading whatever word is being actively written by the microcontroller. This would not be catastrophic, and it could only happen if the microcontroller were unable to write to SRAM fast enough, and the Sega's read caught up to the write position.



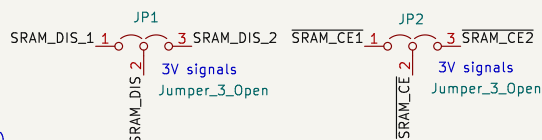
These two jumpers need to be soldered the same way.  
e.g.:

SRAM\_DIS = SRAM\_DIS\_1 and SRAM\_CE = SRAM\_CE\_1

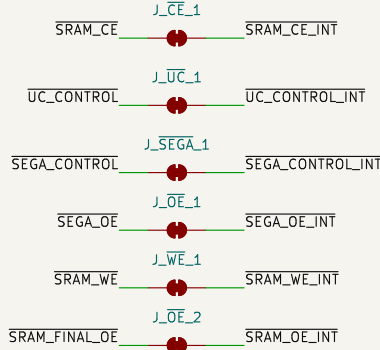
or

SRAM\_DIS = SRAM\_DIS\_2 and SRAM\_CE = SRAM\_CE\_2

This determines whether the board responds as bank 1 (2MB - 3MB range) or bank 2 (3MB - 4MB range).

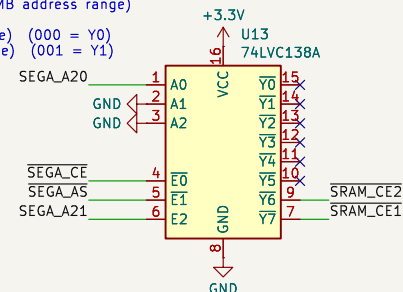


These bridges can be used to snoop on these signals, or cut with a knife to hijack them.



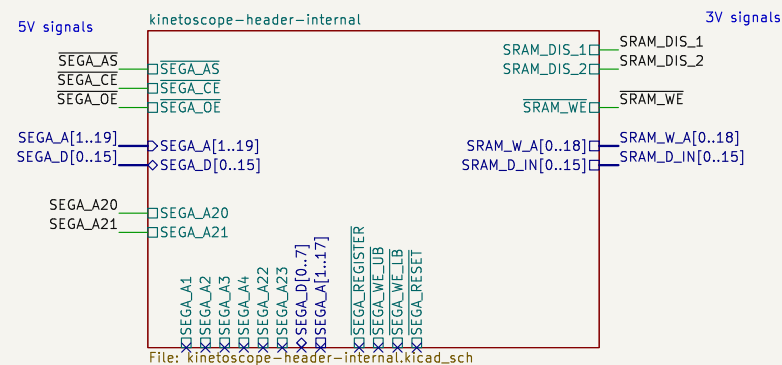
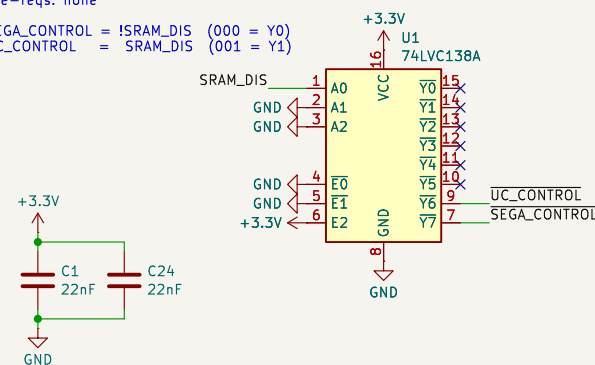
Decoder for SRAM chip-select  
Pre-reqs: A21 & A5 & CE (2MB-4MB address range)

SRAM\_CE1 = !A20 (2MB-3MB range) (000 = Y0)  
SRAM\_CE2 = A20 (3MB-4MB range) (001 = Y1)



Decoder for SRAM disconnect  
Pre-reqs: none

SEGA\_CONTROL = !SRAM\_DIS (000 = Y0)  
UC\_CONTROL = SRAM\_DIS (001 = Y1)



Sheet: /

File: sram-bank.kicad\_sch

**Title: Kinetoscope SRAM Bank**

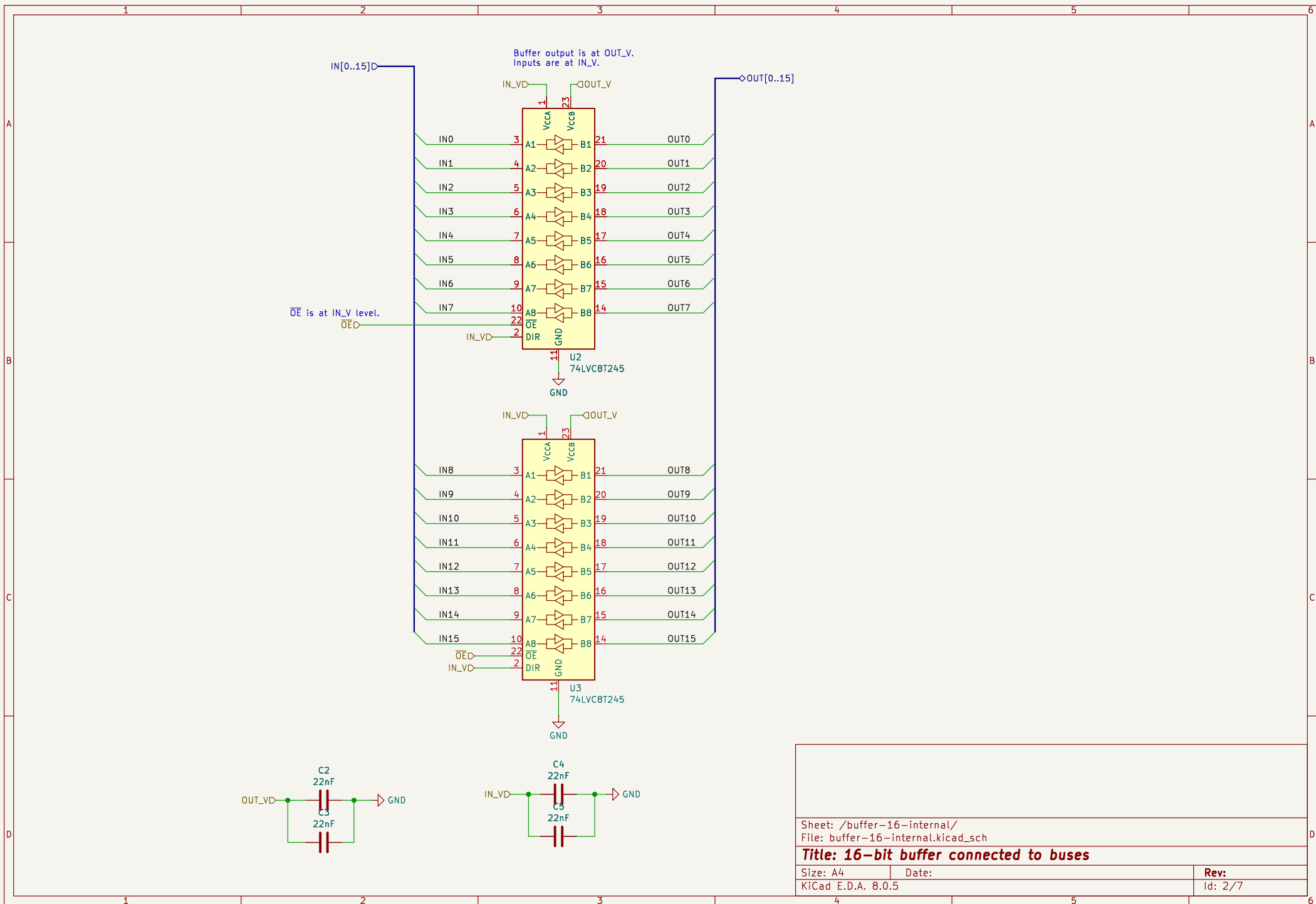
Size: A4

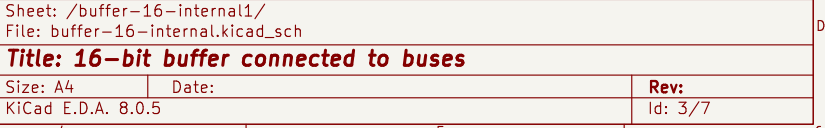
Date:

KiCad E.D.A. 8.0.5

Rev:

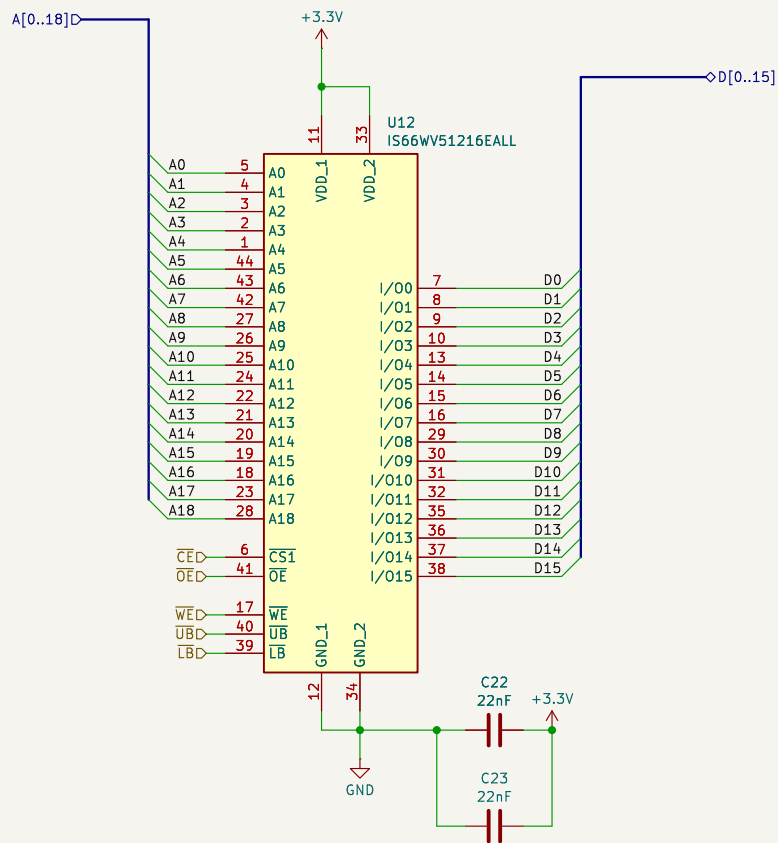
Id: 1/7











Sheet: /sram-internal/  
File: sram-internal.kicad\_sch

**Title: SRAM connected to buses**

Size: A4  
KiCad E.D.A. 8.0.5

Date:

Rev:  
Id: 6/7

