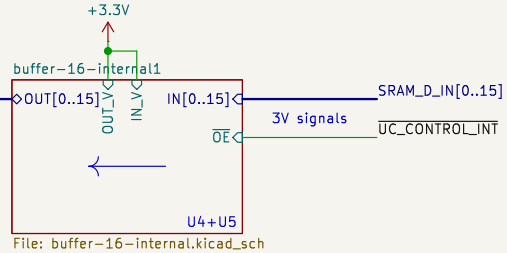
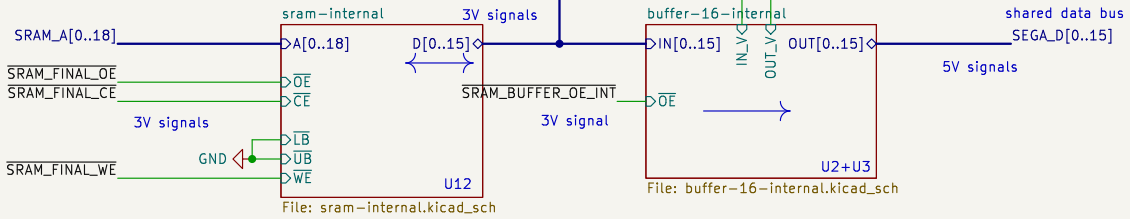
NOTE: Both of these data buffers can be active at once.

SRAM_OE is decoded from Sega address and control signals only.
UC_CONTROL is from the microcontroller only.

If this happens, the Sega will end up reading whatever word is being actively written by the microcontroller. This would not be catastrophic, and it could only happen if the microcontroller were unable to write to SRAM fast enough, and the Sega's read caught up to the write position.

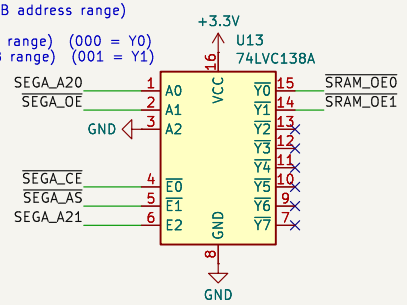


SRAM_DATA[0..15]



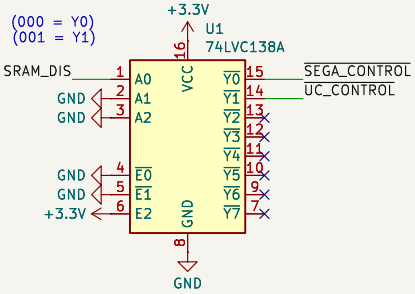
Decoder for SRAM output-enable
Pre-reqs: A21 & AS & CE (2MB-4MB address range)

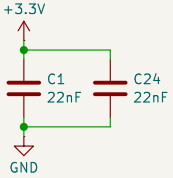
SRAM_OE0 = OE & !A20 (2MB-3MB range) (000 = Y0)
SRAM_OE1 = OE & A20 (3MB-4MB range) (001 = Y1)



Decoder for SRAM disconnect
Pre-reqs: none

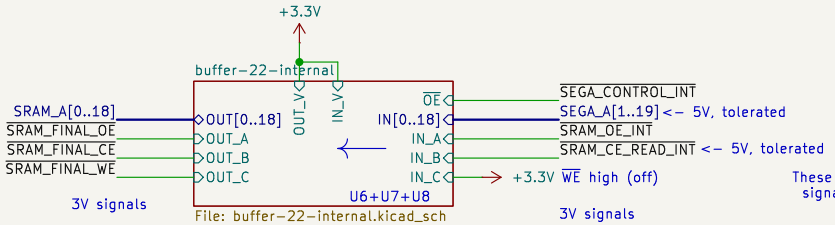
SEGA_CONTROL = !SRAM_DIS (000 = Y0)
UC_CONTROL = SRAM_DIS (001 = Y1)



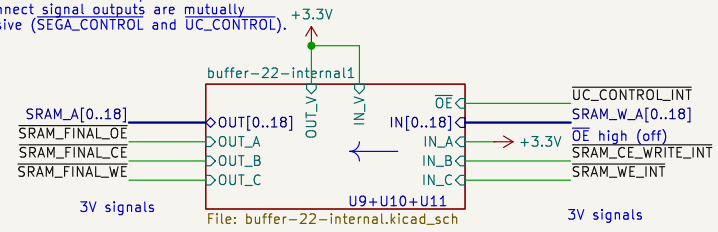


NOTE: A PSRAM's CE signal may not stay on at all times. There is a maximum pulse width of 15us for this chipset, so that the DRAM internal to the PSRAM can go through a refresh cycle.

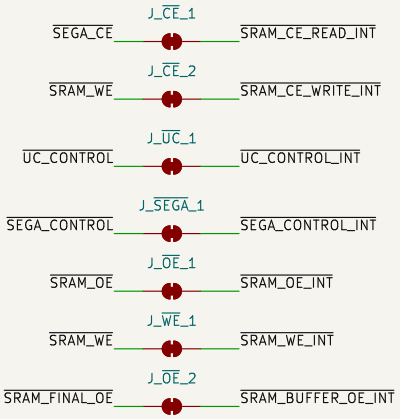
Tying CE to WE (for writes) or SEGA_CE (for reads) seems to meet all the timing requirements.

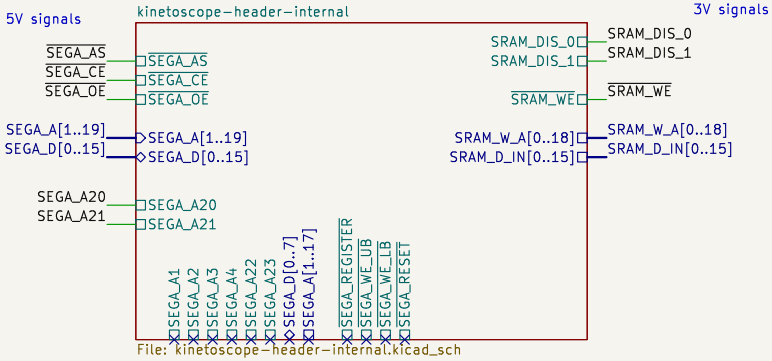


Only one of these is active at a time.
The address decoder outputs for the disconnect signal outputs are mutually exclusive (SEGA_CONTROL and UC_CONTROL).



These bridges can be used to snoop on these signals, or cut with a knife to hijack them.





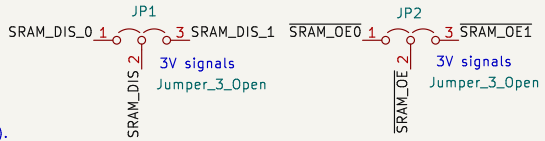
These two jumpers need to be soldered the same way.
e.g.:

SRAM_DIS = SRAM_DIS_0 and SRAM_CE = SRAM_CE_0

or

SRAM_DIS = SRAM_DIS_1 and SRAM_CE = SRAM_CE_1

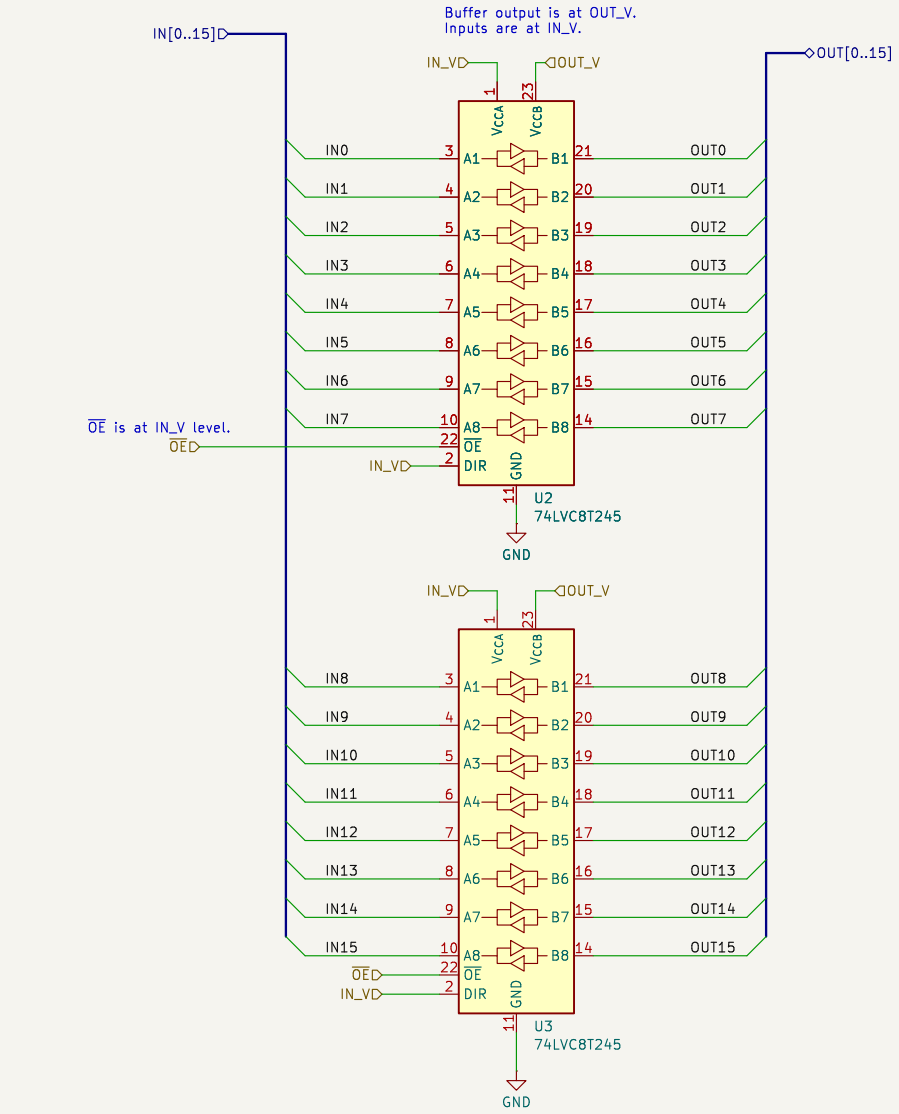
This determines whether the board responds as bank 0 (2MB – 3MB range) or bank 1 (3MB – 4MB range).



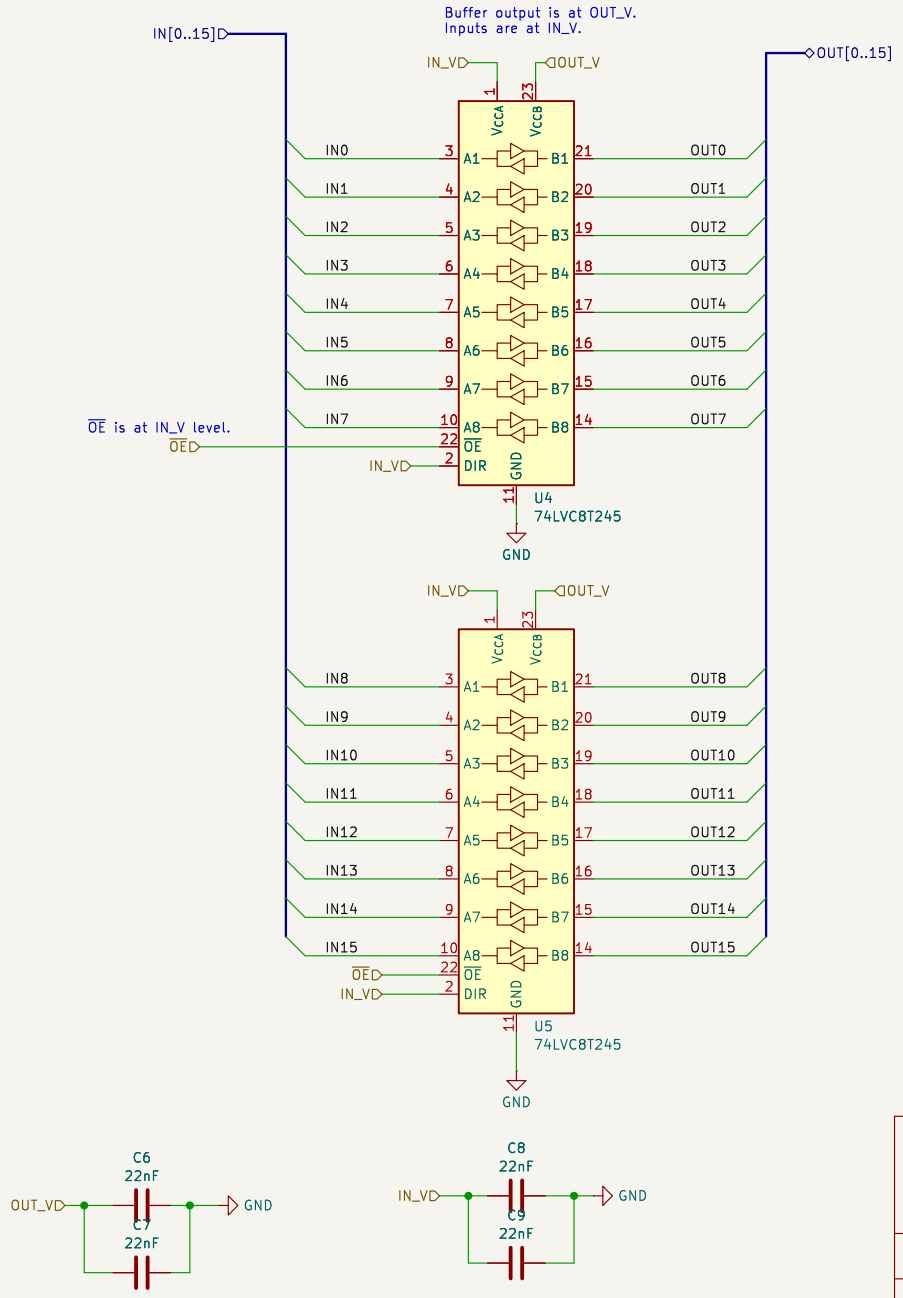
Sheet: /
File: sram-bank.kicad_sch

Title: Kinetoscope SRAM Bank

Size: A4	Date:	Rev:
KiCad E.D.A. 8.0.6		Id: 1/7



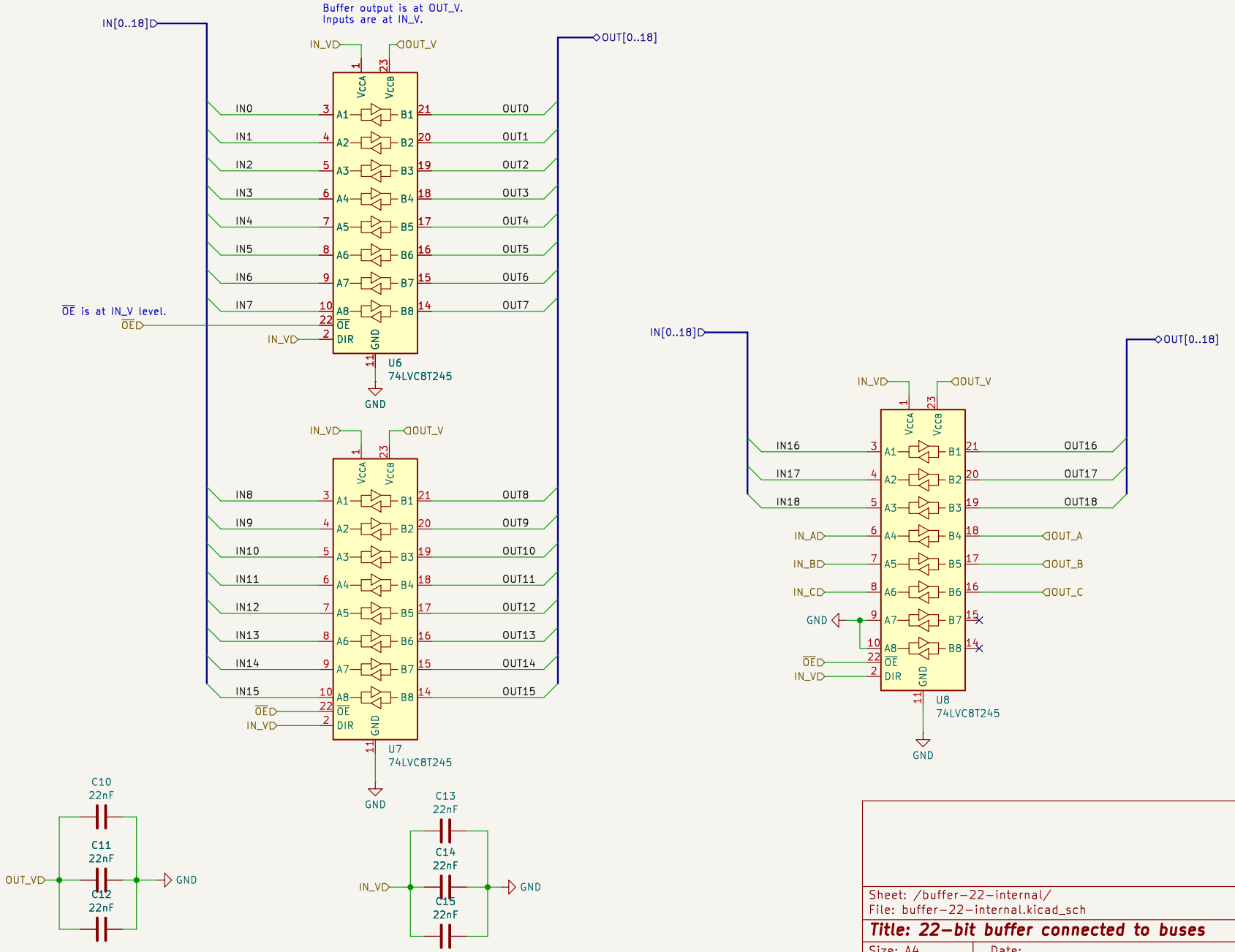
Sheet: /buffer-16-internal/	
File: buffer-16-internal.kicad_sch	
Title: 16-bit buffer connected to buses	
Size: A4	Date:
KiCad E.D.A. 8.0.6	Id: 2/7



Sheet: /buffer-16-internal1/
File: buffer-16-internal.kicad_sch

Title: 16-bit buffer connected to buses

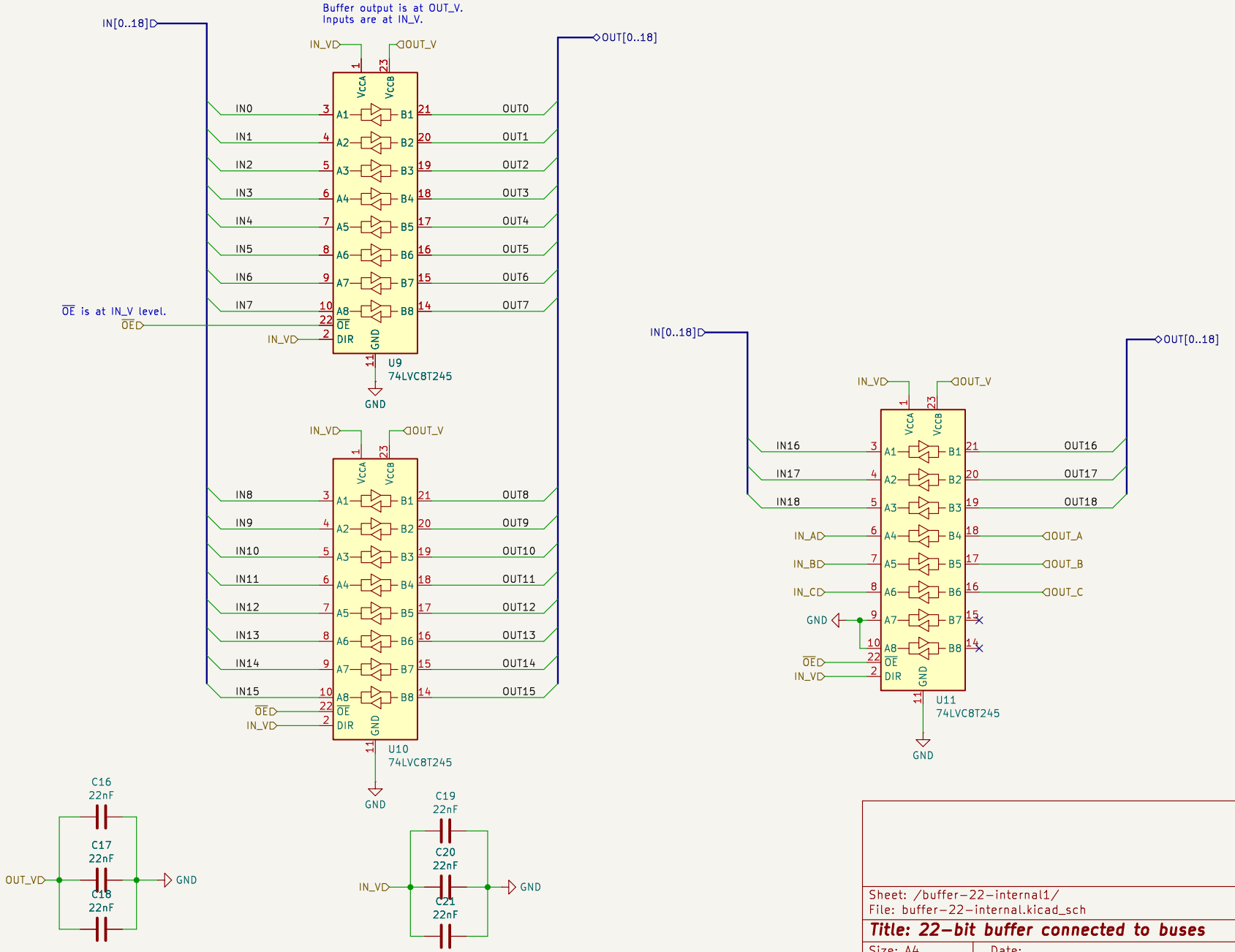
Size: A4	Date:	Rev:
KiCad E.D.A. 8.0.6		Id: 3/7



Sheet: /buffer-22-internal/
File: buffer-22-internal.kicad_sch

Title: 22-bit buffer connected to buses

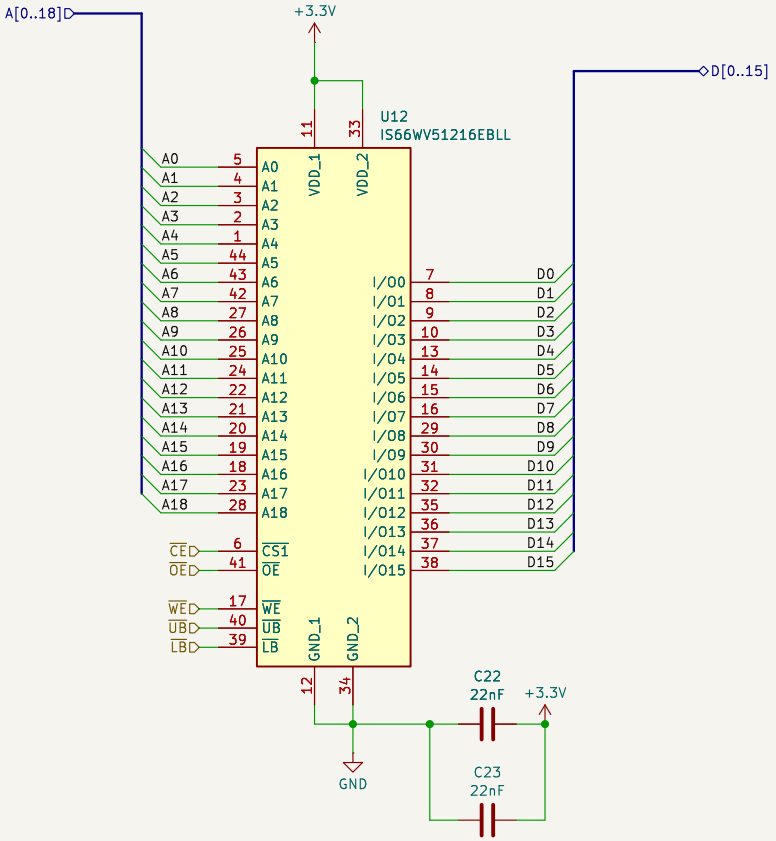
Size: A4	Date:	Rev:
KiCad E.D.A. 8.0.6		Id: 4/7



Sheet: /buffer-22-internal1/
File: buffer-22-internal.kicad_sch

Title: 22-bit buffer connected to buses

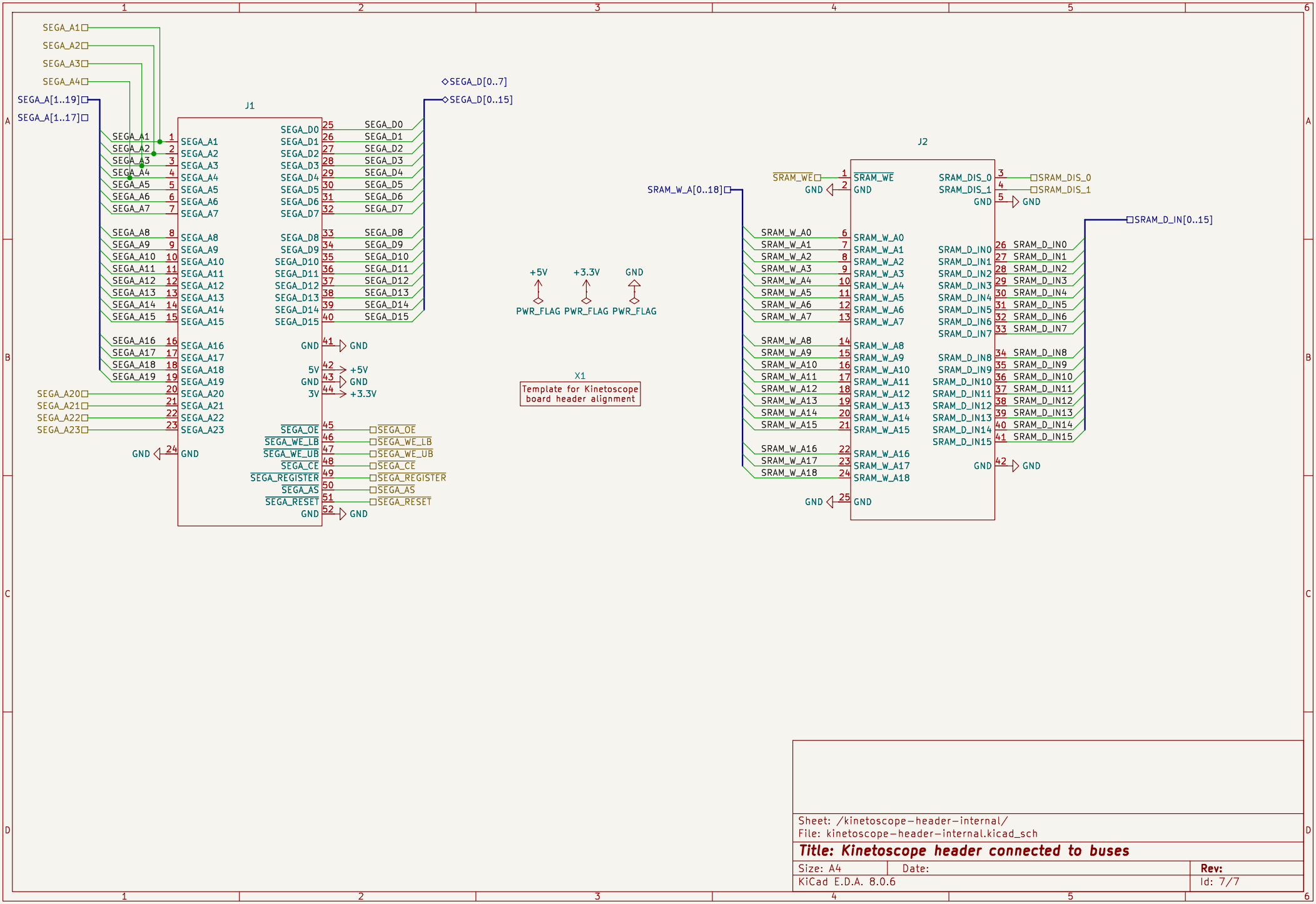
Size: A4	Date:	Rev:
KiCad E.D.A. 8.0.6		Id: 5/7



Sheet: /sram-internal/
File: sram-internal.kicad_sch

Title: SRAM connected to buses

Size: A4	Date:	Rev:
KiCad E.D.A. 8.0.6		Id: 6/7


SEGA_A1
SEGA_A2
SEGA_A3
SEGA_A4
SEGA_A[1..19]
SEGA_A[1..17]
J1
SEGA_D[0..7]
SEGA_D[0..15]
SEGA_A20
SEGA_A21
SEGA_A22
SEGA_A23
GND
SEGA_OE
SEGA_WE_LB
SEGA_WE_UB
SEGA_CE
SEGA_REGISTER
SEGA_AS
SEGA_RESET
+5V
+3.3V
PWR_FLAG
X1
Template for Kinetoscope board header alignment
J2
SRAM_W_A[0..18]
SRAM_WE
SRAM_DIS_0
SRAM_DIS_1
SRAM_D_IN[0..15]
Sheet: /kinetoscope-header-internal/
File: kinetoscope-header-internal.kicad_sch
Title: Kinetoscope header connected to buses
Size: A4
Date:
Rev:
KiCad E.D.A. 8.0.6
Id: 7/7