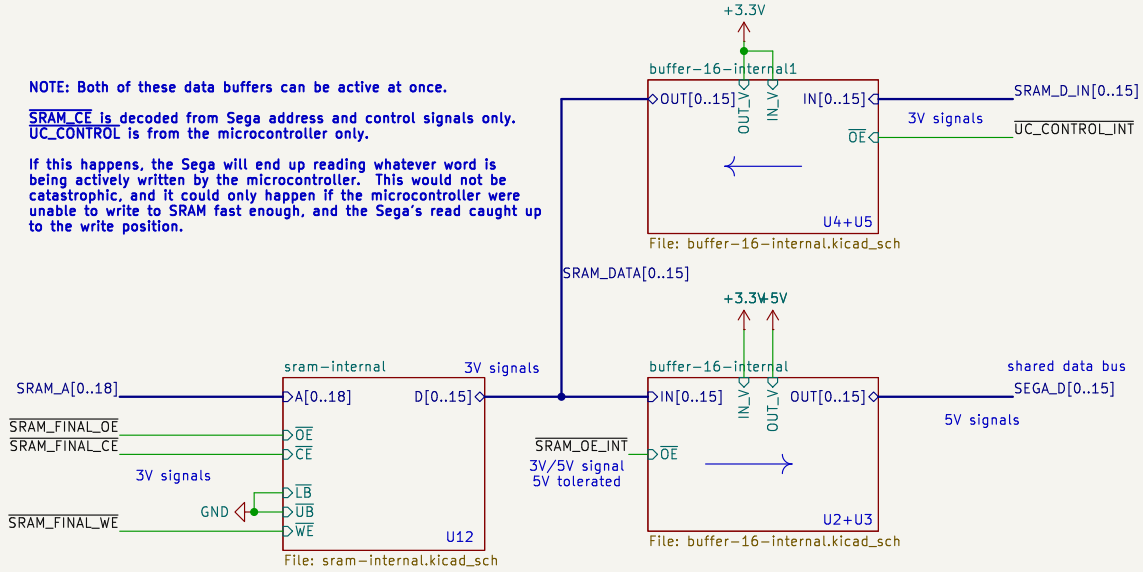
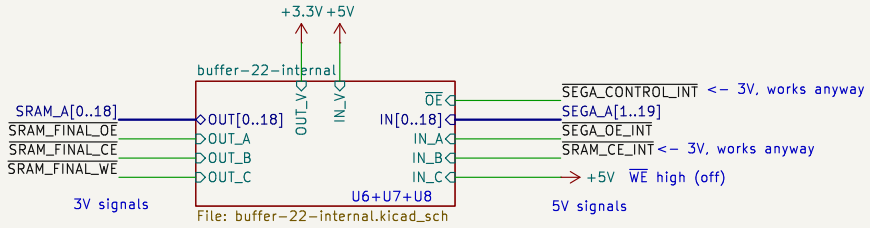
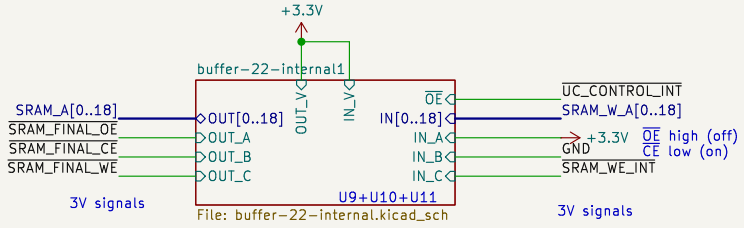
NOTE: Both of these data buffers can be active at once.

$\overline{\text{SRAM\_CE}}$ is decoded from Sega address and control signals only. $\overline{\text{UC\_CONTROL}}$ is from the microcontroller only.

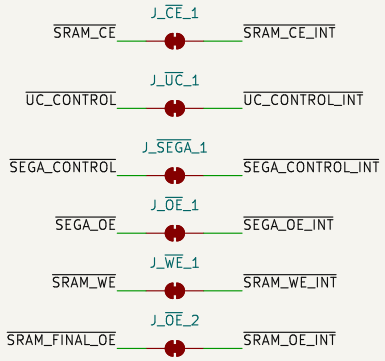
If this happens, the Sega will end up reading whatever word is being actively written by the microcontroller. This would not be catastrophic, and it could only happen if the microcontroller were unable to write to SRAM fast enough, and the Sega's read caught up to the write position.







These bridges can be used to snoop on these signals, or cut with a knife to hijack them.



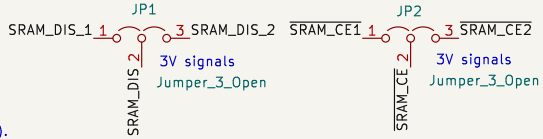
These two jumpers need to be soldered the same way.
e.g.:

SRAM_DIS = SRAM_DIS_1 and $\overline{\text{SRAM\_CE}}$ = $\overline{\text{SRAM\_CE\_1}}$

or

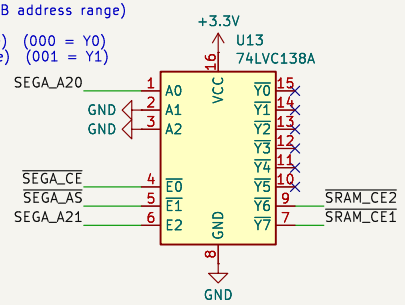
SRAM_DIS = SRAM_DIS_2 and $\overline{\text{SRAM\_CE}}$ = $\overline{\text{SRAM\_CE\_2}}$

This determines whether the board responds as bank 1 (2MB – 3MB range) or bank 2 (3MB – 4MB range).



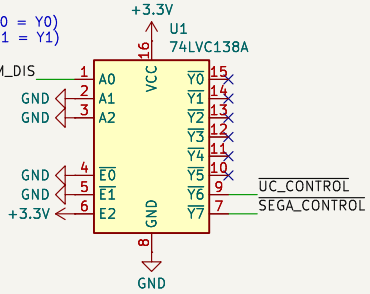
Decoder for SRAM chip-select
Pre-reqs: A21 & AS & CE (2MB-4MB address range)

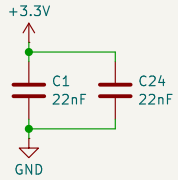
SRAM_CE1 = !A20 (2MB-3MB range) (000 = Y0)
SRAM_CE2 = A20 (3MB-4MB range) (001 = Y1)

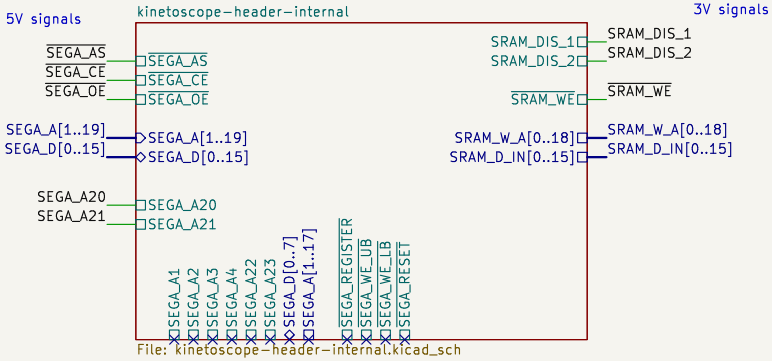


Decoder for SRAM disconnect
Pre-reqs: none

SEGA_CONTROL = !SRAM_DIS (000 = Y0)
UC_CONTROL = SRAM_DIS (001 = Y1)



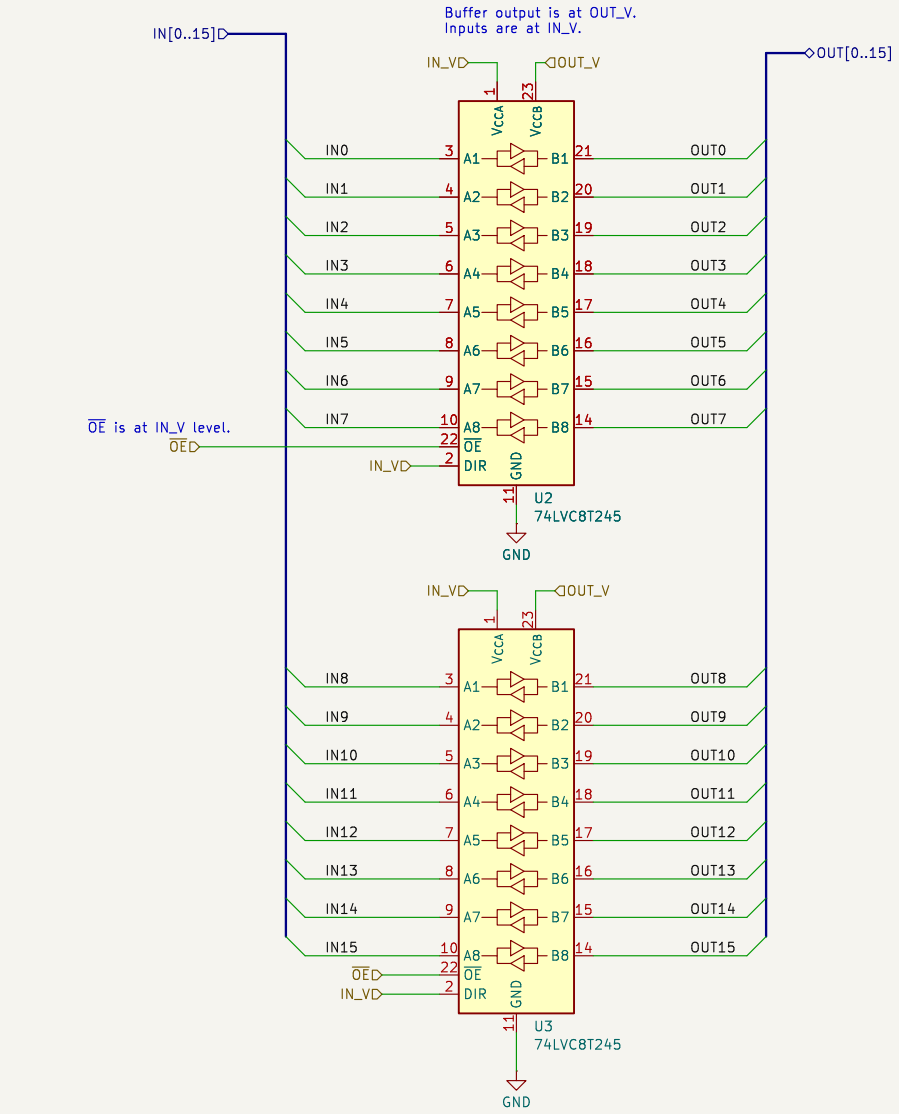




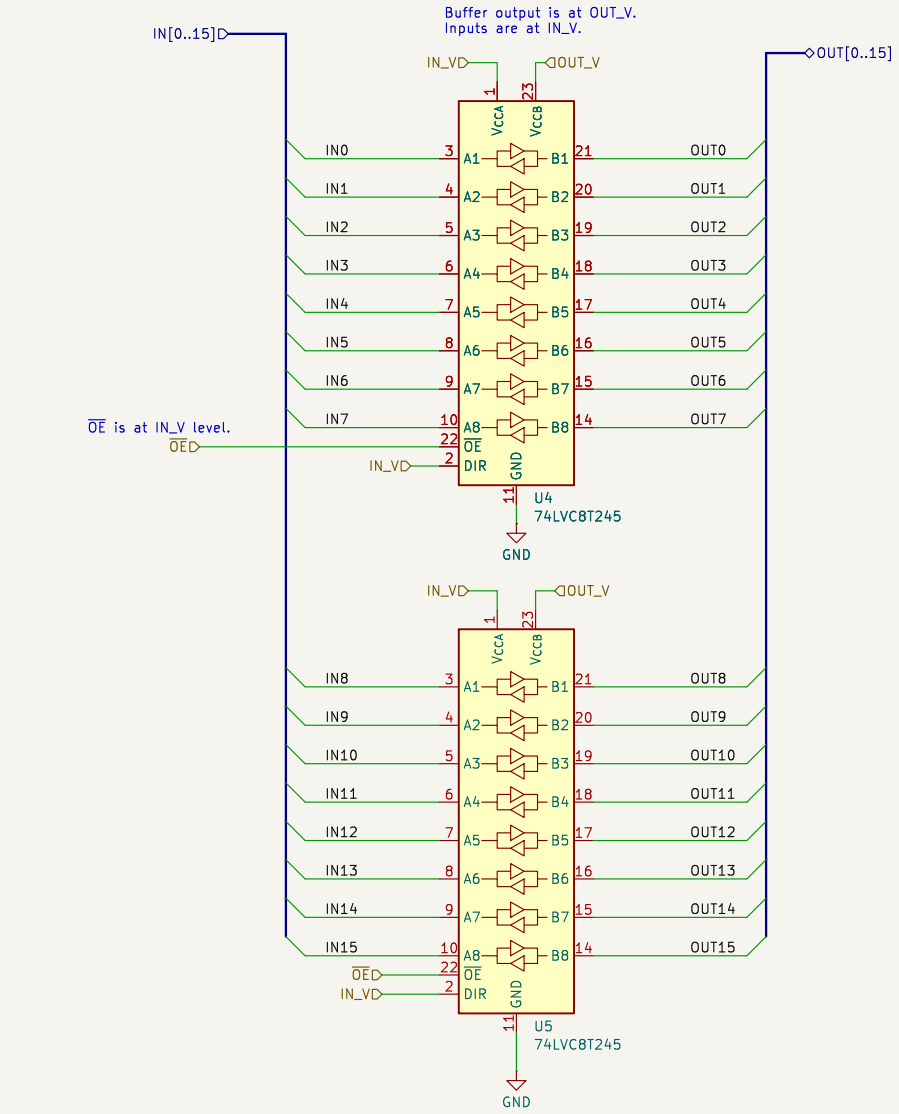
Sheet: /
File: sram-bank.kicad_sch

Title: Kinetoscope SRAM Bank

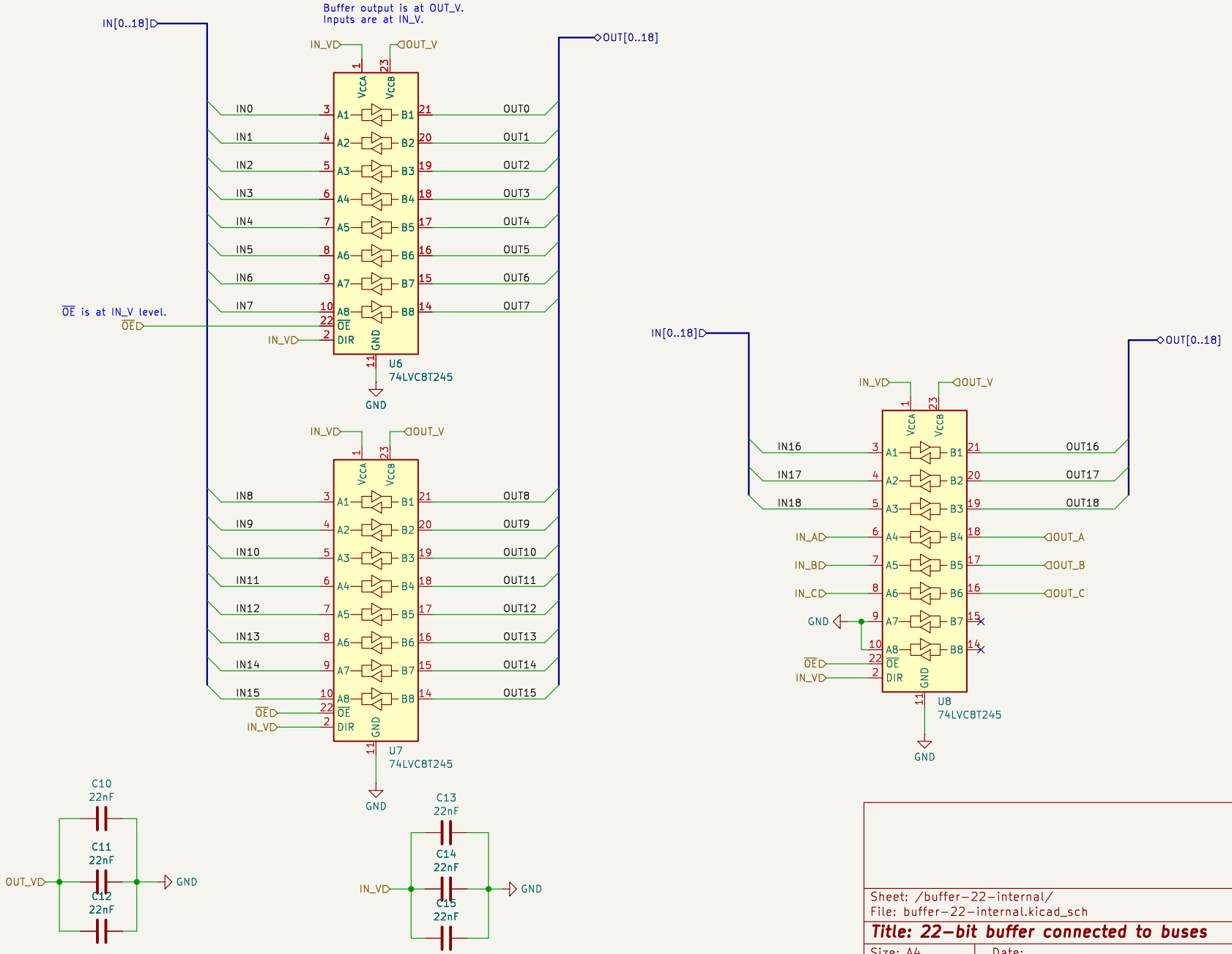
Size: A4	Date:	Rev:
KiCad E.D.A. 8.0.5		Id: 1/7



Sheet: /buffer-16-internal/	
File: buffer-16-internal.kicad_sch	
Title: 16-bit buffer connected to buses	
Size: A4	Date:
KiCad E.D.A. 8.0.5	Id: 2/7



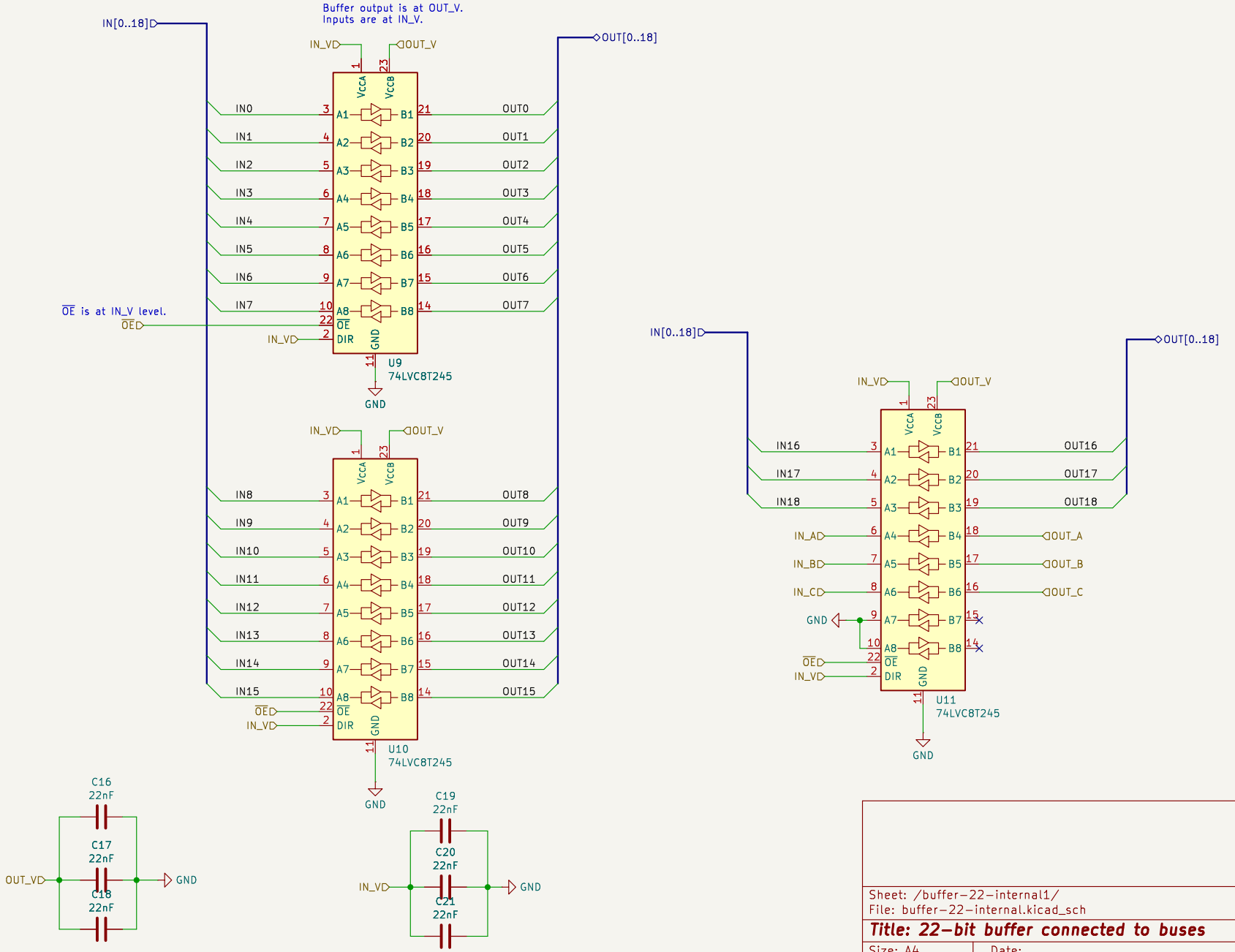
Sheet: /buffer-16-internal1/	
File: buffer-16-internal.kicad_sch	
Title: 16-bit buffer connected to buses	
Size: A4	Date:
KiCad E.D.A. 8.0.5	Id: 3/7

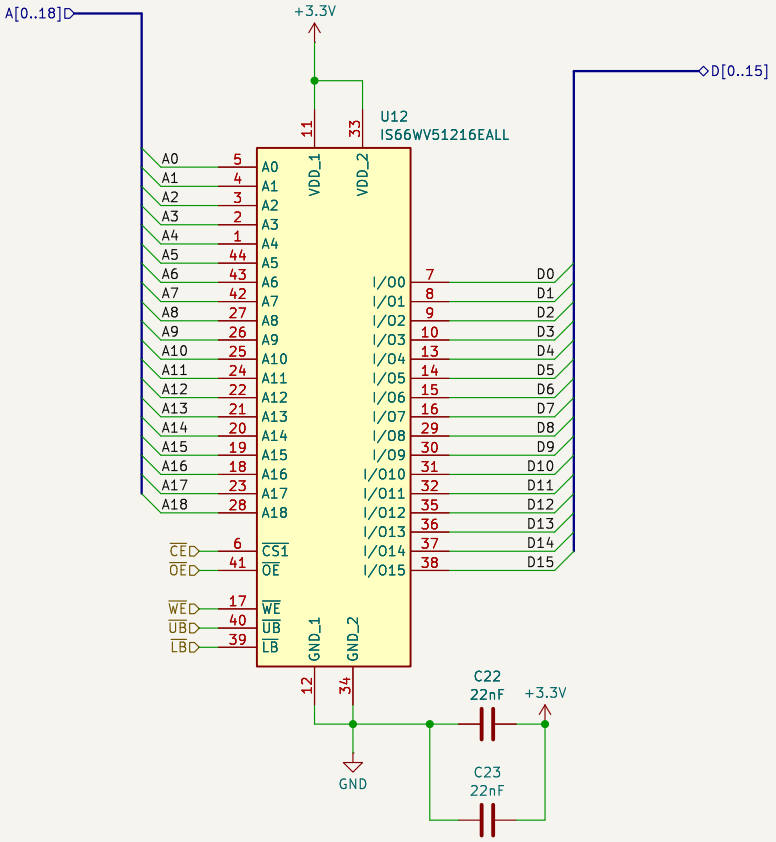


Sheet: /buffer-22-internal/
File: buffer-22-internal.kicad_sch

Title: 22-bit buffer connected to buses

Size: A4	Date:	Rev:
KiCad E.D.A. 8.0.5		Id: 4/7

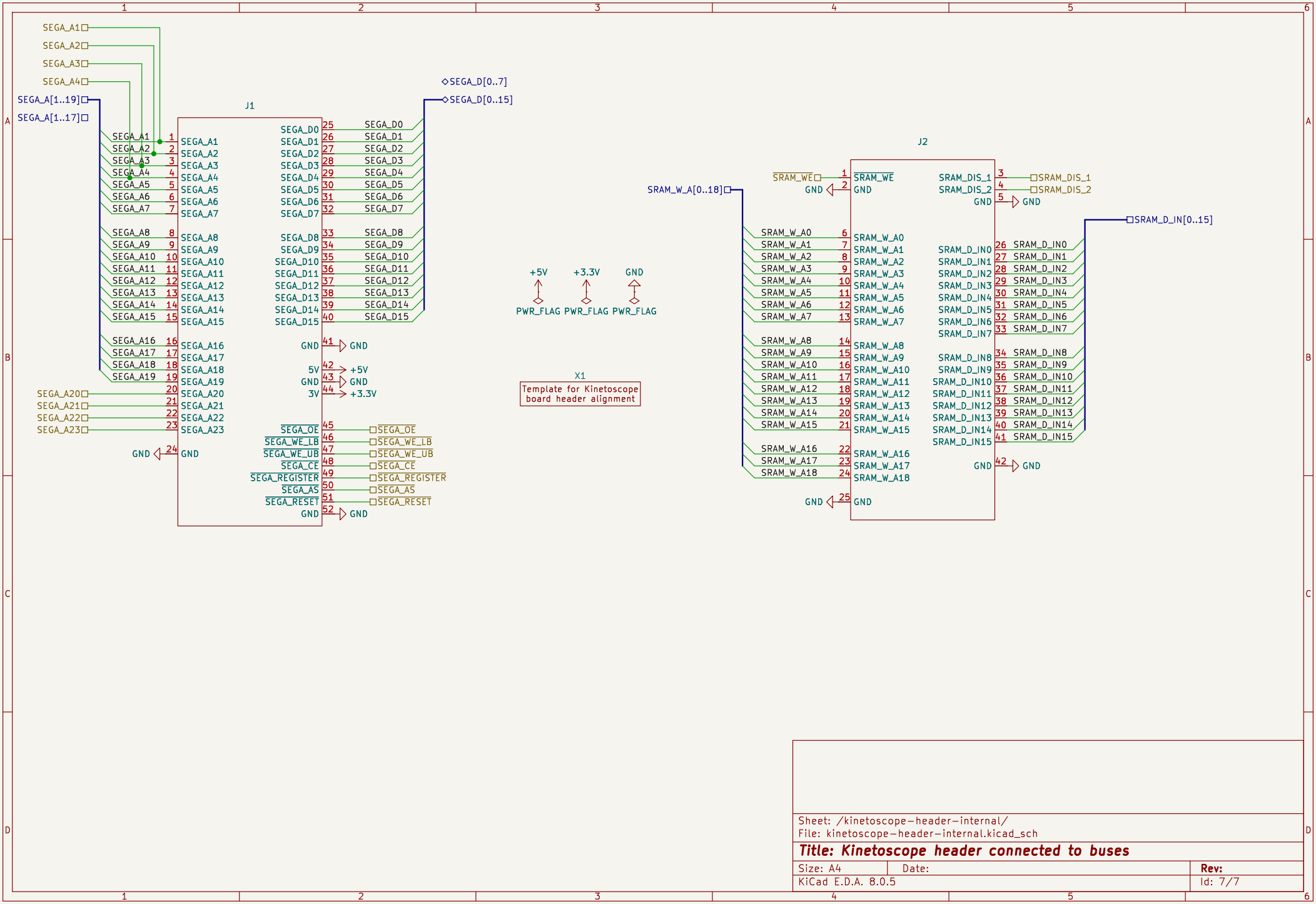

Buffer output is at OUT_V.
Inputs are at IN_V.
IN[0..18]
OUT[0..18]
IN_V
OUT_V
VCCA
VCCB
GND
DIR
OE
IN0
IN1
IN2
IN3
IN4
IN5
IN6
IN7
OUT0
OUT1
OUT2
OUT3
OUT4
OUT5
OUT6
OUT7
OE is at IN_V level.
U9
74LVC8T245
IN8
IN9
IN10
IN11
IN12
IN13
IN14
IN15
OUT8
OUT9
OUT10
OUT11
OUT12
OUT13
OUT14
OUT15
U10
74LVC8T245
IN16
IN17
IN18
IN_A
IN_B
IN_C
OUT16
OUT17
OUT18
OUT_A
OUT_B
OUT_C
U11
74LVC8T245
C16
22nF
C17
22nF
C18
22nF
C19
22nF
C20
22nF
C21
22nF
OUT_V
Sheet: /buffer-22-internal1/
File: buffer-22-internal.kicad_sch
Title: 22-bit buffer connected to buses
Size: A4
Date:
Rev:
KiCad E.D.A. 8.0.5
Id: 5/7



Sheet: /sram-internal/
File: sram-internal.kicad_sch

Title: SRAM connected to buses

Size: A4	Date:	Rev:
KiCad E.D.A. 8.0.5		Id: 6/7


SEGA_A1
SEGA_A2
SEGA_A3
SEGA_A4
SEGA_A[1..19]
SEGA_A[1..17]
J1
SEGA_D[0..7]
SEGA_D[0..15]
SEGA_A20
SEGA_A21
SEGA_A22
SEGA_A23
GND
+5V
3V
+3.3V
SEGA_OE
SEGA_WE_LB
SEGA_WE_UB
SEGA_CE
SEGA_REGISTER
SEGA_AS
SEGA_RESET
+5V
+3.3V
GND
PWR_FLAG
X1
Template for Kinetoscope board header alignment
J2
SRAM_W_A[0..18]
SRAM_WE
SRAM_DIS_1
SRAM_DIS_2
SRAM_D_IN[0..15]
Sheet: /kinetoscope-header-internal/
File: kinetoscope-header-internal.kicad_sch
Title: Kinetoscope header connected to buses
Size: A4
Date:
Rev:
KiCad E.D.A. 8.0.5
Id: 7/7