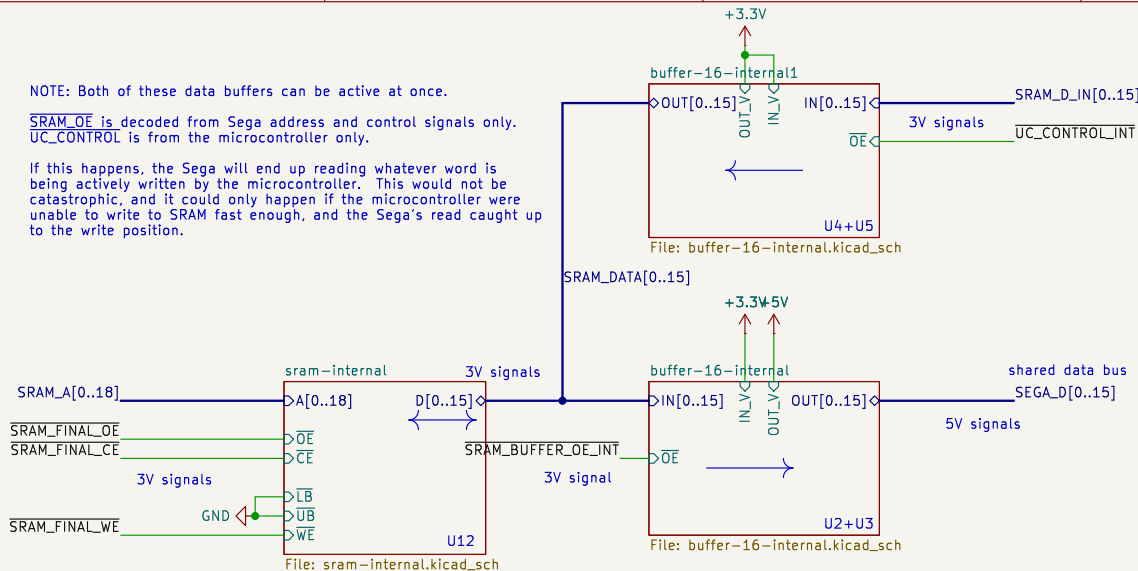


NOTE: Both of these data buffers can be active at once.

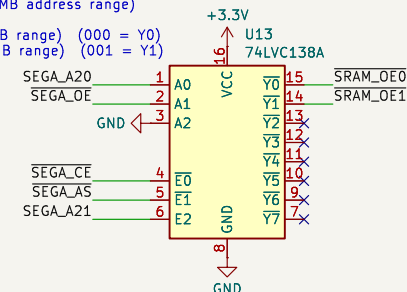
SRAM_OE is decoded from Sega address and control signals only.
UC_CONTROL is from the microcontroller only.

If this happens, the Sega will end up reading whatever word is being actively written by the microcontroller. This would not be catastrophic, and it could only happen if the microcontroller were unable to write to SRAM fast enough, and the Sega's read caught up to the write position.



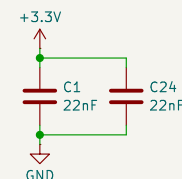
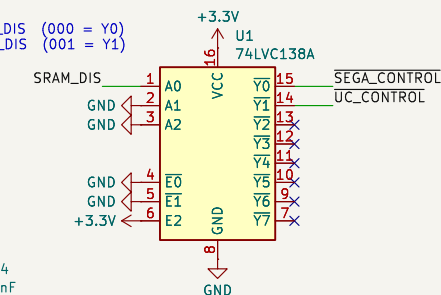
Decoder for SRAM output-enable
Pre-reqs: A21 & A5 & CE (2MB-4MB address range)

SRAM_OE0 = OE & !A20 (2MB-3MB range) (000 = Y0)
SRAM_OE1 = OE & A20 (3MB-4MB range) (001 = Y1)



Decoder for SRAM disconnect
Pre-reqs: none

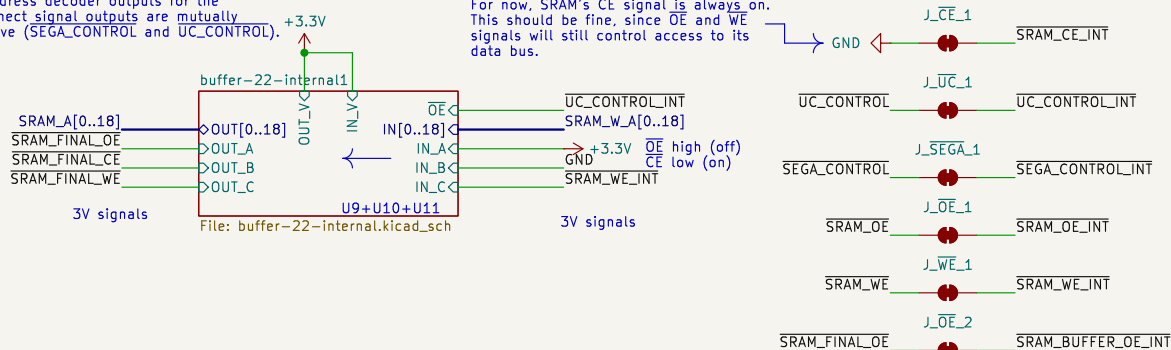
SEGA_CONTROL = !SRAM_DIS (000 = Y0)
UC_CONTROL = SRAM_DIS (001 = Y1)



Only one of these is active at a time.
The address decoder outputs for the disconnect signal outputs are mutually exclusive (SEGA_CONTROL and UC_CONTROL).

For now, SRAM's CE signal is always on.
This should be fine, since OE and WE signals will still control access to its data bus.

These bridges can be used to snoop on these signals, or cut with a knife to hijack them.



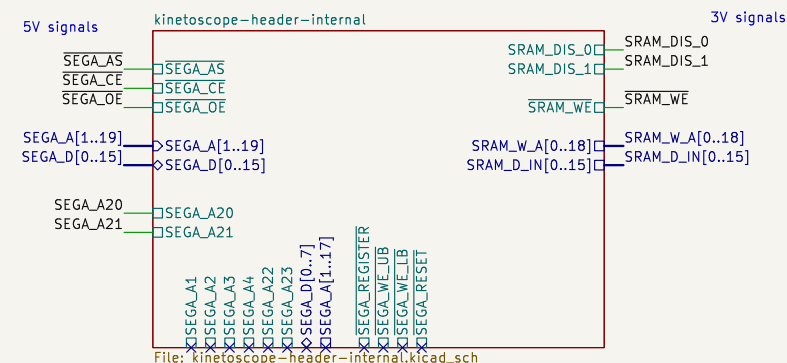
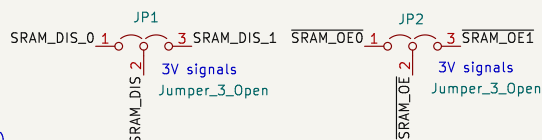
These two jumpers need to be soldered the same way.
e.g.:

SRAM_DIS = SRAM_DIS_0 and SRAM_CE = SRAM_CE_0

or

SRAM_DIS = SRAM_DIS_1 and SRAM_CE = SRAM_CE_1

This determines whether the board responds as bank 0 (2MB - 3MB range) or bank 1 (3MB - 4MB range).



Sheet: /

File: sram-bank.kicad_sch

Title: Kinetoscope SRAM Bank

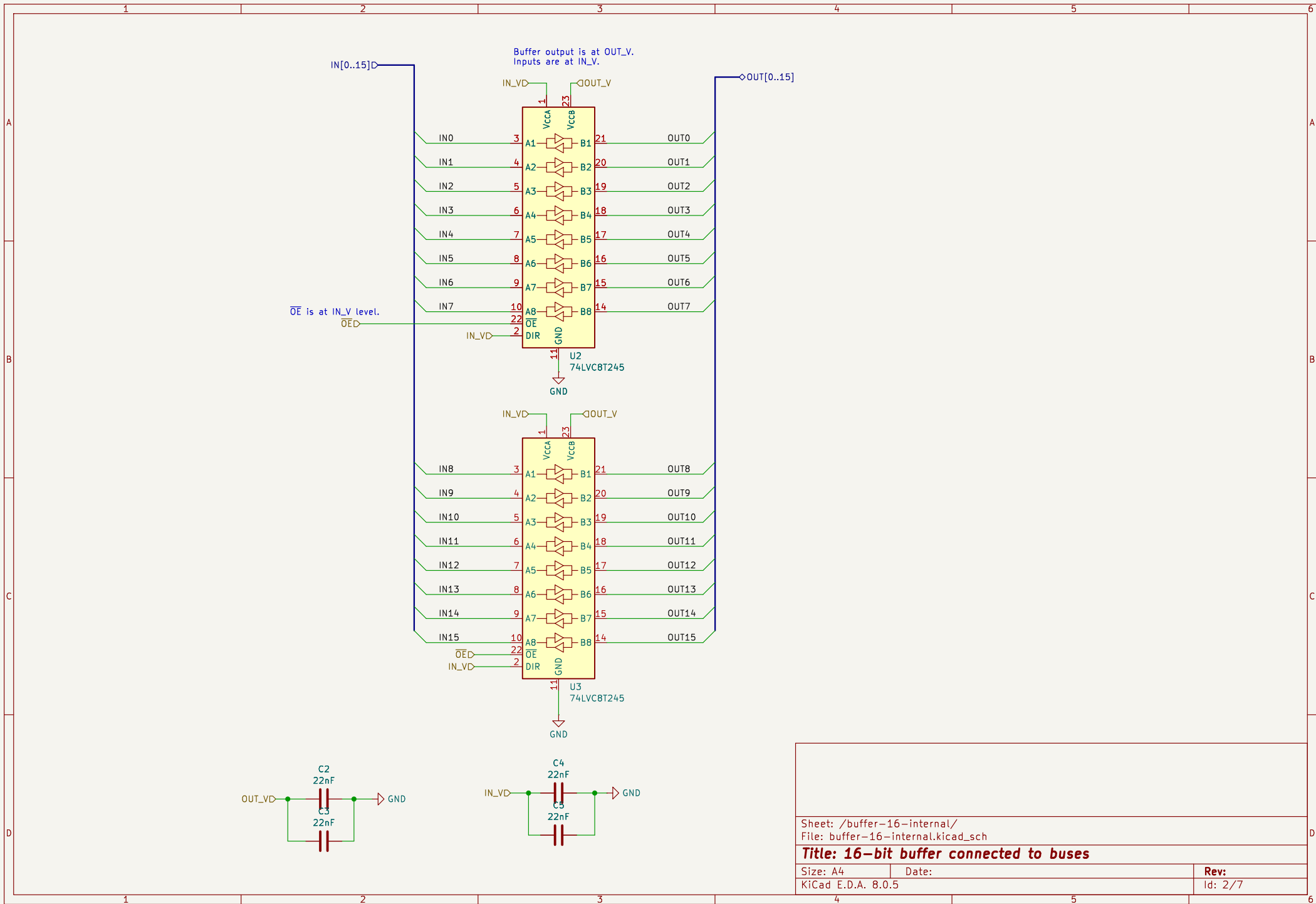
Size: A4

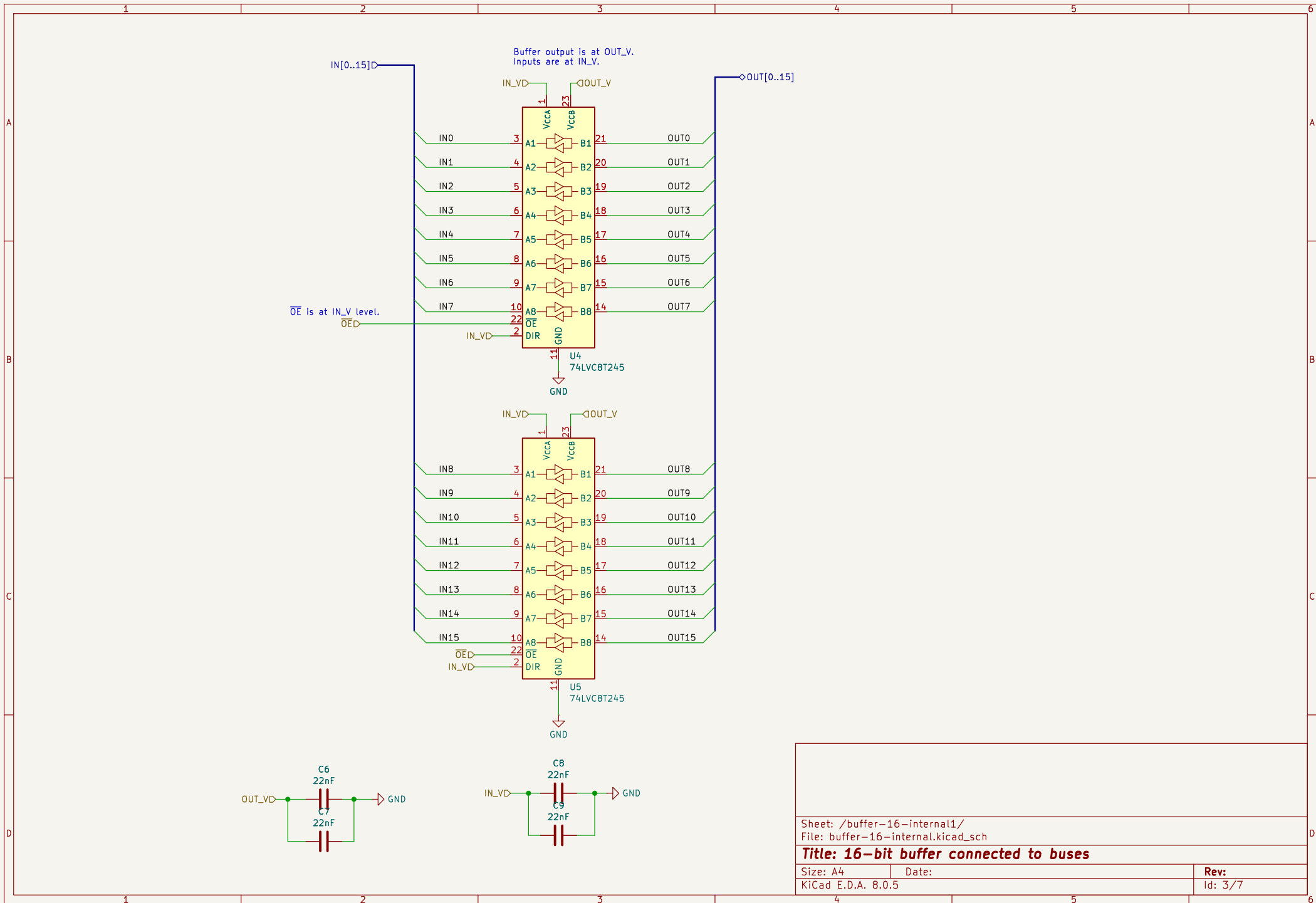
Date:

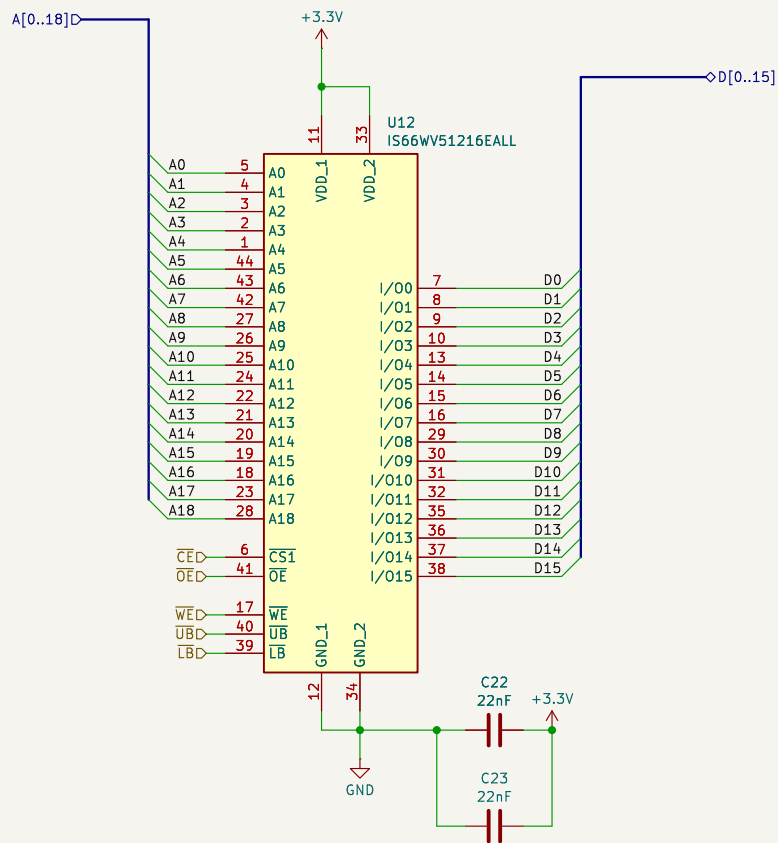
KiCad E.D.A. 8.0.5

Rev:

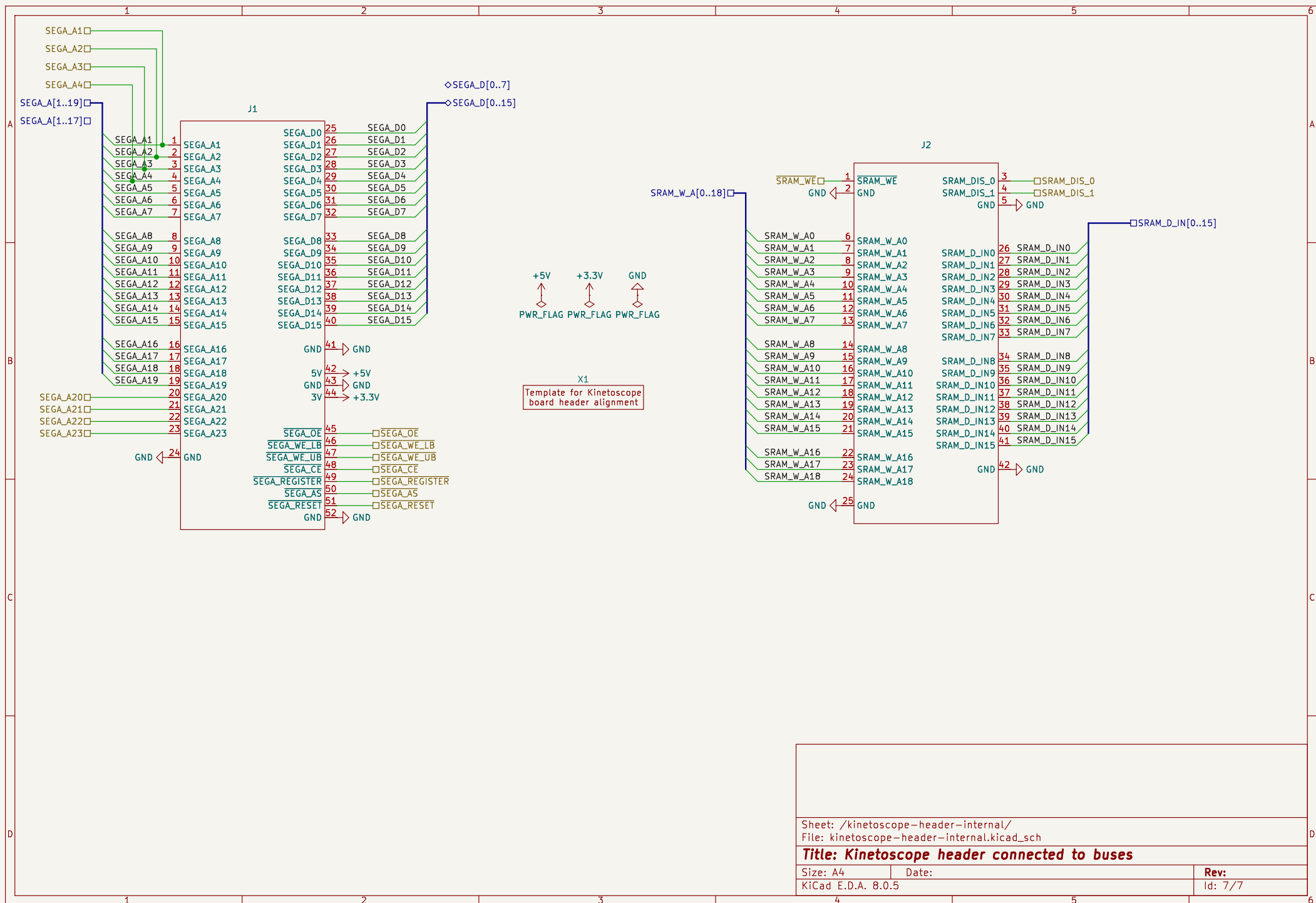
Id: 1/7







Sheet: /sram-internal/ File: sram-internal.kicad_sch		
Title: SRAM connected to buses		
Size: A4	Date:	Rev:
KiCad E.D.A. 8.0.5	Id: 6/7	



Sheet: /kinetoscope-header-internal/
File: kinetoscope-header-internal.kicad_sch

Title: Kinetoscope header connected to buses

Size: A4	Date:	Rev:
KiCad E.D.A. 8.0.5		Id: 7/7