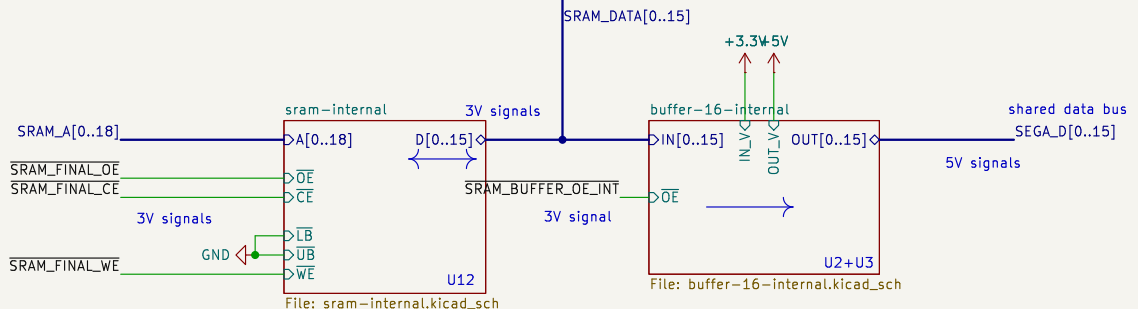


NOTE: Both of these data buffers can be active at once.

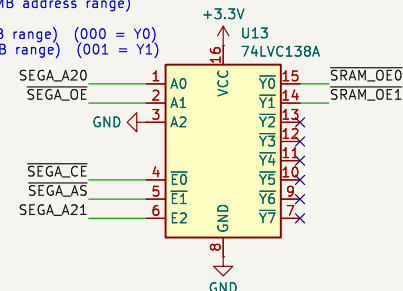
SRAM\_OE is decoded from Sega address and control signals only.  
UC\_CONTROL is from the microcontroller only.

If this happens, the Sega will end up reading whatever word is being actively written by the microcontroller. This would not be catastrophic, and it could only happen if the microcontroller were unable to write to SRAM fast enough, and the Sega's read caught up to the write position.



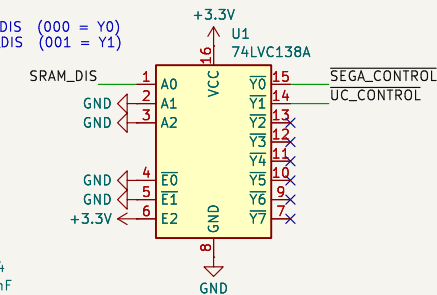
Decoder for SRAM output-enable  
Pre-reqs: A21 & A5 & CE (2MB-4MB address range)

SRAM\_OE0 = OE & !A20 (2MB-3MB range) (000 = Y0)  
SRAM\_OE1 = OE & A20 (3MB-4MB range) (001 = Y1)



Decoder for SRAM disconnect  
Pre-reqs: none

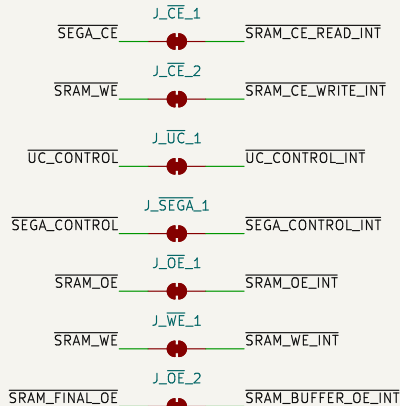
SEGA\_CONTROL = !SRAM\_DIS (000 = Y0)  
UC\_CONTROL = SRAM\_DIS (001 = Y1)



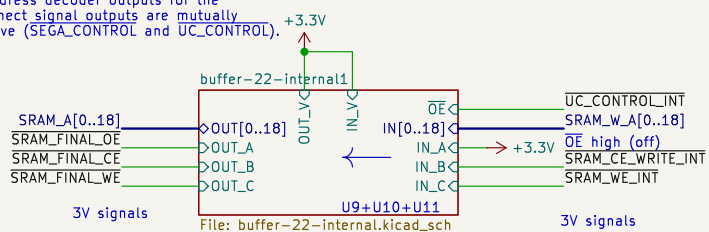
NOTE: A PSRAM's CE signal may not stay on at all times. There is a maximum pulse width of 15us for this chipset, so that the DRAM internal to the PSRAM can go through a refresh cycle.

Tying CE to WE (for writes) or SEGA\_CE (for reads) seems to meet all the timing requirements.

These bridges can be used to snoop on these signals, or cut with a knife to hijack them.



Only one of these is active at a time.  
The address decoder outputs for the disconnect signal outputs are mutually exclusive (SEGA\_CONTROL and UC\_CONTROL).



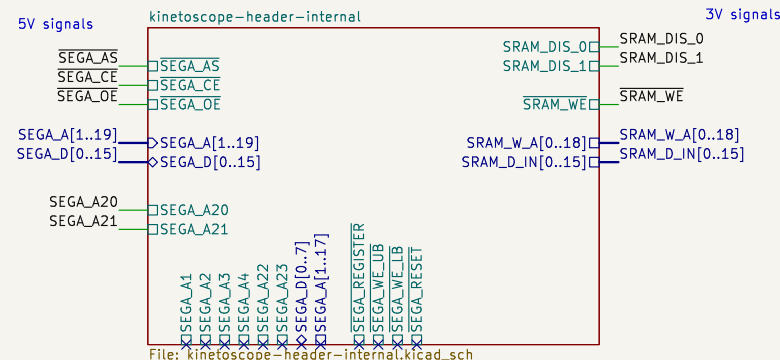
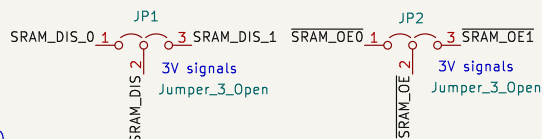
These two jumpers need to be soldered the same way.  
e.g.:

SRAM\_DIS = SRAM\_DIS\_0 and SRAM\_CE = SRAM\_CE\_0

or

SRAM\_DIS = SRAM\_DIS\_1 and SRAM\_CE = SRAM\_CE\_1

This determines whether the board responds as bank 0 (2MB - 3MB range) or bank 1 (3MB - 4MB range).



Sheet: /

File: sram-bank.kicad\_sch

## Title: Kinetoscope SRAM Bank

Size: A4

Date:

KiCad E.D.A. 8.0.5

Rev:

Id: 1/7

