ADVANCED COMPUTER ARCHITECTURE:

Parallelism, Scalability, Programmability

Kai Hwang

Professor of Electrical Engineering and Computer Science University of Southern California

1994

McGraw-Hill, Inc.

New York St. Louis San Francisco Auckland Bogotá
Caracas Lisbon London Madrid Mexico
Milan Montreal New Delhi Paris
San Juan Singapore Sydney Tokyo Toronto

Contents

Forewor	d			xvii
Preface				. xix
Part 1	THEORY OF	Parallelism	:	1
Chapt	er 1 Parallel (Computer Models		3
1.1		aputing		
		er Development Milestones		
		of Modern Computers		
		n of Computer Architecture		
	1.1.4 System A	Attributes to Performance		. 14
1.2	Multiprocessors a	and Multicomputers		. 19
	-	Iemory Multiprocessors		
		ed-Memory Multicomputers		
	1.2.3 Á Taxone	omy of MIMD Computers		. 27
1.3	Multivector and S	SIMD Computers		. 27
		upercomputers		
	1.3.2 SIMD Su	percomputers		3 0
1.4	PRAM and VLSI	[Models		. 32
		Random-Access Machines		
	1.4.2 VLSI Co.	mplexity Model		. 38
1.5	Architectural Dev	velopment Tracks		41
		-Processor Tracks		
		tor and SIMD Tracks		
		eaded and Dataflow Tracks		
1.6	Bibliographic No	tes and Exercises		45

Chapte	er 2 l	Program and Network Properties51
2.1	Conditi	ons of Parallelism51
	2.1.1	Data and Resource Dependences
	2.1.2	Hardware and Software Parallelism57
	2.1.3	The Role of Compilers60
2.2	Prograi	m Partitioning and Scheduling61
	2.2.1	Grain Sizes and Latency
	2.2.2	Grain Packing and Scheduling
	2.2.3	Static Multiprocessor Scheduling67
2.3	_	m Flow Mechanisms70
	2.3.1	Control Flow Versus Data Flow
	2.3.2	Demand-Driven Mechanisms
	2.3.3	Comparison of Flow Mechanisms75
2.4	U	Interconnect Architectures
	$2.4.1 \\ 2.4.2$	Network Properties and Routing
	$\frac{2.4.2}{2.4.3}$	Dynamic Connection Networks
0.5		-
2.5	Bibliog	raphic Notes and Exercises96
Chapte	er 3]	Principles of Scalable Performance105
3.1	Perforn	nance Metrics and Measures105
	3.1.1	Parallelism Profile in Programs
	3.1.2	Harmonic Mean Performance
	3.1.3	Efficiency, Utilization, and Quality112
)	3.1.4	Standard Performance Measures
3.2	Parallel	Processing Applications118
	3.2.1	Massive Parallelism for Grand Challenges118
	3.2.2	Application Models of Parallel Computers122
	3.2.3	Scalability of Parallel Algorithms
3.3	-	p Performance Laws
•	3.3.1	Amdahl's Law for a Fixed Workload
	3.3.2	Gustafson's Law for Scaled Problems
	3.3.3	Memory-Bounded Speedup Model
3.4		lity Analysis and Approaches
	$3.4.1 \\ 3.4.2$	Scalability Metrics and Goals
•	3.4.2 $3.4.3$	Research Issues and Solutions
3.5		raphic Notes and Exercises
ა.ა	Bornera	rapine motes and exercises149

Contents

4.1.1 Advanced Processor Technology 157 4.1.1 Design Space of Processors 157 4.1.2 Instruction-Set Architectures 162 4.1.3 CISC Scalar Processors 165 4.1.4 RISC Scalar Processors 169 4.2 Superscalar and Vector Processors 177 4.2.1 Superscalar Processors 178 4.2.2 The VLIW Architecture 182 4.2.3 Vector and Symbolic Processors 184 4.3 Memory Hierarchy Technology 188 4.3.1 Hierarchical Memory Technology 188 4.3.2 Inclusion, Coherence, and Locality 190 4.3.3 Memory Capacity Planning 194 4.4 Virtual Memory Technology 196 4.4.1 Virtual Memory Models 196 4.4.2 TLB, Paging, and Segmentation 198 4.4.3 Memory Replacement Policies 205 4.5 Bibliographic Notes and Exercises 208 Chapter 5 Bus, Cache, and Shared Memory 213 5.1 Backplane Bus Systems 213 5.1.1 Backplane Bus Specification 213 5.1.2 Addressing and Timing Protocols 216 5.1.3 Arbitration, Transaction, and Interrupt 218 5.1.4 The	Chapte	e r 4	Processors and Memory Hierarchy	157
4.1.1 Design Space of Processors 157 4.1.2 Instruction-Set Architectures 162 4.1.3 CISC Scalar Processors 165 4.1.4 RISC Scalar Processors 169 4.2 Superscalar and Vector Processors 177 4.2.1 Superscalar Processors 178 4.2.2 The VLIW Architecture 182 4.2.3 Vector and Symbolic Processors 184 4.3 Memory Hierarchy Technology 188 4.3.1 Hierarchical Memory Technology 188 4.3.2 Inclusion, Coherence, and Locality 190 4.3.3 Memory Capacity Planning 194 4.4 Virtual Memory Technology 196 4.4.1 Virtual Memory Models 196 4.4.2 TLB, Paging, and Segmentation 198 4.4.3 Memory Replacement Policies 205 4.5 Bibliographic Notes and Exercises 208 Chapter 5 Bus, Cache, and Shared Memory 213 5.1 Backplane Bus Systems 213 5.1.2 Addressing and Timing Protocols 216 5.1.3 Arbitration, Transaction, and Interrupt 218 5.1.4 The IEEE Futurebus+ Standards 221 5.2 Cache Memory Organizations 224 5.2.2 Direct	4.1	Advanc	ced Processor Technology	157
4.1.4 RISC Scalar Processors 165 4.1.4 RISC Scalar Processors 169 4.2 Superscalar and Vector Processors 177 4.2.1 Superscalar Processors 178 4.2.2 The VLIW Architecture 182 4.2.3 Vector and Symbolic Processors 184 4.3 Memory Hierarchy Technology 188 4.3.1 Hierarchical Memory Technology 188 4.3.2 Inclusion, Coherence, and Locality 190 4.3.3 Memory Capacity Planning 194 4.4 Virtual Memory Technology 196 4.4.1 Virtual Memory Models 196 4.4.2 TLB, Paging, and Segmentation 198 4.4.3 Memory Replacement Policies 205 4.5 Bibliographic Notes and Exercises 208 Chapter 5 Bus, Cache, and Shared Memory 213 5.1 Backplane Bus Systems 213 5.1.1 Backplane Bus Specification 213 5.1.2 Addressing and Timing Protocols 216 5.1.3 Arbitration, Transaction, and Interrupt 218 5.1.4 The IEEE Futurebus+ Standards 221 5.2 Cache Memory Organizations 224 5.2.1 Cache Addressing Models 225 5.2.2 Direct Mappi		4.1.1	Design Space of Processors	157
4.1.4 RISC Scalar Processors 169 4.2 Superscalar and Vector Processors 177 4.2.1 Superscalar Processors 178 4.2.2 The VLIW Architecture 182 4.2.3 Vector and Symbolic Processors 184 4.3 Memory Hierarchy Technology 188 4.3.1 Hierarchical Memory Technology 188 4.3.2 Inclusion, Coherence, and Locality 190 4.3.3 Memory Capacity Planning 194 4.4 Virtual Memory Technology 196 4.4.1 Virtual Memory Models 196 4.4.2 TLB, Paging, and Segmentation 198 4.4.3 Memory Replacement Policies 205 4.5 Bibliographic Notes and Exercises 208 Chapter 5 Bus, Cache, and Shared Memory 213 5.1 Backplane Bus Systems 213 5.1.1 Backplane Bus Specification 213 5.1.2 Addressing and Timing Protocols 216 5.1.3 Arbitration, Transaction, and Interrupt 218 5.1.4 The IEEE Futurebus+ Standards 221 5.2 Cache Memory Organizations 224 5.2.1 Cache Addressing Models 225 5.2.2 Direct Mapping and Associative Caches 228 5.2		4.1.2	Instruction-Set Architectures	162
4.2 Superscalar and Vector Processors 177 4.2.1 Superscalar Processors 178 4.2.2 The VLIW Architecture 182 4.2.3 Vector and Symbolic Processors 184 4.3 Memory Hierarchy Technology 188 4.3.1 Hierarchical Memory Technology 188 4.3.2 Inclusion, Coherence, and Locality 190 4.3.3 Memory Capacity Planning 194 4.4 Virtual Memory Technology 196 4.4.1 Virtual Memory Models 196 4.4.2 TLB, Paging, and Segmentation 198 4.4.3 Memory Replacement Policies 205 4.5 Bibliographic Notes and Exercises 208 Chapter 5 Bus, Cache, and Shared Memory 213 5.1 Backplane Bus Systems 213 5.1.1 Backplane Bus Specification 213 5.1.2 Addressing and Timing Protocols 216 5.1.3 Arbitration, Transaction, and Interrupt 218 5.1.4 The IEEE Futurebus+ Standards 221 5.2 Cache Memory Organizations 224 5.2.1 Cache Addressing Models 225 5.2.2 Direct Mapping and Associative Caches 228 5.2.3 Set-Associative and Sector Caches 232		4.1.3		
4.2.1 Superscalar Processors. 178 4.2.2 The VLIW Architecture. 182 4.2.3 Vector and Symbolic Processors. 184 4.3 Memory Hierarchy Technology. 188 4.3.1 Hierarchical Memory Technology. 188 4.3.2 Inclusion, Coherence, and Locality. 190 4.3.3 Memory Capacity Planning. 194 4.4 Virtual Memory Technology. 196 4.4.1 Virtual Memory Models. 196 4.4.2 TLB, Paging, and Segmentation. 198 4.4.3 Memory Replacement Policies. 205 4.5 Bibliographic Notes and Exercises. 208 Chapter 5 Bus, Cache, and Shared Memory. 213 5.1 Backplane Bus Systems. 213 5.1.1 Backplane Bus Specification. 213 5.1.2 Addressing and Timing Protocols. 216 5.1.3 Arbitration, Transaction, and Interrupt. 218 5.1.4 The IEEE Futurebus+ Standards. 221 5.2 Cache Memory Organizations. 224 5.2.2 Direct Mapping and Associative Caches. 228 5.2.2 Direct Mapping and Associative Caches. 238 5.2.3 Set-Associative and Sector Caches. 232 5.2.4 Cache Performance Issues.		4.1.4	RISC Scalar Processors	169
4.2.2 The VLIW Architecture 182 4.2.3 Vector and Symbolic Processors 184 4.3 Memory Hierarchy Technology 188 4.3.1 Hierarchical Memory Technology 188 4.3.2 Inclusion, Coherence, and Locality 190 4.3.3 Memory Capacity Planning 194 4.4 Virtual Memory Technology 196 4.4.1 Virtual Memory Models 196 4.4.2 TLB, Paging, and Segmentation 198 4.4.3 Memory Replacement Policies 205 4.5 Bibliographic Notes and Exercises 208 Chapter 5 Bus, Cache, and Shared Memory 213 5.1 Backplane Bus Systems 213 5.1.1 Backplane Bus Specification 213 5.1.2 Addressing and Timing Protocols 216 5.1.3 Arbitration, Transaction, and Interrupt 218 5.1.4 The IEEE Futurebus+ Standards 221 5.2 Cache Memory Organizations 224 5.2.1 Cache Addressing Models 225 5.2.2 Direct Mapping and Associative Caches	4.2	Superso	calar and Vector Processors	177
4.2.3 Vector and Symbolic Processors 184 4.3 Memory Hierarchy Technology 188 4.3.1 Hierarchical Memory Technology 188 4.3.2 Inclusion, Coherence, and Locality 190 4.3.3 Memory Capacity Planning 194 4.4 Virtual Memory Technology 196 4.4.1 Virtual Memory Models 196 4.4.2 TLB, Paging, and Segmentation 198 4.4.3 Memory Replacement Policies 205 4.5 Bibliographic Notes and Exercises 208 Chapter 5 Bus, Cache, and Shared Memory 213 5.1 Backplane Bus Systems 213 5.1.1 Backplane Bus Specification 213 5.1.2 Addressing and Timing Protocols 216 5.1.3 Arbitration, Transaction, and Interrupt 218 5.1.4 The IEEE Futurebus+ Standards 221 5.2 Cache Memory Organizations 224 5.2.1 Cache Addressing Models 225 5.2.2 Direct Mapping and Associative Caches 232 5.2.2 Direct Mapping and Associative Caches 232 5.2.3 Set-Associative and Sector Caches 232 5.2.4 Cache Performance Issues 236 5.3 Shared-Memory Organizations 238		4.2.1	Superscalar Processors	178
4.3 Memory Hierarchy Technology 188 4.3.1 Hierarchical Memory Technology 188 4.3.2 Inclusion, Coherence, and Locality 190 4.3.3 Memory Capacity Planning 194 4.4 Virtual Memory Technology 196 4.4.1 Virtual Memory Models 196 4.4.2 TLB, Paging, and Segmentation 198 4.4.3 Memory Replacement Policies 205 4.5 Bibliographic Notes and Exercises 208 Chapter 5 Bus, Cache, and Shared Memory 213 5.1 Backplane Bus Systems 213 5.1.2 Addressing and Timing Protocols 216 5.1.3 Arbitration, Transaction, and Interrupt 218 5.1.4 The IEEE Futurebus+ Standards 221 5.2 Cache Memory Organizations 224 5.2.1 Cache Addressing Models 225 5.2.2 Direct Mapping and Associative Caches 238 5.2.3 Set-Associative and Sector Caches 232 5.2.4 Cache Performance Issues 236 5.3 Shared-Memory Organizations		4.2.2	·	
4.3.1 Hierarchical Memory Technology 188 4.3.2 Inclusion, Coherence, and Locality 190 4.3.3 Memory Capacity Planning 194 4.4 Virtual Memory Technology 196 4.4.1 Virtual Memory Models 196 4.4.2 TLB, Paging, and Segmentation 198 4.4.3 Memory Replacement Policies 205 4.5 Bibliographic Notes and Exercises 208 Chapter 5 Bus, Cache, and Shared Memory 213 5.1 Backplane Bus Systems 213 5.1.2 Addressing and Timing Protocols 216 5.1.3 Arbitration, Transaction, and Interrupt 218 5.1.4 The IEEE Futurebus+ Standards 221 5.2 Cache Memory Organizations 224 5.2.1 Cache Addressing Models 225 5.2.2 Direct Mapping and Associative Caches 228 5.2.3 Set-Associative and Sector Caches 238 5.2.4 Cache Performance Issues 236 5.3 Shared-Memory Organizations 238 5.3.1 Interleaved Memory Organization 239 5.3.2 Bandwidth and Fault Tolerance 242 5.3.3 Memory Allocation Schemes 244 5.4.1 Atomicity and Event Ordering 248 <		4.2.3	Vector and Symbolic Processors	184
4.3.2 Inclusion, Coherence, and Locality 190 4.3.3 Memory Capacity Planning 194 4.4 Virtual Memory Technology 196 4.4.1 Virtual Memory Models 196 4.4.2 TLB, Paging, and Segmentation 198 4.4.3 Memory Replacement Policies 205 4.5 Bibliographic Notes and Exercises 208 Chapter 5 Bus, Cache, and Shared Memory 213 5.1 Backplane Bus Systems 213 5.1.1 Backplane Bus Specification 213 5.1.2 Addressing and Timing Protocols 216 5.1.3 Arbitration, Transaction, and Interrupt 218 5.1.4 The IEEE Futurebus+ Standards 221 5.2 Cache Memory Organizations 224 5.2.1 Cache Addressing Models 225 5.2.2 Direct Mapping and Associative Caches 228 5.2.3 Set-Associative and Sector Caches 238 5.2.4 Cache Performance Issues 236 5.3 Shared-Memory Organizations 238 5.3.1 Interleaved Memory Organization 239 5.3.2 Bandwidth and Fault Tolerance 242 5.3.3 Memory Allocation Schemes 244 5.4.1 Atomicity and Event Ordering 248	4.3	Memor	y Hierarchy Technology	188
4.3.3 Memory Capacity Planning. 194 4.4 Virtual Memory Technology 196 4.4.1 Virtual Memory Models 196 4.4.2 TLB, Paging, and Segmentation 198 4.4.3 Memory Replacement Policies 205 4.5 Bibliographic Notes and Exercises 208 Chapter 5 Bus, Cache, and Shared Memory 213 5.1 Backplane Bus Systems 213 5.1.1 Backplane Bus Specification 213 5.1.2 Addressing and Timing Protocols 216 5.1.3 Arbitration, Transaction, and Interrupt 218 5.1.4 The IEEE Futurebus+ Standards 221 5.2 Cache Memory Organizations 224 5.2.1 Cache Addressing Models 225 5.2.2 Direct Mapping and Associative Caches 228 5.2.3 Set-Associative and Sector Caches 232 5.2.4 Cache Performance Issues 236 5.3 Shared-Memory Organizations 238 5.3.1 Interleaved Memory Organization 239 5.3.2 Bandwidth and Fault Tolerance 242 5.3.3 Memory Allocation Schemes 244 5.4 Sequential and Weak Consistency Models 248 5.4.1 Atomicity and Event Ordering 248 <			Hierarchical Memory Technology	188
4.4 Virtual Memory Technology 196 4.4.1 Virtual Memory Models 196 4.4.2 TLB, Paging, and Segmentation 198 4.4.3 Memory Replacement Policies 205 4.5 Bibliographic Notes and Exercises 208 Chapter 5 Bus, Cache, and Shared Memory 213 5.1 Backplane Bus Systems 213 5.1.1 Backplane Bus Specification 213 5.1.2 Addressing and Timing Protocols 216 5.1.3 Arbitration, Transaction, and Interrupt 218 5.1.4 The IEEE Futurebus+ Standards 221 5.2 Cache Memory Organizations 224 5.2.1 Cache Addressing Models 225 5.2.2 Direct Mapping and Associative Caches 228 5.2.3 Set-Associative and Sector Caches 232 5.2.4 Cache Performance Issues 236 5.3 Shared-Memory Organizations 238 5.3.1 Interleaved Memory Organization 239 5.3.2 Bandwidth and Fault Tolerance 242 5.3.3 Memory Allocation Schemes				
4.4.1 Virtual Memory Models 196 4.4.2 TLB, Paging, and Segmentation 198 4.4.3 Memory Replacement Policies 205 4.5 Bibliographic Notes and Exercises 208 Chapter 5 Bus, Cache, and Shared Memory 213 5.1 Backplane Bus Systems 213 5.1.1 Backplane Bus Specification 213 5.1.2 Addressing and Timing Protocols 216 5.1.3 Arbitration, Transaction, and Interrupt 218 5.1.4 The IEEE Futurebus+ Standards 221 5.2 Cache Memory Organizations 224 5.2.1 Cache Addressing Models 225 5.2.2 Direct Mapping and Associative Caches 228 5.2.3 Set-Associative and Sector Caches 232 5.2.4 Cache Performance Issues 236 5.3 Shared-Memory Organizations 238 5.3.1 Interleaved Memory Organization 239 5.3.2 Bandwidth and Fault Tolerance 242 5.3.3 Memory Allocation Schemes 244 5.4 Sequential and Weak Consistency Mo		4.3.3	Memory Capacity Planning	194
4.4.2 TLB, Paging, and Segmentation 198 4.4.3 Memory Replacement Policies 205 4.5 Bibliographic Notes and Exercises 208 Chapter 5 Bus, Cache, and Shared Memory 213 5.1 Backplane Bus Systems 213 5.1.1 Backplane Bus Specification 213 5.1.2 Addressing and Timing Protocols 216 5.1.3 Arbitration, Transaction, and Interrupt 218 5.1.4 The IEEE Futurebus+ Standards 221 5.2 Cache Memory Organizations 224 5.2.1 Cache Addressing Models 225 5.2.2 Direct Mapping and Associative Caches 228 5.2.3 Set-Associative and Sector Caches 232 5.2.4 Cache Performance Issues 236 5.3 Shared-Memory Organizations 238 5.3.1 Interleaved Memory Organization 239 5.3.2 Bandwidth and Fault Tolerance 242 5.3.3 Memory Allocation Schemes 244 5.4 Sequential and Weak Consistency Models 248 5.4.1 Atomicity and Eve	4.4	Virtual	Memory Technology	196
4.4.3 Memory Replacement Policies 205 4.5 Bibliographic Notes and Exercises 208 Chapter 5 Bus, Cache, and Shared Memory 213 5.1 Backplane Bus Systems 213 5.1.1 Backplane Bus Specification 213 5.1.2 Addressing and Timing Protocols 216 5.1.3 Arbitration, Transaction, and Interrupt 218 5.1.4 The IEEE Futurebus+ Standards 221 5.2 Cache Memory Organizations 224 5.2.1 Cache Addressing Models 225 5.2.2 Direct Mapping and Associative Caches 228 5.2.3 Set-Associative and Sector Caches 232 5.2.4 Cache Performance Issues 236 5.3 Shared-Memory Organizations 238 5.3.1 Interleaved Memory Organization 239 5.3.2 Bandwidth and Fault Tolerance 242 5.3.3 Memory Allocation Schemes 244 5.4 Sequential and Weak Consistency Models 248 5.4.1 Atomicity and Event Ordering 248 5.4.2 Sequential Consistency Models 252 5.4.3 Weak Consistency Models 253 5.5 Bibliographic Notes and Exercises 256		4.4.1	·	
4.5 Bibliographic Notes and Exercises. 208 Chapter 5 Bus, Cache, and Shared Memory 213 5.1 Backplane Bus Systems 213 5.1.1 Backplane Bus Specification 213 5.1.2 Addressing and Timing Protocols 216 5.1.3 Arbitration, Transaction, and Interrupt 218 5.1.4 The IEEE Futurebus+ Standards 221 5.2 Cache Memory Organizations 224 5.2.1 Cache Addressing Models 225 5.2.2 Direct Mapping and Associative Caches 228 5.2.3 Set-Associative and Sector Caches 232 5.2.4 Cache Performance Issues 236 5.3 Shared-Memory Organizations 238 5.3.1 Interleaved Memory Organization 239 5.3.2 Bandwidth and Fault Tolerance 242 5.3.3 Memory Allocation Schemes 244 5.4 Sequential and Weak Consistency Models 248 5.4.1 Atomicity and Event Ordering 248 5.4.2 Sequential Consistency Models 252 5.4.3 Weak Consistency Models 253 5.5 Bibliographic Notes and Exercises 256		4.4.2		
Chapter 5 Bus, Cache, and Shared Memory 213 5.1 Backplane Bus Systems 213 5.1.1 Backplane Bus Specification 213 5.1.2 Addressing and Timing Protocols 216 5.1.3 Arbitration, Transaction, and Interrupt 218 5.1.4 The IEEE Futurebus+ Standards 221 5.2 Cache Memory Organizations 224 5.2.1 Cache Addressing Models 225 5.2.2 Direct Mapping and Associative Caches 228 5.2.3 Set-Associative and Sector Caches 232 5.2.4 Cache Performance Issues 236 5.3 Shared-Memory Organizations 238 5.3.1 Interleaved Memory Organization 239 5.3.2 Bandwidth and Fault Tolerance 242 5.3.3 Memory Allocation Schemes 244 5.4 Sequential and Weak Consistency Models 248 5.4.1 Atomicity and Event Ordering 248 5.4.2 Sequential Consistency Models 252 5.4.3 Weak Consistency Models 253 5.5 Bibliographic Notes and Ex			· · · · · · · · · · · · · · · · · · ·	
5.1 Backplane Bus Systems 213 5.1.1 Backplane Bus Specification 213 5.1.2 Addressing and Timing Protocols 216 5.1.3 Arbitration, Transaction, and Interrupt 218 5.1.4 The IEEE Futurebus+ Standards 221 5.2 Cache Memory Organizations 224 5.2.1 Cache Addressing Models 225 5.2.2 Direct Mapping and Associative Caches 228 5.2.3 Set-Associative and Sector Caches 232 5.2.4 Cache Performance Issues 236 5.3 Shared-Memory Organizations 238 5.3.1 Interleaved Memory Organization 239 5.3.2 Bandwidth and Fault Tolerance 242 5.3.3 Memory Allocation Schemes 244 5.4 Sequential and Weak Consistency Models 248 5.4.1 Atomicity and Event Ordering 248 5.4.2 Sequential Consistency Model 252 5.4.3 Weak Consistency Models 253 5.5 Bibliographic Notes and Exercises 256	4.5	Bibliog	raphic Notes and Exercises	208
5.1 Backplane Bus Systems 213 5.1.1 Backplane Bus Specification 213 5.1.2 Addressing and Timing Protocols 216 5.1.3 Arbitration, Transaction, and Interrupt 218 5.1.4 The IEEE Futurebus+ Standards 221 5.2 Cache Memory Organizations 224 5.2.1 Cache Addressing Models 225 5.2.2 Direct Mapping and Associative Caches 228 5.2.3 Set-Associative and Sector Caches 232 5.2.4 Cache Performance Issues 236 5.3 Shared-Memory Organizations 238 5.3.1 Interleaved Memory Organization 239 5.3.2 Bandwidth and Fault Tolerance 242 5.3.3 Memory Allocation Schemes 244 5.4 Sequential and Weak Consistency Models 248 5.4.1 Atomicity and Event Ordering 248 5.4.2 Sequential Consistency Model 252 5.4.3 Weak Consistency Models 253 5.5 Bibliographic Notes and Exercises 256	Chant	ar 5]	Rus Cache and Shared Memory	212
5.1.1 Backplane Bus Specification 213 5.1.2 Addressing and Timing Protocols 216 5.1.3 Arbitration, Transaction, and Interrupt 218 5.1.4 The IEEE Futurebus+ Standards 221 5.2 Cache Memory Organizations 224 5.2.1 Cache Addressing Models 225 5.2.2 Direct Mapping and Associative Caches 228 5.2.3 Set-Associative and Sector Caches 232 5.2.4 Cache Performance Issues 236 5.3 Shared-Memory Organizations 238 5.3.1 Interleaved Memory Organization 239 5.3.2 Bandwidth and Fault Tolerance 242 5.3.3 Memory Allocation Schemes 244 5.4 Sequential and Weak Consistency Models 248 5.4.1 Atomicity and Event Ordering 248 5.4.2 Sequential Consistency Model 252 5.4.3 Weak Consistency Models 253 5.5 Bibliographic Notes and Exercises 256	_			
5.1.2 Addressing and Timing Protocols 216 5.1.3 Arbitration, Transaction, and Interrupt 218 5.1.4 The IEEE Futurebus+ Standards 221 5.2 Cache Memory Organizations 224 5.2.1 Cache Addressing Models 225 5.2.2 Direct Mapping and Associative Caches 228 5.2.3 Set-Associative and Sector Caches 232 5.2.4 Cache Performance Issues 236 5.3 Shared-Memory Organizations 238 5.3.1 Interleaved Memory Organization 239 5.3.2 Bandwidth and Fault Tolerance 242 5.3.3 Memory Allocation Schemes 244 5.4 Sequential and Weak Consistency Models 248 5.4.1 Atomicity and Event Ordering 248 5.4.2 Sequential Consistency Model 252 5.4.3 Weak Consistency Models 253 5.5 Bibliographic Notes and Exercises 256	5.1	_		
5.1.3 Arbitration, Transaction, and Interrupt 218 5.1.4 The IEEE Futurebus+ Standards 221 5.2 Cache Memory Organizations 224 5.2.1 Cache Addressing Models 225 5.2.2 Direct Mapping and Associative Caches 228 5.2.3 Set-Associative and Sector Caches 232 5.2.4 Cache Performance Issues 236 5.3 Shared-Memory Organizations 238 5.3.1 Interleaved Memory Organization 239 5.3.2 Bandwidth and Fault Tolerance 242 5.3.3 Memory Allocation Schemes 244 5.4 Sequential and Weak Consistency Models 248 5.4.1 Atomicity and Event Ordering 248 5.4.2 Sequential Consistency Models 252 5.4.3 Weak Consistency Models 253 5.5 Bibliographic Notes and Exercises 256		•		
5.1.4 The IEEE Futurebus+ Standards 221 5.2 Cache Memory Organizations 224 5.2.1 Cache Addressing Models 225 5.2.2 Direct Mapping and Associative Caches 228 5.2.3 Set-Associative and Sector Caches 232 5.2.4 Cache Performance Issues 236 5.3 Shared-Memory Organizations 238 5.3.1 Interleaved Memory Organization 239 5.3.2 Bandwidth and Fault Tolerance 242 5.3.3 Memory Allocation Schemes 244 5.4 Sequential and Weak Consistency Models 248 5.4.1 Atomicity and Event Ordering 248 5.4.2 Sequential Consistency Model 252 5.4.3 Weak Consistency Models 253 5.5 Bibliographic Notes and Exercises 256				
5.2 Cache Memory Organizations 224 5.2.1 Cache Addressing Models 225 5.2.2 Direct Mapping and Associative Caches 228 5.2.3 Set-Associative and Sector Caches 232 5.2.4 Cache Performance Issues 236 5.3 Shared-Memory Organizations 238 5.3.1 Interleaved Memory Organization 239 5.3.2 Bandwidth and Fault Tolerance 242 5.3.3 Memory Allocation Schemes 244 5.4 Sequential and Weak Consistency Models 248 5.4.1 Atomicity and Event Ordering 248 5.4.2 Sequential Consistency Model 252 5.4.3 Weak Consistency Models 253 5.5 Bibliographic Notes and Exercises 256				
5.2.1 Cache Addressing Models 225 5.2.2 Direct Mapping and Associative Caches 228 5.2.3 Set-Associative and Sector Caches 232 5.2.4 Cache Performance Issues 236 5.3 Shared-Memory Organizations 238 5.3.1 Interleaved Memory Organization 239 5.3.2 Bandwidth and Fault Tolerance 242 5.3.3 Memory Allocation Schemes 244 5.4 Sequential and Weak Consistency Models 248 5.4.1 Atomicity and Event Ordering 248 5.4.2 Sequential Consistency Model 252 5.4.3 Weak Consistency Models 253 5.5 Bibliographic Notes and Exercises 256	5.2			
5.2.2 Direct Mapping and Associative Caches 228 5.2.3 Set-Associative and Sector Caches 232 5.2.4 Cache Performance Issues 236 5.3 Shared-Memory Organizations 238 5.3.1 Interleaved Memory Organization 239 5.3.2 Bandwidth and Fault Tolerance 242 5.3.3 Memory Allocation Schemes 244 5.4 Sequential and Weak Consistency Models 248 5.4.1 Atomicity and Event Ordering 248 5.4.2 Sequential Consistency Model 252 5.4.3 Weak Consistency Models 253 5.5 Bibliographic Notes and Exercises 256	0.2			
5.2.3 Set-Associative and Sector Caches 232 5.2.4 Cache Performance Issues 236 5.3 Shared-Memory Organizations 238 5.3.1 Interleaved Memory Organization 239 5.3.2 Bandwidth and Fault Tolerance 242 5.3.3 Memory Allocation Schemes 244 5.4 Sequential and Weak Consistency Models 248 5.4.1 Atomicity and Event Ordering 248 5.4.2 Sequential Consistency Model 252 5.4.3 Weak Consistency Models 253 5.5 Bibliographic Notes and Exercises 256				
5.2.4 Cache Performance Issues 236 5.3 Shared-Memory Organizations 238 5.3.1 Interleaved Memory Organization 239 5.3.2 Bandwidth and Fault Tolerance 242 5.3.3 Memory Allocation Schemes 244 5.4 Sequential and Weak Consistency Models 248 5.4.1 Atomicity and Event Ordering 248 5.4.2 Sequential Consistency Model 252 5.4.3 Weak Consistency Models 253 5.5 Bibliographic Notes and Exercises 256		*		
5.3 Shared-Memory Organizations 238 5.3.1 Interleaved Memory Organization 239 5.3.2 Bandwidth and Fault Tolerance 242 5.3.3 Memory Allocation Schemes 244 5.4 Sequential and Weak Consistency Models 248 5.4.1 Atomicity and Event Ordering 248 5.4.2 Sequential Consistency Model 252 5.4.3 Weak Consistency Models 253 5.5 Bibliographic Notes and Exercises 256				
5.3.1 Interleaved Memory Organization 239 5.3.2 Bandwidth and Fault Tolerance 242 5.3.3 Memory Allocation Schemes 244 5.4 Sequential and Weak Consistency Models 248 5.4.1 Atomicity and Event Ordering 248 5.4.2 Sequential Consistency Model 252 5.4.3 Weak Consistency Models 253 5.5 Bibliographic Notes and Exercises 256	5.3	Shared.		
5.3.2 Bandwidth and Fault Tolerance 242 5.3.3 Memory Allocation Schemes 244 5.4 Sequential and Weak Consistency Models 248 5.4.1 Atomicity and Event Ordering 248 5.4.2 Sequential Consistency Model 252 5.4.3 Weak Consistency Models 253 5.5 Bibliographic Notes and Exercises 256	0.0			
5.3.3 Memory Allocation Schemes 244 5.4 Sequential and Weak Consistency Models 248 5.4.1 Atomicity and Event Ordering 248 5.4.2 Sequential Consistency Model 252 5.4.3 Weak Consistency Models 253 5.5 Bibliographic Notes and Exercises 256				
5.4 Sequential and Weak Consistency Models		5.3.3		
5.4.1 Atomicity and Event Ordering	5.4	Sequen	•	
5.4.2 Sequential Consistency Model	• • •	-	· ·	
5.4.3 Weak Consistency Models		5.4.2		
Chapter 6 Displining and Supercolon Techniques	5.5	Bibliog	raphic Notes and Exercises	256
	Chart	om 6 1	Pinelining and Supergalar Techniques	265

xii Contents

6.1	Linear Pipeline Processors	
	6.1.1 Asynchronous and Synchronous Models	265
	6.1.2 Clocking and Timing Control	
	6.1.3 Speedup, Efficiency, and Throughput	268
6.2	Nonlinear Pipeline Processors	270
	6.2.1 Reservation and Latency Analysis	
	6.2.2 Collision-Free Scheduling	
	6.2.3 Pipeline Schedule Optimization	276
6.3	Instruction Pipeline Design	
	6.3.1 Instruction Execution Phases	
	6.3.2 Mechanisms for Instruction Pipelining	
	6.3.3 Dynamic Instruction Scheduling	
	6.3.4 Branch Handling Techniques	291
6.4	Arithmetic Pipeline Design	
	6.4.1 Computer Arithmetic Principles	
	6.4.2 Static Arithmetic Pipelines	
	6.4.3 Multifunctional Arithmetic Pipelines	307
6.5	Superscalar and Superpipeline Design	
	6.5.1 Superscalar Pipeline Design	310
	6.5.2 Superpipelined Design	
	6.5.3 Supersymmetry and Design Tradeoffs	320
6.6	Bibliographic Notes and Exercises	322
	•	
Part	III Parallel and Scalable Architectures	329
Chapt		
7.1	Multiprocessor System Interconnects	331
	7.1.1 Hierarchical Bus Systems	
	7.1.2 Crossbar Switch and Multiport Memory	
	7.1.3 Multistage and Combining Networks	341
7.2	Cache Coherence and Synchronization Mechanisms	
	7.2.1 The Cache Coherence Problem	
	7.2.2 Snoopy Bus Protocols	
	7.2.3 Directory-Based Protocols	
	7.2.4 Hardware Synchronization Mechanisms	364
7.3	Three Generations of Multicomputers	368
	7.3.1 Design Choices in the Past	368
	7.3.2 Present and Future Development	
	7.3.3 The Intel Paragon System	372
7.4	Message-Passing Mechanisms	375
	7.4.1 Message-Routing Schemes	

	7.4.2	Deadlock and Virtual Channels	379
	7.4.3	Flow Control Strategies	
	7.4.4	Multicast Routing Algorithms	. 387
7.5	Bibliog	graphic Notes and Exercises	393
Chapte	er 8	Multivector and SIMD Computers	. 403
8.1	Vector	Processing Principles	. 403
	8.1.1	Vector Instruction Types	. 403
	8.1.2	Vector-Access Memory Schemes	
	8.1.3	Past and Present Supercomputers	410
8.2	Multiv	ector Multiprocessors	415
	8.2.1	Performance-Directed Design Rules	
	8.2.2	Cray Y-MP, C-90, and MPP	
	8.2.3	Fujitsu VP2000 and VPP500	
	8.2.4	Mainframes and Minisupercomputers	
8.3	Compo	ound Vector Processing	435
	8.3.1	Compound Vector Operations	
	8.3.2	Vector Loops and Chaining	
	8.3.3	Multipipeline Networking	
8.4	SIMD	Computer Organizations	
	8.4.1	Implementation Models	
	8.4.2	The CM-2 Architecture	
	8.4.3	The MasPar MP-1 Architecture	
8.5		onnection Machine CM-5	
	8.5.1	A Synchronized MIMD Machine	
	8.5.2	The CM-5 Network Architecture	
	8.5.3	Control Processors and Processing Nodes	
	8.5.4	Interprocessor Communications	
8.6	Bibliog	graphic Notes and Exercises	468
Chapt		Scalable, Multithreaded, and Dataflow Architectures	
9.1	Latenc	y-Hiding Techniques	
	9.1.1		
	9.1.2	Prefetching Techniques	
	9.1.3	Distributed Coherent Caches	
	9.1.4	Scalable Coherence Interface	
	9.1.5	Relaxed Memory Consistency	
9.2	-	ples of Multithreading	
	9.2.1	Multithreading Issues and Solutions	
	9.2.2	Multiple-Context Processors	
_ *	9.2.3	Multidimensional Architectures	
0.3	Fine C	Prain Multicomputers	504

	9.3.1 Fine-Grain Parallelism	
	9.3.2 The MIT J-Machine	
	9.3.3 The Caltech Mosaic C	514
9.4	Scalable and Multithreaded Architectures	516
	9.4.1 The Stanford Dash Multiprocessor	
	9.4.2 The Kendall Square Research KSR-1	
	9.4.3 The Tera Multiprocessor System	
9.5	Dataflow and Hybrid Architectures	
	9.5.1 The Evolution of Dataflow Computers	531
	9.5.2 The ETL/EM-4 in Japan	
	9.5.3 The MIT/Motorola *T Prototype	536
9.6	Bibliographic Notes and Exercises	539
Part I	V Software for Parallel Programming	545
Chapte	, , , ,	
10.1	Parallel Programming Models	547
	10.1.1 Shared-Variable Model	
•	10.1.2 Message-Passing Model	
	10.1.3 Data-Parallel Model	
	10.1.4 Object-Oriented Model	
	10.1.5 Functional and Logic Models	
10.2	Parallel Languages and Compilers	
	10.2.1 Language Features for Parallelism	
	10.2.2 Parallel Language Constructs	
	10.2.3 Optimizing Compilers for Parallelism	
10.3	Dependence Analysis of Data Arrays	
	10.3.1 Iteration Space and Dependence Analysis	
	10.3.2 Subscript Separability and Partitioning	
	10.3.3 Categorized Dependence Tests	
10.4	Code Optimization and Scheduling	
	10.4.1 Scalar Optimization with Basic Blocks	
	10.4.2 Local and Global Optimizations	
	10.4.3 Vectorization and Parallelization Methods	
	10.4.4 Code Generation and Scheduling	
	10.4.5 Trace Scheduling Compilation	
10.5	Loop Parallelization and Pipelining	
	10.5.1 Loop Transformation Theory	
	10.5.2 Parallelization and Wavefronting	
	10.5.3 Tiling and Localization	
	10.5.4 Software Pipelining	610

Contents

10.6	Bibliographic Notes and Exercises	612
Chapte	r 11 Parallel Program Development and Environments	617
11.1	Parallel Programming Environments	617
	11.1.1 Software Tools and Environments	
	11.1.2 Y-MP, Paragon, and CM-5 Environments	
	11.1.3 Visualization and Performance Tuning	
11.2	Synchronization and Multiprocessing Modes	
	11.2.1 Principles of Synchronization	
	11.2.2 Multiprocessor Execution Modes	
	11.2.3 Multitasking on Cray Multiprocessors	
11.3	Shared-Variable Program Structures	
22.0	11.3.1 Locks for Protected Access	
	11.3.2 Semaphores and Applications	
	11.3.3 Monitors and Applications	
11.4	Message-Passing Program Development	
12.1	11.4.1 Distributing the Computation	
	11.4.2 Synchronous Message Passing	
	11.4.3 Asynchronous Message Passing	
11.5	Mapping Programs onto Multicomputers	
11.0	11.5.1 Domain Decomposition Techniques	
	11.5.2 Control Decomposition Techniques	
	11.5.3 Heterogeneous Processing	
11.6	Bibliographic Notes and Exercises	
,		
Chapte	r 12 UNIX, Mach, and OSF/1 for Parallel Computers	667
12.1	Multiprocessor UNIX Design Goals	667
	12.1.1 Conventional UNIX Limitations	668
	12.1.2 Compatibility and Portability	670
	12.1.3 Address Space and Load Balancing	671
	12.1.4 Parallel I/O and Network Services	671
12.2	Master-Slave and Multithreaded UNIX	672
	12.2.1 Master-Slave Kernels	672
	12.2.2 Floating-Executive Kernels	674
	12.2.3 Multithreaded UNIX Kernel	678
12.3	Multicomputer UNIX Extensions	683
	12.3.1 Message-Passing OS Models	
	12.3.2 Cosmic Environment and Reactive Kernel	
	12.3.3 Intel NX/2 Kernel and Extensions	685
12.4	Mach/OS Kernel Architecture	686
/_	12.4.1 Mach/OS Kernel Functions	
	12.4.2 Multithreaded Multitasking	688

	12.4.3	Message-Based Communications	694
	12.4.4	Virtual Memory Management	697
12	2.5 OSF/1	Architecture and Applications	701
	12.5.1	The OSF/1 Architecture	702
	12.5.2	The OSF/1 Programming Environment	707
	12.5.3	Improving Performance with Threads	709
12	2.6 Biblio	graphic Notes and Exercises	712
Biblio	graphy		717
`			7
Index			739
A news	ers to Sele	ected Problems	765