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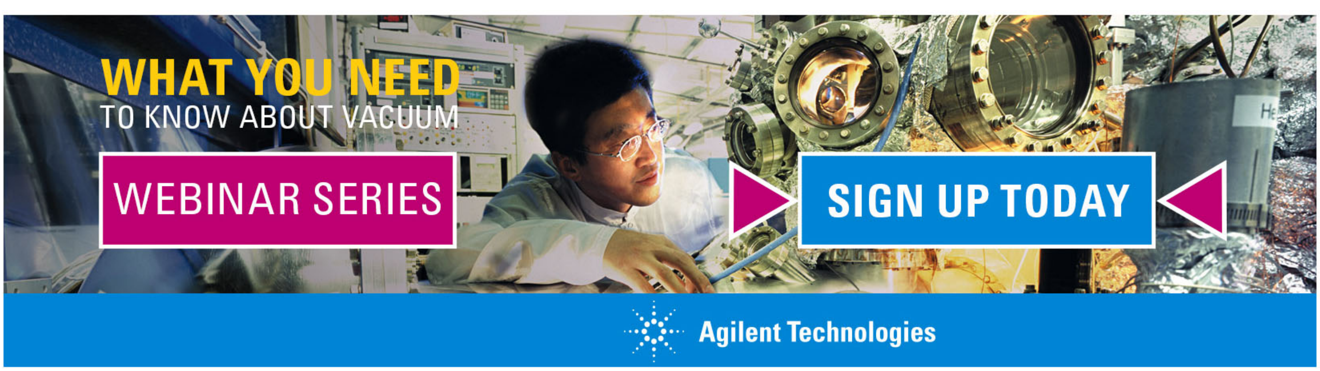

Low-temperature-processed (150–175 °C) Ge/Pd-based Ohmic contacts ($\rho_c \sim 1 \times 10^{-6}\,\Omega\,\mathrm{cm}^2$) to *n*-GaAs

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We have developed low resistance ($\rho_c \sim 1 \times 10^{-6}$ Ω cm^2) Ge/Pd-based (the Au/Ge/Pd and the Ag/Ge/Pd contacts) Ohmic contact schemes processed at temperatures 150–175 °C to *n*-GaAs ($n \sim 1 \times 10^{18}$ cm^{-3}). The Ohmic contact formation mechanism can be rationalized in terms of the solid phase regrowth (SPR) principle and the interdiffusion between Au (or Ag) and Ge. © *1995 American Institute of Physics.*

The annealing temperatures for forming Ohmic contacts to *n*-GaAs are normally higher than 300 °C. For the commonly used Au–Ge based contacts, the annealing temperature is generally higher than the Au–Ge eutectic temperature (361 °C). It is well known that the Ohmic behavior of the Au–Ge based contacts is a result of liquid phase reactions. For other contact schemes based on solid phase reactions, the Ohmic contact formation temperature varies depending on the contact structures.[1] The interfacial morphology and thermal stability of contacts formed via solid phase reactions are generally superior to those via liquid phase reactions.

Since the early 1980's, a series of Ohmic contacts based on a solid phase regrowth (SPR)[2,3] principle has been developed for *n*- and *p*-type GaAs and AlGaAs. Among these contact schemes, the Ge/Pd/*n*-GaAs contact system developed by Marshall *et al.*[4] has drawn great attention. Due to its superior electrical properties and uniform interfacial morphology,[5,6] the Ge/Pd contact has played an important role in novel GaAs-based device fabrications, including high electron mobility transistors,[7] heterojunction transistors,[8] resonant tunneling structure,[9] vertical-cavity surface-emitting laser,[10] and epitaxially lifted-off layers.[11] The details of the Ohmic contact formation mechanism of the Ge/Pd contact have been discussed in Ref. 12 in terms of the SPR process and are summarized in the following. (i) It starts with a limited solid phase reaction between the Pd layer and the GaAs substrate to form a thin metastable ternary Pd_xGaAs ($x \sim 4$) layer at low temperature ($\sim$100 °C or lower). (ii) When annealed at elevated temperatures, another solid phase reaction begins at the Ge/Pd interface to form PdGe until all the Pd is consumed. (iii) Then, the excess Ge for the formation of PdGe drives the Pd_xGaAs layer at the metal-semiconductor interface to decompose, resulting in a solid phase regrowth of a Ge-doped n^+-GaAs layer. Following the solid phase regrowth of the n^+-GaAs layer, the excess Ge is transported to the contact-semiconductor interface and epitaxially grows on the regrown GaAs layer, as a result of a solid phase epitaxy process.[13] The final contact structure is PdGe/epi-Ge/regrown n^+-GaAs/*n*-GaAs substrate. The contact is therefore a tunneling Ohmic contact as well as a heterostructure Ohmic contact.

Contact resistivities, ρ_c, in the order of 10^{-6} Ω cm^2 or lower on *n*-GaAs substrates ($n \sim 1 \times 10^{18}$ cm^{-3}) have been reported for the Ge/Pd contact annealed at 250 °C or above.[6] In contrast, high contact resistivities ($\geqslant 10^{-4}$ Ω cm^2) were obtained for the Ge/Pd contact annealed at temperatures below 225 °C. However, there is perhaps a need to have low resistance Ohmic contact schemes processed at low temperatures (e.g., $\leqslant$200 °C) in device fabrications. For example, the fabrication of ZnSe-based blue-green laser diodes grown on *n*-GaAs substrates requires such low processing temperatures. In this letter, we report the formation of low resistance Ge/Pd-based contacts annealed at temperatures 150–175 °C. We have also achieved ρ_c of $\sim 2 \times 10^{-6}$ Ω cm^2 for the Ge/Pd-based contacts processed at $\sim$140 °C for long annealing time.

The substrates for this study were semi-insulating GaAs (100) wafers with Si-doped surface layers ($\sim 1 \times 10^{18}$ cm^{-3}, 0.2 μm, $\sim$100 $\Omega/\square$) prepared by metalorganic chemical vapor deposition (MOCVD). Prior to contact deposition, the substrates were cleaned using organic solvents followed by a rinse in deionized (DI) water. The native oxide was then removed using HCl:H_2O (1:1 by volume) followed by a DI water rinse and blown dry with nitrogen. The following contact structures were prepared on the substrates described above in a multipocket electron beam evaporator with a base pressure of $\sim 5 \times 10^{-8}$ Torr: (a) Ge(1100 Å)/Pd(500 Å); (b) Au(1200 Å)/Ge(1100 Å)/Pd(500 Å); (c) Ge(500 Å)/Pd(100 Å), (d) Au(1200 Å)/Ge(500 Å)/Pd(100 Å), (e) Ag(1000 Å)/Ge(500 Å)/Pd(100 Å), and (f) Au(500 Å)/Ge(500 Å)/Pd(50 Å), with Pd layers deposited first. The contacts were annealed in a conventional tube furnace in flowing nitrogen gas at temperatures ranging from 150 to 325 °C for various amounts of time. The annealing temperatures were monitored with a thermal couple directly contacting the sample holder. The contact resistivities of the contacts were obtained using the transmission line model (TLM)[14] measurement.

Figure 1 shows the contact resistivities as a function of annealing time at 175 °C for samples A and B. The scattering

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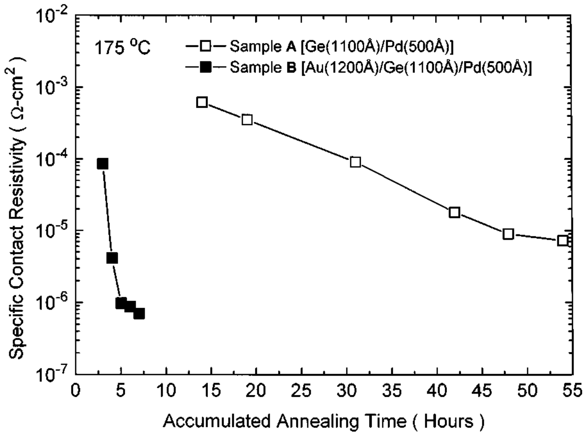

FIG. 1. The contact resistivities of samples A and B as a function of annealing time at 175 °C. It shows that low contact resistivity (~low 10^{-6} Ω cm^2) was obtained for sample B annealed for more than about 4 h. In contrast, the contact resistivity of sample A remains $\sim 10^{-5}$ Ω cm^2 even after annealing for 54 h.

in contact resistivities is very small. This is a typical characteristic of contacts formed via the solid phase regrowth process.[6] Sample A did not show Ohmic behavior until annealed for ~10 h. The contact resistivity for sample A annealed in this condition (175 °C, 10 h) was high (10^{-4} Ω cm^2). It was about two orders of magnitude higher than that for the same structure annealed at 325 °C for 30 min. In contrast, it took less than 3 h for sample B to become Ohmic at 175 °C. The final contact resistivity of sample B annealed at 175 °C was $\sim 1\times10^{-6}$ Ω cm^2. It is clear from Fig. 1 that capping the Ge/Pd contact with a Au overlayer not only shortens the annealing time to obtain Ohmic behavior but also lowers the final contact resistivity. Although low contact resistivity can be obtained for sample B, the required annealing time (4 h), however, is not practical from a processing point of view.

Figure 2 shows the contact resistivities as a function of annealing time at 175 °C for samples C and D, and E with thinner Pd layers in the contact structures. The lowest contact resistivity of $\sim 10^{-4}$ Ω cm^2 of sample C was obtained. In contrast, the contact resistivity of sample D was $\sim 1\times10^{-6}$ Ω cm^2 after annealing at 175 °C for less than 1 h. To the best of our knowledge, 175 °C is the lowest processing temperature reported for the formation of low resistance Ohmic contacts ($\rho_c \sim 1\times10^{-6}$ Ω cm^2) on *n*-GaAs. Figure 2 also indicates that sample D is stable at 175 °C. Comparing the results shown in Figs. 1 and 2, it is clear that it requires shorter annealing time for samples with thinner Pd layers to achieve Ohmic behavior. This suggests a kinetics-controlled nature of the ohmic contact formation via the solid phase regrowth process. The function of the Au overlayer which leads to low final contact resistivities is discussed in the following.

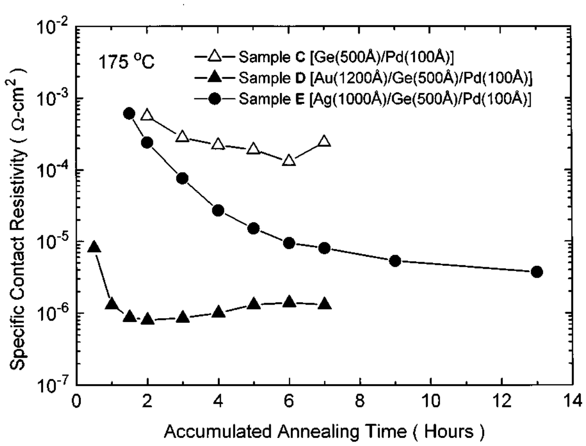

FIG. 2. The contact resistivities of samples C, D, and E as a function of annealing time at 175 °C. It is clear that low contact resistivities in the order of 1×10^{-6} Ω cm^2 were obtained for sample D annealed for more than 1 h. Low contact resistivity can also be obtained for the Ge/Pd-based samples capped with Ag overlayers.

As previously discussed in this letter, the final contact layer structure of the sample A annealed at temperatures above 250 °C is PdGe/epi-Ge/regrown n^+-GaAs/*n*-GaAs substrate. The overall resistance between the contact surface (i.e., PdGe) and the *n*-GaAs substrate is low since the resistivities of PdGe and epi-Ge are low and the contact resistivity between the epi-Ge and the regrown n^+-GaAs is also low. As mentioned above the SPR process—the decomposition of the Pd_xGaAs layer and the solid phase regrowth of an n^+-GaAs layer, is a kinetics-controlled process. This SPR process can occur at 175 °C. The time required for the SPR process to be completed depends on the thickness of the Pd layer. Contacts with thicker Pd layers require more time to become Ohmic when annealed at 175 °C. However, the solid phase transport of the excess Ge through the PdGe layer and the formation of the epitaxial Ge on the regrown n^+-GaAs layer are not expected at 175 °C.[13] Thus, the final layer structures for samples A and C annealed at 175 °C for 10 h are believed to be α-Ge (amorphous Ge)/PdGe/regrown n^+-GaAs/*n*-GaAs substrate, as shown in Fig. 3(a). The resistivity of the α-Ge layer is expected to be high, which results in a high overall contact resistivity between the contact surface (α-Ge) and the *n*-GaAs substrate. In order to reduce the overall contact resistance, the surface α-Ge layer needs to be transported and epitaxially grown on the regrown n^+-GaAs layer or the conductivity of the surface α-Ge layer needs to be enhanced. The former case can be achieved by annealing samples at higher temperatures (>250 °C), while the latter case can be achieved by capping samples with Au layers and annealing them at low temperatures ($\leqslant$200 °C). Au and Ge do not form compounds below their eutectic temperature,[15] however, significant interdiffusion between Au and Ge has been observed at temperatures below 250 °C.[16] It is very likely that the final layer structures of samples B and D annealed at 175 °C are both Au/α-Ge:Au/PdGe/n^+-GaAs/*n*-GaAs [shown in Fig. 3(b)], where α-Ge:Au denotes the incorporation of Au in the amorphous Ge layer. It is believed that the incorporation of Au in the amorphous Ge layer increases the conductivity of amorphous Ge. Therefore, the overall contact resistance between the sample surface (Au) and *n*-GaAs is significantly reduced.

Based on this model, a lower processing temperature (e.g., 150 °C) to obtain low contact resistance may be feasible by further reducing the thickness of the Pd layer. Figure 4 shows the contact resistivities of samples D and F as a

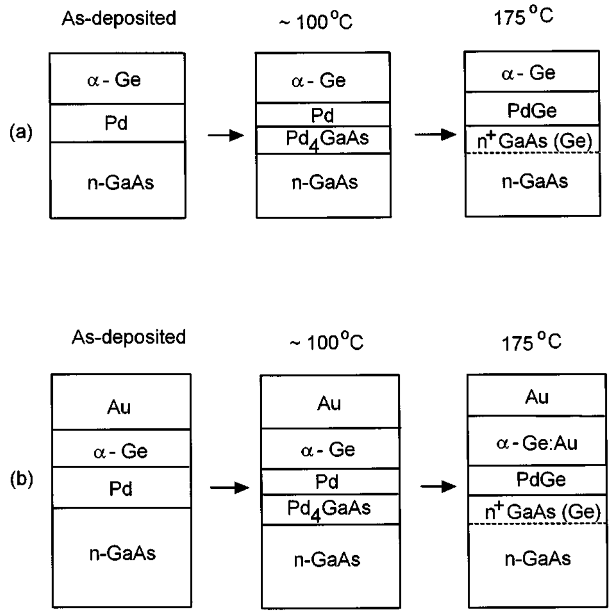

FIG. 3. The schematic diagrams rationalizing the Ohmic contact formation mechanism for the Ge/Pd-based contacts to *n*-GaAs processed at 175 °C: (a) for the Ge/Pd-based samples without overlayer metallization, and (b) for the samples with Au overlayers.

function of annealing time at 150 °C. It is clear that contact resistivities about 10^{-6} Ω cm^2 can be obtained for these contacts annealed at 150 °C. It requires less time for the contact of a thinner Pd layer to research low contact resistivity. Furthermore, other metal overlayers which diffuse into amorphous Ge layer at low temperatures can be used to reduce the contact resistivity for samples annealed at low temperatures. We tested this hypothesis on sample E in which Ag is used as an overlayer. The result is shown in Fig. 2 for

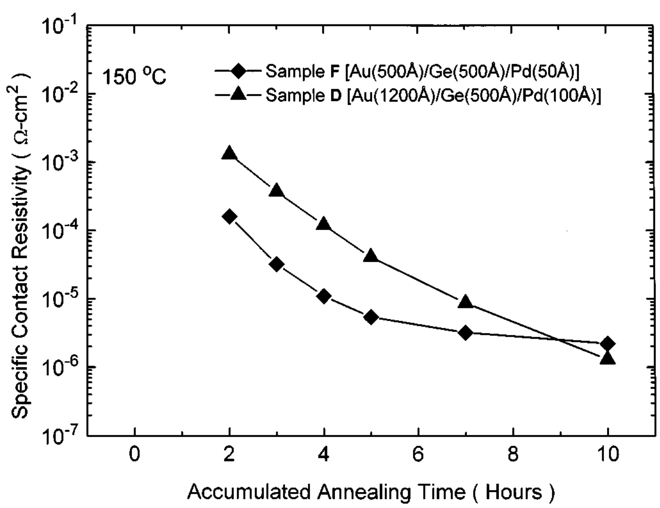

FIG. 4. The contact resistivities as a function of annealing time for samples D and F at 150 °C. It shows that the contacts with thinner Pd layers requires less time to reach low contact resistivities.

comparison with samples C and D. Indeed, contact resistivities in the order of 10^{-6} Ωcm^2 can be obtained for the Ag/Ge/Pd contact scheme. Longer annealing time is required for sample E to reach low contact resistivity. This may be due to a slower interdiffusion rate between Ag and Ge, compared with that between Au and Ge. We also "baked" sample D in a conventional oven at 140 °C in air overnight and obtained ρ_c of $\sim 2\times 10^{-6}$ Ω cm^2. Further study to verify this model is currently under investigation.

In summary, we have developed low resistance ($\rho_c \sim 1\times 10^{-6}$ Ω cm^2) Ohmic contact schemes, the Au/Ge/Pd and the Ag/Ge/Pd contacts with Pd layer thickness in the range of 50–100 Å, to *n*-GaAs processed at temperatures 150–175 °C with good reproducibility. The formation mechanism of these Ohmic contacts can be rationalized in terms of the solid phase regrowth mechanism and the interdiffusion between Au (or Ag) and Ge. The interfacial morphology of these contacts processed at a low temperature is expected to be very uniform and shallow, which is desired for shallow junction device applications. Furthermore, we tested the reliability of sample D by passing a current of density $\sim$1000 A/cm^2, a typical operating current density for semiconductor laser diodes, through the contact for more than 100 h at room temperature. No degradation in contact resistivity has been observed.

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