YAMAHA



NO.85-08 2

V9938

(MSX-VIDEO)

■ GENERAL DESCRIPTION

V9938 (MSX-VIDEO) is a video display processor (VPD) using an N-channel silicon gate MOS and a 64-pin shrink DIL plastic package. TMS9918A is software compatible.

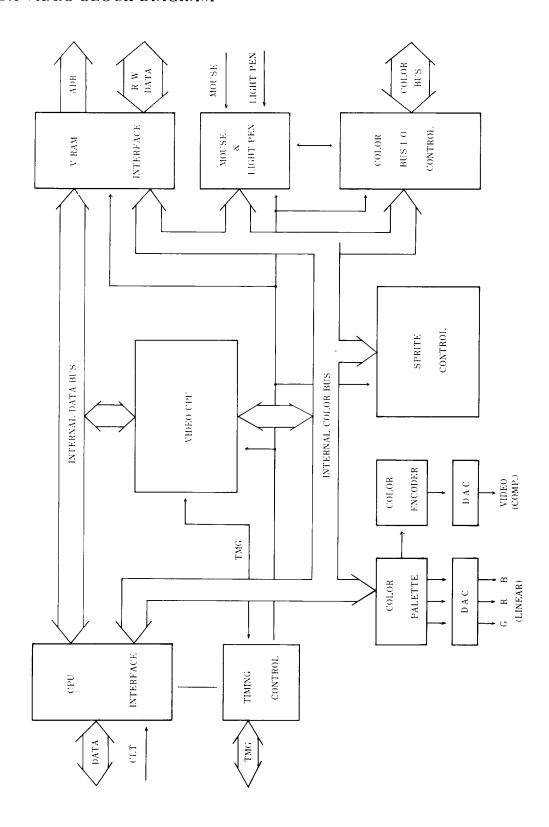
■ FEATURES

- 5V power supply
- Linear RGB and composite video output
- Built-in palette for displays in up to 512 colors.
- Maximum of 512 x 424 pixels and 16 colors.
- Bit mapped graphics
- A maximum of 256 colors can be displayed at the same time.
- 16 k-byte ~ 128 k-byte display memory
- 16K x 1b, 16K x 4b, 64K x 1b, 64K x 4b DRAMs can be used.
- 256 address, 4ms DRAM auto refresh.
- Expansion video memory can be connected.
- Built-in mouse and light pen interfaces.
- Eight sprites can be displayed for each horizontal line.
- Colors for sprites can be specified for each horizontal line.
- Area move, line, search and other commands.
- Logical operation function.
- Addresses can be specified by coordinates.
- External sync is possible.
- Superimpose is possible.
- Digitize is possible.
- Multi MSX-VIDEO configurations are possible.
- Additional external color palettes using the Color-Bus output.

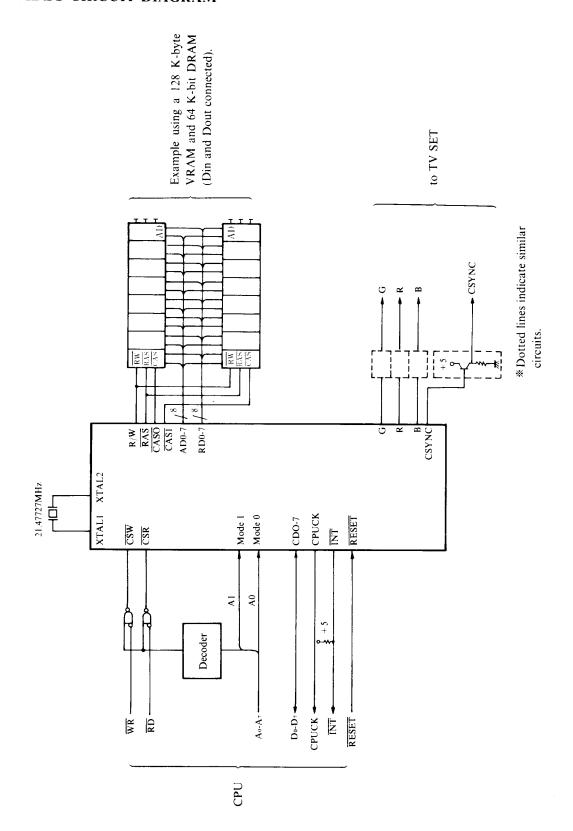
NIPPON GAKKI CO., LTD.

CATALOG No.:LSI-2199380

■ MSX-VIDEO BLOCK DIAGRAM



■ MSX-VIDEO CIRCUIT DIAGRAM



■ PIN LAYOUT AND FUNCTIONS

Pin Name	Pin No.	I/O	Function
CD0 LSB	40	I/O	CPU data bus
CD1	39	I/O	
CD2	38	I/O	
CD3	37	I/O	GND 1 64 XTAL 2
CD4	36	I/O	DHCLK 2 63 XTAL 1
CD5	35	I/O	DLČLK ☐ 3 62 ☐ RAS VDS ☐ 4 61 ☐ ČÁS 0
CD6	34	I/O	$ \begin{array}{c ccccc} \hline VDS & 4 & 61 & \hline CAS 0 \\ HSYNC & 5 & 60 & \hline CAS T \end{array} $
CD7 MSB	32	I/O	CSYNC
MODE 0	29	Ī	CPU interface mode select BLEO 7 58 V.c. CPUCLK 8 57 R W
MODE 1	28	I	RESET 9 56 AD 7
\overline{CSR}	31	I	VS 10 55 AD 6 CPU-VDP read strobe CBDR 11 54 AD 5
CSW	30	Ī	CPU-VDP write strobe
RD0 LSB	41	I/O	VRAN data bus C5 14 51 AD 2
RD1	42	I/O	C4 15 50 AD 1
RD2	43	I/O	C3
RD3	44	I/O	CI 18 47 RD 6
RD4	45	I/O	C0 19 46 RD 5 GND DAC 20 45 RD 4
RD5	46	I/O	GND:DAC
RD6	47	I/O	G □ 22 43 □ RD 2
RD7 MSB	48	I/O	$ \begin{array}{ccc} R $
AD0 LSB	49	O	VP AM address bus
AD1	50	O	VKAIVI address bus LPS
AD2	51	0	MODE ☐ 28 37 ☐ CD 3
AD3	52	0	MODE 0 ☐ 29 36 ☐ CD 4 CSW ☐ 30 35 ☐ CD 5
AD4	53	0	CSR 31 34 CD 6
AD5	54	0	CD7 32 33 V ₈₈
AD6	55	0	
AD7 MSB	56	0	
$\frac{AB}{RAS}$	62	0	VRAM row address strobe
$\frac{\text{CAS }0}{\text{CAS }0}$	61	0	VRAM row address strobe VRAM column address strobe 0 (first half of VRAM)
CAS 1	60	0	VRAM column address strobe 0 (first half of VRAM) VRAM column address strobe 1 (last half of VRAM)
$\frac{CAST}{CASX}$	59	0	VRAM column address strobe Y (last han of VRAM) VRAM column address strobe X (for expansion VRAM)
R/\overline{W}	57	0	VRAM write strobe
$\frac{R}{VDS}$	4	0	VRAM data select
V D3		O	$\overline{VDS} = Low$; VRAM access for display data.
			$\frac{\text{VDS}}{\text{VDS}} = \text{High}$; VRAM access for other than the above.
VIDEO	21	О	Composite video signal output
G	22	o	Linear RGB signal output
R	23	O	Linear ROB signar output
В	24	0	
$\frac{\mathbf{B}}{\mathbf{YS}}$	10	0	Signal for avitahing between VDD DCD autnut and automal video signals
13	10	O	Signal for switching between VDP RGB output and external video signals. (For superimpose)
			\overline{YS} = High; VDP output is transparent
			\overline{YS} = Low; VDP output is not transparent
BLEO	7	О	Indicates No. 1 field/No. 2 field blanking for 3-value output.
			Open drain output
			High; No. 2 field or active.
			Middle; No. 1 field or active.
			Low; Linear erase interval.

Pin Name	Pin No.	I/O	Function
HSYNC	5	I/O	High order level (High ~ Middle) output for 3-value logic.
			Lower order level (Middle ~ Low) input.
			High ; No HSYNC timing or color burst timing.
			Middle; HSYNC or no color burst timing.
			Low : HSYNC input.
CSYNC	6	I/O	Composite sync output in high order level for 3-value logic.
			Lower order level is VSYNC input.
CBDR	11	О	This pin shows the direction of the color bus.
			High ; color bus is input
			Low; color bus is output
C0 LSB	19	I/O	Color bus
C1	18	I/O	Color code is normally output, used as input port for digitize. The 4 high
C2	17	I/O	order bits are used for mouse input when a mouse is used.
C3	16	I/O	
C4	15	I/O	C4 = XA
C5	14	I/O	C5 = XB
C6	13	I/O	C6 = YA
C7 MSB	12	I/O	C7 = YB
LPS	26	I	Light pen SW input. Mouse SW input when a mouse is used.
			Low; SW ON
			High ; SW OFF
LPD	27	I	Light pen light detection input. Mouse SW input when a mouse is used.
			Low; light detection or SW ON.
			High; other than the above.
DHCLK	2	O	Dot clock output for high resolution. Approx. 10.74 MHz, open drain output.
DLCLK	3	I/O	Dot clock output for low resolution. Approx. 5.37 MHz, open drain output.
			Input is also possible using the mode register, used for multi VDP.
XTAL 1	63	I	This pin is used for XTAL connection. Also used for input when using an externally
			generated clock.
XTAL 2	64	I	
CPUCLK	8	О	Outputs 1/6 the XTAL frequency.
INT	25	О	CPU interrupt output, open drain output.
			Low; generates interrupts.
RESET	9	I	Resets all circuits in the VDP.
Vcc	58	I	5V power supply
GND	1	I	Ground 0 V
GND DAC	20	I	Ground 0 V
V_{BB}	33	O	Baseboard voltage

■ ELECTRICAL CHARACTERISTICS

1. Maximum Ratings

Symbol	Item	Rating	Unit
Vec	Power supply voltage	$-0.5 \sim +7.0$	V
Vin	Input voltage	$-0.5 \sim +7.0$	V
Ts	Storage temperature	-50 ~ +125	°C
То	Operating temperature	0~+70	°C

2. Recommended Operating Conditions

Symbol	Îtem	Minimum	Reference	Maximum	Unit
Vec	Power supply voltage	4.75	5.00	5.25	V
Vss	Power supply voltage		0		v
TA	Operating ambient temperature	0		70	°C
VIL 1	Low level input voltage (group 1)	-0.3		0.8	v
VIL 2	Low level input voltage (group 2)	-0.3		0.8	v
VIL 3	External clock low level input voltage (group 3)	-0.3		0.8	v
ViH 1	High level input voltage (group 1)	2.2		Vcc	v
Vih 2	High level input voltage (group 2)	2.2		Vcc	v
ViH 3	External clock high level input voltage (group 3)	3.5		Vcc	v

Group 2 CDO-7, MODE 0, MODE 1, CSW

Group 3 XTAL 1, XTAL 2

3. AC Characteristics

Symbol	Item	Condition	Minimum	Reference	Maximum	Unit
Vol 4	Low level output voltage (group 4)	IOL = 1.6 mA			0.4	v
Vol 5	Low level output voltage (group 5)	IOL = 1.6mA			0.4	v
Vol 6	Low level output voltage (group 6)	IOL = 10mA			0.4	v
Vol 7	Low level output voltage (group 7)	IOL = 1.6mA			0.4	v
Vон 4	High level output voltage (group 4)	Іон = 100μΑ	2.4			v
Voн 5	High level output voltage (group 5)	Iон = 60µA	2.7			v
ILI	In-put leak current				10	μА
ILO	Output leak current (when floating)				25	μА
Icc	Current consumption				230	mA

Note: Group 4 CDO-7, RDO-7, ADO-7, VDS, CBDR, CPUCLK, CO-7

Group 5 \overline{RAS} , \overline{CAS} 0, \overline{CAS} 1, \overline{CASX} , R/\overline{W}

Group 6 DLCLK, DHCLK

Group 7 INT

4. Composite Video Signal Output Level

Symbol	Item	Measurement Conditions	Minimum	Reference	Maximum	Unit
VWHITE	White level output voltage		2.20	2.60	3.00	V
VWHITE(B/W)	White level output voltage (monochrome mode)		2.50	2.80	3.20	v
VBLACK	Black level output voltage		1.80	2.20	2.50	V
VSYNC	Sync level output voltage	$RL = 470\Omega$	1.60	2.00	2.30	v
VCB	Color burst amplitude		0.16	0.22	0.28	v
VP-P	White level, sync level potential differential.		0.40	0.60	0.75	v
VP-P(B/W)	White level, sync level potential differential (monochrome mode)		0.60	0.80	0.95	v

^{*} Reference values are indicated by Vcc = 5.00V, TA = 25 °C.

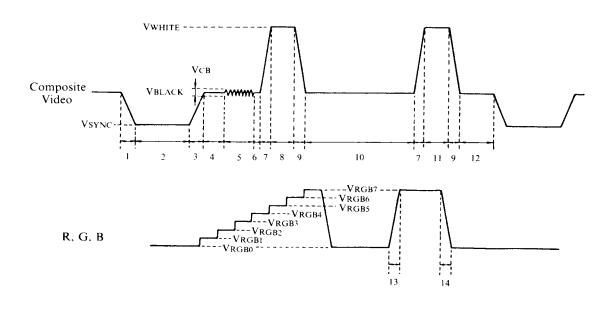
5. RGB Output Level

Symbol	Item	Measurement Conditions	Minimum	Reference	Maximum	Unit
VRGB 7	R, G, B maximum output voltage		2.5	2.8	3.2	v
VRGB 0	R. G, B minimum output voltage (black level)		1.7	2.0	2.4	v
VP-P	R. G. B VRGB7-VRGB0 potential differential.	$RL = 470\Omega$	0.65	0.8	1.00	v
Drgb	R, G, B VP-P deviation				5.0	%

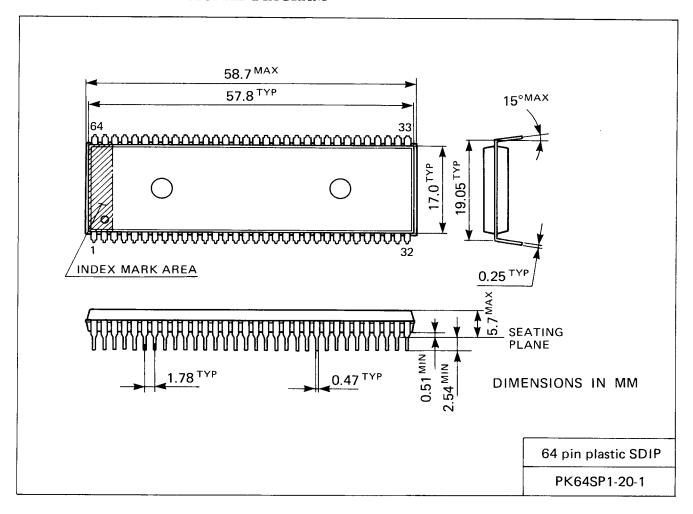
* Reference values are indicated by Vcc = 5.00V, TA = 25 °C.

6. Sync Signal Output Level

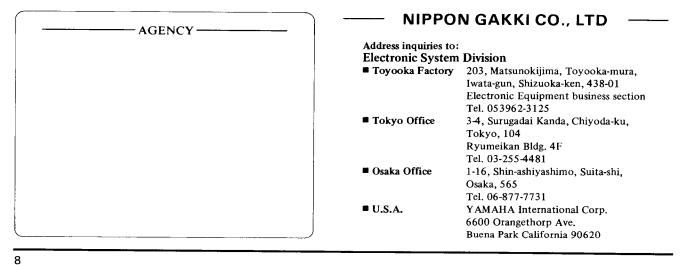
Symbol	Item	Measurement Conditions	Minimum	Reference	Maximum	Unit
VTLVH 1	3-value output high level BLEO		4.5		Vec	v
VTLVM 1	3-value output intermediate level BLEO	$RL = 1K\Omega$	2.5		3.5	v
VTLVL 1	3-value output low level BLEO	$RL = 1K\Omega$			0.4	V
VTLVH 2	3-value output high level HSYNC, CSYNC		4.5		Vcc	v
VTLVM 2	3-value output intermediate level HSYNC, CSYNC	No load	2.7		3.7	v
VTLVL 2	3-value output low level HSYNC, CSYNC	1			0.8	
Vyh	Ys output high level	Іон = 100μА	2.4			v
VYL	Ys output low level	IOL = 1.6mA			0.4	V
ITLVH	High level input current HSYNC, CSYNC	VI + 0.4V			-4.0	mA
ITLVL	Intermediate level input current HSYNC, CSYNC	VI = 0.4V			-2.0	mA



■ PACKAGE DIMENSIONAL DIAGRAM



The specifications of this product are subject to improvement changes without prior notice.



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