

# 8K x 8 Power-Switched and Reprogrammable PROM

#### **Features**

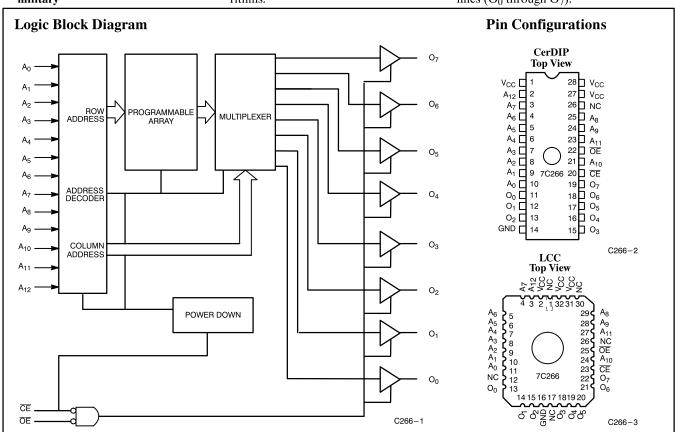
- CMOS for optimum speed/power
- Windowed for reprogrammability
- High speed
  - 20 ns (commercial)
  - 25 ns (military)
- Low power
  - 660 mW (commercial)
  - -770 mW (military)
- Super low standby power
  - Less than 85 mW when deselected
- EPROM technology 100% programmable
- $5V \pm 10\% V_{CC}$ , commercial and military

- TTL-compatible I/O
- Direct replacement for 27C64 **EPROM**s

### **Functional Description**

The CY7C266 is a high-performance 8192 word by 8 bit CMOS PROM. When deselected, the CY7C266 automatically powers down into a low-power standby mode. It is packaged in a 600-mil-wide package. The reprogrammable packages are equipped with an erasure window; when exposed to UV light, these PROMs are erased and can then be reprogrammed. The memory cells utilize proven EPROM floating-gate technology and byte-wide intelligent programming algoThe CY7C266 is a plug-in replacement for EPROM devices. The EPROM cell requires only 12.5V for the super voltage and low-current requirements allow for gang programming. The EPROM cells allow for each memory location to be tested 100%, as each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming, the product will meet DC and AC specification limits.

Reading is accomplished by placing an active LOW signal on  $\overline{OE}$  and  $\overline{CE}$ . The contents of the memory location addressed by the address lines (A<sub>0</sub> through  $A_{12}$ ) will become available on the output lines ( $O_0$  through  $O_7$ ).



### **Selection Guide**

		7C266-20	7C266-25	7C266-35	7C266-45
Maximum Access Time (ns)		20	25	35	45
Maximum Operating	Commercial	120	120	100	100
Current (mA)	Military		140		120
Maximum Standby Current (mA)	Commercial	15	15	15	15
	Military		15		15



## **Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)
Storage Temperature $\dots -65^{\circ}$ C to $+150^{\circ}$ C
Ambient Temperature with Power Applied
Supply Voltage to Ground Potential (Pin 28 to Pin 14)
DC Voltage Applied to Outputs in High Z State0.5V to +7.0V
DC Input Voltage3.0V to +7.0V
DC Program Voltage

Static Discharge Voltage	)1V
Latch-Up Current	mΑ
UV Exposure	cm <sup>2</sup>

## **Operating Range**

Range	Ambient Temperature	$v_{cc}$
Commercial	$0^{\circ}$ C to $+70^{\circ}$ C	$5V \pm 10\%$
Industrial <sup>[1]</sup>	-40°C to +85°C	5V ± 10%
Military <sup>[2]</sup>	−55°C to +125°C	$5V \pm 10\%$

## Electrical Characteristics Over the Operating Range<sup>[3, 4]</sup>

				7C26	6-20	7C26	6-25	
Parameter	Description	Test Conditions	<b>Test Conditions</b>		Max.	Min.	Max.	Unit
$V_{OH}$	Output HIGH Voltage	$V_{CC} = Min.,$	Com'l	2.4		2.4		V
		$I_{OH} = -2.0 \text{ mA}$	Mil			2.4		
$V_{OL}$	Output LOW Voltage	$V_{CC}$ = Min., $I_{OL}$ = 8.0 mA	Com'l		0.4		0.4	V
		$V_{CC}$ = Min., $I_{OL}$ = 6.0 mA	Mil				0.4	
$V_{\mathrm{IH}}$	Input HIGH Voltage		•	2.0		2.0		V
$V_{ m IL}$	Input LOW Voltage				0.8		0.8	V
$I_{IX}$	Input Current	$GND \le V_{IN} \le V_{CC}$		-10	+10	-10	+10	μΑ
$V_{CD}$	Input Diode Clamp Voltage				No	te 5		
$I_{OZ}$	Output Leakage Current	$V_{OL} \le V_{OUT} \le V_{OH}$ , Output Disabled		-40	+40	-40	+40	μА
$I_{OS}$	Output Short Circuit Current <sup>[5]</sup>	$V_{CC} = Max., V_{OUT} = GND$	$V_{CC} = Max., V_{OUT} = GND$		-90	-20	-90	mA
$I_{CC}$	Power Supply Current	$V_{CC} = Max., V_{IN} = 2.0V,$	Com'l		120		120	mA
		$I_{OUT} = 0 \text{ mA}$	Mil				140	
$I_{SB}$	Standby Supply Current	Chip Enable Inactive,	Com'l		15		15	mA
		$\overline{\text{CE}} \geq \text{V}_{\text{IH}}, \text{I}_{\text{OUT}} = 0 \text{ mA}$	Mil				15	

#### Notes

- 1. Contact a Cypress representative regarding industrial temperature range specification.
- 2.  $T_A$  is the "instant on" case temperature.
- 3. See the last page of this specification for Group A subgroup testing information.
- 4. See the "Introduction to CMOS PROMs" section of the Cypress Data Book for general information on testing.
- 5. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.



## **Electrical Characteristics** Over the Operating Range<sup>[3, 4]</sup> (continued)

				7C26	6-35	7C26	6-45	
Parameter	Description	Test Conditions		Min.	Max.	Min.	Max.	Unit
$V_{\mathrm{OH}}$	Output HIGH Voltage	$V_{CC} = Min., I_{OH} = -4.0 \text{ mA}$		2.4		2.4		V
$V_{OL}$	Output LOW Voltage	$V_{CC}$ = Min., $I_{OL}$ = 16.0 mA			0.4		0.4	V
$V_{\mathrm{IH}}$	Input HIGH Voltage			2.0		2.0		V
$V_{\mathrm{IL}}$	Input LOW Voltage				0.8		0.8	V
I <sub>IX</sub>	Input Current	$GND \leq V_{IN} \leq V_{CC}$	$GND \le V_{IN} \le V_{CC}$		+10	-10	+10	μΑ
$V_{CD}$	Input Diode Clamp Voltage				No	te 5		
$I_{OZ}$	Output Leakage Current	$V_{OL} \le V_{OUT} \le V_{OH}$ , Output Disabled	$V_{\rm OL} \leq V_{\rm OUT} \leq V_{\rm OH},$ Output Disabled		+10	-10	+10	μΑ
$I_{OS}$	Output Short Circuit Current <sup>[5]</sup>	$V_{CC} = Max., V_{OUT} = GND$	$V_{CC} = Max., V_{OUT} = GND$		-90	-20	-90	mA
$I_{CC}$	Power Supply Current	$V_{CC} = Max., V_{IN} = 2.0V,$	Com'l		100		100	mA
		$I_{OUT} = 0 \text{ mA}$	Mil				120	
$I_{SB}$	Standby Supply Current	Chip Enable Inactive, Com'l			15		15	mA
		$\overline{\text{CE}} \ge \text{V}_{\text{IH}}, \text{I}_{\text{OUT}} = 0 \text{ mA}$	Mil				15	

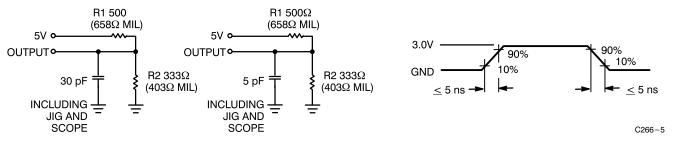
## Capacitance<sup>[4]</sup>

Parameter	Description	Test Conditions	Max.	Unit
$C_{IN}$	Input Capacitance	$T_A = 25^{\circ}C, f = 1 \text{ MHz},$	10	pF
C <sub>OUT</sub>	Output Capacitance	$V_{CC} = 5.0V$	10	pF



## **AC Test Loads and Waveforms**

## Test Load for −20 through −25 speeds



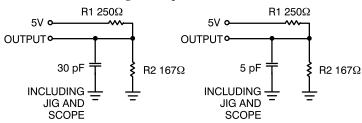
(a) Normal Load

(b) High Z Load

C266-4

Equivalent to: THEVENIN EQUIVALENT

### Test Load for −35 through −55 speeds



(c) Normal Load

(d) High Z Load

C266-6

Equivalent to: THEVENIN EQUIVALENT  $R_{TH} 100\Omega$ 

## Switching Characteristics Over the Operating Range<sup>[2,3,4]</sup>

		7C26	6-20	7C26	6-25	7C26	6-35	7C26	6-45	
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
$t_{AA}$	Address to Output Valid		20		25		35		45	ns
t <sub>HZCE</sub>	Chip Enable Inactive to High Z		25		30		40		45	ns
t <sub>HZOE</sub>	Output Enable Inactive to High Z		12		12		20		25	ns
t <sub>AOE</sub>	Output Enable Active to Output Valid		12		12		20		25	ns
t <sub>ACE</sub>	Chip Enable Active to Output Valid		25		30		40		45	ns
t <sub>OHA</sub>	Data Hold from Address Change	3		3		3		3		ns
$t_{\mathrm{PU}}$	Chip Enable Active to Power-Up		25		30		40		45	ns
t <sub>PD</sub>	Chip Enable Inactive to Power-Down		25		30		40		45	ns



### **Erasure Characteristics**

Wavelengths of light less than 4000 angstroms begin to erase the devices in the windowed package. For this reason, an opaque label should be placed over the window if the EPROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 angstroms for a minimum dose (UV intensity multiplied by exposure time) of 25 Wsec/cm<sup>2</sup>. For an ultraviolet lamp with a 12 mW/cm<sup>2</sup> power rating, the exposure time would be approximately 35 minutes. The CY7C266 needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the

EPROM is exposed to high-intensity UV light for an extended period of time.

7258 Wsec/cm<sup>2</sup> is the recommended maximum dosage.

### **Programming Modes**

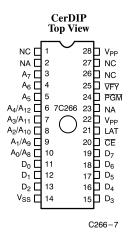
Programming support is available from Cypress as well as from a number of third party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

**Table 1. Mode Selection** 

			Pin Function <sup>[6, 7]</sup>						
	Normal Operation	A <sub>8</sub>	A9	A <sub>10</sub>	A <sub>11</sub>	A <sub>12</sub>	CE	ŌE	$D_7 - D_0$
Mode	Program	VFY	PGM	LAT	NA	NA	CE	V <sub>PP</sub>	$D_7 - D_0$
Rea	d	A <sub>8</sub>	$A_9$	$A_{10}$	A <sub>11</sub>	A <sub>12</sub>	$V_{\mathrm{IL}}$	$V_{\mathrm{IL}}$	$O_7 - O_0$
Stan	ndby	X	X	X	X	X	$V_{\mathrm{IH}}$	X	Three-Stated
Outj	put Disable	A <sub>8</sub>	<b>A</b> 9	$A_{10}$	A <sub>11</sub>	A <sub>12</sub>	$V_{\mathrm{IL}}$	$V_{IH}$	Three-Stated
Prog	gram	$V_{IHP}$	$V_{ILP}$	$V_{ILP}$	$V_{ILP}$	$V_{\rm ILP}$	$V_{\rm ILP}$	$V_{PP}$	$D_7 - D_0$
Prog	gram Verify	$V_{\rm ILP}$	$V_{\mathrm{IHP}}$	$V_{\rm ILP}$	$V_{\rm ILP}$	$V_{\rm ILP}$	$V_{\rm ILP}$	$V_{PP}$	$O_7 - O_0$
Prog	gram Inhibit	$V_{\mathrm{IHP}}$	$V_{\mathrm{IHP}}$	$V_{\rm ILP}$	$V_{\rm ILP}$	$V_{\rm ILP}$	$V_{\rm ILP}$	$V_{PP}$	Three-Stated
Blank Check		$V_{ILP}$	$V_{\mathrm{IHP}}$	$V_{\rm ILP}$	$V_{\rm ILP}$	$V_{\rm ILP}$	$V_{\rm ILP}$	$V_{PP}$	$O_7 - O_0$

#### Notes:

7. Address  $A_8 - A_{12}$  must be latched through lines  $A_0 - A_4$  in Programming modes.



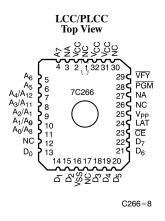
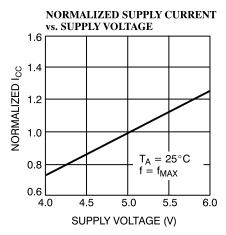


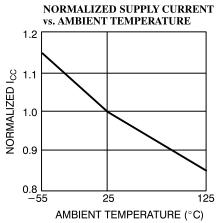
Figure 1. Programming Pinout

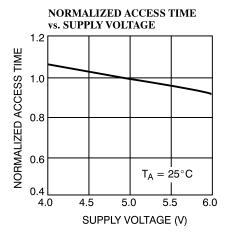
<sup>6.</sup> X = "don't care" but must not exceed  $V_{CC} + 5\%$ .

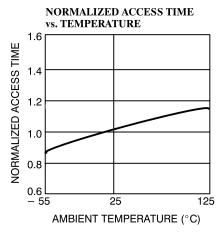


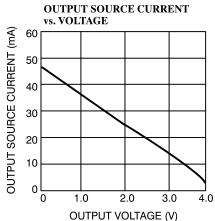
## **Typical DC and AC Characteristics**

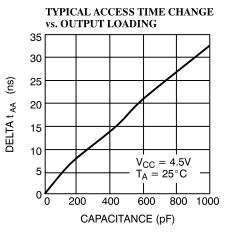


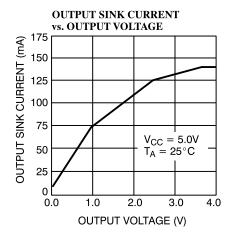


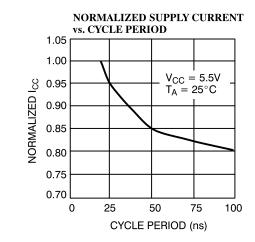














## **Ordering Information**<sup>[8]</sup>

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
20	CY7C266-20PC	P15	28-Lead (600-Mil) Molded DIP	Commercial
	CY7C266-20WC	W16	28-Lead (600-Mil) Windowed CerDIP	
25	CY7C266-25PC	P15	28-Lead (600-Mil) Molded DIP	Commercial
	CY7C266-25WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY7C266-25DMB	D16	28-Lead (600-Mil) CerDIP	Military
	CY7C266-25LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY7C266-25QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY7C266-25WMB	W16	28-Lead (600-Mil) Windowed CerDIP	
35	CY7C266-35PC	P15	28-Lead (600-Mil) Molded DIP	Commercial
	CY7C266-35WC	W16	28-Lead (600-Mil) Windowed CerDIP	
45	CY7C266-45PC	P15	28-Lead (600-Mil) Molded DIP	Commercial
	CY7C266-45WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY7C266-45DMB	D16	28-Lead (600-Mil) CerDIP	Military
	CY7C266-45LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY7C266-45QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY7C266-45WMB	W16	28-Lead (600-Mil) Windowed CerDIP	

#### Note

## MILITARY SPECIFICATIONS Group A Subgroup Testing

## **DC** Characteristics

Parameter	Subgroups
$V_{\mathrm{OH}}$	1, 2, 3
$V_{OL}$	1, 2, 3
$V_{ m IH}$	1, 2, 3
$ m V_{IL}$	1, 2, 3
$I_{IX}$	1, 2, 3
$I_{OZ}$	1, 2, 3
$I_{CC}$	1, 2, 3
$I_{SB}$	1, 2, 3

## **Switching Characteristics**

Parameter	Subgroups
$t_{AA}$	7, 8, 9, 10, 11
$t_{AOE}$	7, 8, 9, 10, 11
$t_{ m ACE}$	7, 8, 9, 10, 11

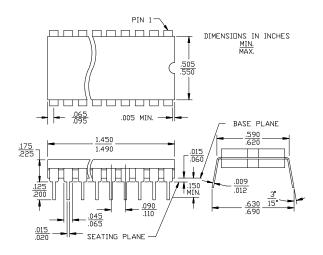
Document #: 38-00086-D

Most of these products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

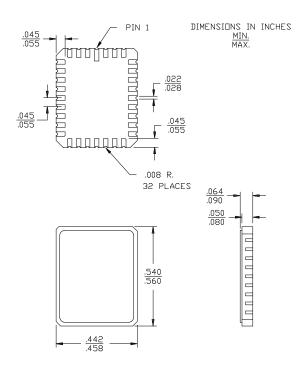


## **Package Diagrams**

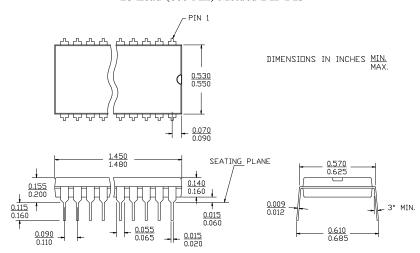
# **28-Lead (600-Mil) CerDIP D16** MIL-STD-1835 D-10 Config. A



# **32-Pin Rectangular Leadless Chip Carrier L55**MIL-STD-1835 C-12



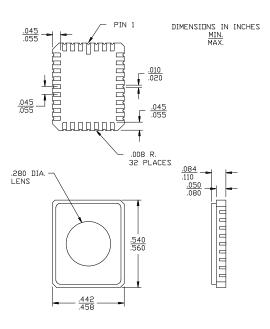
## 28-Lead (600-Mil) Molded DIP P15



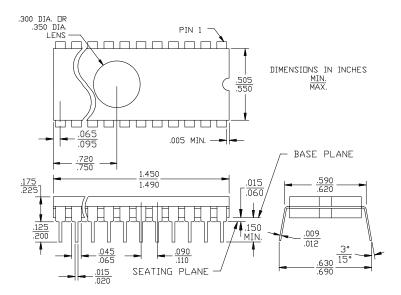


## Package Diagrams (continued)

# **32-Pin Windowed Rectangular Leadless Chip Carrier Q55** MIL-STD-1835 C-12



# **28-Lead (600-Mil) Windowed CerDIP W16** MIL-STD-1835 D-10 Config. A



<sup>©</sup> Cypress Semiconductor Corporation, 1990. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress Semiconductor Corporation product. Nor does it convey or imply any license under patent or other rights. Cypress Semiconductor does not authorize its products for use as critical components in life-support systems where a malfunction or failure of the product may reasonably be expected to result in significant injury to the user. The inclusion of Cypress Semiconductor products in life-support systems applications implies that the manufacturer assumes all risk of such use and in so doing indemnifies Cypress Semiconductor against all damages.