



i486 Level II Cache Module Family

Features

- Cache sizes of 64 KB, 256 KB, or 1 MB
- Tag width of 8 bits
- Independent dirty bit
- Operates with 33-MHz Intel i486 processors
- Zero-wait-state operation
- Constructed using standard asynchronous SRAMs
- 64-position (128-signal) dual-readout SIMM
- Single 5V (±5%) power supply
- TTL-compatible inputs/outputs

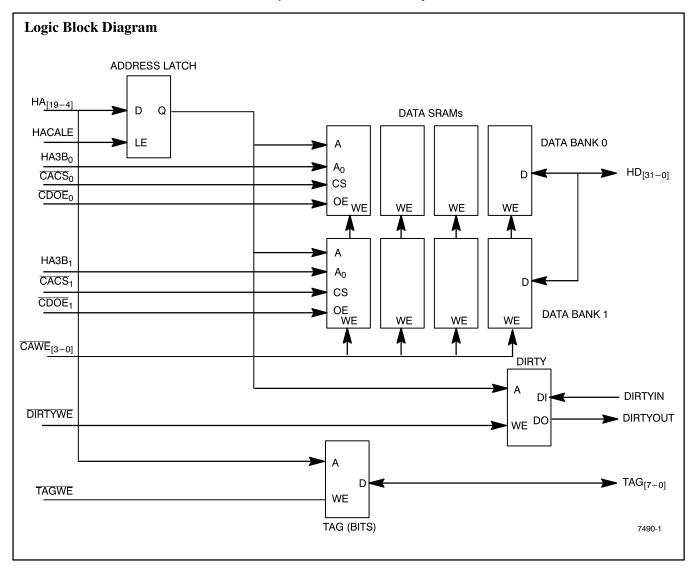
Functional Description

The CYM7490 module series is a family of cache memory subsystems for Intel i486-based systems. Each module contains two banks of 32-bit-wide data SRAM, an 8-bit-wide tag SRAM, and a single-bit-wide, separate I/O dirty SRAM. Bank sizes of 8K x 32, 32K x 32, and 128K x 32 are supported, yielding cache sizes of 64 kilobytes, 256 kilobytes, and 1 megabyte. The address signals for the data and dirty SRAMs are latched.

The module is configured as a 128-pin dual-readout single-in-line memory module (SIMM). It is constructed using standard asynchronous SRAMs in SOJ pack-

ages mounted on an epoxy laminate substrate. The SIMM contacts are plated with five micro-inches of gold over 100 micro-inches of nickel. Module dimensions are 3.85 inches long by 1.15 inches high by 0.33 inches thick.

These modules are designed for zero-waitstate operation in 486-based systems operating at a bus speed of 33 MHz. They are designed for compatibility with off-theshelf cache controllers and chipsets. The 15-ns device is built using data and tag SRAMs with an access time of 15 ns, while the 20-ns version is built with 15-ns tag SRAMs and 20-ns data SRAMs.





Dual-Readout SIMM Top View

```
GND ☐ 65
                                                  1 GND
         PD<sub>0</sub> | 66
PD<sub>2</sub> | 67
NC | 68
NC | 69
NC | 70
GND | 71
                                                 2 PD<sub>1</sub>
3 PD<sub>3</sub>
                                                  4 NC
                                                  5 6
                                                            NC
                                                           NC
                                                  7 🏻
                                                           GND
         NC  72
TAG<sub>7</sub> 73
                                                 8 9
                                                            NC
                                                            TAG<sub>6</sub>
                                                  9
           V<sub>CC</sub> ☐ 74
                                                10 □ V<sub>CC</sub>
         TAG<sub>5</sub> □ 75
                                                11 ☐ TĂĞ₄
12
                                                            TAG<sub>2</sub>
                                               13
14
                                                           GND
                                                            TAG<sub>0</sub>
                                               15 TAGWE
  V<sub>CC</sub>  80
DIRTYIN 81
                                               16  ∨<sub>CC</sub>
17  DIRTYOUT
  HACALE B2
GND 83
                                                18 □ NC
                                                19 GND
                                               20 □ HA<sub>5</sub>
            HA₄ ☐ 84
            HA<sub>6</sub> ☐ 85
                                                21 | HA<sub>7</sub>
                                               22 V<sub>CC</sub>
23 HA<sub>9</sub>
            V<sub>CC</sub> □ 86
         24 | HA<sub>11</sub>
                                                25 🗀
                                                           GND
         26 HA<sub>13</sub>
                                                27 HA<sub>15</sub>
                                                28 V<sub>CC</sub>
                                                       □ HĀ<sub>17</sub>
                                                29
         HA<sub>18</sub> ☐ 94
GND ☐ 95
                                               30 HA<sub>19</sub>
31 GND
      GND | 99
CDOE<sub>0</sub> | 100
GND | 101
CAWE<sub>0</sub> | 102
CAWE<sub>2</sub> | 103
GND | 104
HD<sub>0</sub> | 105
HD<sub>2</sub> | 106
V<sub>CC</sub> | 107
HD<sub>4</sub> | 108
HD<sub>6</sub> | 109
GND | 111
HD<sub>10</sub> | 112
V<sub>CC</sub> | 111
HD<sub>10</sub> | 111
HD<sub>11</sub> | 111
GND | 116
HD<sub>14</sub> | 115
GND | 116
HD<sub>16</sub> | 117
                                                35 GND
                                               39 ☐ CAWE<sub>3</sub>
                                               40 GND
41 HD<sub>1</sub>
42 HD<sub>3</sub>
                                                43 \ V<sub>CC</sub>
                                                44 HD<sub>5</sub>
                                                45 \ HD<sub>7</sub>
                                                46 GND
                                                       Б но₃
                                                47
                                                48 HD11
                                                49 □ V<sub>C</sub>C
                                                50 HD<sub>13</sub>
                                               51 HD<sub>15</sub>
52 GND
         GND | 116

HD<sub>16</sub> | 117

HD<sub>18</sub> | 118

V<sub>CC</sub> | 119

HD<sub>20</sub> | 120

HD<sub>22</sub> | 121

GND | 122

HD<sub>24</sub> | 123

HD<sub>26</sub> | 124

V<sub>CC</sub> | 125

HD<sub>28</sub> | 126

HD<sub>28</sub> | 126

HD<sub>28</sub> | 126

HD<sub>29</sub> | 127
                                                           HD<sub>17</sub>
                                                53
                                               54 HD<sub>19</sub>
                                                            V_{CC}
                                                55
                                                56 ☐ HD<sub>21</sub>
                                                57 HD<sub>23</sub>
                                                58 GND
                                                       □ HD<sub>25</sub>
                                                59
                                               60 ☐ HD<sub>27</sub>
                                               62 HD<sub>29</sub>
          HD<sub>30</sub> □ 127
                                               63 ☐ HD<sub>31</sub>
           GND ☐ 128
                                                64 GND
```

7490-2





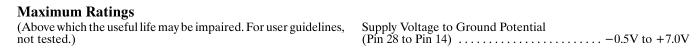
Signal Descriptions

Signal	Туре	Description
TAG ₇₋₀	I/O	Cache Tag Data Bus
TAGWE	I	Tag Write Enable
DIRTYWE	I	Dirty Bit Write Enable
DIRTYIN	I	Dirty Bit In
DIRTYOUT	0	Dirty Bit Out
HACALE	I	Host Address Bus Latch Enable
HA ₁₉₋₄	I	Host Address Bus.
$\overline{\text{CACS}}_{1-0}$	I	Cache Memory Chip Selects
$HA3B_{1-0}$	I	Host Address A3 Bank Select
$\overline{\text{CDOE}}_{1-0}$	I	Cache Data Output Enable
CAWE _{3−0}	I	Cache Write Enables
HD ₃₁₋₀	I/O	Host Data Bus
PD ₃₋₀	0	Presence Detect Pins (see below)
NC	_	Reserved for future use.

Presence Detect Scheme

Device	PD ₃	PD ₂	PD ₁	PD ₀
CYM7490	Open	Open	Open	GND
CYM7491	Open	Open	GND	Open
CYM7492	Open	Open	GND	GND

Storage Temperature $\dots -55^{\circ}$ C to $+150^{\circ}$ C





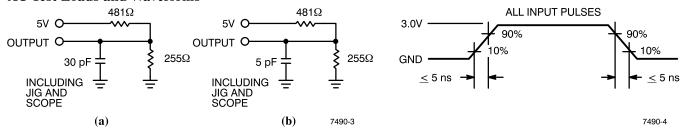
Electrical Characteristics Over the Operating Range

			CYM7490-15, 20 CYM7491-15, 20 CYM7492-15, 20		
Parameter	Description	Test Conditions	Min.	Min. Max.	
V_{CC}	Supply Voltage		4.5	5.5	V
T _{AMB}	Ambient Temperature	Commercial	0	70	°C
V _{OH}	Output HIGH Voltage	$V_{\rm CC}$ = Min. $I_{\rm OH}$ = -4.0 mA	2.4		V
V_{OL}	Output LOW Voltage	$V_{CC} = Min. I_{OL} = 80 \text{ mA}$		0.4	V
V_{IH}	Input HIGH Voltage Level		2.2	V_{CC}	V
$V_{\rm IL}$	Input LOW Voltage Level		-0.5	0.8	V
L _{IN}	Input Leakage Output	$V_{CC} = Max., 0 \le V_{IN} \le V_{SS}$		±20	μΑ
I _{OUT}	Operating Leakage Current	$\overline{\text{CS}} = V_{\text{IH}}, V_{\text{CC}} = \text{Max.}, V_{\text{SS}} \le V_{\text{OUT}} \le V_{\text{CC}}$		±20	μΑ
I _{CC1}	Operating Current	$\overline{\text{CACSn}} = V_{\text{IL}}$, Outputs Open, $f = f_{\text{MAX}}$		1300	mA
I_{SB1}	Standby Current – TTL Levels			800	mA
I_{SB2}	Standby Current – CMOS Levels			400	mA

Capacitance

Parameter	Description	Test Conditions	Max.	Unit
C_{ADDR}	Input Capacitance, HA ₁₉₋₄ , CAA3 ₁₋₀	f=1 MHz	50	pF
$C_{ m WE}$	Input Capacitance, CAWE ₁₋₀ , TAGWE	f=1 MHz	30	pF
C_{WE2}	Input Capacitance, DIRTYWE, HACALE	f=1 MHz	20	pF
C _{CSOE}	Input Capacitance, \overline{CACS}_{1-0} , \overline{CDOE}_{1-0}	f=1 MHz	50	pF
C_{DATA}	Input/Output Capacitance, HD ₃₁₋₀	f=1 MHz	90	pF
C_{TAG}	Input/Output Capacitance, TAG ₇₋₀ , DIRTYIN, DIRTYOUT	f=1 MHz	30	pF

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT OUTPUT $0 - \frac{167\Omega}{\sqrt{}}$ 1.73V



Switching Characteristics Over the Operating Range

		7490-15 7491-15 7492-15		7490-20 7491-20 7492-20		
Parameter	Parameter Description		Max.	Min.	Max.	Unit
ADDRESS LAT	ГСН		•	•	•	•
$t_{ m LPW}$	Latch Pulse Width	5		5		ns
$t_{ m LSD}$	Data Set-Up to ALE Positive	2		2		ns
t _{LHD}	Data Hold from ALE Positive	1.5		1.5		ns
READ CYCLE	- Data SRAM Read Timing			•	•	•
t_{RC}	Read Cycle Time	20		25		ns
t _{AA}	Address Access Time (Latch Transparent)		20		25	ns
t _{OE}	Output Enable to Output Valid		10		10	ns
t_{CE}	Chip Enable to Data Valid		15		20	ns
t _{OHA}	Data Hold After Address Change	3		3		ns
t _{LZCE}	Chip Enable to Outputs in Low Z	3		3		ns
t _{HZCE}	Chip Disable to Outputs in High Z		8		10	ns
t _{OLZ}	Output Enable to Outputs in Low Z	0		0		ns
t _{OHZ}	Output Disable to Outputs in High Z		8		10	ns
READ CYCLE	- Tag SRAM Read Timing		1	•	•	
t _{TDRC}	Read Cycle Time	15		20		ns
t _{TAA}	Address Access Time		15		20	ns
t _{TCE}	Chip Enable to Data Valid		15		20	ns
t _{TOHA}	Data Hold After Address Change	3		3		ns
t _{TLZCE}	Chip Enable to Outputs in Low Z	3		3		ns
t _{THZCE}	Chip Disable to Outputs in High Z		8		8	ns
READ CYCLE	- Dirty SRAM Read Timing		1	•		
t_{DRC}	Read Cycle Time	20		25		ns
t_{DAA}	Address Time		20		25	ns
t _{DOHA}	Data Hold After Address Change	3		3		ns
WRITE CYCLE	E – Data SRAM Write Timing		•	•	•	
t _{WC}	Write Cycle Time	20		25		ns
t _{SCE}	Chip Enable to End of Write	10		15		ns
t_{AW}	Address Set-Up to End of Write	20		25		ns
t_{AH}	Address Hold from End of Write	0		0		ns
t_{SA}	Address Set-Up from Beginning of Write	5		5		ns
t _{PWE}	Write Pulse Width	10		15	<u> </u>	ns
t _{SD}	Data Set-Up to End of Write	7		10		ns
t _{HD}	Data Hold from End of Write	0		0		ns
t _{LZWE}	Write HIGH to Outputs in Low Z	3		3		ns
t _{HZWE}	Write LOW to Outputs in High Z		7		10	ns



Switching Characteristics (continued)

		7490-15 7491-15 7492-15		7490-20 7491-20 7492-20		
Parameter Description		Min.	Max.	Min.	Max.	Unit
WRITE CYCLE	- Tag SRAM Write Timing		•			
t_{TWC}	Write Cycle Time	15		15		ns
t _{TSCE}	Chip Enable to End of Write	10		10		ns
t _{TAW}	Address Set-Up to End of Write	10		10		ns
t _{TAH}	Address Hold from End of Write	0		0		ns
t _{TSA}	Address Set-Up from Beginning of Write	0		0		ns
t _{TPWE}	Write Pulse Width	10		10		ns
t _{TSD}	Data Set-Up to End of Write	7		7		ns
t _{THD}	Data Hold from End of Write	0		0		ns
t _{TLZWE}	Write HIGH to Outputs in Low Z	3		3		ns
t _{THZWE}	Write LOW to Outputs in High Z		7		7	ns
WRITE CYCLE	- Dirty SRAM Write Timing		•		•	•
$t_{ m DWC}$	Write Cycle Time	20		20		ns
t_{DAW}	Address Set-Up to End of Write	17		17		ns
t _{DAH}	Address Hold from End of Write	0		0		ns
t _{DSA}	Address Set-Up from Beginning of Write	5		5		ns
t _{DPWE}	Write Pulse Width	12		12		ns
$t_{ m DSD}$	Data Set-Up to End of Write	10		10		ns
t _{DHD}	Data Hold from End of Write	0		0		ns
t _{DLZWE}	Write HIGH to Outputs in Low Z	5		5		ns
t _{DHZWE}	Write LOW to Outputs in High Z		7		7	ns

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Cache Size
15 (Data and Tag/Dirty)	CYM7490PM-15	PM05	128-Pin Dual-Readout SIMM	64 Kbyte
20 (Data), 15 (Tag/Dirty)	CYM7490PM-20	PM05	128-Pin Dual-Readout SIMM	
Speed (ns)	Ordering Code	Package Name	Package Type	Cache Size
Speed (ns) 15 (Data and Tag/Dirty)	Ordering Code CYM7491PM-15		Package Type 128-Pin Dual-Readout SIMM	

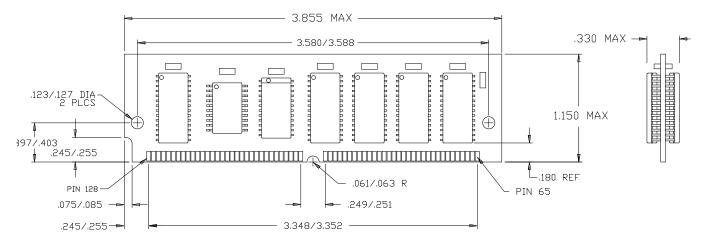
Speed (ns)	Ordering Code	Package Name	Package Type	Cache Size
15 (Data and Tag/Dirty)	CYM7492PM-15	PM07	128-Pin Dual-Readout SIMM	1 Mbyte
20 (Data), 15 (Tag/Dirty)	CYM7492PM-20	PM07	128-Pin Dual-Readout SIMM	

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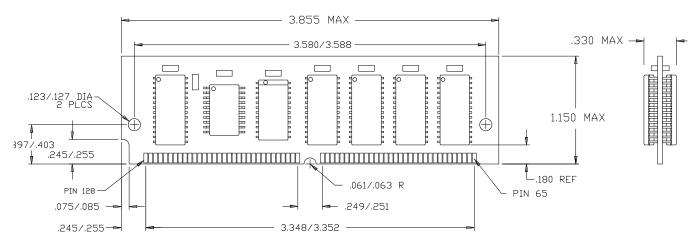


Package Diagrams

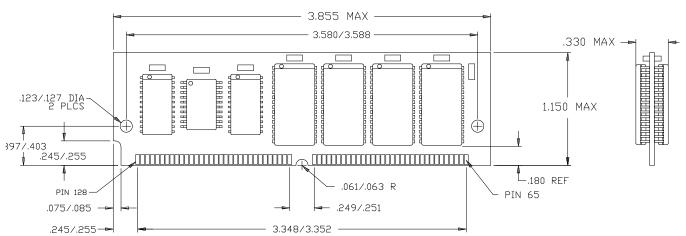
128-Pin Dual-Readout SIMM Module PM05



128-Pin Dual-Readout SIMM Module PM06



128-Pin Dual-Readout SIMM Module PM07



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