Albert-Ludwigs-Universität Freiburg

Master Thesis

Readout of a five dimensional Calorimeter

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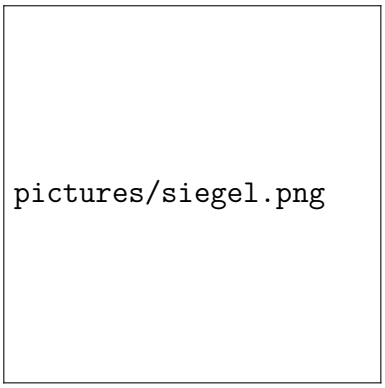
June 20, 2022



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Abstract

The SHiP experiment is planned to be a zero background beam dump experiment at the CERN's SPS accelerator. To achieve the zero background goal, the SBT is under development to tag all background events. It is a five-dimensional tagger based on a liquid scintillator. The scintillation light caused by particles traveling through the scintillator is captured by WOMs and detected by SiPMs. This thesis is in the framework of R&D of these SiPMs. Therefore the Citiroc 1A ASIC was used and tested with a array of 40 SiPMs. Using the Citiroc 1A evaluation board for a compact and easy to use DAQ measurements with the SiPMs in darkness as well as with a controlled light exposure via a LED and a Laser were performed. Also the effects of up to five SiPMs connected in parallel were analysed. A calibration of one SiPM and up to five SiPMs in parallel was performed as well as a measurement of the dark count rate.

Zusammenfassung

asdf

Contents

Chapter 1

Introduction

The Standard Model (SM) provides the best description of the universe. But through observations of different phenomena, which the SM can not explain, like neutrino oscillation [] and the rotation velocity in galaxies [], it is known, that the SM can not be a complete theory []. Therefore different experiments are in developement or are operating to search for new physics and new particles outside the SM. One of these experiments is the proposed Search for Hidden Particle (SHiP) experiment. Some experiments are at the energy frontier, using large energy scale trying to discover new particles. The experiments at the Large Hadron Colider (LHC) are examples for energy frontier experiments. Other experiments are at the cosmic frontieri, using for example cosmic background radiation. The third frontier is the intensity frontier. The zero background SHiP experiment is one of the intensity frontier experiment searching for rare events. Observing such rare events requires a high interaction rate. To achieve this, SHiP is planned to be a beam dump experiment at the Super Proton Synchrotron (SPS) accelerator ring at CERN, as shown in Figure 1.1. The goal is to dump the high intensity 400 GeV proton beam into a fixed target and thereby creating long lived particles outisde of the SM, e.g. heavy neutral leptons and light supersymmetric particles [1].

Figure 1.1: An overview of the SPS area with the SHiP experiment planed as beam dump experiment in the north area. [2]

Figure 1.2: Overview of the proposed setup for the SHiP experiment. The target on the left is used as a beam dump for the SPS. Most standard model particles get absorbed by the hadron absorber directly behind the targed. A magnetic muon shield deflects the muon, which won't be absorbed by the hadron absorber, away from the beam line. After the muon shield is a scattering and neutrino detector and afterwards the 50 m long decay volume in which non standard model particles created at the target can decay into standard model particles. To achieve the zero background goal, the Sourrund Background Tagger is around the decay volume. Behind the decay volume the decay spectrometer is placed. [3]

In Figure 1.2 the overall struckture of SHiP is shown. At the beginning, the 400 GeV gets dumped into the fixed targed. Through the many interactions happening at the target, a lot of SM particles will be created. In order to block the SM particles, two shields are placed after the target. The first is a hadron absorber in which all SM particles except muons and neutrinos are absorbed. The second is the muon shield. It uses magnetic fields to deflect the muons away from the beam line. The neutrinos cannot be blocked or deflected, but they are likely to be detected in the scattering and neutrino detector behind the muon shield. After the neutrino detector a 50 m long vacuum chamber is positioned. If a non SM particle is created at the target, is can decay inside the vacuum decay chamber back into SM particles. The decay products than get measured in the decay spectrometer behind the decay chamber.

One problem for the measurement are SM particles entering the decay volume and causing events in the spectrometer. An example of such a background are muons deflected by the muon shield but afterwrads reflected by the walls of the facility into to decay volume. Therefore it is crucial for the zero background requirment to detect the particles entering the decay volume and tagging every event that could be caused by the entering particle as background. For this the Surround Background Tagger (SBT) is in developement. It is presented in the next chapter.

Chapter 2

The SBT as 5 Dimensional Calorimeter

For the SBT to allow the tagging of background events, it needs to provide multiple pieces of information about the measured events and therefore the particles entering the decay volume. To achieve this, the SBT is designed to be a five-dimensional tagger around the decay volume. It consists out of 2000 cells, each filled with with the liquid scintillator **lab!** (**lab!**). If a particle passes through the cell, it deposits energy in it, causing the emittance of scintillation light. The amount of scintillation light is proportional to the deposited energy and therefore it depends on the energy of the particle, the interaction crosssection of the particle and the length of the path inside the cell that the particle traveled. Each cell houses two Wavelengthshifting Optical Modules (WOMs). If the scintillation light enters a WOM, the wavelength get shifted and through total reflection the photons stay in the WOM until they reache the end of the WOM tube. There they get detected by an array of photosensors. The concept of the cells, scintillator, WOMs and photosensor is depicted in Figure 2.1 By comparing the amount of light detected in each of the two WOMs one can estimate roughly the path of the particle. Adding this information to the information in which of the cells the particle was detected, the three spacial dimensions of the particle entering the SBT are known. Also by the detected amount of light, the energy as fourth dimension can be measured. The fifth dimension is the timing of the event. By using Silicon Photomultiplier as

Figure 2.1: Overview of the functionality of the Surround Background Tagger consisting out of 2000 cells. The cells are filled with liquid scintillator and are housing two Wavelength-shifting Optical Modules which capture the scintillation light and guide it to the Silicon Photomultipliers mounted at one and of the WOM. [9]

photosensor, a good time resolution can be achieved.

This thesis is about the readout of these Silicon Photomultipliers and therefore they are presented in this chapter with more detail.

2.1 Silicon Photomultiplier

In order to correctly identify and tag background events, the light detection of the SBT has to provide accurate timing information. Therefore Silicon Photomultipliers (SiPMs) were chosen as photodetectors. These photodetectors consist of up to thousands of pixels. Each pixel is a photodiode with a typical edge length between 10 µm and 100 µm [5]. If triggered by light, a SiPM sends out a charge signal proportional to the incoming light. This charge possesses a fast-rising edge with a rise time of the order of tens of s [5]. Besides the good time resolution, SiPMs also make it possible to count the arriving photos with a sensitivity down to single photons [6].

Similar to every photodiode, Avalanche Photodiodes (APDs) utilize the photoelectric effect, to generate an electric charge signal in response to a light signal. This is made possible by using silicon as a base material and introducing impurities. This process is called doping and there are two different possibilities for doping. In the n-doping, the impurities are atoms with five valence electrons. Four of these electrons are part of boundings with silicon atoms, and the fifth electron is only weakly bound. When p-doping, atoms with only three valence electrons are inserted into the silicon. This leads to missing charges in the silicon, called holes. By having an n-doped and a p-doped region in the silicon, the excess electrons from the n-doped region combine with the holes from the p-doped region, resulting in a depleted region at the pn-junction. If a photon hits the photodiode, it can create an electron-hole pair, or eh-pair. The electron and the hole get split by the electric field and thus

Figure 2.2: Composition of a avalanche photo diode with the bias voltage V_{B} applied in reverse direction. Between the contact to ground and the strongly doped n^+ layer is the quenching resistor R_{q} connected in series. Next to the n^+ layer is a strongly doped p^+ layer. In the region of these two layers is the electric field, shown on the right figure, the strongest. There a electron or hole can initiate an avalanche. After the p^+ layer comes a intrinsic weakly doped π layer. This layer increases the sensitive volume of the diode. If a electron-hole pair is created and seperated by the electric field. The hole drifts towards the multiplication region and can start an avalanche. The next layer is a p^+ layer which connects to a metal connector and high voltage. [4]

create a charge signal. In order to increase the sensitivity of the photodiode, an intrinsic layer can be added in between the two doped regions, thus increasing the depletion layer and therefore the photosensitive area. Such a photodiode is called a pin-diode. An APD with a weakly doped π intrinsic layer and strongly doped p^+ and n^+ layers is shown in Figure 2.2. This intrinsic layer can either be not doped at all or weakly doped. In the case of APDs the intrinsic layer is weakly doped. In order to amplify the signal, a strong doped region is inserted, thus creating a multiplication zone.

When a reverse bias voltage is applied to the APD, the electric field between the n^+ and p^+ layers is strong enough that a created eh-pair creates more eh-pairs, resulting in an avalanche. For this avalanche process to be possible the reverse bias voltage must be at or above the breakdown voltage of the APD. With such a bias voltage applied, the APD operates in the Geiger mode and the avalanche is then self-sustaining. This results in a macroscopic signal and makes the detection of single photons possible. Therefore these diodes are also called Single Photon Avalanche Diode (SPAD). To stop the avalanche, a quenching resistor is connected in series with the SPAD. With an increasing current signal flowing through the quenching resistor, the voltage drop at this resistor increases, and thus the bias voltage at the SPAD decreases. When the bias voltage drops under the breakdown voltage, the avalanche is no longer self-sustaining and stops. Thus the signal amplitude of a SPAD is always similar, independent of how many photons arrive at the same moment. In SiPMs hundreds to thousand SPADs are connected in parallel, each with a high resistance quenching resistor in series. Usually, the SPAD pixels are

Figure 2.3: Single photon avalanche diode signal shape. The exponential rise with the time constant $R_S \cdot C_d$ is followed by the exponential decay with the time constants $R_q \cdot C_d$. The maximum of the current signal is at approximately V_{ov}/R_q [6]

placed in a rectangular form with an edge length of a few mm. **??** shows a picture of a SiPM and one picture of a single pixel of a SiPM. Due to the property of the SPADs that the output signal is always similar for each SPAD, the output signal of a SiPM is the output signal of one SPAD multiplicated with the number of triggered SPADs. Therefore, if the number of photons arriving simultaneously at a SiPM is low enough, that the probability of one SPAD being hit by two or more photons is low, one can count photons with a SiPM. This and the relatively low cost, high durability, and impassivity to magnetic fields make them a good option for photodetection for the SBT and similar detectors.

In the following different properties of SiPMs are presented, beginning with the signal shape of a single SPAD and of a SiPM.

The signal shape of a SPADs starts with a fast exponential rise with the time constant

$$\tau_{rise} = R_S \cdot C_d \tag{2.1}$$

with the resistance R_{rise} and capacitance C_d of the SPAD [6]. After the signal reached its maximum current at around

$$I_{max} \approx \frac{V_{ov}}{R_q} \tag{2.2}$$

the quenching and recharging of the SPAD starts. Thus the current signal decreases again exponentially. The time constant for the signal decay

$$\tau_{decay} = R_q \cdot C_d \tag{2.3}$$

depends on the capacitance C_d of the SPAD and the quenching resistor R_q [6]. This signal develpment is shown in Figure 2.3.

When multiple SPADs in a SiPM are triggered, the output signal will be the summation of the signals from all triggered SPADs. Besides the number of triggered SPADs, the time difference between the signals from the single SPADs influences the signal. In the case, that all SPADs are triggered at the same time, the SiPM signal will have the shape of a SPAD signal scaled up by the factor of the number of triggered SPADs. If the signals form the individual SPADs have a small difference in time, the SiPM signal will become broader.

The gain G of a SiPM describes the number of charge carriers released in each avalanche. Due to the quenching, this parameter is well defined []. It can be calculated from the applied voltage U_{bias}, the breakdown voltage U_{bd} and the capacitance C_{d} of a SPAD with

$$G = \frac{(V_{\text{bias}} - V_{\text{bd}}) \cdot C_{\text{d}}}{\text{e}}. \tag{2.4}$$

Here e represents the charge of one electron. Usually the gain is in the order of 10^5 to 10^7 [5].

The noise in SiPMs can be sorted into two categories. The first is primary noise, it describes the triggering of avalanches by thermaly created *eh*-pairs and not by incident photons. Because the rate of theses thermaly caused events increases and decreases with the temperature, by controling the temperatur one can influence and decrease the rate of primary noise events. The second category is the correlated noise. It includes all events triggered by a primary event. This correlated noise does have two causes. One cause is the trapping and releasing of charge carriers from the avalanche. When the time between the trapping and releasing is long enough, the avalanche of the primary event stoped and the released carrier can trigger another avalanche.

2.1.1 Photoelectron spectrum

After the theory and important properties of SiPMs are now introduced, the next chapter will present the measurement setup and data acquisition used for this thesis.

Chapter 3

Setup

In this chapter, the setup and its components are introduced. First, the Citiroc 1A Application Specific Integrated Circuit (ASIC) and its evaluation board are presented. Then the used SiPM array is shown and in the last part of this chapter the box housing the SiPMs during the measurements is presented.

3.1 Citiroc 1A

Developed by the company Weeroc, the Citiroc 1A is an ASIC for the readout of SiPMs. In essence, it is an amplifier and shaper for an input signal with trigger capabilities and a multiplexer output for the shaper signal amplitude. So the charge signal coming from a SiPM gets amplified by the amplifier and integrated by the shaper. The maximum of this integrated signal is than connected to a multiplexed output. With this multiplexed output, all channels can be read out one after another at the same output of the Citiroc 1A. Therefore the number of Analog to Digital Converters (ADCs) needed to digitize the signals from every channel is reduced by a factor of 31. A sketch of the internal electronics of the Citiroc 1A is shown in Figure 3.1.

The Citiroc 1A has 32 channels. Each channel has an 8-bit input Digital to Analog Converter (DAC) which allows tuning the high voltage on a channel by channel

Figure 3.1: Depiction of the main components of the Citiroc 1A. The 32 channels with the inputs and the input DACs are followed by a low and a high gain preamplifier. Both amplified signals are shaped by slow shapers and the peak sensing cell returns the shaper signal amplitude to a multiplexer common to all channels. Also, the trigger part with a fast shaper followed by two discriminators is shown. One discriminator output is connected to a common multiplexer and an OR of the 32 channels. The other discriminator is connected to a channel by channel time trigger output and also to a common OR. The trigger threshold of both discriminators can be set individually but common for all channels via a 10-bit DAC. [8]

level. When the high voltage V_{HV} is supplied to the SiPMs and the DAC voltage is V_{DAC} the bias voltage on the SiPMs is

$$V_{\mathrm{bias}} = V_{\mathrm{HV}} - V_{\mathrm{DAC}}. \tag{3.1}$$

The input DACs are connected to the inputs with resistors in series, so that the fast charge signal from the SiPMs is not disturbed by the input DAC. Besides the 32 inputs, one *IN_CALIB* input exists with which a signal can be injected into one of the 32 channels. The injected signal goes over a 3 F capacitor into the preamplifier. A sketch of this is shown in Figure 3.2. After the input, there are two amplifiers in parallel. One high gain amplifier and one low gain amplifier so that a broader input range can be covered. The structure of both amplifiers is the same and shown in Figure 3.2. They each have a capacitor $\mathrm{C_{in}}$ in series and then a variable feedback capacitor $\mathrm{C_f}$ in parallel, which can be set to values from 0 fF to 1575 fF in 25 fF steps. The capacitors connected in series have fixed capacitances. The low gain preamplifier capacitor has 1.5 F and the high gain preamplifier has a 15 F capacitance. The Citiroc 1A datasheet states that the resulting amplification can be calculated with

$$AMP = \frac{\mathrm{C_{in}}}{\mathrm{C_f}}. \tag{3.2}$$

Since this equation is not defined for $\mathrm{C_f} = 0\,\mathrm{fF}$, that value was not used for the measurements in this thesis. For the other possible feedback capacitor values the resulting high gain and low gain amplifications are 9.5 V/V to 60 V/V and 0.95 V/V to 6 V/V, respectively. Each amplifier output is connected to a slow shaper and in

Figure 3.2: Illustration of the preamplifiers in the Citiroc 1A. The signal is injected either through the IN input or through the IN_Calib input. By changing the capacitance of the feedback capacitor, the gain can be set. [8]

Figure 3.3: The fast shaper of the Citiroc 1A with the 5 F capacitor C_{in} and the 500 Ω resistor R_{in} functioning as high pass filter. The capacitor $C_f = 100$ fF and the resistor $R_f = 25$ kΩ working as a low pass filter. The resulting peaking time is $t_{peak} = 15$ ns. [8]

addition one of the outputs can be connected to the trigger block of the Citiroc 1A.

The trigger unit starts with the shaping of the amplifier output connected to the trigger unit. This is done by a CRRC fast shaper with a 15 ns peaking time [8]. The high pass filter of the fast shaper consists of a $C_{in} = 5$ F capacitor and a $R_{in} = 500\,\Omega$ resistor. The low pass filter constists of a $C_f = 100$ fF capacitor and a $R_f = 25$ kΩ resistor. In Figure 3.3 the schematics of the fast shaper are shown. After the shaping, the signal goes into two discriminators. By using the two 10-bit DACs and the 4-bit DACs, also connected to the discriminator, a trigger threshold can be set. While the two 10-bit DACs are common for all the 32 channels, each channel has its own two 4-bit DACs. This allows to fine-tune the common threshold set by the 10-bit DACs on a channel by channel level. The time discriminator output is connected to an open-collector NOR of all 32 channels and can also be read out channel by channel, enabling the setting of time stamps for each channel. The charge discriminator is followed by masking opting, which allows the channel by channel masking of the charge trigger. After the masking option, the charge trigger signal is connected to an OR of the 32 channels which can be read out as an OR or as an open-collector NOR. The charge trigger can also be connected to a multiplexed output of all channels. With this output, one can easily see in the measurement data which channel was triggered in each event. Both triggers are sensitive down to 1/3 of a photoelectron [8].

For the charge measurement the outputs of the two preamplifiers are connected to two $CRRC^2$ slow shapers, depicted in Figure 3.4. The time constant for the high

Figure 3.4: Schematic of the Citiroc 1As $CRRC^2$ slow shapers. Each CR or RC part has a time constant changeable from 12.5 ns to 87.5 ns in 12.5 ns by changing the capacitance of the capacitors. [8]

pass filter and the two low pass filters can be set from 12.5 ns to 87.5 ns in 12.5 ns steps. This results in an overall peaking time of 25 ns to 175 ns in 25 ns. The slow shapers are followed by a peak sensing cell which gives the maximum shaper amplitude out to a multiplexer. Two options for finding the amplitude to put out are built in the peak sensing cell. The first option is the *SCA* which works with the *sample and hold* method. It recuires an external hold signal. The SCA tracks the shaper output constantly, until the external hold signal rises from low to high. On the rising edge of the hold signal, it samples the shaper amplitude and holds it until the hold signal falls back to low. In order to sample the maximum of the shaper amplitude, the rising edge of the hold signal must arrive, when the shaper signal is at its maximum.

The second peak sensing option is the *peak detector*. It starts in an idle phase and upon an arriving trigger, the internal charge trigger or an external trigger, it starts tracking the maximum of the shaper amplitude. When the external hold signal rises to high, the maximum amplitude is held, as long as the hold signal is high. During that time, the amplitude can be read out via the multiplexer. When the hold signal falls back to low, the peak detector enters the idle phase again.

The trigger starting the peak sensing tracking phase as well as the hold signal required for the peak sensing and the SCA are both common to all 32 channels. While the amplitudes of all channels are held, the three multiplexers put out the low gain amplitude, the high gain amplitude, and the charge trigger, one channel after another. The multiplexer requires an external clock signal to shift between the channels. In order to achieve a 10-bit resolution on the output, the clock's frequency should be less than 5 MHz. This leads to a readout time per channel of at least 200 ns and a total readout time of more than 6.4 µs. Since the Citiroc 1A holds the shaper amplitude during that time, it is blind to other events happening while the read-out of the multiplexed output is going on. Therefore a continuous readout is not possible with the Citiroc 1A.

In order to simplify working with the Citiroc 1A and getting to know it, the Citiroc 1A evaluation board was used. It is presented in the following section.

3.1.1 Citiroc 1A evaluation board

To make it easier to work with the Citiroc 1A, the corresponding evaluation board houses everything necessary except a computer to operate the Citiroc 1A. A picture of the Citiroc 1A evaluation board is shown in Figure 3.5. In the center of the evaluation board is the Citiroc 1A ASIC placed. Next to it are 32 pairs of pins for connecting the SiPMs. One row is connected to the 32 inputs of the Citiroc 1A and the other one can be used to supply the SiPMs via the evaluation board with high voltage. For this purpose, a connector can be soldered on the evaluation board over which the board can be supplied with the high voltage for the SiPMs. Over an SMA connector signals can be injected into the Citiroc 1As IN_CALIB input. Via three SMA connectors, the analog probes of the Citiroc 1A can be read out. With two onboard 12-bit ADCs to read out the low gain and high gain multiplexer outputs of the Citiroc 1A. Optional one of the ADCs can be used to digitize a test signal which can be injected into the ADC over a connector on the evaluation board. The other ADC can also be used to read out the temperature probe in the Citiroc 1A. For processing the digitized measurement data an FPGA is placed on the evaluation board. The firmware for the FPGA as well as the slow control parameters for the Citiroc 1A can be provided via the USB interface. This interface can also be used to supply the evaluation board with power instead of using the power connector on the board. In order to operate the Citiroc 1A evaluation board, Weeroc developed a computer program for the Windows operating system. With this program, the Citiroc 1A slow control parameter can be chosen and sent to the ASIC as well as some FPGA settings. The most important FPGA settings are the trigger settings, meaning which signal from the trigger block of the Citiroc 1A is used to trigger an event and the time delay between the arrival of the trigger signal and the sending of the hold signal for the peak sensing cell.

The evaluation board also provides multiple FPGA input/outputs. With these, for example, the digital trigger signal can be read out or a clock on the evaluation board can be put out and connected as a trigger to a light source.

In the following section, the SiPM array which was read out with the Citiroc 1A evaluation board is presented.

Figure 3.5: The Citiroc 1A evaluation board with the Citiroc 1A ASIC, the 32 input pins, the probe outputs, two ADCs, one FPGA with its input/output connectors, and the USB interface.

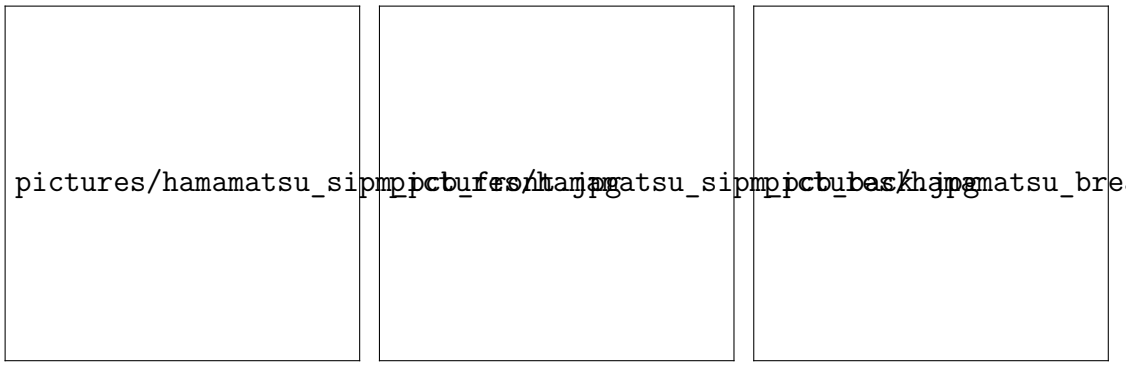
3.2 Silicon Photomultiplier Array

The SiPM array that was used for the measurements consists of forty *Hamamtsu S14160-3050HS* SiPMs which were soldered in a circle onto the Printed Circuit Board (PCB) shown in Figure 3.7a and Figure 3.7b. In Table 3.1 are the specifications of these SiPMs listed. The SiPMs were placed in a 6 cm outer diameter circle onto the PCB. The connections on the PCB were made so that the SiPMs are connected parallel in groups of five. Each group has a dip switch with five switches placed between the SiPMs and the high voltage. Therefore every individual SiPM can be turned on and off, simplifying debugging and allowing the examination of the signal difference between different numbers of SiPMs in parallel. The circuit diagram of one example SiPM group is shown in Figure 3.6.

In order to connect the SiPM outputs to the Citiroc 1A evaluation board inputs and to supply the SiPMs with high voltage, a breakout board was used. It can be connected to the back of the SiPM PCB. On the back of the breakout board are eight SMA connectors for the signal output of eight SiPM groups and one SMA connector for the common high voltage supply. A picture of the breakout board is shown in Figure 3.7c.

In order to be able to control the light exposure of the SiPMs during the measurements, they were placed inside of a light-tight box, which is described in the following chapter.

Figure 3.6: Circuit diagram of the connections on the SiPM PCB for one group of five SiPMs. Each SiPM can be disconnected from the high voltage via a switch. The high voltage side of the SiPMs is connected to ground over a 100 nF capacitor.



(a) The PCB front of the PCB. (b) The back of the PCB (c) The breakout board

Figure 3.7: The PCB with the forty Hamamtsu S14160-3050HS SiPMs. The SiPM circle has an outer diameter of 6 cm (a). On the back of the PCB the eight dip switches are placed and the connector is soldered in the middle of the back (b). Via the SMA connectors on the breakout board, the SiPMs can be supplied with power and the signals can be read out (c).

Table 3.1: Specifications of the *Hamamatsu S14160-3050HS* SiPMs. [7]

SiPM type	*S14160-3050HS*
Effective photosensitive area [mm^2]	3.0×3.0
Pixel pitch [µm]	50
Number of pixels	3531
Window material	Silicone
Window refractive index	1.57

3.3 Dark box

A aluminum box was used to place the SiPM PCB in and block the unwanted light from the surroundings from reaching the SiPMs. On the inside, it was covered with black aluminum foil by Thorlabs [**?**], with a reflectivity of less than 5 % for light in the visible spectrum. By this, the probability of photons entering the box to hit the SiPMs was decreased. In addition, the weak points of the box for which the light tightness can not be guaranteed were covered with multiple layers of tape.

Multiple SMA, SMC, and BNC feedthroughs were added for high voltage and signal transfer in and out of the box. Another self-made fiber feedthrough was used to lay two optical fibers stable from the outside into the box without causing light leaks. The two fibers were used for guiding the light from a LED and a Laser into the box.

To fix the SiPM PCB in place the optical rail was used. Besides the SiPM array also mounts for the two optical fibers as well as a diffuser [**?**] could be mounted if needed for a measurement.

To further decrease the probability of light leaks an optical blanket was used to cover the box after closing and the room was darkened during the measurements.

In the last part of this chapter, the LED used as a light source in this thesis is presented.

Figure 3.8: The setup inside the aluminum box with the SiPM array, the diffusor and the fiber coming from the LED.

3.4 Light sources

To have a controlled light exposure a 460 nm LED setup was used. This setup was built in the bachelor thesis by Alexander Bismark [**?**]. It consists of a small light-tight box with a LED inside, which is connected to a BNC feedthrough. Via a waveform generator connected to the BNC feedthrough the LED can be supplied with voltage pulses adjustable in length and amplitude. One end of an optical fiber is placed inside the LED box to capture a small part of the light emitted by the LED. The other end of the SMA terminated fiber is outside of the LED box and fed into and mounted inside of the aluminum box with the SiPMs. By using a diffusor by Thorlabs [**?**] multiple SiPMs can be exposed to the light at the same time.

For the measurements in this thesis which used the LED the length of the voltage pulses was set to 10 ns with a rise time and fall time of 2.5 ns. The amplitude of the pulses was adjusted to achieve the desired light exposure.

In Figure 3.9 a sketch of the complete assembled setup is shown. The SiPMs were placed inside the box and supplied with high voltage from the outside of the box by a high voltage supply. The signal outputs of the SiPMs are connected to the Citiroc 1A evaluation boards inputs. A laptop was used to load the slow control for the Citiroc 1A on the evaluation board, to save the data measured by the evaluation board and to supply power to the evaluation board. With the waveform generator supplying the LED with voltage pulses for it to emit the light which was guided inside the aluminum box. In the aluminum box a diffusor ensured even light exposure of the whole SiPM array.

In the next chapter the measurements performed with this setup are presented.

Figure 3.9: Illustration of the setup used for the measurements. The SiPMs array was placed inside the aluminum box to shield it from unwanted light. A power supply was used to supply the SiPMs with high voltage. The signal outputs from the SiPM array were connected to the inputs of the Citiroc 1A evaluation boards inputs. The data processed on the evaluation board was send to the laptop for storage. The laptop also provided the power for the evaluation board and was used to control the Citiroc 1A and load the slow control for it onto the evaluation board. With the waveform generator a LED was pulsed and the emitted light was guided into the aluminum box and there diffused for an even light exposure of the SiPMs.

Chapter 4

Conclusion and Outlook

Within the scope of this Thesis a setup for measuring SiPM output signals was assembled. A readout of the SiPMs has been realized using the Citiroc 1A ASIC with the corresponding evaluation board. The dark count rate (Dark Count Rate (DCR)) of single SiPMs and up to five SiPMs in parallel was determined. The measured DCRs are listed in **??**. As expected increases the DCR approximatley linear with the number of SiPMs in parallel. Due to the measurement methode with the peak detector the small undercount of dark counts with increasing DCR is expected.

Also a calibration of the SiPMs was done by using dark counts and a LED as light source. The determined gains of the measurements are listed in **??**. The gains of both the dark count measurements and the measurements with light source show the same behavior. With more SiPMs in parallel the gain increases. This is the opposite of what was expected based on the simulations from [9] and should be invested further.

In conclusion, the Citiroc 1A can be used to read out the SiPMs and therefore is suitable for testing prototypes of the SBT cells at a testbeam. But because the readout is not continous and the Citiroc 1A is blind while the multiplexer output signals are getting digitized, it is not usable for the final SBT. Without the multiplexed output and with an channel by channel signal output this would most likely change but with the price of an increase in ADCs. To reduce that increase in ADCs, the number of SiPMs read out in parallel would need to be increased. Therefore an

investigation on how many one SiPMs can be read out in parallel and still produce good results would be very interesting.

Appendix A

List of acronyms

SM Standard Model

LHC Large Hadron Colider

SHiP Search for Hidden Particle

SPS Super Proton Synchrotron

SBT Surround Background Tagger

SiPM Silicon Photomultiplier

PCB Printed Circuit Board

ASIC Application Specific Integrated Circuit

DAC Digital to Analog Converter

ADC Analog to Digital Converter

APD Avalanche Photodiode

DAQ Data Acquisition

WOM Wavelengthshifting Optical Module

SPAD Single Photon Avalanche Diode

DC Dark Count

DCR Dark Count Rate

FPGA Field Programmable Gate Array

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