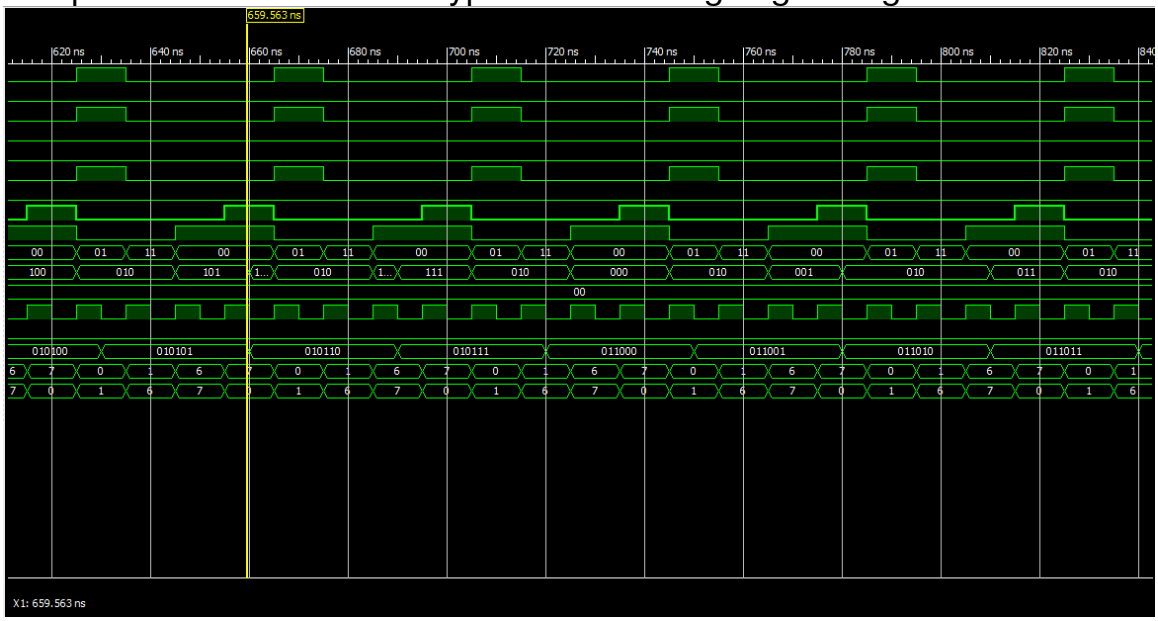
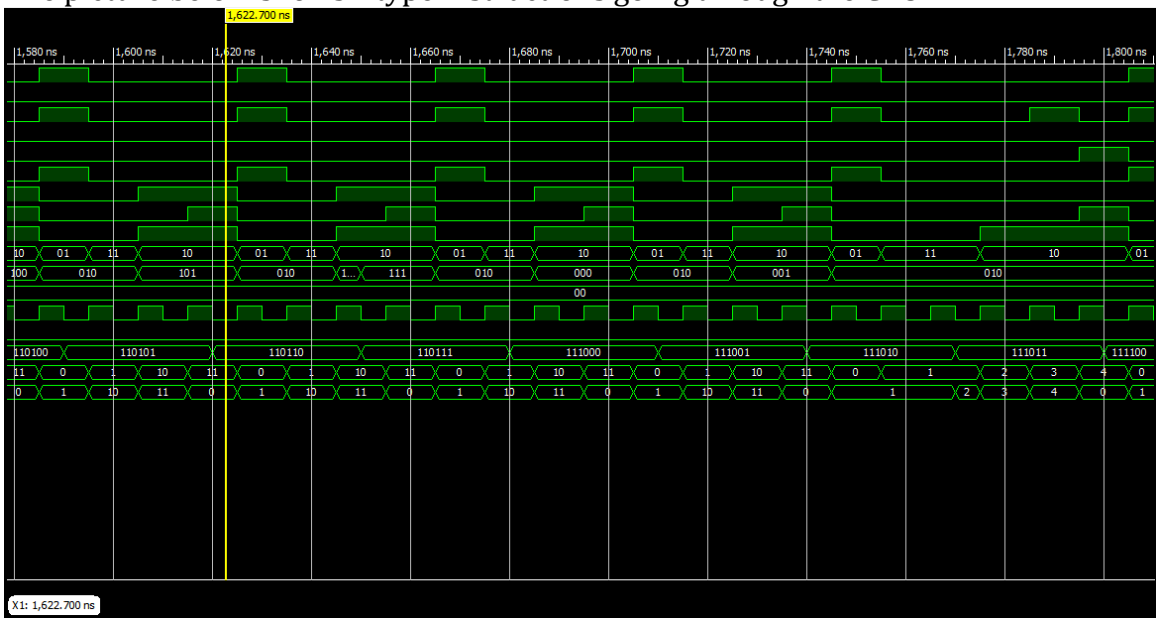
Johan Ospina Michael Ethier EC413 Control Milestone

Control Description:
The control design implemented is based off of the one from the lecture slides with slight modifications. In our design the instruction memory and the data memory are separated. In the finite state machine, 2 more stated were added for the I-type instructions, which gives a total of 11 states. The BE states were adjusted to work for BNE. The LW and SW states were adjusted to take in immediates because LWI and SWI are being implemented in the project. The control was tested using a test bench file that incremented through all the opcodes, while checking the current and next states.

Waveforms:
The picture below shows R-type instructions going through the CPU.



The picture below shows I-type instructions going through the CPU.



The picture below shows Jump instructions going through the CPU.