Project Name : Design of Current Starved Ring Oscillators

Course Name : VLSI-1 LAB
Course No : EEE4134
Section : C
Year : 4th
Semester : 1st

Submitted by

Name : Md.Johir Raihan
ID : 190105105
Section : C
Semester : 2nd
Year :4th

Circuit Diagram

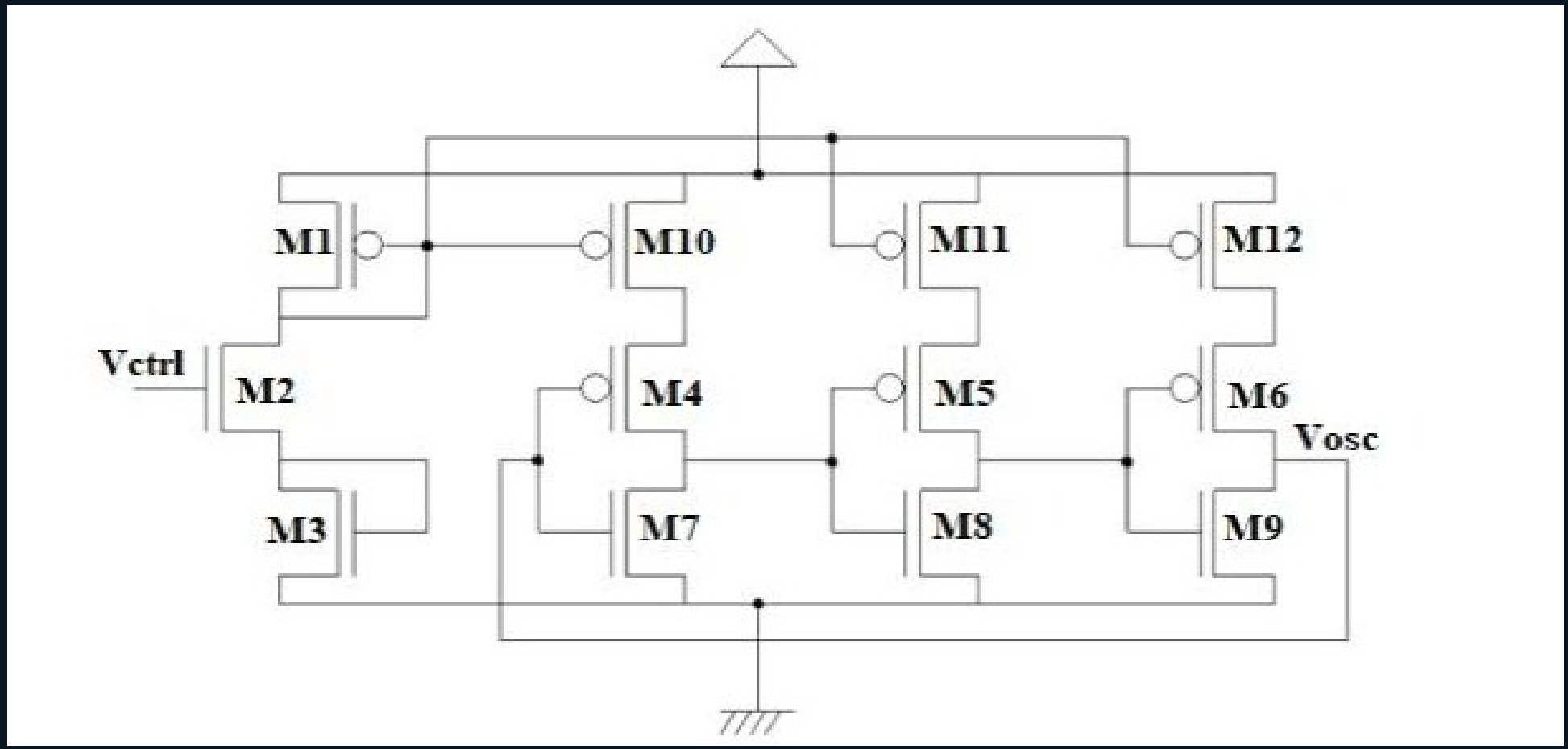
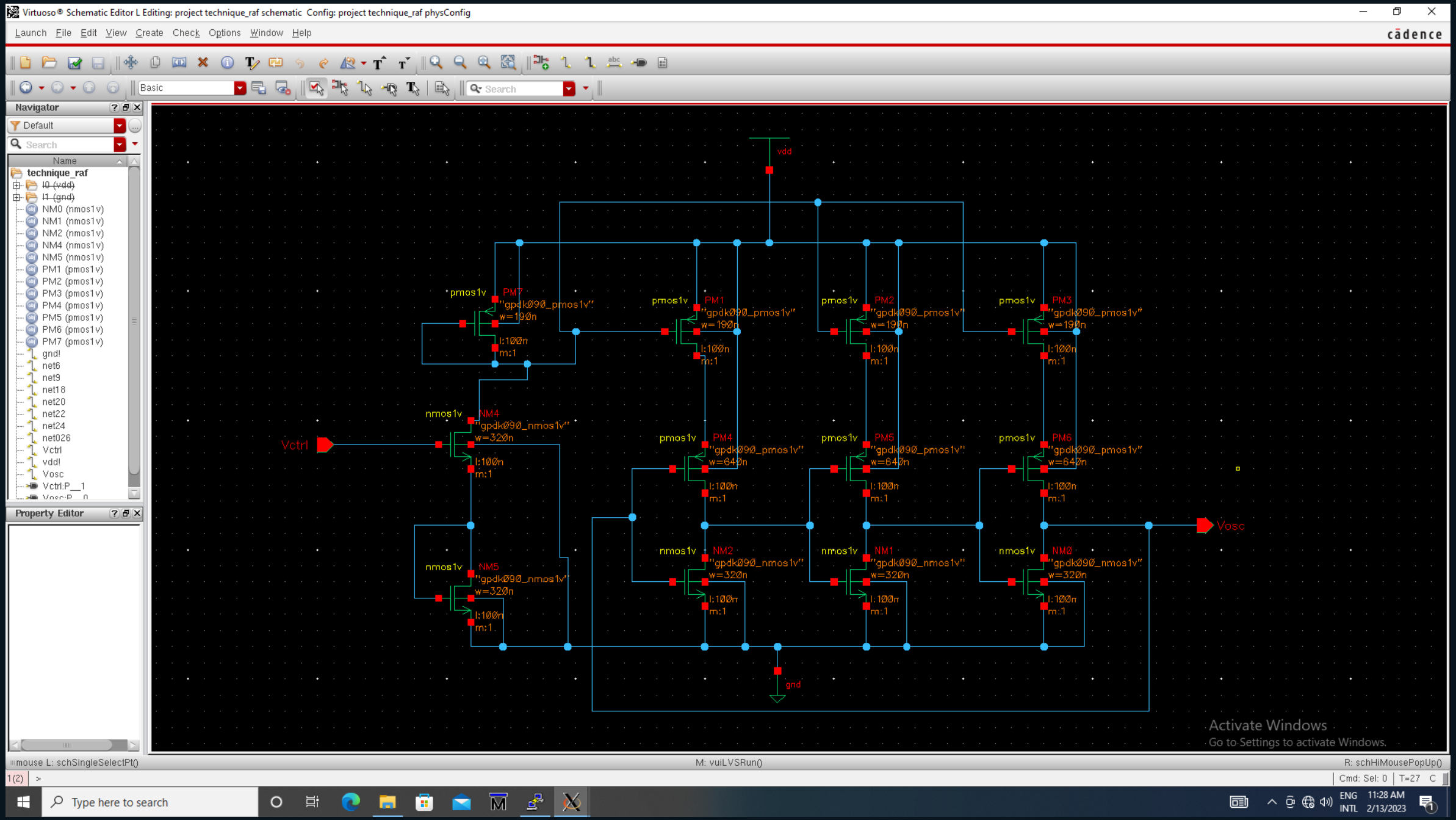
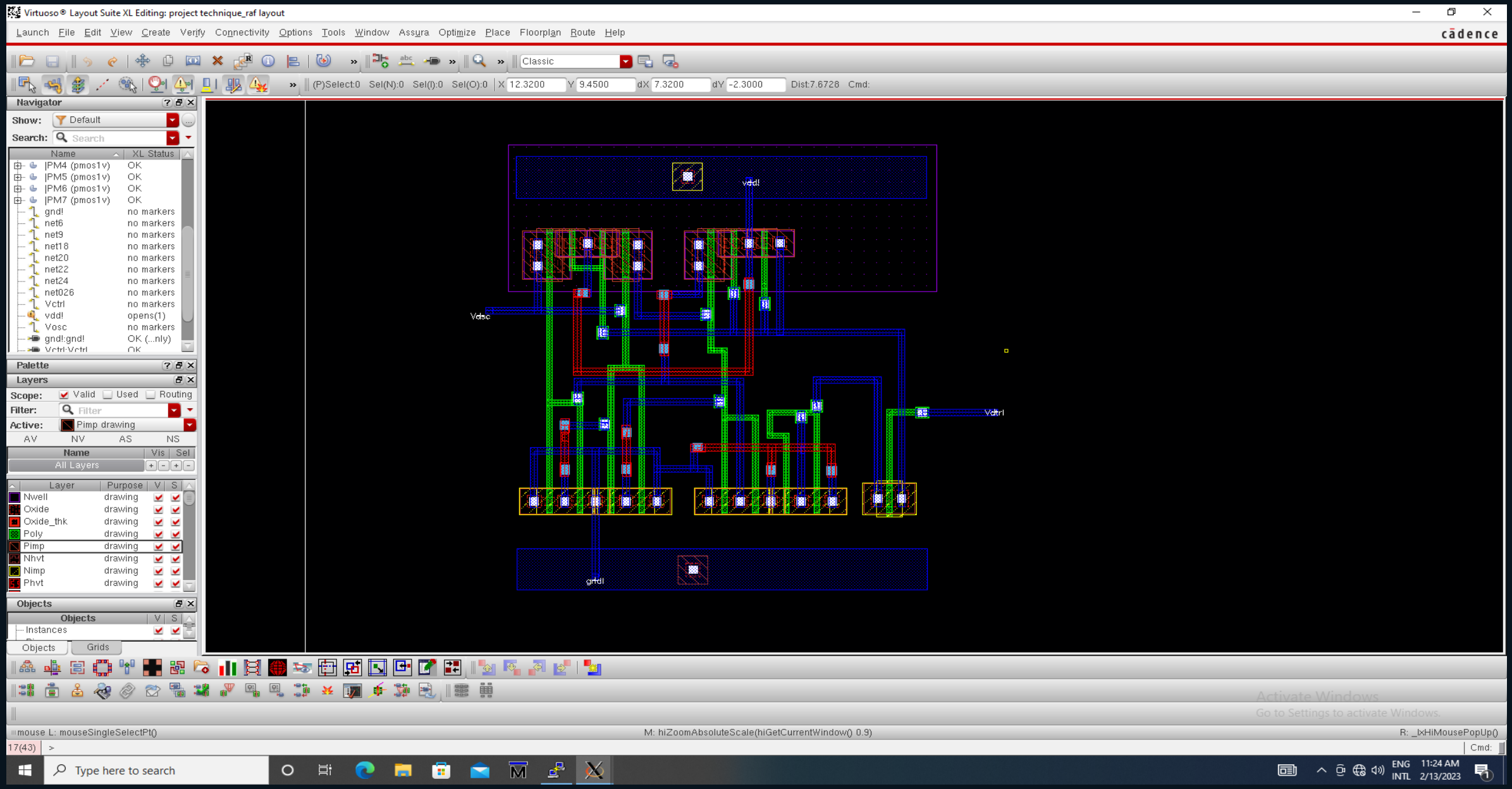


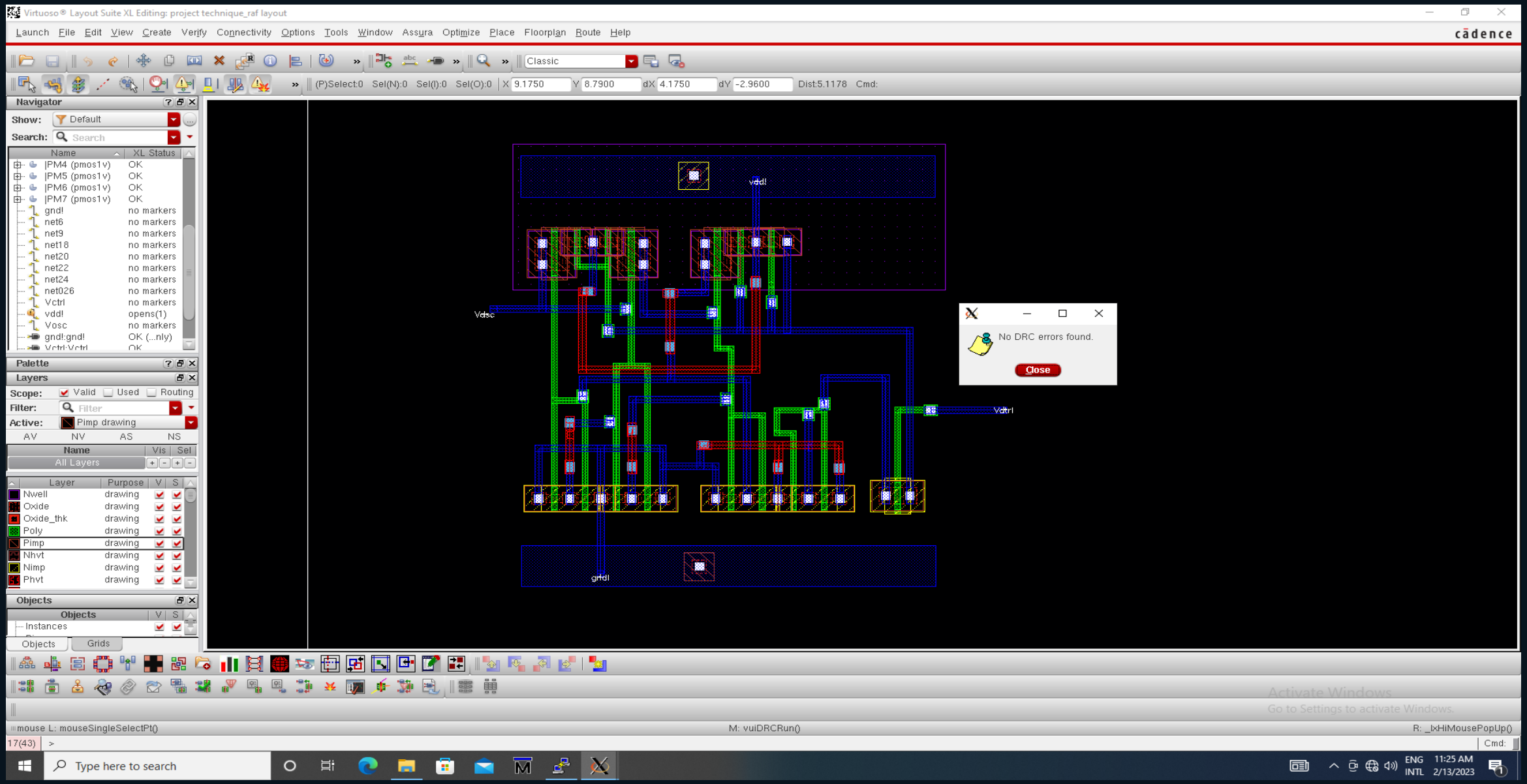
Figure : CSRO with only PMOS Source


Virtuoso® Schematic Editor L Editing: project technique_raf schematic Config: project technique_raf physConfig
Launch File Edit View Create Check Options Window Help
cadence
Navigator
Default
Search
Name
technique_raf
I0 (vdd)
I1 (gnd)
NM0 (nmos1v)
NM1 (nmos1v)
NM2 (nmos1v)
NM4 (nmos1v)
NM5 (nmos1v)
PM1 (pmos1v)
PM2 (pmos1v)
PM3 (pmos1v)
PM4 (pmos1v)
PM5 (pmos1v)
PM6 (pmos1v)
PM7 (pmos1v)
gnd!
net6
net9
net18
net20
net22
net24
net026
Vctrl
vdd!
Vosc
Vctrl:P__1
Property Editor
vdd
gnd
Vctrl
Vosc
pmos1v PM7 "gpdk090_pmos1v" w=190n l:100n m:1
pmos1v PM1 "gpdk090_pmos1v" w=190n l:100n m:1
pmos1v PM2 "gpdk090_pmos1v" w=190n l:100n m:1
pmos1v PM3 "gpdk090_pmos1v" w=190n l:100n m:1
nmos1v NM4 "gpdk090_nmos1v" w=320n l:100n m:1
pmos1v PM4 "gpdk090_pmos1v" w=640n l:100n m:1
pmos1v PM5 "gpdk090_pmos1v" w=640n l:100n m:1
pmos1v PM6 "gpdk090_pmos1v" w=640n l:100n m:1
nmos1v NM5 "gpdk090_nmos1v" w=320n l:100n m:1
nmos1v NM2 "gpdk090_nmos1v" w=320n l:100n m:1
nmos1v NM1 "gpdk090_nmos1v" w=320n l:100n m:1
nmos1v NM0 "gpdk090_nmos1v" w=320n l:100n m:1
Activate Windows
Go to Settings to activate Windows.
mouse L: schSingleSelectPt()
M: vuiLVSRun()
R: schHiMousePopUp()
Cmd: Sel: 0
T=27 C
Type here to search
ENG INTL
11:28 AM
2/13/2023

Layout Diagram



DRC Check


Virtuoso® Layout Suite XL Editing: project technique_raf layout
Launch File Edit View Create Verify Connectivity Options Tools Window Assura Optimize Place Floorplan Route Help
cadence
Navigator
Palette
Layers
Objects
vdd!
Vosc
Vctrl
gnd!
No DRC errors found.
Close
mouse L: mouseSingleSelectPt()
M: vuiDRCRun()
R: _lxHiMousePopUp()
Type here to search
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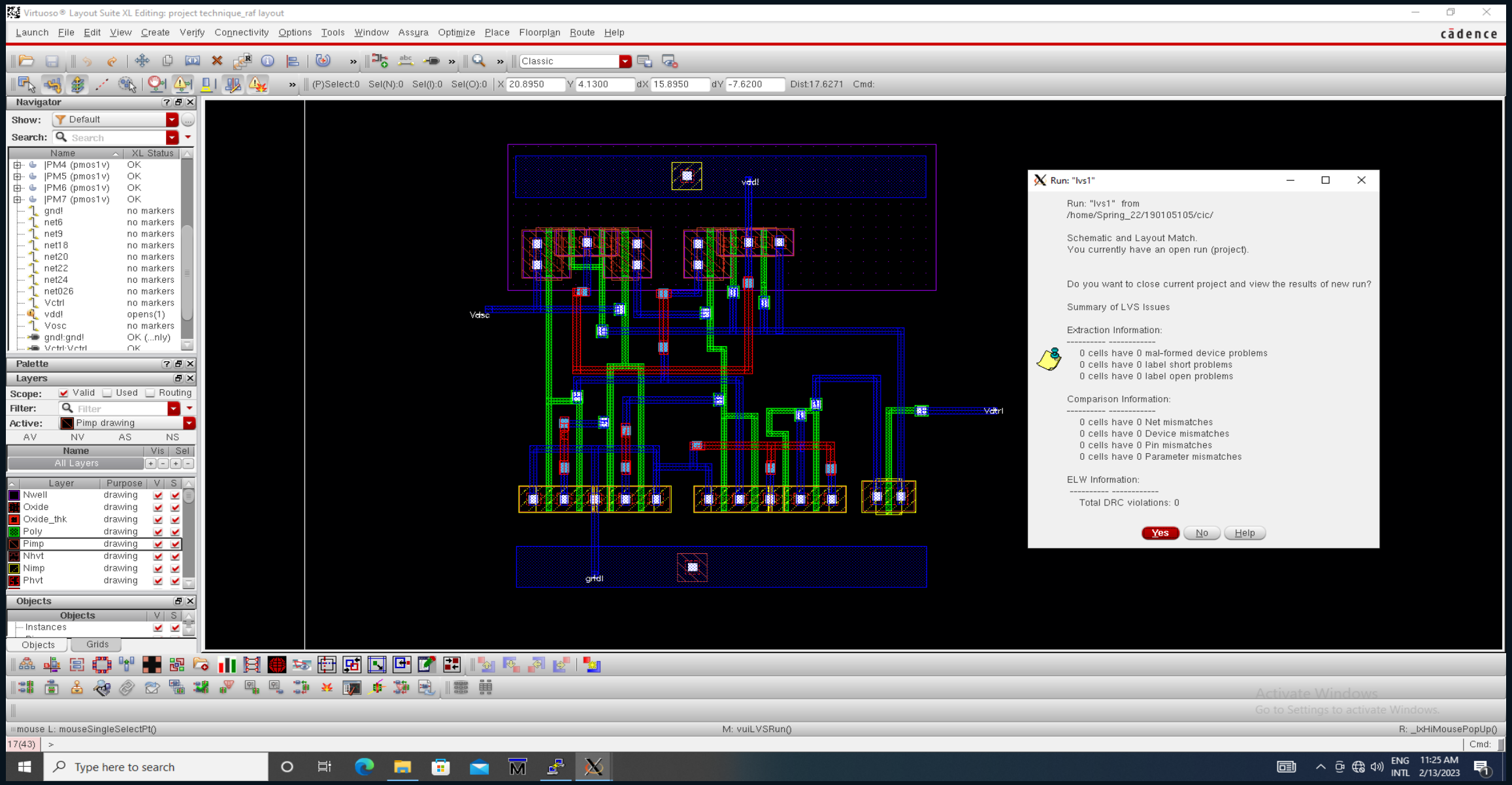
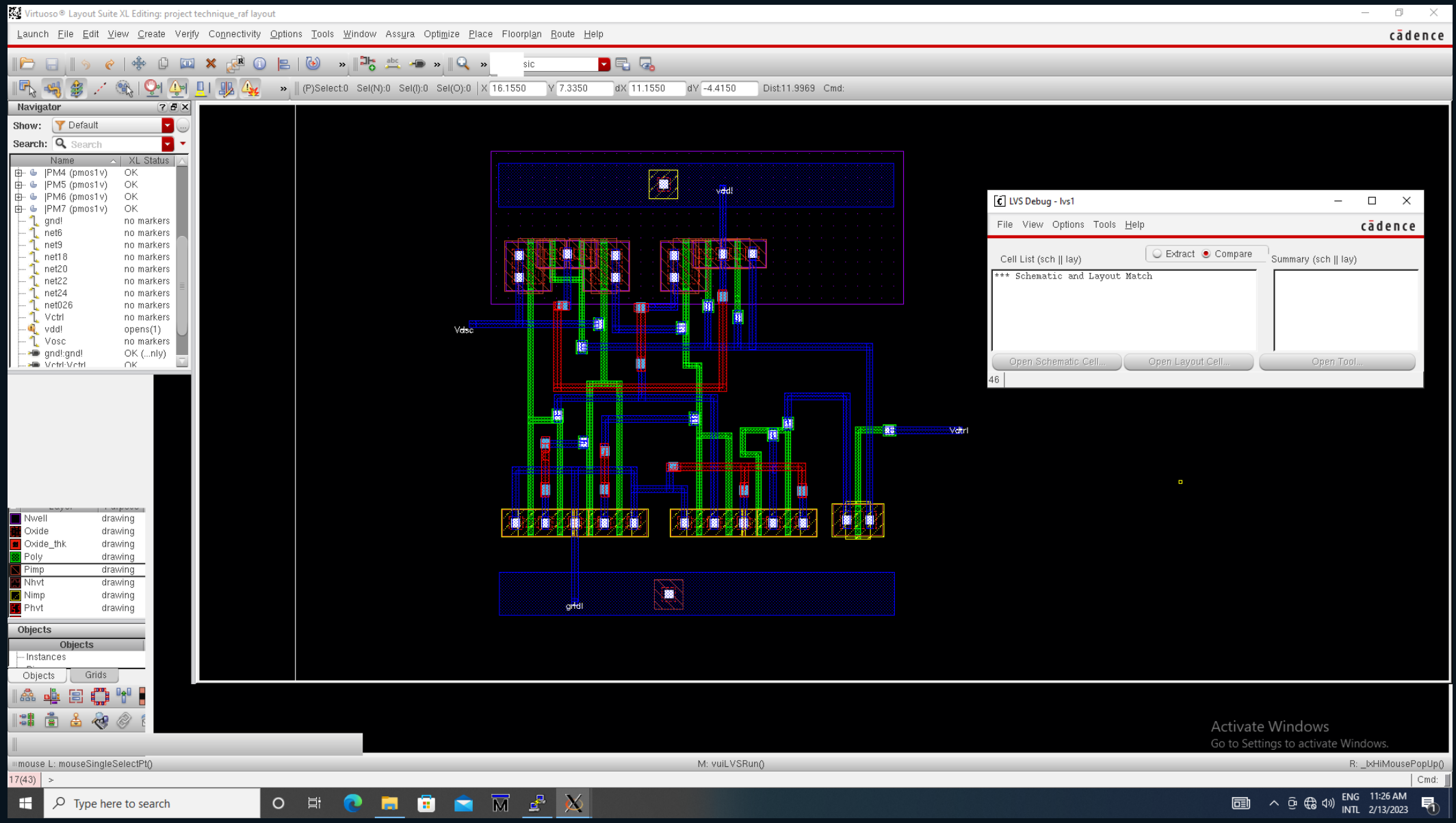
2/13/2023

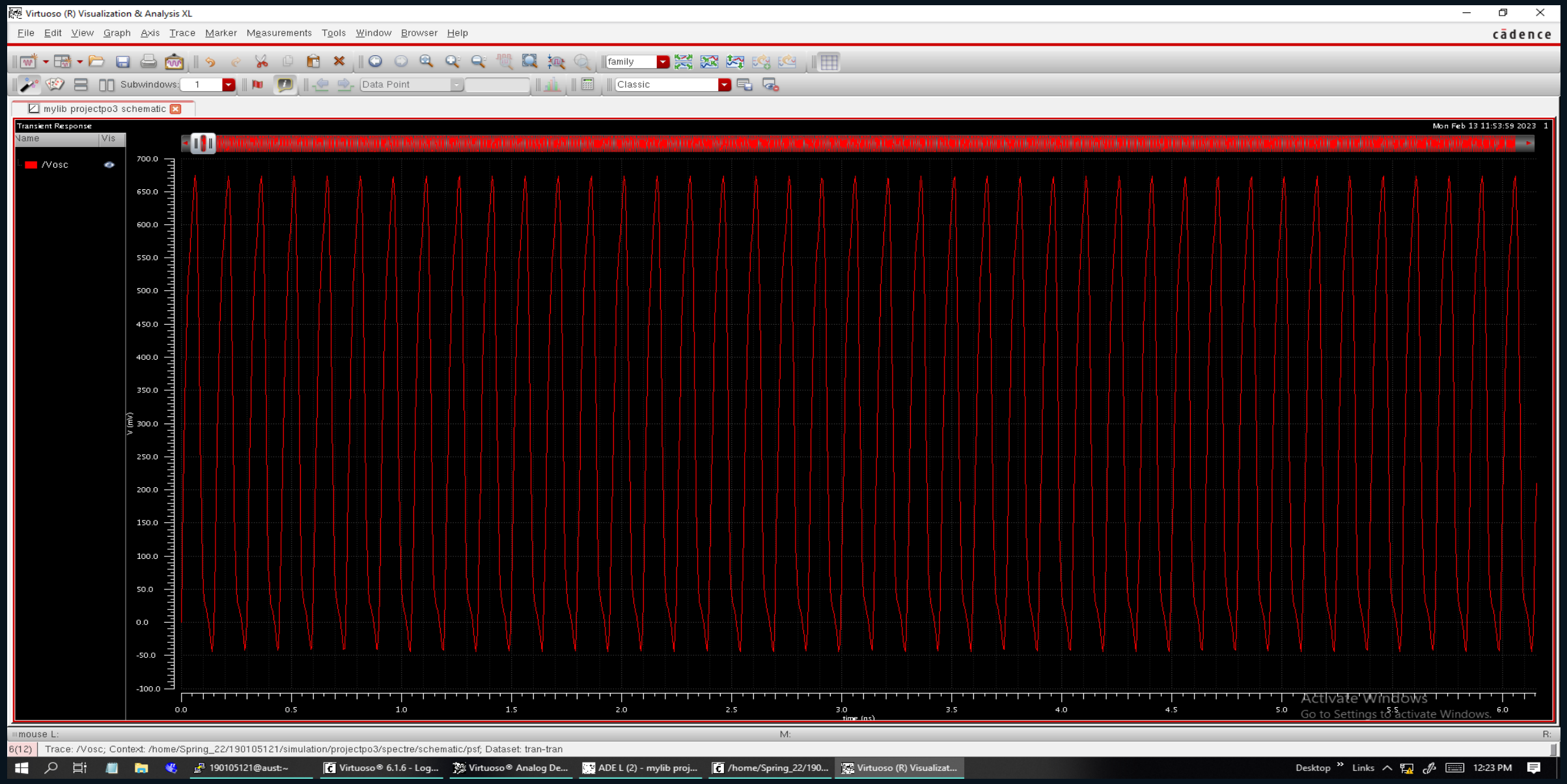
LVS Check


Virtuoso® Layout Suite XL Editing: project technique_raf layout
Launch File Edit View Create Verify Connectivity Options Tools Window Assura Optimize Place Floorplan Route Help
cadence
Navigator
Palette
Layers
Objects
vdd!
Vosc
Vctrl
gnd!
Run: "lvs1"
Run: "lvs1" from
/home/Spring_22/190105105/cic/
Schematic and Layout Match.
You currently have an open run (project).
Do you want to close current project and view the results of new run?
Summary of LVS Issues
Extraction Information:
0 cells have 0 mal-formed device problems
0 cells have 0 label short problems
0 cells have 0 label open problems
Comparison Information:
0 cells have 0 Net mismatches
0 cells have 0 Device mismatches
0 cells have 0 Pin mismatches
0 cells have 0 Parameter mismatches
ELW Information:
Total DRC violations: 0
Yes
No
Help
Activate Windows
Go to Settings to activate Windows.
Type here to search
ENG
INTL
11:25 AM
2/13/2023

Schematic and Layout Match Check



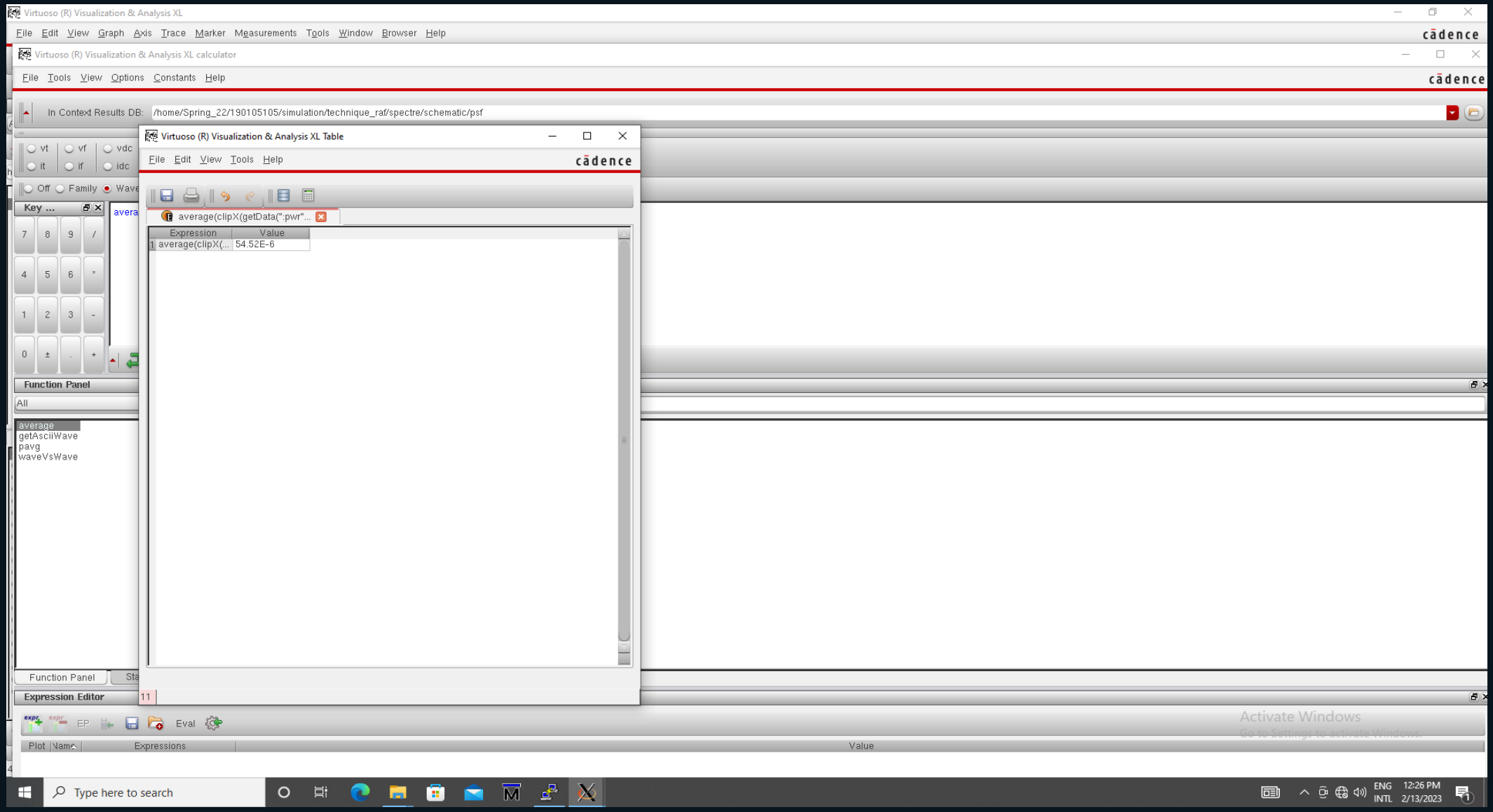
Oscillation Output Wave



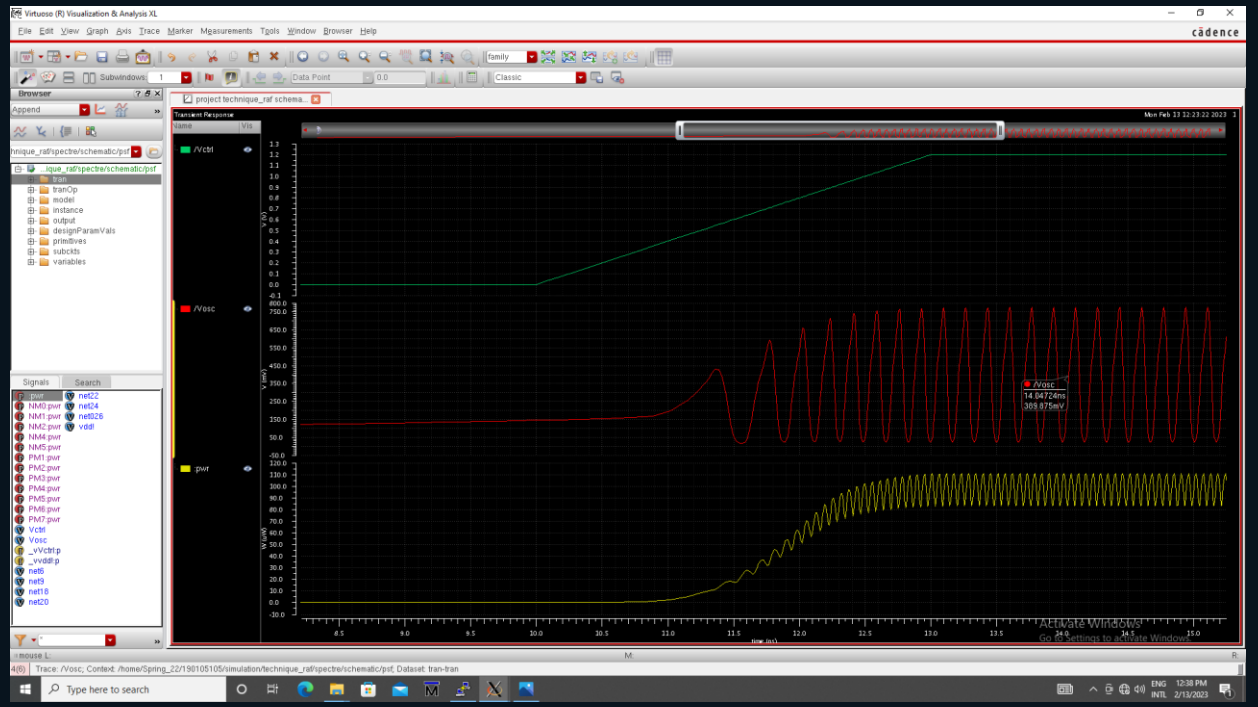
Waveform


Virtuoso (R) Visualization & Analysis XL
File Edit View Graph Axis Trace Marker Measurements Tools Window Browser Help
cadence
Browser
project technique_raf schema...
Transient Response
Mon Feb 13 12:23:22 2023
/Vctrl
/Vosc
:pwr
V (V)
V (mV)
W (uW)
time (ns)
Signals
Search
Activate Windows
Go to Settings to activate Windows.
Type here to search
ENG INTL
12:27 PM
2/13/2023

Average Power



Power Delay Product



Here we have, time period = (14.05-13.88)= 0.17n

So, $f = \frac{1}{n}$ = 588.2E6= 588MHz

We know the equation of Power Delay Product

$$PDP(\text{fJ}) = \frac{power(\text{nW})}{maximum\ frequency\ (\text{MHz})}$$

So, PDP= $\frac{52.2E-6}{588.2E6}$ = 89.2fj

Comparison Table

Method	Average Power	Maximum Frequency (MHz)	Power Delay Product (fj)	Cell Area	No. of Transistor
CSRO with only PMOS sources	54.5E-6	588	89.2	62.75	12