DESIGN OF AN OLD MOS 6502 CPU IN VERY LARGE-SCALE INTEGRATION SYSTEM

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***Abstract*- Microprocessor design and production have advanced significantly as a result of the computer industry's quick development. This article details a ground-breaking initiative to close the gap between traditional CPU design and cutting-edge Very Large-Scale Integration (VLSI) methods. This research shows how to construct and design a MOS 6502 CPU utilizing Cadence tools inside a VLSI architecture, focusing on the classic MOS 6502 CPU, a cornerstone of early computing. By employing Cadence tools, the MOS 6502's architecture is systematically translated into Register Transfer Level (RTL) designs, which are synthesized into gate-level representations. In-depth coverage of synthesis, place and route, and verification sheds light on how the RTL design is converted into physical gates and their ideal placement on the chip. Timing studies and functional simulations verify the effectiveness and accuracy of the design.**

BACKGROUND

A number of technical innovations have changed the landscape of contemporary computing, with the invention of the microprocessor serving as a turning point in the development of the field. Among these, the MOS 6502 CPU has a special position due to its ground-breaking architecture, which was essential in the development of personal computing. The MOS 6502, which debuted in the middle of the 1970s and powered enduring devices like the Commodore 64, Apple II, and Atari 2600, came to be identified with the microcomputing period. . The 6502 has a 16-bit address bus and an 8-bit little-endian CPU. The earliest versions had a die size of 3.9 mm x 4.3 mm (advertised as 153 mils x 168 mils), for a total area of 16.6 mm2, and were made using an 8 m process technology chip. [1]. The goal of this research is to bridge the gap between the early CPU era's simplicity and the present VLSI era's complexity. This research tries to combine the best of both worlds by trying to revive the MOS 6502 CPU within a VLSI architecture. The 6502-team had to create a digital design of instruction decoders, an arithmetic/logic unit (ALU), registers, and data paths (high-level register-centric design) that could be realized using individual gates made out of NMOS transistors and depletion loads (low-level circuit design) in order to reduce this to a working circuit design. The register structure and other components of the high-level architecture were worked out by Peddle, Orgill, Mathys, and Mensch, with Mathys converting a series of data transfers for each instruction into state diagrams and logic equations.[2] While Wil Mathys worked on other tasks, Mensch and Orgill finished converting the register-centric architecture from logic equations into a circuit schematic of the NMOS transistors and depletion loads (officially known as the "650X-C Microprocessor Logic Diagram"[3]).

METHODOLOGY

To dsign an old mos 6502 CPU, initially, create a directory file in the open terminal. Then from there, source the physical design. The edit file, input file, and io file were all produced after the source, as can be seen. Modify the code for the circuit connection with the pad by going to the input file after that. After it is finished, I will enter the synthesis file and modify the settings as necessary. Execute the genus next.Check the error after the genus has been successfully run; if it reveals a problem with the pad and circuit connection, go to the input file and repair it. Genus then takes off again. If it works, go to source synthesis. If there is a mistake, I will correct it; if not, I'll check the gui display to make sure the connection is good. Next, import the design into the encounter by going to the encounter. Then launch the MMMC browser and configure everything as needed. Save and leave when finished. You can then see where the pins are positioned in the encounter window. I now have to make a corner cell. To do that, I'll open the cpu_wpad.io file and make the necessary modifications. They will be connected to the circuit in the manner of VDD, VSS, VDDIOR, and VSSIOR. The floorplane is the next item. Go to floorplan, then choose a specific floorplan, and set core utilization to 0.4. I'll also set the core to 10, in addition to the core to left, the core to right, the core to top, and the core to bottom. After that, I'll plan my power. Metal 6 will be assigned to metals in the horizontal direction and Metal 5 to metals in the vertical direction. I'll make a unique design once it is finished. The circuit will thus be linked to utilizing a bespoke layer, which will connect VDD and VSS. Physical verification should happen right away. Here, I'll look at the DRC, LVS, ARC, and ERC. I will correct any infractions if I get any. Two different kinds of infractions are present here. These are violations of geometry and connection. The final SoC design will be revealed once everything has been resolved.

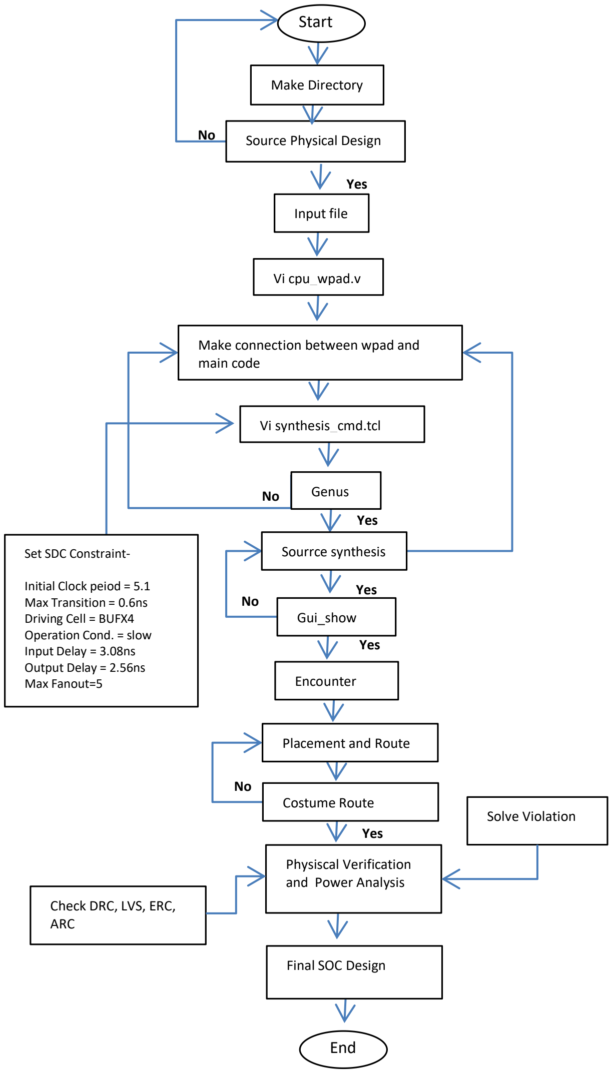


Fig. 1.The basic flow chart of design a SOC of old mos 6502 cpu.

RESULT ANALYSIS

TABLE. SOC results of Old mos 6502 CPU

Parameter Name	***Results***
Final Desnsity	101.12%
Total placed cells	1445
Remaining Violation	Connectivity (18 violation) Geometry (98 violation)
Gate Count	3184
Placement	32644
Area	3266.8 um^2

CONCLUSION

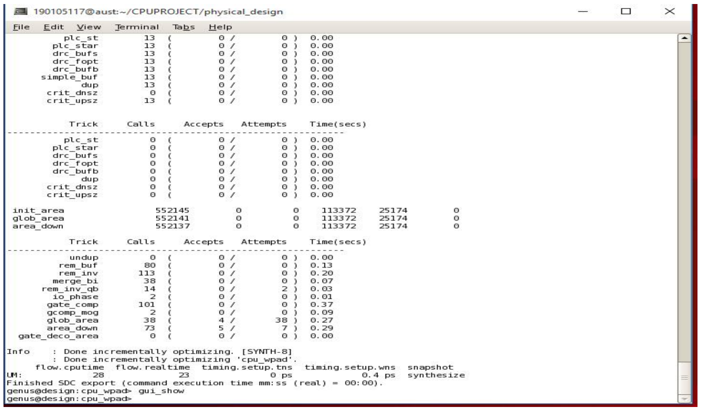
During physical design, we face a problem in the customer layer section. We can't connect the VDD and VSS to the circuit. We didn't face this type of issue previously. Then, when we login to another PC and do the same thing again, Then the problem is solved. Maybe it's a server issue. We face another problem in our encounter. After placement, we can't see the pin in the encounter window. Then, when we check the wpad code.I can see that the pin name PADDI is PADDI. I thought it was the pin name. Another surprising result I am facing is that when I was giving the repeat STA and verification command to take the screenshot, I got a DRC violation of 1000. Because the same things were overlapping. Otherwise, we didn't have any problems.

REFERENCES

[1] Wikipedia contributors, “MOS Technology 6502,” Wikipedia, Jul. 2023, [Online].Available:https://en.wikipedia.org/wiki/MOS_Technology_6502#:~:text=The%206502%20is%20a%20little,area%20of%2016.6%20mm2.

[2] Wil Mathys, A Little History Lesson, published on team6502.org, Jun 6 2022.

[3] Greg James, Barry Silverman, and Brian Silverman, 650X Schematic Notes, from their website visual6502.org, circa 2011.


190105117@aust:~/CPUPROJECT/physical_design
File Edit View Terminal Tabs Help

```
         plc_st        13  (          0 /         0 )  0.00
       plc_star        13  (          0 /         0 )  0.00
       drc_bufs        13  (          0 /         0 )  0.00
       drc_fopt        13  (          0 /         0 )  0.00
       drc_bufb        13  (          0 /         0 )  0.00
     simple_buf        13  (          0 /         0 )  0.00
            dup        13  (          0 /         0 )  0.00
      crit_dnsz         0  (          0 /         0 )  0.00
      crit_upsz        13  (          0 /         0 )  0.00


          Trick     Calls     Accepts   Attempts    Time(secs)
------------------------------------------------------------
         plc_st         0  (          0 /         0 )  0.00
       plc_star         0  (          0 /         0 )  0.00
       drc_bufs         0  (          0 /         0 )  0.00
       drc_fopt         0  (          0 /         0 )  0.00
       drc_bufb         0  (          0 /         0 )  0.00
            dup         0  (          0 /         0 )  0.00
      crit_dnsz         0  (          0 /         0 )  0.00
      crit_upsz         0  (          0 /         0 )  0.00

 init_area                 552145        0         0    113372    25174        0
 glob_area                 552141        0         0    113372    25174        0
 area_down                 552137        0         0    113372    25174        0

          Trick     Calls     Accepts   Attempts    Time(secs)
------------------------------------------------------------
          undup         0  (          0 /         0 )  0.00
        rem_buf        80  (          0 /         0 )  0.13
        rem_inv       113  (          0 /         0 )  0.20
       merge_bi        38  (          0 /         0 )  0.07
     rem_inv_qb        14  (          0 /         2 )  0.03
       io_phase         2  (          0 /         0 )  0.01
      gate_comp       101  (          0 /         0 )  0.37
      gcomp_mog         2  (          0 /         0 )  0.09
      glob_area        38  (          4 /        38 )  0.27
      area_down        73  (          5 /         7 )  0.29
 gate_deco_area         0  (          0 /         0 )  0.00

Info    : Done incrementally optimizing. [SYNTH-8]
        : Done incrementally optimizing 'cpu_wpad'.
     flow.cputime  flow.realtime  timing.setup.tns  timing.setup.wns  snapshot
UM:            28             23              0 ps            0.4 ps  synthesize
Finished SDC export (command execution time mm:ss (real) = 00:00).
genus@design:cpu_wpad> gui_show
genus@design:cpu_wpad>
```

Fig. 2. Synthesis Result

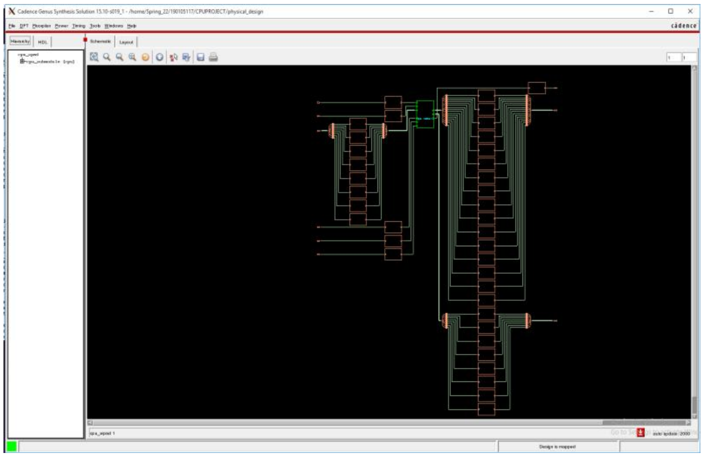
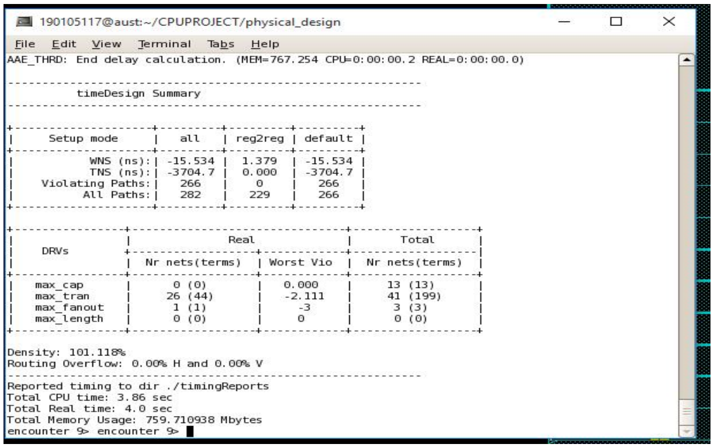
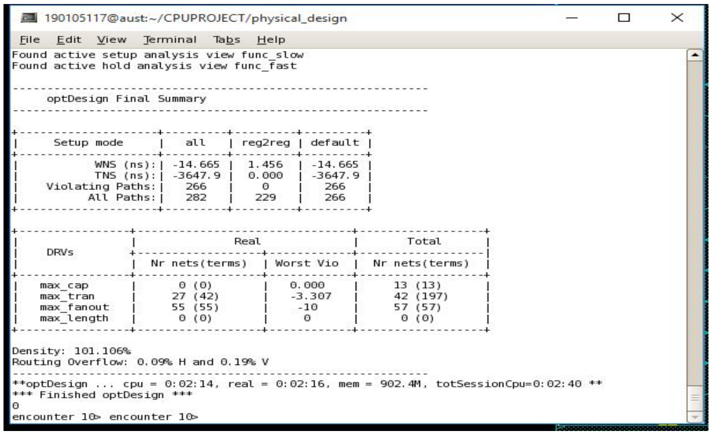

Cadence Genus Synthesis Solution 15.10-s019_1 - /home/Spring_22/190105117/CPUPROJECT/physical_design
File DFT Floorplan Power Timing Tools Windows Help
cadence
Hierarchy
HDL
Schematic
Layout
cpu_wpad
Design is mapped

Fig. 3. Synthesized Circuit


190105117@aust:~/CPUPROJECT/physical_design
File Edit View Terminal Tabs Help

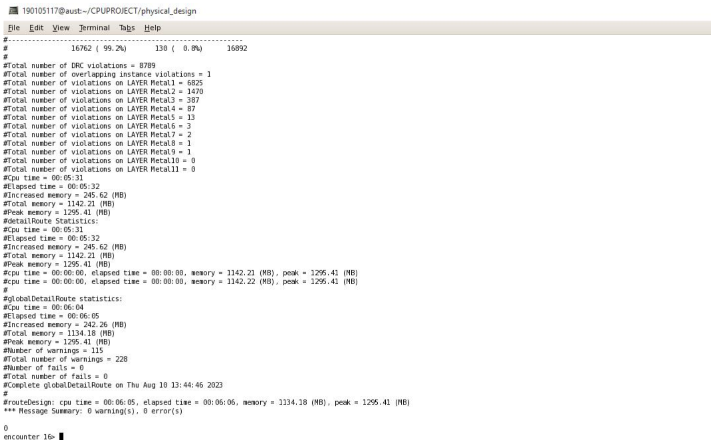
```
AAE_THRD: End delay calculation. (MEM=767.254 CPU=0:00:00.2 REAL=0:00:00.0)

------------------------------------------------------------
        timeDesign Summary
------------------------------------------------------------

+--------------------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):| -15.534 |  1.379  | -15.534 |
|           TNS (ns):| -3704.7 |  0.000  | -3704.7 |
|    Violating Paths:|   266   |    0    |   266   |
|          All Paths:|   282   |   229   |   266   |
+--------------------+---------+---------+---------+

+----------------+-------------------------------+------------------+
|                |              Real             |       Total      |
|    DRVs        +------------------+------------+------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)  |
+----------------+------------------+------------+------------------+
|   max_cap      |      0 (0)       |   0.000    |     13 (13)      |
|   max_tran     |     26 (44)      |   -2.111   |     41 (199)     |
|   max_fanout   |      1 (1)       |     -3     |      3 (3)       |
|   max_length   |      0 (0)       |     0      |      0 (0)       |
+----------------+------------------+------------+------------------+

Density: 101.118%
Routing Overflow: 0.00% H and 0.00% V
------------------------------------------------------------
Reported timing to dir ./timingReports
Total CPU time: 3.86 sec
Total Real time: 4.0 sec
Total Memory Usage: 759.710938 Mbytes
encounter 9> encounter 9>
```

Fig. 4.Time Design_preCTS


190105117@aust:~/CPUPROJECT/physical_design
File Edit View Terminal Tabs Help

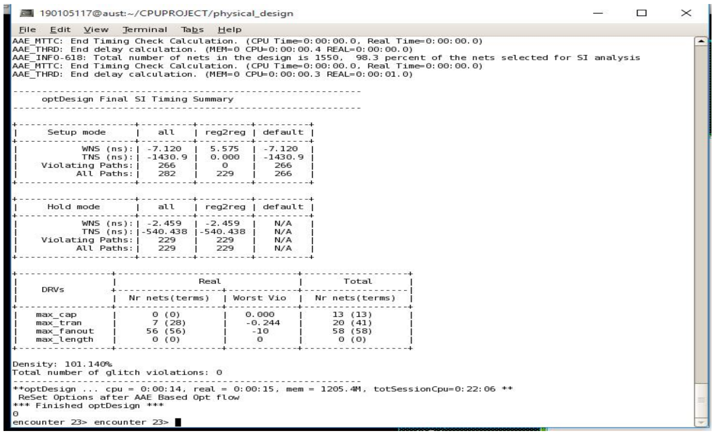
```
Found active setup analysis view func_slow
Found active hold analysis view func_fast

------------------------------------------------------------
     optDesign Final Summary
------------------------------------------------------------

+--------------------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):| -14.665 |  1.456  | -14.665 |
|           TNS (ns):| -3647.9 |  0.000  | -3647.9 |
|    Violating Paths:|   266   |    0    |   266   |
|          All Paths:|   282   |   229   |   266   |
+--------------------+---------+---------+---------+

+----------------+-------------------------------+------------------+
|                |              Real             |       Total      |
|    DRVs        +------------------+------------+------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)  |
+----------------+------------------+------------+------------------+
|   max_cap      |      0 (0)       |   0.000    |     13 (13)      |
|   max_tran     |     27 (42)      |   -3.307   |     42 (197)     |
|   max_fanout   |     55 (55)      |    -10     |     57 (57)      |
|   max_length   |      0 (0)       |     0      |      0 (0)       |
+----------------+------------------+------------+------------------+

Density: 101.106%
Routing Overflow: 0.09% H and 0.19% V
------------------------------------------------------------
**optDesign ... cpu = 0:02:14, real = 0:02:16, mem = 902.4M, totSessionCpu=0:02:40 **
*** Finished optDesign ***
0
encounter 10> encounter 10>
```

Fig.5.Opt Design_preCTS


190105117@aust:~/CPUPROJECT/physical_design
File Edit View Terminal Tabs Help

```
#------------------------------------------------------------
#               16762 ( 99.2%)       130 (  0.8%)       16892
#
#Total number of DRC violations = 8789
#Total number of overlapping instance violations = 1
#Total number of violations on LAYER Metal1 = 6825
#Total number of violations on LAYER Metal2 = 1470
#Total number of violations on LAYER Metal3 = 387
#Total number of violations on LAYER Metal4 = 87
#Total number of violations on LAYER Metal5 = 13
#Total number of violations on LAYER Metal6 = 3
#Total number of violations on LAYER Metal7 = 2
#Total number of violations on LAYER Metal8 = 1
#Total number of violations on LAYER Metal9 = 1
#Total number of violations on LAYER Metal10 = 0
#Total number of violations on LAYER Metal11 = 0
#Cpu time = 00:05:31
#Elapsed time = 00:05:32
#Increased memory = 245.62 (MB)
#Total memory = 1142.21 (MB)
#Peak memory = 1295.41 (MB)
#detailRoute Statistics:
#Cpu time = 00:05:31
#Elapsed time = 00:05:32
#Increased memory = 245.62 (MB)
#Total memory = 1142.21 (MB)
#Peak memory = 1295.41 (MB)
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 1142.21 (MB), peak = 1295.41 (MB)
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 1142.22 (MB), peak = 1295.41 (MB)
#
#globalDetailRoute statistics:
#Cpu time = 00:06:04
#Elapsed time = 00:06:05
#Increased memory = 242.26 (MB)
#Total memory = 1134.18 (MB)
#Peak memory = 1295.41 (MB)
#Number of warnings = 115
#Total number of warnings = 228
#Number of fails = 0
#Total number of fails = 0
#Complete globalDetailRoute on Thu Aug 10 13:44:46 2023
#
#routeDesign: cpu time = 00:06:05, elapsed time = 00:06:06, memory = 1134.18 (MB), peak = 1295.41 (MB)
*** Message Summary: 0 warning(s), 0 error(s)

0
encounter 16>
```

Fig.6.Route Design


190105117@aust:~/CPUPROJECT/physical_design
File Edit View Terminal Tabs Help

```
AAE_MTTC: End Timing Check Calculation. (CPU Time=0:00:00.0, Real Time=0:00:00.0)
AAE_THRD: End delay calculation. (MEM=0 CPU=0:00:00.4 REAL=0:00:00.0)
AAE_INFO-618: Total number of nets in the design is 1550,  98.3 percent of the nets selected for SI analysis
AAE_MTTC: End Timing Check Calculation. (CPU Time=0:00:00.0, Real Time=0:00:00.0)
AAE_THRD: End delay calculation. (MEM=0 CPU=0:00:00.3 REAL=0:00:01.0)

------------------------------------------------------------
     optDesign Final SI Timing Summary
------------------------------------------------------------

+--------------------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):| -7.120  |  5.575  | -7.120  |
|           TNS (ns):| -1430.9 |  0.000  | -1430.9 |
|    Violating Paths:|   266   |    0    |   266   |
|          All Paths:|   282   |   229   |   266   |
+--------------------+---------+---------+---------+

+--------------------+---------+---------+---------+
|     Hold mode      |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):| -2.459  | -2.459  |   N/A   |
|           TNS (ns):|-540.438 |-540.438 |   N/A   |
|    Violating Paths:|   229   |   229   |   N/A   |
|          All Paths:|   229   |   229   |   N/A   |
+--------------------+---------+---------+---------+

+----------------+-------------------------------+------------------+
|                |              Real             |       Total      |
|    DRVs        +------------------+------------+------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)  |
+----------------+------------------+------------+------------------+
|   max_cap      |      0 (0)       |   0.000    |     13 (13)      |
|   max_tran     |      7 (28)      |   -0.244   |     20 (41)      |
|   max_fanout   |     56 (56)      |    -10     |     58 (58)      |
|   max_length   |      0 (0)       |     0      |      0 (0)       |
+----------------+------------------+------------+------------------+

Density: 101.140%
Total number of glitch violations: 0
------------------------------------------------------------
**optDesign ... cpu = 0:00:14, real = 0:00:15, mem = 1205.4M, totSessionCpu=0:22:06 **
 ReSet Options after AAE Based Opt flow
*** Finished optDesign ***
0
encounter 23> encounter 23>
```

Fig.7.optDesign postRoute hold

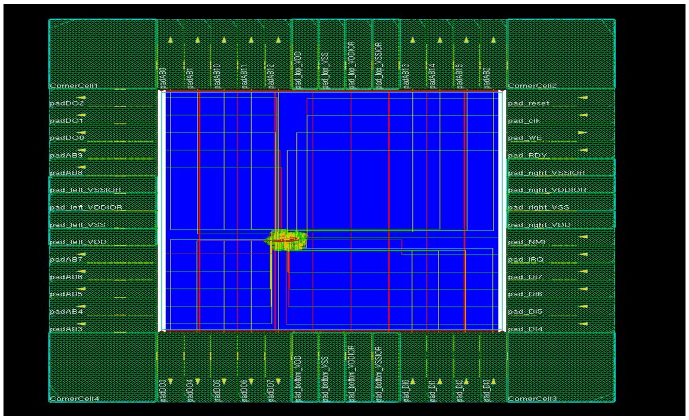
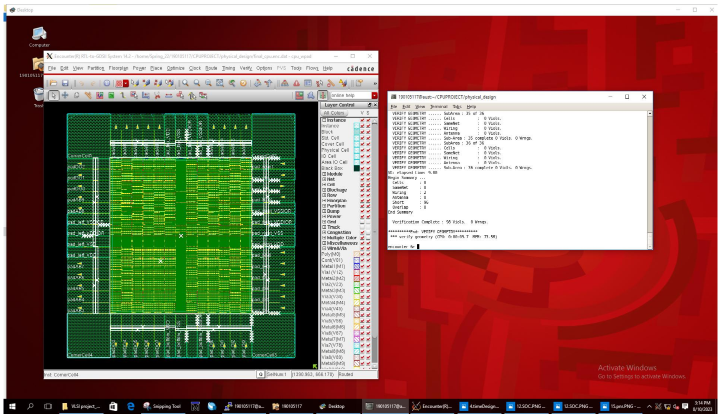


Fig.8.PnR before Routing



190105117@aust:~/CPUPROJECT/physical_design

```
  VERIFY GEOMETRY ...... SubArea : 35 of 36
  VERIFY GEOMETRY ...... Cells          :  0 Viols.
  VERIFY GEOMETRY ...... SameNet        :  0 Viols.
  VERIFY GEOMETRY ...... Wiring         :  0 Viols.
  VERIFY GEOMETRY ...... Antenna        :  0 Viols.
  VERIFY GEOMETRY ...... Sub-Area : 35 complete 0 Viols. 0 Wrngs.
  VERIFY GEOMETRY ...... SubArea : 36 of 36
  VERIFY GEOMETRY ...... Cells          :  0 Viols.
  VERIFY GEOMETRY ...... SameNet        :  0 Viols.
  VERIFY GEOMETRY ...... Wiring         :  0 Viols.
  VERIFY GEOMETRY ...... Antenna        :  0 Viols.
  VERIFY GEOMETRY ...... Sub-Area : 36 complete 0 Viols. 0 Wrngs.
VG: elapsed time: 9.00
Begin Summary ...
  Cells       : 0
  SameNet     : 0
  Wiring      : 2
  Antenna     : 0
  Short       : 96
  Overlap     : 0
End Summary

  Verification Complete : 98 Viols.  0 Wrngs.

**********End: VERIFY GEOMETRY**********
 *** verify geometry (CPU: 0:00:09.7  MEM: 73.5M)

encounter 6>
```

Fig.12. Verify Geometry

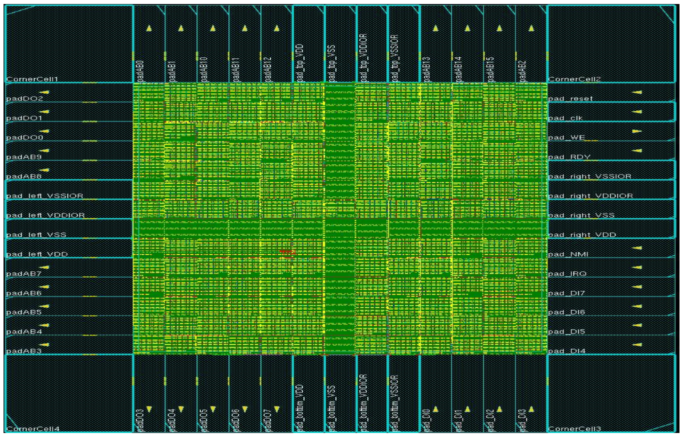
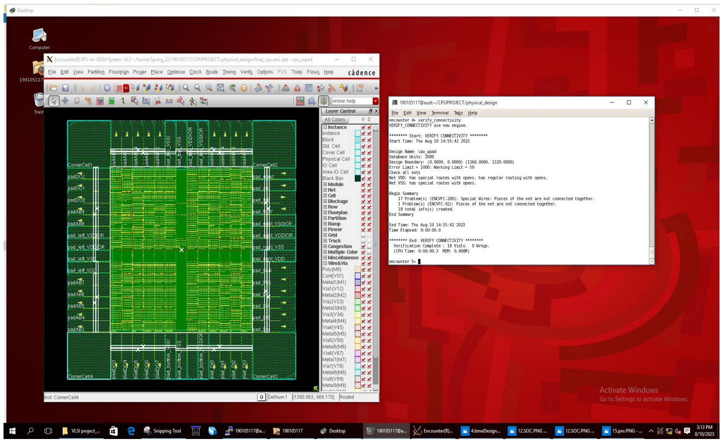


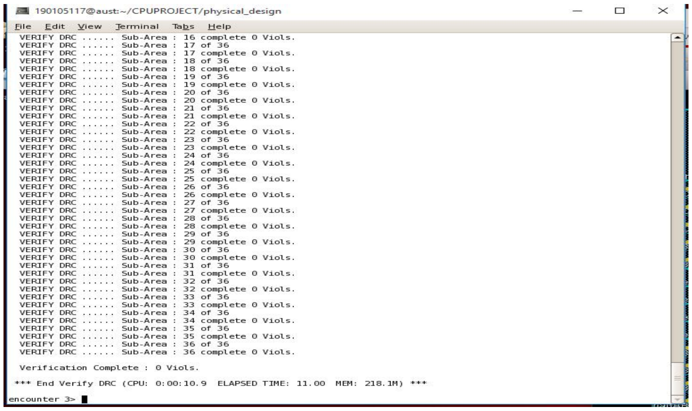
Fig.9.PnR after Routing



190105117@aust:~/CPUPROJECT/physical_design

```
encounter 4> verify_connectivity
VERIFY_CONNECTIVITY use new engine.

******** Start: VERIFY CONNECTIVITY ********
Start Time: Thu Aug 10 14:55:42 2023

Design Name: cpu_wpad
Database Units: 2000
Design Boundary: (0.0000, 0.0000) (1260.0000, 1320.0000)
Error Limit = 1000; Warning Limit = 50
Check all nets
Net VDD: has special routes with opens, has regular routing with opens.
Net VSS: has special routes with opens.

Begin Summary
    17 Problem(s) (ENCVFC-200): Special Wires: Pieces of the net are not connected together.
    1 Problem(s) (ENCVFC-92): Pieces of the net are not connected together.
    18 total info(s) created.
End Summary

End Time: Thu Aug 10 14:55:42 2023
Time Elapsed: 0:00:00.0

******** End: VERIFY CONNECTIVITY ********
  Verification Complete : 18 Viols.  0 Wrngs.
  (CPU Time: 0:00:00.3  MEM: 0.000M)

encounter 5>
```

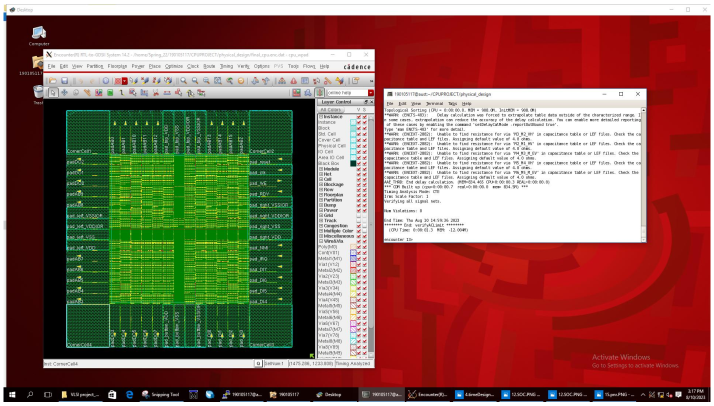
Fig.13.Verify Connectivity



190105117@aust:~/CPUPROJECT/physical_design

```
 VERIFY DRC ...... Sub-Area : 16 complete 0 Viols.
 VERIFY DRC ...... Sub-Area : 17 of 36
 VERIFY DRC ...... Sub-Area : 17 complete 0 Viols.
 VERIFY DRC ...... Sub-Area : 18 of 36
 VERIFY DRC ...... Sub-Area : 18 complete 0 Viols.
 VERIFY DRC ...... Sub-Area : 19 of 36
 VERIFY DRC ...... Sub-Area : 19 complete 0 Viols.
 VERIFY DRC ...... Sub-Area : 20 of 36
 VERIFY DRC ...... Sub-Area : 20 complete 0 Viols.
 VERIFY DRC ...... Sub-Area : 21 of 36
 VERIFY DRC ...... Sub-Area : 21 complete 0 Viols.
 VERIFY DRC ...... Sub-Area : 22 of 36
 VERIFY DRC ...... Sub-Area : 22 complete 0 Viols.
 VERIFY DRC ...... Sub-Area : 23 of 36
 VERIFY DRC ...... Sub-Area : 23 complete 0 Viols.
 VERIFY DRC ...... Sub-Area : 24 of 36
 VERIFY DRC ...... Sub-Area : 24 complete 0 Viols.
 VERIFY DRC ...... Sub-Area : 25 of 36
 VERIFY DRC ...... Sub-Area : 25 complete 0 Viols.
 VERIFY DRC ...... Sub-Area : 26 of 36
 VERIFY DRC ...... Sub-Area : 26 complete 0 Viols.
 VERIFY DRC ...... Sub-Area : 27 of 36
 VERIFY DRC ...... Sub-Area : 27 complete 0 Viols.
 VERIFY DRC ...... Sub-Area : 28 of 36
 VERIFY DRC ...... Sub-Area : 28 complete 0 Viols.
 VERIFY DRC ...... Sub-Area : 29 of 36
 VERIFY DRC ...... Sub-Area : 29 complete 0 Viols.
 VERIFY DRC ...... Sub-Area : 30 of 36
 VERIFY DRC ...... Sub-Area : 30 complete 0 Viols.
 VERIFY DRC ...... Sub-Area : 31 of 36
 VERIFY DRC ...... Sub-Area : 31 complete 0 Viols.
 VERIFY DRC ...... Sub-Area : 32 of 36
 VERIFY DRC ...... Sub-Area : 32 complete 0 Viols.
 VERIFY DRC ...... Sub-Area : 33 of 36
 VERIFY DRC ...... Sub-Area : 33 complete 0 Viols.
 VERIFY DRC ...... Sub-Area : 34 of 36
 VERIFY DRC ...... Sub-Area : 34 complete 0 Viols.
 VERIFY DRC ...... Sub-Area : 35 of 36
 VERIFY DRC ...... Sub-Area : 35 complete 0 Viols.
 VERIFY DRC ...... Sub-Area : 36 of 36
 VERIFY DRC ...... Sub-Area : 36 complete 0 Viols.

 Verification Complete : 0 Viols.

*** End Verify DRC (CPU: 0:00:10.9  ELAPSED TIME: 11.00  MEM: 218.1M) ***

encounter 3>
```

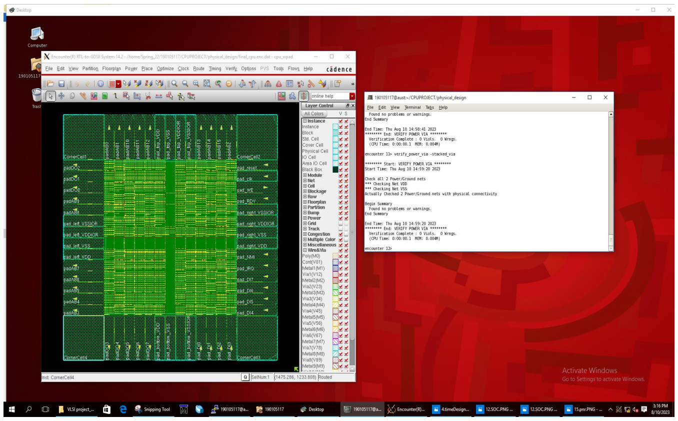
Fig.10.DRC verification



190105117@aust:~/CPUPROJECT/physical_design

```
Topological Sorting (CPU = 0:00:00.0, MEM = 908.0M, InitMEM = 908.0M)
**WARN: (ENCTS-403):    Delay calculation was forced to extrapolate table data outside of the characterized range. I
n some cases, extrapolation can reduce the accuracy of the delay calculation. You can enable more detailed reporting
 of these cases by enabling the command 'setDelayCalMode -reportOutBound true'.
Type 'man ENCTS-403' for more detail.
**WARN: (ENCEXT-2882):  Unable to find resistance for via 'M3_M2_VH' in capacitance table or LEF files. Check the ca
pacitance table and LEF files. Assigning default value of 4.0 ohms.
**WARN: (ENCEXT-2882):  Unable to find resistance for via 'M2_M1_HV' in capacitance table or LEF files. Check the ca
pacitance table and LEF files. Assigning default value of 4.0 ohms.
**WARN: (ENCEXT-2882):  Unable to find resistance for via 'M4_M3_M_EV' in capacitance table or LEF files. Check the
capacitance table and LEF files. Assigning default value of 4.0 ohms.
**WARN: (ENCEXT-2882):  Unable to find resistance for via 'M5_M4_VH' in capacitance table or LEF files. Check the ca
pacitance table and LEF files. Assigning default value of 4.0 ohms.
**WARN: (ENCEXT-2882):  Unable to find resistance for via 'M6_M5_M_EV' in capacitance table or LEF files. Check the
capacitance table and LEF files. Assigning default value of 4.0 ohms.
AAE_THRD: End delay calculation. (MEM=834.465 CPU=0:00:00.3 REAL=0:00:00.0)
*** CDM Built up (cpu=0:00:00.7  real=0:00:00.0  mem= 834.5M) ***
Timing Analysis Mode: CTE
Irms Scale Factor: 1
Verifying all signal nets.

Num Violations: 0

End Time: Thu Aug 10 14:59:36 2023
******** End: verifyACLimit ********
  (CPU Time: 0:00:01.3  MEM: -12.004M)

encounter 13>
```

Fig.14.Verify AC limit



190105117@aust:~/CPUPROJECT/physical_design

```
  Found no problems or warnings.
End Summary

End Time: Thu Aug 10 14:58:41 2023
******** End: VERIFY POWER VIA ********
  Verification Complete : 0 Viols.  0 Wrngs.
  (CPU Time: 0:00:00.1  MEM: 0.004M)

encounter 11> verify_power_via -stacked_via

******** Start: VERIFY POWER VIA ********
Start Time: Thu Aug 10 14:59:20 2023

Check all 2 Power/Ground nets
*** Checking Net VDD
*** Checking Net VSS
Actually Checked 2 Power/Ground nets with physical connectivity

Begin Summary
  Found no problems or warnings.
End Summary

End Time: Thu Aug 10 14:59:20 2023
******** End: VERIFY POWER VIA ********
  Verification Complete : 0 Viols.  0 Wrngs.
  (CPU Time: 0:00:00.1  MEM: 0.004M)

encounter 12>
```

Fig.11.Verify power via shacked via

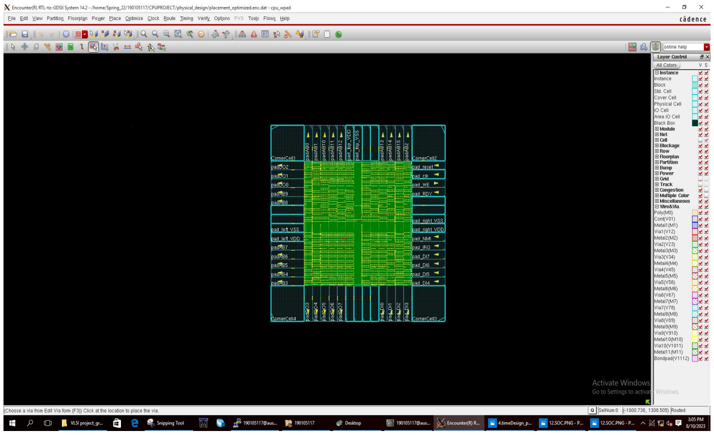


Fig.15.Final SOC of old mos 6502 cpu