Soc Design Laboratory – Lab3

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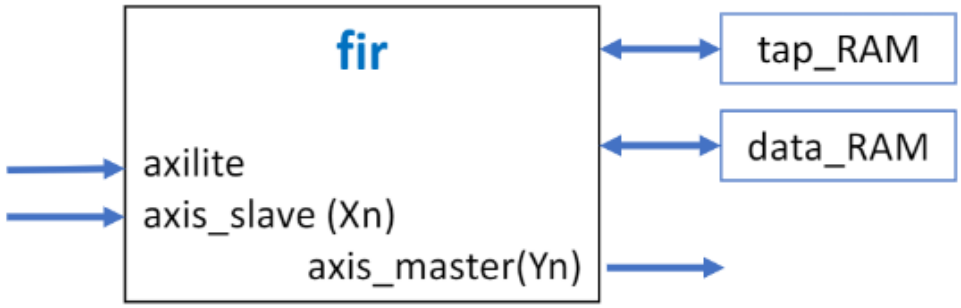
• Introduction

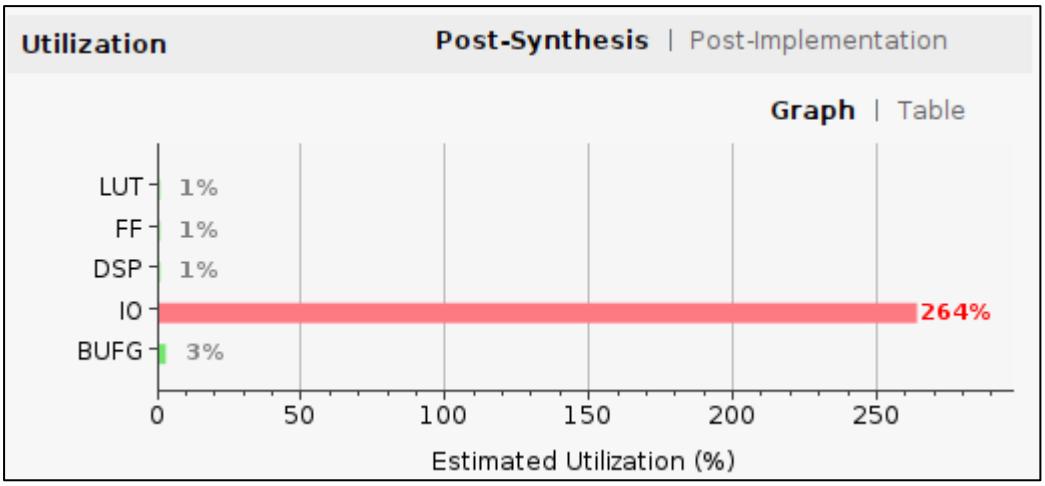
此次實驗是使用 Verilog 設計 Finite-Impulse-Response IP，再根據 BUS 將設計好的硬體 IP 做 Wrapper，最後在 Xsim 進行模擬，驗證自行設計的 IP 功能是否正確。

除了 FIR IP 設計也有應用不同 BUS(axi-lite、axi-stream) 進行 dataflow 的優化，提升整體系統的效能。

• Block diagram



- **Resource usage**

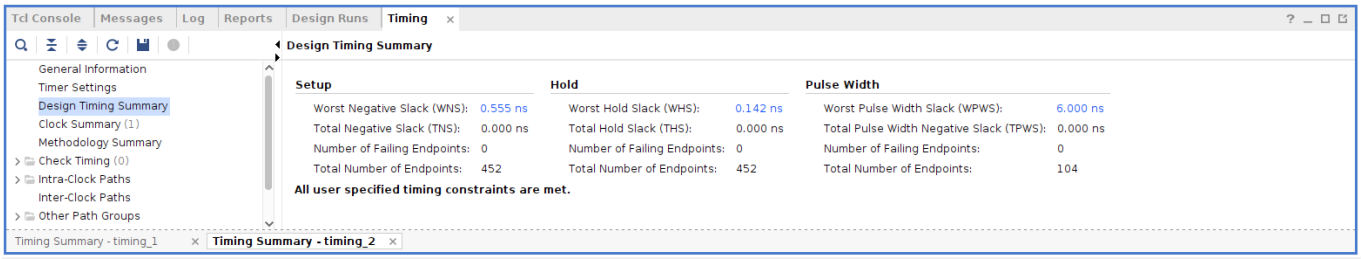


Utilization — **Post-Synthesis** | Post-Implementation

Graph | **Table**

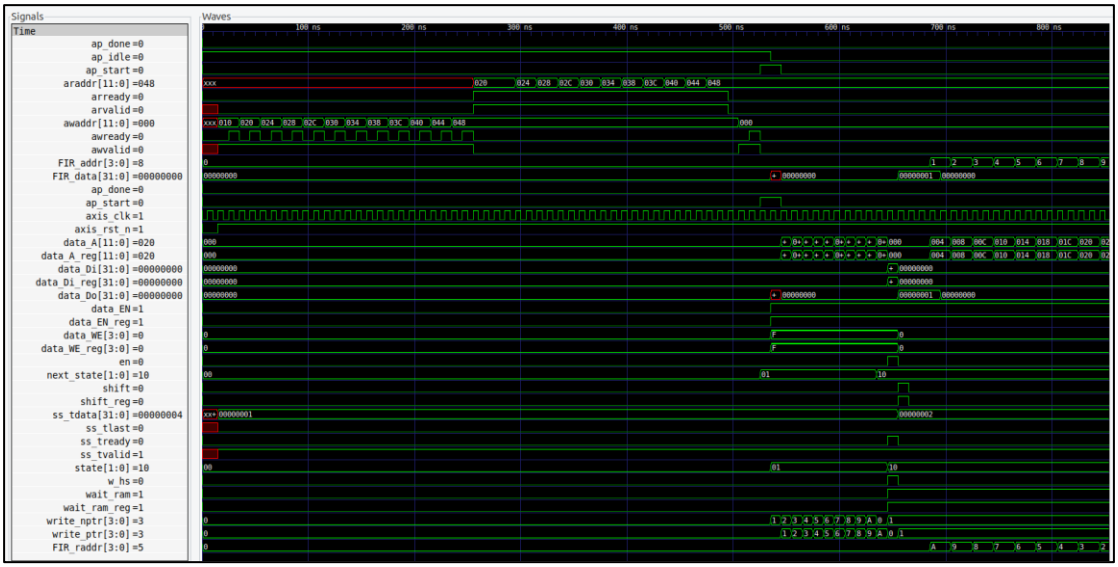
Resource	Estimation	Available	Utilization %
LUT	251	53200	0.47
FF	103	106400	0.10
DSP	3	220	1.36
IO	330	125	264.00
BUFG	1	32	3.13

- **Timing Report**



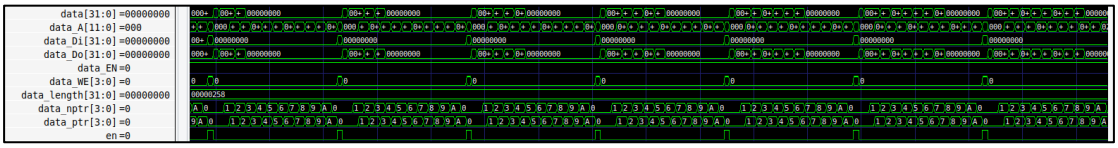
- **Simulation waveform**

Coefficient program and read back



Data stream-in and stream-out

RAM access control



- **FSM**