Memory Hierarchy Simulator

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Brief Explanation:

The code takes some inputs form the user: *the address length, memory access time , cache line size, cache size and cache access time*. From this data, we can get the size of the cache and the size of the line in cache or block of data in memory.

The addresses are inputted to the system through a file. The file is randomly generated but with the same values each run. The file has 10 addresses.

The cache is built through a list of dictionaries. Each dictionary has 3 keys: (index, valid, data).
For each address, the address will be split into ***Tag, Line index, offset (displacement)*** and the tag and index will be used to access the cache. A simple comparison is then handled to see if the data is valid and if the tags match. If this is the case, it is a *cache hit, otherwise is a miss.* In the case of a miss, the cache gets updated. The update affects two keys in the dictionary, first the validity bit and second the tag.

Decisions/Assumptions:
We did not need to implement an actual memory since we thought we needed to update the cache upon different requests and the validity of the actual data will be easily maintained by copying the block of data from memory to cache.

Bugs/Issues:

User Guide:

Screenshots:

List of programs: