**Quadrant Readout Map (m-column \* n-row pixels)**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1 | 5 | 9 |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 10 | 6 | 2 |
| 2m+1 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 3 | 7 | 11 |  |  |  |  |  |  |  | 2m |  |  |  |  |  |  | 12 | 8 | 4 |

The numbers represent the order of pixel readout.

**CMOS CDS readout order (m-column \* n-row pixels)**

Generally, in CDS readout, it is read row-by-row. After one row is read, there is a reset for every pixel in that row. Then the reset level is read for every pixel in that row. This reset level would be used to be subtracted from the next frame.

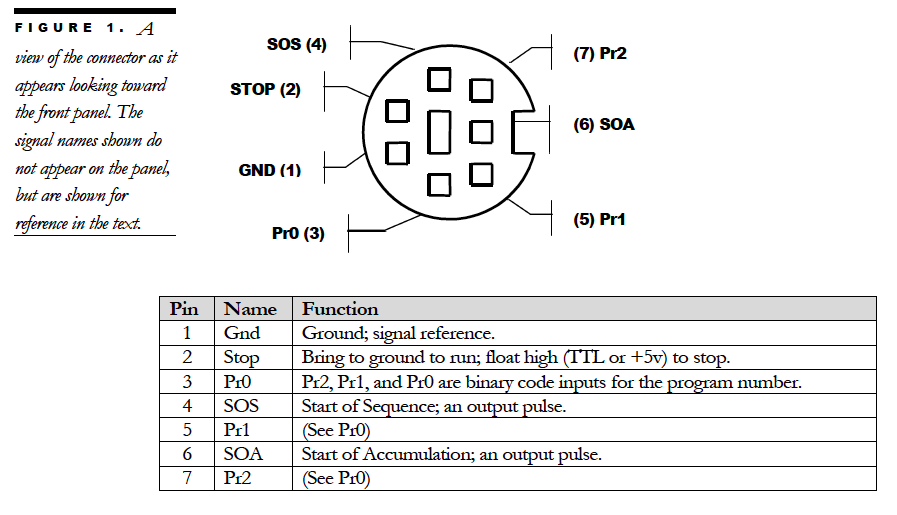
In quadrant CMOS chip as DM46 (128X), the top and bottom rows are read out as one row before reset. Therefore, before de-interleaving, the quadrant CDS readout order is as below.

|  |  |
| --- | --- |
| Photons from top and bottom rows  Frame 1 – interlaced (2\*m pixels) | Resets from top and bottom rows  Frame 2 – interlaced (2\*m pixels) |
|  |  |
|  |  |
|  |  |
|  |  |
|  |  |
|  |  |
|  |  |
|  |  |
| Photons from middle 2 rows  Frame 1 – interlaced (2\*m pixels) | Resets from top and bottom rows  Frame 2 – interlaced (2\*m pixels) |

n/2

\*\*\*The relevant coding is in quadrant\_c\_code.rtf

**Triggers**

****

B > C

Internal Integration

Time

Actual Integration

Time

A > B

Trigger

B = 1/sm\_cam\_lib\_rates (msec)

C

1. “@TXC 1” command sets the camera to frame-by-frame trigger mode via STOP pin (Black BNC). High to Stop and low to go. “@TXC 0” to turn it off.

Please note that the beginning of first acquired frame is not locked by the Frame Valid Trigger.

B

Internal Integration

Time

Frame Valid Trigger

B = 1/sm\_cam\_lib\_rates (msec)

This trigger pulse should be longer total number of frames to be acquired. Camera runs on its internal rate. But only after trigger pulse (from Yellow BNC) goes up, the frame grabber begins to acquire until the set number of frames are collected.

2. “@FVI 0002” command sets the frame-grabber (Yellow BNC) to trigger mode. Low to Stop and high to go. “@FVI 0000” to turn it off.