CSCI 2500 — Computer Organization
Homework 07 (document version 1.0) — Due December 7, 2021
More Circuits

- This homework is due by the midnight EST on the above date via a Submitty gradeable.
- This homework is to be completed **individually**. Do not share your code with anyone else.
- Plan to start each homework early. You can ask questions during office hours, in the Submitty forum, and during your lab session.
- You **must** use C for this homework assignment, and your code **must** successfully execute on Submitty to receive credit.

1 Implementing a Carry Lookahead Adder and Divider

This assignment will be an extension of Lab 5 and Lab 6. You will implement a divider and replace your 32-bit ripple carry adder with a 16-bit carry lookahead adder. The input OP bits are given below (modified from Lab 5 and Lab 6).

Instruction	Input symbol	OP bits	Operation
add	+	011	Integer addition
div	/	111	Integer division

See slides in the last section of `csci2500-f21-ch03b-slides.pdf` (starting from slide "Improving Our ALU") for implementation details on a 4x4 16-bit carry lookahead adder and slide "Division Hardware" for the logic of a divider. Optionally, you may implement the divider according to the slide "Optimized Divider" instead of the one shown in the slide "Division Hardware". You may assume that the maximum inputs for the divider can fit in 16 bits. You only need to return the quotient.

1.1 Assignment Rules

The "rules" will be the same as with Lab 5 and Lab 6. Your implementation should be directly representative of a circuit.

2 Submission and Grading Criteria

For this assignment, you will submit your code to the Submitty gradeable. No credit will be given if a ripple carry adder is used.

1. Autograding: 40%
   - Standard visible and hidden test cases
2. TA grading: 60%
   - Solution is representative of an implementable circuit
   - Solution otherwise adheres to the Lab 5 and Lab 6 rules