

tb_cocotb.v

AUTHORS

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DATES

2025/03/26

INFORMATION

Brief

Test bench wrapper for cocotb

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tb_cocotb

```
module tb_cocotb #(
    parameter
        integer
        ADDRESS_WIDTH
        =
        32,
    parameter
        integer
        BUS_WIDTH
        =
        4,
    parameter
        [ADDRESS_WIDTH-1:0]
        SLAVE_ADDRESS
```

```
=  
32'h44A20000,  
parameter  
    [ADDRESS_WIDTH-1:0]  
SLAVE_REGION  
=  
32'h0000FFFF  
)  
  
output  
wire  
connected,  
input  
wire  
aclk,  
input  
wire  
arstn,  
input  
wire  
[ADDRESS_WIDTH-1:0]  
s_axi_awaddr,  
input  
wire  
[2:0]  
s_axi_awprot,  
input  
wire  
s_axi_awvalid,  
output  
wire  
s_axi_awready,  
input  
wire  
[BUS_WIDTH*8-1:0]  
s_axi_wdata,  
input  
wire  
[BUS_WIDTH-1:0]  
s_axi_wstrb,  
input  
wire  
s_axi_wvalid,  
output  
wire  
s_axi_wready,  
output  
wire  
[1:0]  
s_axi_bresp,  
output  
wire  
s_axi_bvalid,  
input  
wire  
s_axi_bready,  
output  
wire  
[ADDRESS_WIDTH-1:0]  
m_axi_awaddr,  
output  
wire  
[2:0]  
m_axi_awprot,  
output  
wire
```

```

m_axi_awvalid,
input
wire
m_axi_awready,
output
wire
[BUS_WIDTH*8-1:0]
m_axi_wdata,
output
wire
[BUS_WIDTH-1:0]
m_axi_wstrb,
output
wire
m_axi_wvalid,
input
wire
m_axi_wready,
input
wire
[1:0]
m_axi_bresp,
input
wire
m_axi_bvalid,
output
wire
m_axi_bready,
input
wire
[ADDRESS_WIDTH-1:0]
s_axi_araddr,
input
wire
[2:0]
s_axi_arprot,
input
wire
s_axi_arvalid,
output
wire
s_axi_arready,
output
wire
[BUS_WIDTH*8-1:0]
s_axi_rdata,
output
wire
[1:0]
s_axi_rresp,
output
wire
s_axi_rvalid,
input
wire
s_axi_rready,
output
wire
[ADDRESS_WIDTH-1:0]
m_axi_araddr,
output
wire
[2:0]
m_axi_arprot,
output
wire

```

```

    m_axi_arvalid,
    input
    wire
    m_axi_arready,
    input
    wire
        [BUS_WIDTH*8-1:0]
    m_axi_rdata,
    input
    wire
        [1:0]
    m_axi_rresp,
    input
    wire
    m_axi_rvalid,
    output
    wire
    m_axi_rready
)

```

Parameters

ADDRESS_WIDTH	Width of the AXI LITE address port in bits.
parameter integer	
BUS_WIDTH	Width of the AXI LITE bus data port in bytes.
parameter integer	
DATA_BUFFER	Buffer data channel, 0 to disable.
TIMEOUT_BEATS	Number of clock cycles (beats) to count till timeout. 0 disables timeout.
SLAVE_ADDRESS	Array of Addresses for each slave (0 = slave 0 and so on).
parameter [ADDRESS_WIDTH- 1:0]	
SLAVE_REGION	Region for the address that is valid for the SLAVE ADDRESS.
parameter [ADDRESS_WIDTH- 1:0]	

Ports

connected	Core has established channel connection
output wire	
aclk	Input clock
input wire	
arstn	Input negative reset
input wire	
s_axi_awaddr	Slave write input channel address
input wire [ADDRESS_WIDTH- 1:0]	
s_axi_awprot	Slave write input channel protection mode
input wire [2:0]	
s_axi_awvalid	Slave write input channel address is valid.
input wire	
s_axi_awready	Slave write input channel is ready.
output wire	
s_axi_wdata	Slave write input channel data
input wire [BUS_WIDTH* 8- 1:0]	
s_axi_wstrb	Slave write input channel valid bytes
input wire [BUS_WIDTH- 1:0]	
s_axi_wvalid	Slave write input channel data valid
input wire	
s_axi_wready	Slave write input channel is ready.
output wire	

s_axi_bresp	Slave write input channel response to write(s).
s_axi_bvalid	Slave write input channel response valid.
s_axi_bready	Slave write input channel response ready.
m_axi_awaddr	Master write output channel address.
m_axi_awprot	Master write output channel protection mode.
m_axi_awvalid	Master write output channel address is valid.
m_axi_awready	Master write output channel is ready.
m_axi_wdata	Master write output channel data.
m_axi_wstrb	Master write output channel data bytes valid.
m_axi_wvalid	Master write output channel data is valid.
m_axi_wready	Master write output channel data ready.
m_axi_bresp	Master write output channel response.
m_axi_bvalid	Master write output channel response valid.
m_axi_bready	Master write output channel response ready.

INSTANTIATED MODULES

dut

Device under test, axi_lite_wr_addr